SFP-DD MSA

SFP-DD Hardware Specification

for

SFP DOUBLE DENSITY 2X PLUGGABLE TRANSCEIVER

Revision 4.2

August 17, 2020

Abstract: This specification defines: the electrical and optical connectors, electrical signals and power supplies, mechanical and thermal requirements of the pluggable SFP Double Density (SFP-DD) module, connector and cage system. This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules.

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Change History:

Revision	Date	Changes
1.0	September 14 2017	First public release
2.0	September 17, 2018	Updates to Figures 9,10,11,12,13,16,17,18,19, 20, 21. Added Type 2 module. Changed IntL pin to reserved, Changed TxFault to TxFault/Int Updated drawings to include new key, changed some pin names to use channel 0, 1. Added test conditions for insertion removal forces.
3.0	April 10 2019	Updated connector drawings Fig. 11, 20, 21. Updated Fig. 3, added bail latch sentence, added 5W power option. Added Fig. 15b (bottom pad field). Added SN, MDC connectors. Deleted requirement that host shall not change the state of LPMode when module is present (4.1.1.7). Added 'Latch disengaged' to first four entries in Table 8(10).
4.0	Withdrawn	
4.1	August 10, 2020	Added ResetL, IntL, ePPS, Fault signals. Added timing tables for low speeds signals, soft control and status. Chapter 7-Management Interface is now part of Chapter 4-Electrical Specification. Port mapping, optical connectors, and module color coding moved out of Mechanical and Board Definition Chapter-5 and into a new Chapter-5. Appendix A- Normative Connector Performance Requirements added.
4.2	August 17, 2020	Added dual functionality IntL/TXFaultDD signal definition.

Foreword

The development work on this specification was done by the SFP-DD MSA, an industry group. The membership of the committee since its formation in May 2017 has included a mix of companies which are leaders across the industry.

The members of the SFP-DD MSA would like to acknowledge the contributions of Edmund Poh. He was an excellent engineer; his technical skills and collaborative attitude will be missed.

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1. Scope

The scope of this specification is the definition of a high density 2-channel module, cage and connector system. SFP-DD supports up to 100 Gb/s in aggregate over a 2 x 50Gb/s electrical interface. The cage and connector design provides backwards compatibility to SFP28 modules which can be inserted into a SFP-DD cage and connector using 1 of the electrical channels.

1.1 Overview of SFP-DD Chapters

SFP-DD specifications is organized into 7 chapters and one appendix addressing electrical, mechanical, environmental, and management aspects of the module.

- Chapter 1 Scope
- Chapter 2 References and Related Standards and SFF Specifications
- Chapter 3 Introduction
- Chapter 4 Electrical specifications and management interface timing
- Chapter 5 Optical port mapping and optical interfaces
- Chapter 6 Mechanical specifications, printed circuit board recommendations, labeling, color code recommendations and optical interface examples
- Chapter 7 Environmental and thermal considerations
- Appendix A Normative module and connector performance requirements.

2. References

2.1 Industry Documents

The following interface standards and specifications are relevant to this Specification.
- ASME Y14.5-2009 Dimensioning and Tolerancing
- EIA-364-09 Durability Test Procedure for Electrical Connectors and Contacts
- EIA-364-13 Mating and Unmating Force Test Procedure for Electrical Connectors and Sockets
- EIA-364-23 Low Level Contact Resistance Test Procedure for Electrical Connectors and Sockets
- EIA-364-35 Insert Retention Test for Electrical Connectors and Sockets
- EN61000-4-2 Testing and measurement techniques - Electrostatic discharge immunity test, criterion B test specification
- FC-PI-6 32GFC (INCITS 533)
- FC-PI-7 64GFC (INCITS 543)
- Human Body Model per ANSI/ESDA/JEDEC JS-001
- IEEE Std 802.3-2018 annex 86A, 83E, and 120E
- IEEE Std 802.3cd clause 136 and annex 136A
- InfiniBand Architecture Specifications
- JEDEC JESD8C.01 Interface Standard for Nominal 3.0/3.3 V Supply Digital Integrated Circuit (LVCMOS)
- Keysight Technologies application brief 5991-2778EN.pdf
- OIF CEI-28G-VSR
- OIF CEI-56G-VSR-PAM4
- NEBS GR-63 Physical Protection Requirements for Network Telecommunications Equipment
- NXP UM10204, I2C-bus specification and user manual, Rev 6 – 4 April 2014.
- SFP-DD Management Interface
- SN-60092019 (SN optical connector and receptacle), see http://www.qsfp-dd.com/optical-connector/
- TIA-604-5, IEC 61754-7 (MPO-12 connector)
- TIA-604-10, IEC 61754-20 (Dual LC optical patchcord and module receptacle)
- USC-11383001 (MDC optical plug and receptacle), see http://www.qsfp-dd.com/optical-connector/

SFF/MSA Specifications:
- INF-8074i SFP (Small Formfactor Pluggable) Transceiver
- SFP-DD MIS
- SFF-8419 SFP+ Power and Low Speed Interface, see A.1.1
- SFF-8431 SFP+ 10 Gb/s and Low Speed Electrical Interface
- SFF-8432 SFP+ Module and Cage
- SFF-8472 Diagnostic Monitoring Interface for Optical Transceivers
- SFF-8432 SFP+ Module and Cage
- SFF-8636 Management Interface for 4-lane Modules and Cables.

2.2 Sources

The SFP-DD MSA SFP-DD Hardware Specification for SFP DOUBLE DENSITY 2X PLUGGABLE TRANSCEIVER can be obtained via the www.SFP-DD.com web site.

3. Introduction

This Specification covers the following items:

- Electrical interfaces including pad assignments for data, control, status and power supplies and host PCB layout requirements.
- Optical interfaces (including optical receptacles and mating fiber plugs for multimode and single-mode duplex and parallel fiber applications). Breakout cable applications are also specified.
- Mechanical specifications including dimensions and tolerances for the connector, cage and module system. Includes details of the requirements for correct mating of the module and host sides of the connector.
- Thermal requirements
- Management Interface Timing requirements
- Electrostatic discharge (ESD) requirements by reference to industry standard limits and test methods.

This Specification does not cover the following items:

- Electromagnetic interference (EMI) protection. EMI protection is the responsibility of the implementers of the cages and modules.
- Optical signaling specifications are not included in this document but are defined in the applicable industry standards.
- Management Registers.

3.1 Objectives

Implementations compliant to electrical signal contact and channel assignments, electrical, timing, and power requirements defined in Chapter 4 and optical port mapping and optical interfaces defined in Chapter 5 ensure that the pluggable modules and cable assemblies are functionally interchangeable. Implementations compliant to dimensions, mounting and insertion requirements defined in Chapter 6 for the bezel, optical module, cable plug, cage and connector system on a circuit board ensure that these products are mechanically interchangeable.

3.2 SFP-DD System Overview

The SFP-DD form factor system consisting of a transceiver module, cage and connector provides two channels for high speed signals that can support a two-lane trunked application or two independent single-lane applications. The cage and socket can also accept SFP (SFP10 and later) modules in which case a single lane channel is supported. To support SFP modules the electrical connector maintains the twenty contacts row defined for SFP modules and adds another twenty contacts row to support a second channel.

In addition to contacts for the high speed data signals, the connector provides contacts for module and channel control and status signals including a pair that form a Two-Wire Interface (TWI) for communication with the module's memory. Contacts for high speed data signals, channel level control and status indicator signals and power supply sources for the SFP module are repeated in the row for the second channel. Contacts for module level control and status signals in the SFP module remain in place and signals for new module level functions were added to the second row.

New global features and associated signals, Low Power Mode, Reset and Interrupt were added and the memory map for SFP-DD was expanded and reorganized for better alignment with CMIS functionality and structure. Within the SFP-DD MIS the name used for channel items associated with the SFP row is Channel 1 and the name used for channel items associated with the second channel is Channel 2. Within this document the name, Channel 1, is synonymous with the name SFP Channel and Channel 2 is synonymous with the name DD Channel.

Adding a second channel results in increased module power consumption. Accommodations for the increased consumption include defining additional power classes, defining a Type 2 module and defining an enlarged heat sink seating area with surface flatness and roughness requirements. A low power mode was added to provide the host a means for power management.

Another accommodation for a second channel was the inclusion of addition optical connectors including MPO, duplex LC and dual duplex LC options, see Figure 14.

3.3 Applications

This specification defines a connector, cage and module for single or double lane applications at up to 58 Gb/s per lane. Intended applications include but are not limited to Ethernet and/or InfiniBand and/or Fibre Channel. The SFP-DD interface can support pluggable modules or direct attach cables based on multimode fiber, single mode fiber or copper wires.

An application reference Model, shown in Figure 1, shows the high-speed data interface between an ASIC and the SFP-DD module.

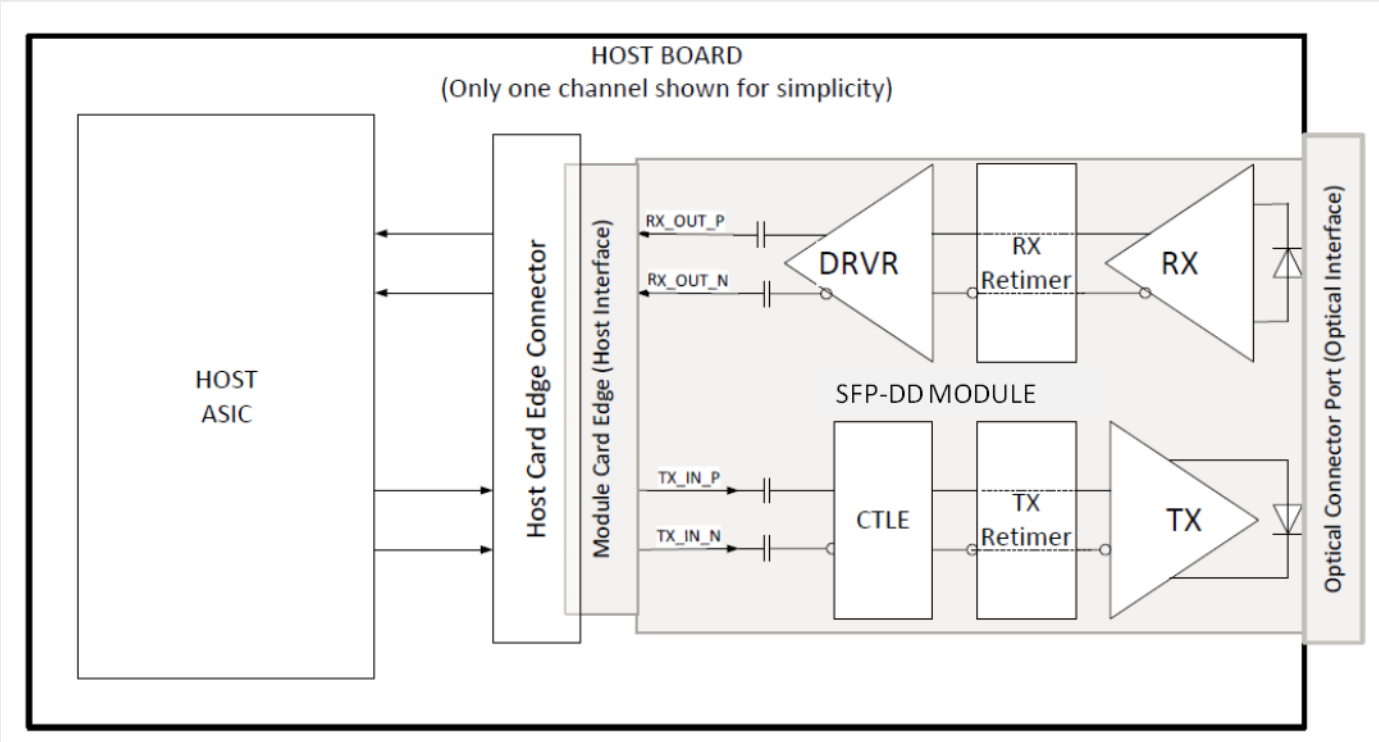


Figure 1: Application Reference Model

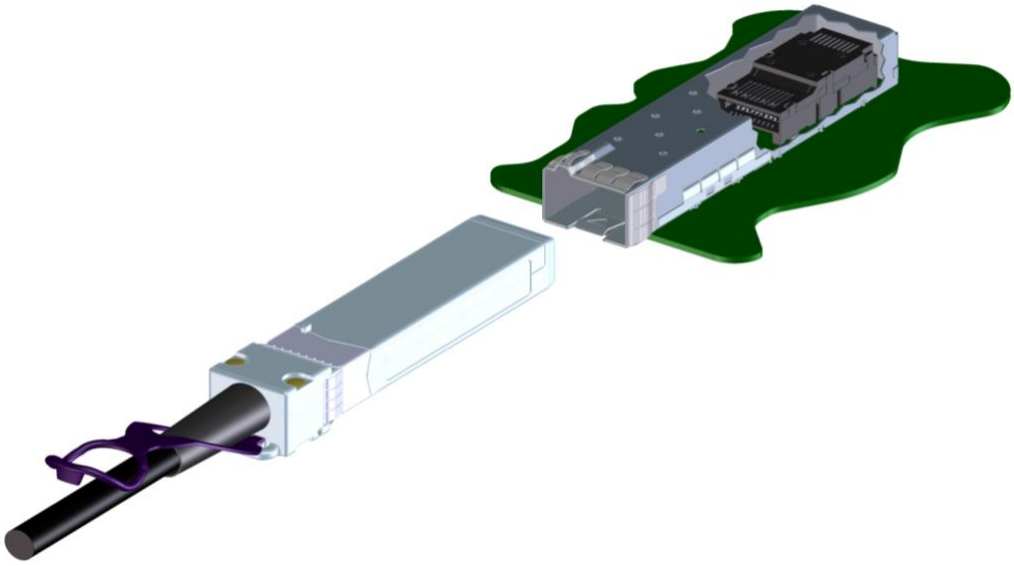


Figure 2: SFP-DD Cage, Connector and Module

4. Electrical Specification and Management Interface Timing

This chapter contains signal definitions and requirements that are specific to the SFP-DD module. High-speed signal requirements including compliance points for electrical measurements are defined in the applicable industry standard.

4.1 Electrical Connector

The SFP-DD module edge connector consists of a single paddle card with 20 pads on the top and 20 pads on the bottom of the paddle card for a total of 40 pads. The pads positions are defined to allow insertion of either an SFP-DD module or an SFP28 into the SFP-DD receptacle. The legacy signal locations are deeper on the paddlecard, so that legacy SFP module pads only connect to the longer row of connector pins, leaving the short row of connector pins open circuited in an SFP application.

The pads are designed for a sequenced mating:

- First mate – ground pads
- Second mate – power pads
- Third mate – signal pads.

Because the SFP-DD module has 2 rows of pads, the additional SFP-DD pads will have an intermittent connection with the legacy SFP/SFP+ pins in the connector during the module insertion and removal. The 'legacy' SFP/SFP+ pads have a “B” label shown in Table 1 to designate them as the first row of module pads to contact the SFP-DD connector. The additional SFP-DD pads have a “A” label with first, second and third mate to the connector pins for both insertion and removal. Each of the first, second and third mate connections of the legacy SFP pads and the respective additional SFP-DD pads are simultaneous.

Figure 3 shows the signal symbols and pad numbering for the SFP-DD module edge connector. The diagram shows the module PCB edge as a top and bottom view. There are 40 pads intended for high speed signals, low speed signals, power and ground connections.

Table 1 provides more information about each of the 40 pads. Figure 24 and Figure 25 show pad dimensions. The surface mount configuration is shown in Figure 30.

For EMI protection the signals from the host connector should be shut off when the SFP-DD module is not present. Standard board layout practices such as connections to Vcc and GND with vias, use of short and equal-length differential signal lines are recommended. The chassis ground (case common) of the SFP-DD module should be isolated from the module’s circuit ground, GND, to provide the equipment designer flexibility regarding connections between external electromagnetic interference shields and circuit ground, GND, of the module.

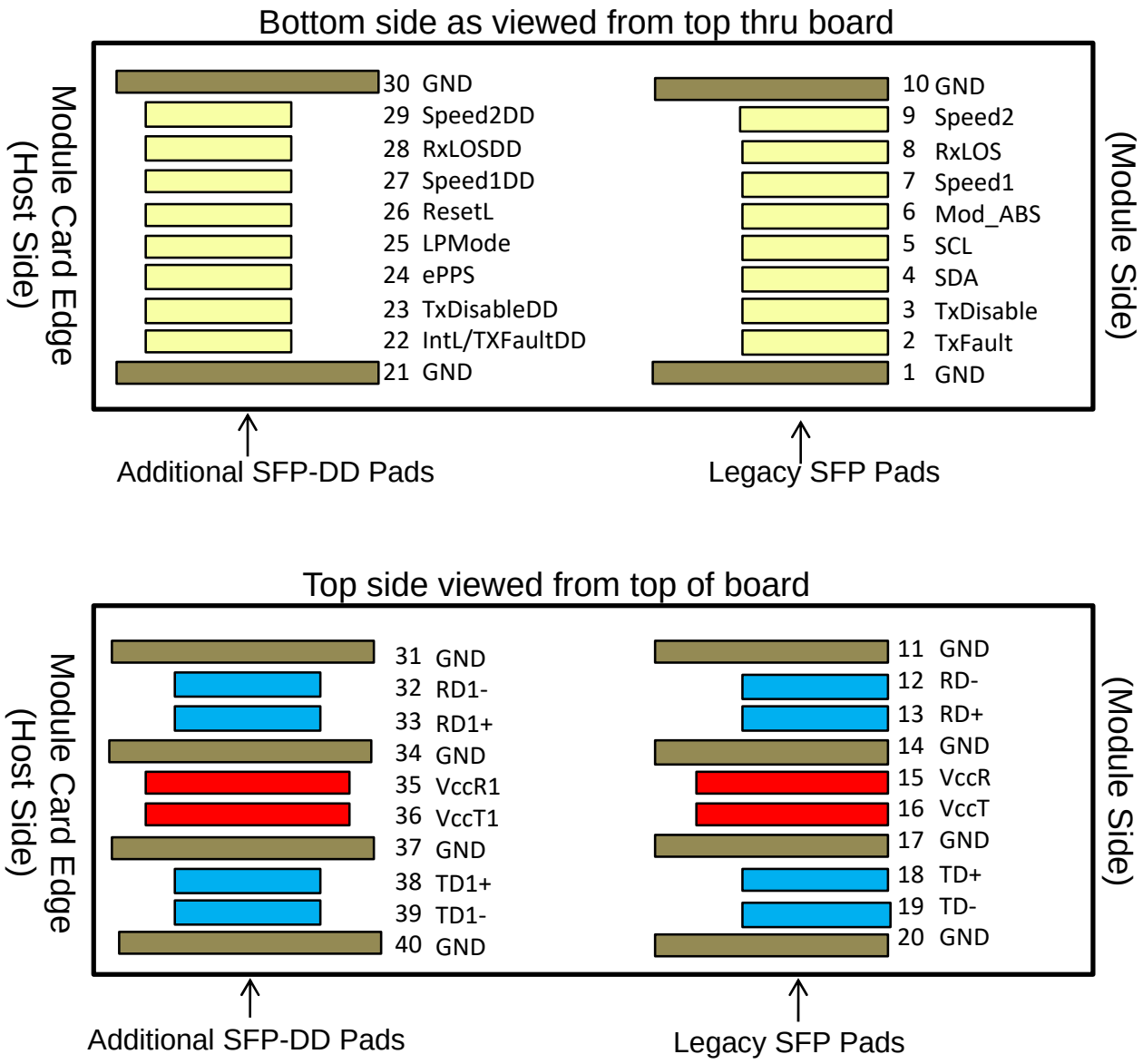


Figure 3: Module pad layout

Because the SFP-DD module has 2 rows of pads, the additional SFP-DD pads will have an intermittent connection with the legacy SFP pins in the connector during the module insertion and removal. SFP-DD module pads compatible with SFP/SFP+ are designated as “legacy” pads in Table 1 to designate them as the second row of module pads to contact the SFP-DD connector. The additional module pads are designated as ”DD” pads in Table 1 to designate them as the first row of module pads to contact the SFP-DD connector. The additional SFP-DD pads have first, second and third mate to the connector pins for both insertion and removal. Each of the first, second and third mate connections of the legacy SFP pads and the respective additional SFP-DD pads are simultaneous. For a reliable interconnect, a sufficient contact wipe of the connector pins sliding over the module gold pads is required. In the past, long signal pads have been used to provide the mechanical wipe. As operating speeds were relatively slow, the electrical stub was not an issue with signal integrity.

As operating speeds have increased, signal pad lengths have become shorter and shorter to reduce electrical stubs, however this caused insufficient mechanical wipe. A solution is to add a small separation of the signal pad such that there is a passive 'pre-wipe" pad and an active signal pad. In SFP-DD, there are also long pre-wipe pads between the additional SFP-DD pads and the legacy SFP pads. This provides connector pins a gold platted pad surface over which to slide between rows.

Table 1- Pad Function Definition

Pad	Logic	Symbol	Module Pad Descriptions	Plug Sequence[4]	Notes
0		Case	Module case		
1		GND	Ground	1B	1
2	LVTTL-O	TxFault	Module Fault Indication; optionally configured as legacy SFP Module Fault Indication via TWI as described in the SFP-DD MIS	3B	
3	LVTTL-I	TxDisable	Transmitter Disable for legacy SFP channel	3B	
4	LVCMOS-I/O	SDA	Management I/F data line	3B	
5	LVCMOS-I/O	SCL	Management I/F clock	3B	
6	LVTTL-O	Mod_ABS	Module Absent	3B	
7	LVTTL-I	Speed1	Rx Rate Select for legacy SFP channel	3B	
8	LVTTL-O	RxLOS	Rx Loss of Signal for legacy SFP channel	3B	
9	LVTTL-I	Speed2	Tx Rate Select for legacy SFP channel	3B	
10		GND	Ground	1B	1
11		GND	Ground	1B	1
12	CML-O	RD0-	Inverse Received Data Out for legacy SFP+ channel	3B	
13	CML-O	RD0+	Received Data Out for legacy SFP+ channel	3B	
14		GND	Ground	1B	1
15		VccR	Receiver Power	2B	2
16		VccT	Transmitter Power	2B	2
17		GND	Ground	1B	1
18	CML-I	TD0+	Transmit Data In for legacy SFP channel	3B	
19	CML-I	TD0-	Inverse Transmit Data In for legacy SFP channel	3B	
20		GND	Ground	1B	1
21		GND	Ground	1A	1
22	LVTTL-O	IntL/ TxFaultDD	Interrupt; optionally configured as TxFaultDD via TWI as described in the SFP-DD MIS	3A	
23	LVTTL-I	TxDisableDD	Transmitter Disable for DD channel	3A	
24	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input	3A	3
25	LVTTL-I	LPMode	Low Power Mode Control	3A	
26	LVTTL-I	ResetL	Module Reset	3A	
27	LVTTL-I	Speed1DD	Rx Rate Select for DD channel	3A	
28	LVTTL-O	RxLOSDD	Loss of Signal for DD channel	3A	
29	LVTTL-I	Speed2DD	Tx Rate Select for DD channel	3A	
30		GND	Ground	1A	1
31		GND	Ground	1A	1
32	CML-O	RD1-	Inverse Received Data Out for DD channel	3A	
33	CML-O	RD1+	Received Data Out for DD channel	3A	
34		GND	Ground	1A	1
35		VccR1	Receiver Power for DD channel	2A	2
36		VccT1	Transmitter Power for DD channel	2A	2
37		GND	Ground	1A	1
38	CML-I	TD1+	Transmit Data In for DD channel	3A	
39	CML-I	TD1-	Inverse Transmit Data In for DD channel	3A	
40		GND	Ground	1A	1

Notes:

1. SFP-DD uses common ground (GND) for all signals and supply (power). All are common within the SFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccR, VccT shall be applied concurrently and VccR1, VccT1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 8. VccR, VccT, VccR1, VccT1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. The ePPS pins (if not used) may be terminated with 50 Ω to ground on the host.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 0, 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 3 for pad locations) Contact sequence A will make, then break contact with additional SFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.

4.2 Overview of the Low Speed Electrical Hardware Signals

The SFP-DD connector allocates contacts for a set of low speed signals for control, status and management by the host. These include dedicated hardware signals and TWI signals. The dedicated hardware signals are the following:

- TxDisable, TxDisableDD
- RxLOS, RxLOSDD
- Speed1, Speed2, Speed1DD, Speed2DD
- TxFault
- IntL/TXFaultDD
- Mod_ABS
- LPMode
- ResetL
- ePPS.

The TWI signals are the following:

- SCL – clock
- SDA – data.

4.2.1 TxDisable, TxDisableDD

TxDisable and TxDisableDD are module input signals. When TxDisable or TxDisableDD are asserted high or left open, the appropriate SFP-DD module transmitter output shall be turned off unless the module is a passive cable assembly in which case this signal may be ignored. This signal shall be pulled up to VccT in modules and cable assemblies. When TxDisable or TxDisableDD are asserted low or grounded the module transmitter is operating normally.

4.2.2 RxLOS, RxLOSDD

RxLOS (Rx Loss of Signal) and RxLOSDD are open drain/collector outputs that require a resistive pull up to Vcc_Host with a resistor in the range 4.7 kΩ to 10 kΩ, or with an active termination according to Table 2. When high it indicates an optical signal level below that specified in the relevant standard.

LOS may be an optional function depending on the supported standard. If the LOS function is not implemented, or is reported via the TWI only, the RxLOS contact shall be held low by the module and may be connected to GND within the module.

RxLOS, RxLOSDD assert min and de-assert max are defined in the relevant standard. To avoid spurious transition of LOS a minimum hysteresis of 0.5 dBo is recommended.

4.2.3 Speed1, Speed2, Speed1DD, Speed2DD

Speed1, Speed2, Speed1DD and Speed2DD are module inputs and are pulled low to GND with >30 kΩ resistors in the module. Speed1 optionally selects the optical receive signaling rate for channel 1. Speed1DD optionally selects the optical receive signaling rate for channel 2. Speed2 optionally selects the optical transmit signaling rate for the channel 1. Speed2DD optionally selects the optical transmit signaling rate for channel 2. For logical definitions of hardware rate selects Speed1, Speed2, Speed1DD, Speed2DD, see 4.8.

4.2.4 TxFault

TxFault is a module wide (channel 1 and channel 2) output signal that when high, indicates that the module has detected a fault condition and has entered the Fault state. TxFault signal can optionally be configured as legacy SFP Module (channel 1) Fault Indication via TWI as described in the SFP-DD MIS. If TxFault is not implemented, the contact signal shall be held low by the module and may be connected to GND within the

module. The TxFault output is open drain/collector and shall be pulled up to the Vcc_Host on the host board with a resistor in the range 4.7 kΩ to 10 kΩ, or with an active termination according to Table 2.

4.2.5 IntL/TxFaultDD

IntL/TxFaultDD is an open collector output that optionally can be configured for either the IntL signal or the TxFaultDD signal. It shall be pulled to Vcc Host on the host board with a resistor in the range 4.7 kΩ to 10 kΩ, or with an active termination according to Table 2. At power-up or after ResetL is released to high, IntL/TxFaultDD is configured as IntL. If supported IntL/TxFaultDD can be optionally programmed as TxFaultDD using TWI as defined in the SFP-DD Management Interface Specification.

When IntL/TxFaultDD is configured as IntL, a Low indicates a change in module state, a possible operational fault or a status critical to the host system. The host identifies the source of the interrupt using TWI. The IntL signal is de-asserted High after all set flags are read.

When IntL/TxFaultDD is configured as TxFaultDD, a High indicates that the module has detected a fault condition in lane 1 and has entered the Fault state. (See SFP-DD MIS section 6.3.1.11) and if TxFaultDD is not implemented, the contact signal shall be held low by the module.

4.2.6 Mod_ABS

Mod_ABS must be pulled up to Vcc Host on the host board and pulled low in the module. The Mod_ABS is asserted “Low” when the module is inserted. The Mod_ABS is deasserted “High” when the module is physically absent from the host connector due to the pull up resistor on the host board.

4.2.7 LPMode

LPMode is an input signal from the host operating with active high logic. The LPMode signal must be pulled up to Vcc in the SFP-DD module. The LPMode signal allows the host to define whether the SFP-DD module will remain in Low Power Mode until software enables the transition to High Power Mode as defined in the SFP-DD management specification. In Low Power Mode (LPMode de-asserted Low), the module may immediately transition to High Power Mode after the management interface is initialized.

4.2.8 ResetL

The ResetL signal shall be pulled to Vcc in the module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) (See Table 4) initiates a complete module reset, returning all user module settings to their default state.

4.2.9 ePPS PTP Reference Clock (Optional)

For Precision Time Protocol (PTP) applications, a PTP reference clock with Pulse Per Second modulation, Enhanced Pulse Per Second (ePPS) may be provided from the host to the module. This can be used for either offline delay characterization or real-time delay compensation within the module. The clock is used to synchronize tightly the Host Time-of-Day counter to the module internal Time-of-Day Counter.

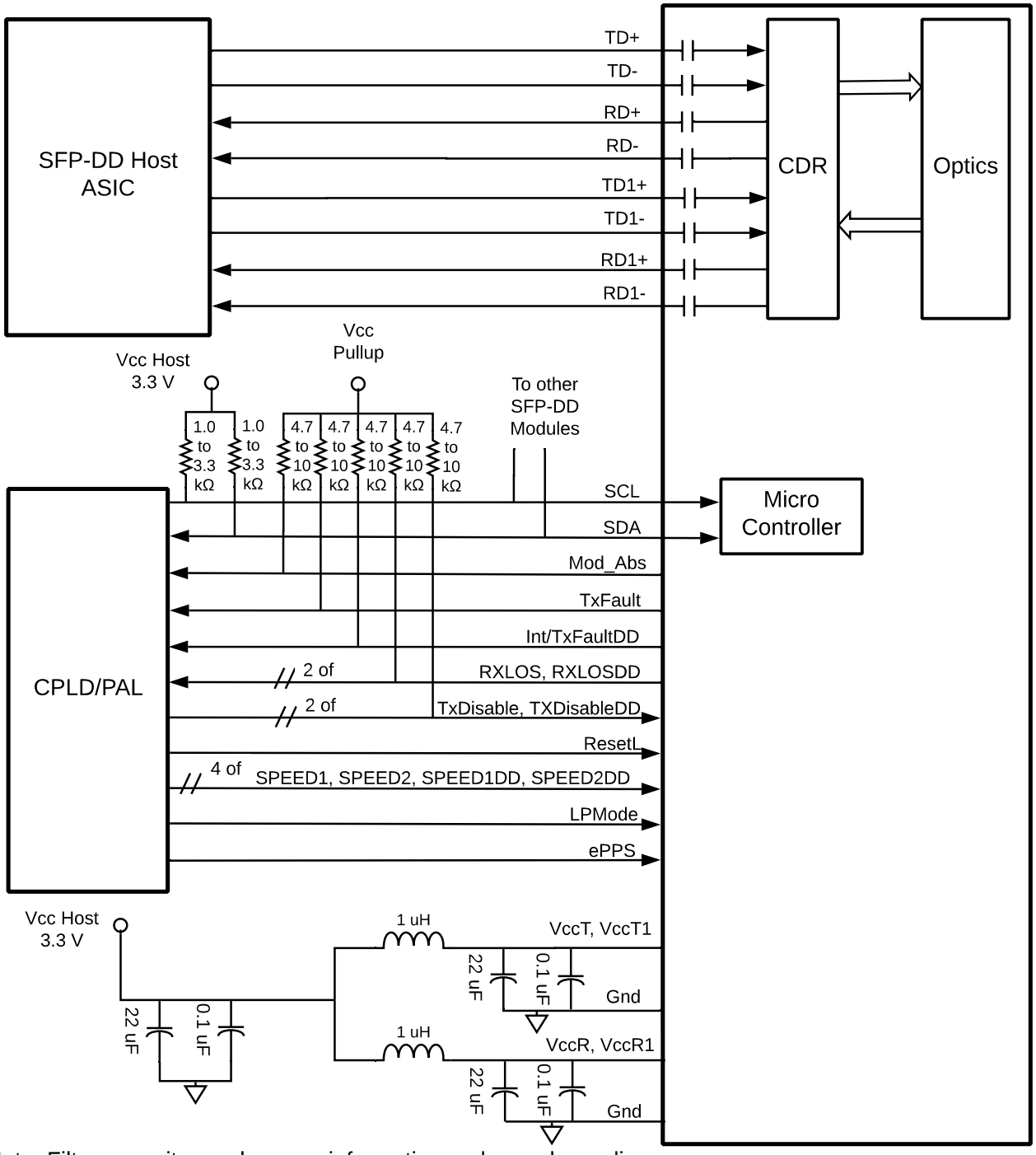
Editor’s Note – Full definition of ePPS is currently under development.

4.2.10 TWI Signals SCL, SDA

SCL is the TWI clock and SDA is the TWI data line. SCL and SDA are pulled up to Vcc_Host by resistors on the host board. For TWI electrical specifications see 4.4.1 and for TWI protocol and timing specifications see Figure 8.

4.3 Example SFP-DD Host Board Schematics

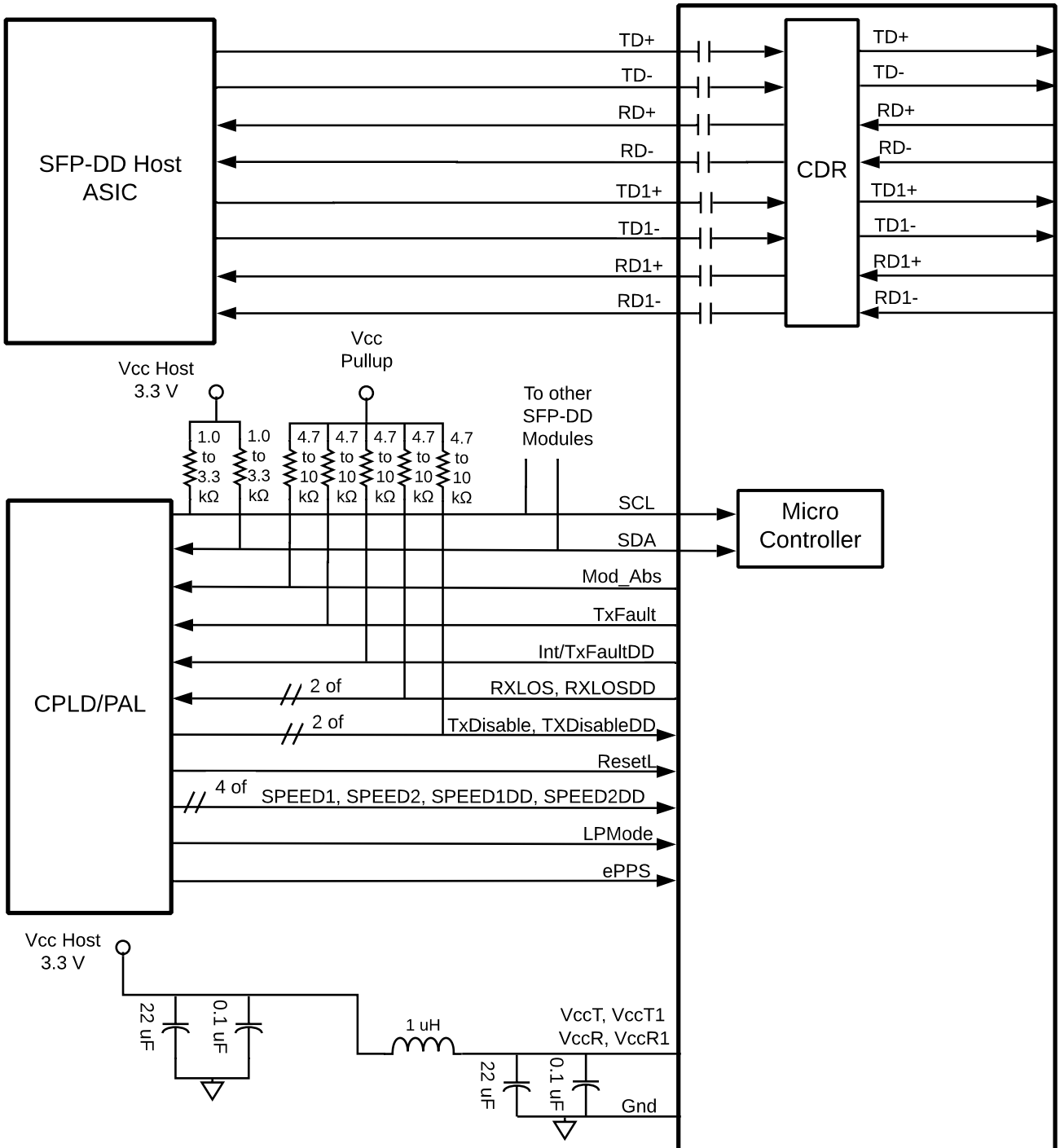
Figure 4, Figure 5 and Figure 6 show examples of SFP-DD host PCB schematics with connections to CDR and control ICs. Note alternate electrical/optical interfaces are supported using optical multiplexing (WDM) or electrical multiplexing.



Note: Filter capacitors values are informative and vary depending on applications, 0.1 uF capacitors should be placed in close proximity to power pins and may be duplicated for individual pins to provide addtional high frequency filtering.

Note: VccT, VccT1 may be connected to VccR, VccR1 provided the applicable derating of the maximum current limit is used.

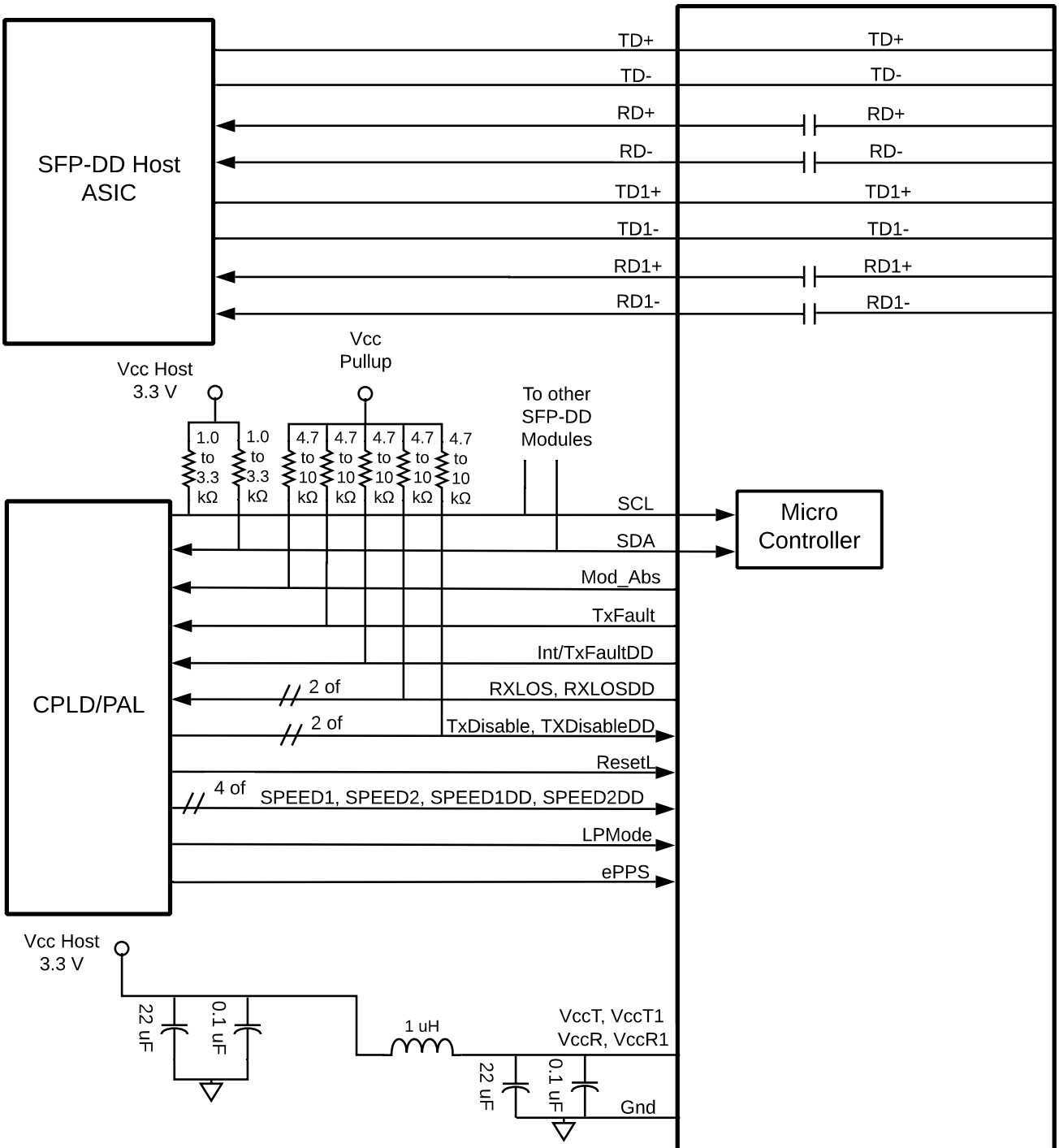
Figure 4: Example SFP-DD Host Board Schematic for Optical Modules



Note: Filter capacitors values are informative and vary depending on applications, 0.1 uF capacitors should be placed in close proximity to power pins and may be duplicated for individual pins to provide addtional high frequency filtering.

Note: Recomended filtering is only valid for dedicated passive copper cable ports. For ports supporting both passive and active modules use recomended filtering from Figures 4 and 5.

Figure 5: Example SFP-DD Host Board Schematic for active copper cables



Note: Filter capacitors values are informative and vary depending on applications, 0.1 uF capacitors should be placed in close proximity to power pins and may be duplicated for individual pins to provide addtional high frequency filtering.

Note: Recomended filtering is only valid for dedicated passive copper cable ports. For ports supporting both passive and active modules use recomended filtering from Figures 4 and 5.

Figure 6: Example SFP-DD Host Board Schematic for passive copper cables

4.4 Low Speed Electrical Specification

Low Electrical requirements for low speed signals TxDisable, TxDisableDD, RxLOS, RxLOSDD, Speed1, Speed2, Speed1DD, Speed2DD, TxFault, IntL/TXFaultDD, Mod_ABS, LPMode, ResetL and ePPS are based on Low Voltage TTL (LVTTL) operating at a module supply voltage Vcc of 3.3V +/- 5% and with a host supply voltage Vcc_Host range of 2.38 to 3.46V. Vcc is used as a generic term for the supply voltages of VccTx, VccRx, VccPullup or Vcc1. Host biasing requirements (e.g. pullup resistors) are defined in 4.2 and illustrated in 4.3.

Electrical requirements for the TWI signals, SCL and SDA are based on Low Voltage CMOS (LVCMOS) operating at Vcc and the NXP I2C-bus specification and user manual. Host biasing requirements (e.g. pullup resistors) are defined in 4.2 and illustrated in 4.3. Capacitance loading requirements are defined in Table 2 and tradeoffs are illustrated in Figure 7.

4.4.1 TWI Logic Levels and Bus Loading

The SFP-DD low speed electrical specifications are given in Table 2. Implementations compliant to this specification ensures compatibility between host bus masters and TWI. Tradeoffs among Pull up resistor values, bus capacitance and rise time are shown in Figure 7.

Table 2- Low Speed Control and Sense Signals

Parameters	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0	0.4	V	open-drain or open-collector at 3 mA sink current; VDD > 2 V, IOL=3.0 mA for fast mode, 20 mA for fast mode plus
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	Vcc*0.7	Vcc+0.5	V	
Capacitance for SCL and SDA I/O signal	Ci		14	pF	
Total bus capacitive load for SCL and SDA	Cb		100	pF	For 400 kHz clock rate use 3.0 kΩ Pullup resistor, max. For 1000 kHz clock rate refer to Figure 7.
			200	pF	For 400 kHz clock rate use 1.6 kΩ pullup resistor max. For 1000 kHz clock rate refer to Figure 7.
TxDisable(DD), ResetL, LPMode, Speed(n) and ePPS	VIL	-0.3	0.8	V	For 0V<Vin<Vcc
	VIH	2	Vcc+0.3	V	
LPMode, ResetL, TxDisable(DD), Speed(n)	|Iin|		360	μA	
ePPS	|Iin|		TBD	μA	
Mod_ABS	VOL	0	0.4	V	IOL=2.0 mA, Mod_ABS can be implemented as a short-circuit to GND on the module
RxLOS(DD), TxFault(DD)	VOL	-0.3	0.40	V	4.7 kΩ Pullup resistor to Vcc_Host where Vcc_Host_min<Vcc_Host<Vcc_Host_max
	IOH	-50	37.5	uA	
IntL	VOL	0	0.4	V	IOL = 2.0 mA

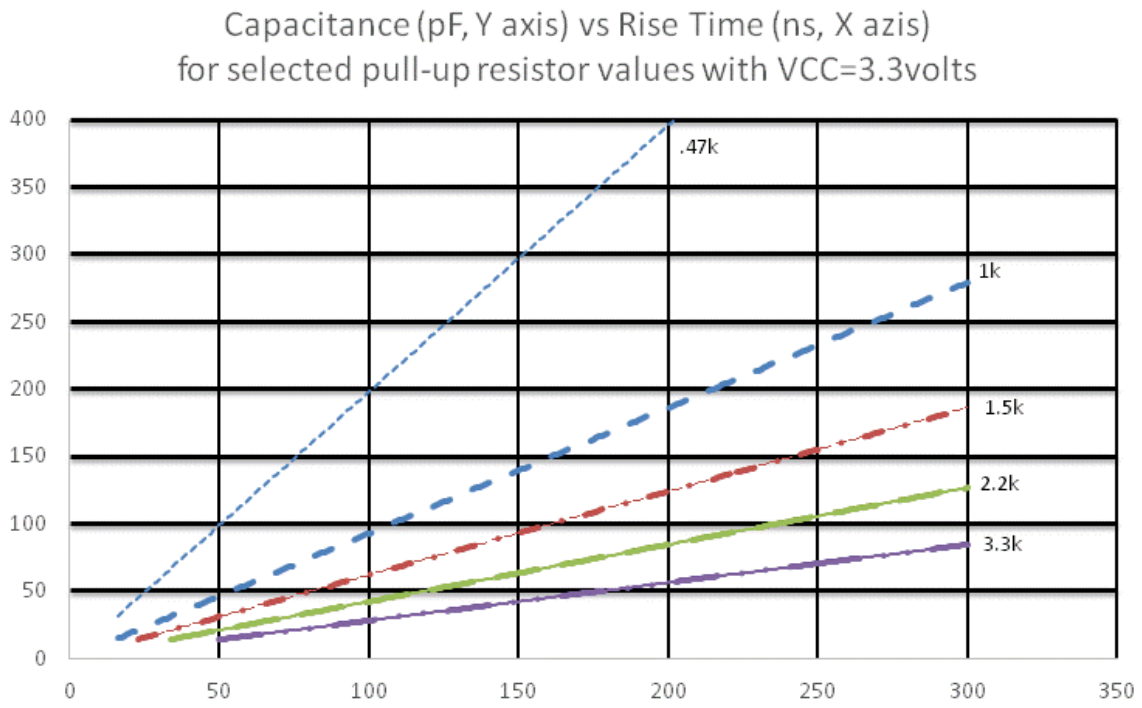


Figure 7: SDA/SCL options for pull-up resistor, bus capacitance and rise/fall times

4.5 Management Interface and Timing

A management memory interface (See SFP-DD Management Interface Specification), as already commonly used in other form factors like QSFP, SFP, and CDFP, enables module functionality and flexibility beyond that supported by the dedicated hardware signals. Read/Write functionality and protocols are defined in SFP-8419 rev 1.3 Specification for SFP+ Power and Low Speed Interface.

Some timing requirements are critical, especially for a multi-channel device, so the interface speed may optionally be increased. Byte 00 on the Lower Page or Address 128 Page 00 is used to advertise the use of the SFP-DD memory map rather than the SFP memory map. When a legacy SFP28 module is inserted into an SFP-DD port the host must use the SFP memory map (i.e. SFF-8472. This case is outside the scope of this document.

In some applications, muxing or demuxing may occur in the module. In this specification, all references to channel numbers are based on the electrical connector interface channels, unless otherwise indicated. In cases where a status or control aspect is applicable only to channels after muxing or demuxing has occurred, the status or control is intended to apply to all channels in the mux group, unless otherwise indicated.

Timing requirements for the TWI signals, SCL and SDA are based the NXP I2C-bus specification and user manual.

4.5.1 Management Timing Specification

The SFP-DD TWI and memory management timing illustrated in in Figure 8 and the parameters given in Table 3. Implementations compliant to these specifications ensure compatibility between host bus masters and the TWI.

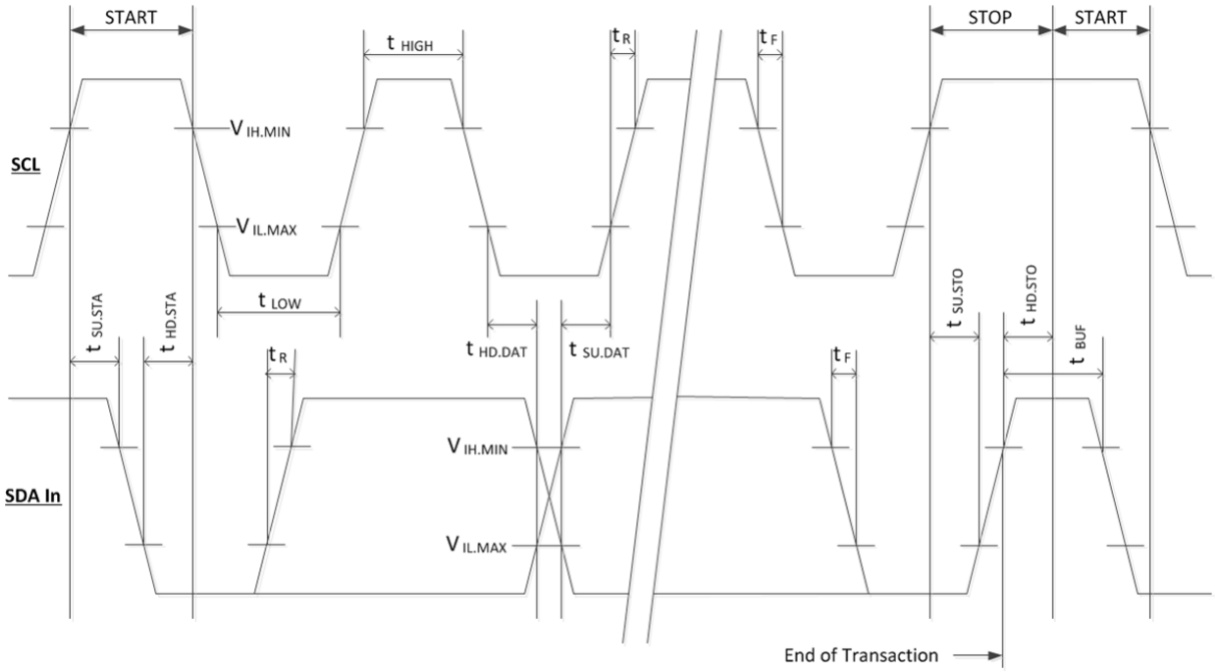


Figure 8: SFP-DD Two Wire Interface Timing

Table 3- Management Interface timing parameters

Parameters	Symbol	Min	Max	Min	Max	Unit	Conditions
		Fast Mode (400 KHz)		Fast Mode Plus (1 MHz)			
Clock Frequency	fSCL	0	400	0	1000	KHz	
Clock Pulse Width Low	tLOW	1.3		0.50		µs	
Clock Pulse Width High	tHIGH	0.6		0.26		µs	
Time bus free before new transmission can start	tBUF	20		20		µs	Between STOP and START and between ACK and ReStart
START Hold Time	tHD.STA	0.6		0.26		µs	The delay required between SDA becoming low and SCL starting to go low in a START
START Setup Time	tSU.STA	0.6		0.26		µs	The delay required between SCL becoming high and SDA starting to go low in a START
Data In Hold Time	tHD.DAT	0		0		µs	
Data In Setup Time	tSU.DAT	0.1		0.1		µs	
Input Rise Time	t_R		300		120	ns	From (VIL, MAX=0.3*Vcc) to (VIH, MIN=0.7*Vcc)
Input Fall Time	t_F		300		120	ns	From (VIH, MIN=0.7*Vcc) to (VIL, MAX=0.3*Vcc)
STOP Setup Time	tSU.STO	0.6		0.26		µs	
STOP Hold Time	tHD.STO	0.6		0.26		µs	
Serial Interface Clock Holdoff “Clock Stretching”	T_clock_hold		500		500	µs	Maximum time the SFP-DD module may hold the SCL line low before continuing with a read or write operation
Complete Single or Sequential Write	tWR		80		80	ms	Complete (up to) 8 Byte Write
Accept a single or sequential write to volatile memory	tNACK		10		10	ms	Time to complete a Single or Sequential Write to volatile registers.
Time to complete a memory bank/page	tBPC		10		10	ms	Time to complete a memory bank and/or page change.
Endurance (Write Cycles)		50K		50k		cycles	Module Case Temperature = 70 ^oC

4.5.1.1 Bus timing tBUF

The timing attribute tBUF is the bus free time between sequential TWI transactions, see Figure 8. It’s measured from the low to high SDA edge of the Stop condition of the Write transaction to the high to low SDA edge of the Start condition for the next transaction.

4.5.1.2 Bus timing tWR

The timing attribute tWR is the time required for a module to complete its internally timed write cycle after a single or sequential write to non-volatile memory before the next basic management operation can be accepted, see Figure 9. It’s measured from the low to high SDA edge of the Stop condition of the Write transaction to the high to low SDA edge of the Start condition for the next transaction.

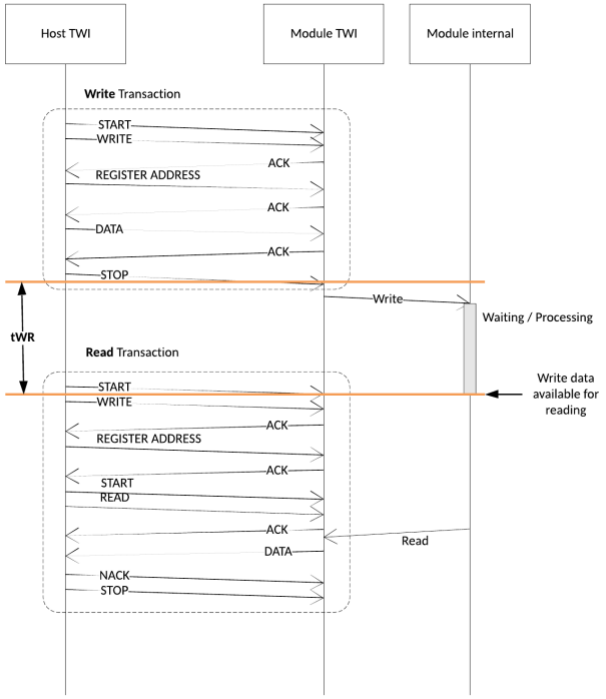


Figure 9: Bus timing tWR

4.5.1.3 Bus timing tNACK

The timing attribute tNACK is the time required for a module to complete its internally timed write cycle after a single or sequential write to volatile memory before the next basic management operation can be accepted, see Figure 10. It's measured from the low to high SDA edge of the Stop condition of the Write transaction to the high to low SDA edge of the Start condition for the next transaction.

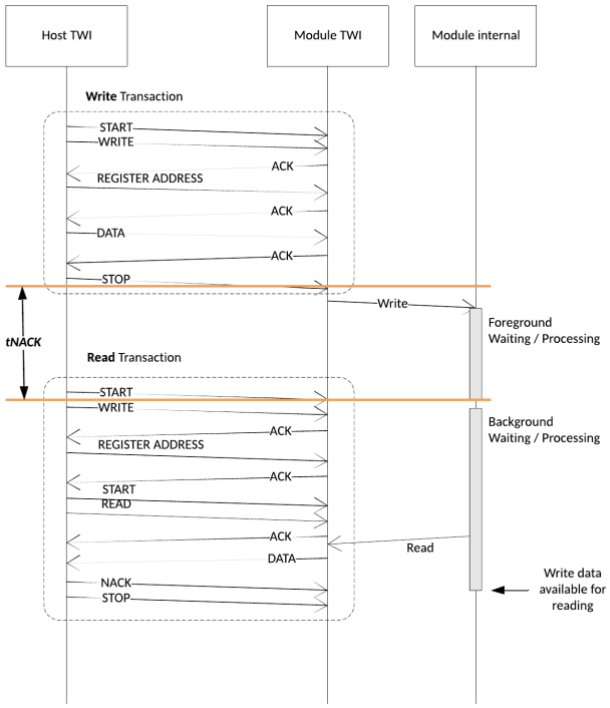


Figure 10: Bus timing tNACK

4.5.1.4 Bus timing tBPC

The timing attribute tBPC is the time required for a module to complete the change for the requested Bank and/or Page selection, see Figure 11. It's measured from the low to high SDA edge of the Stop condition of the Write transaction to the high to low SDA edge of the Start condition for the next transaction.

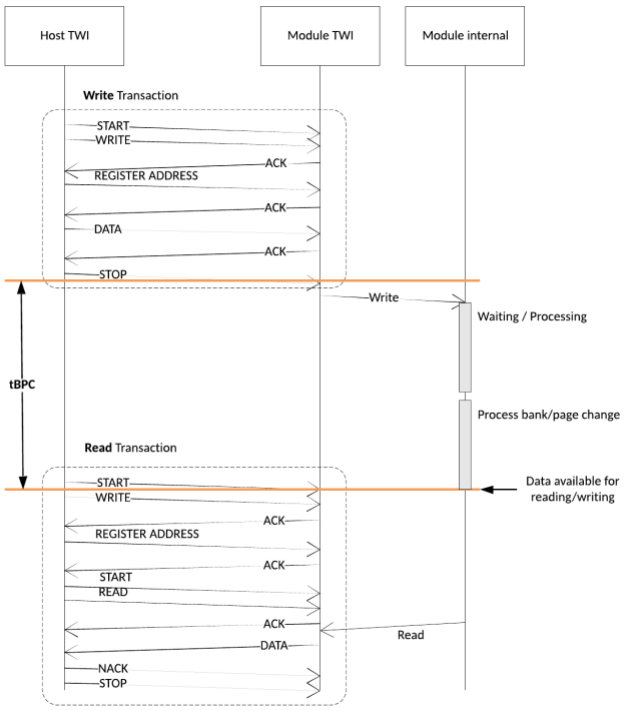


Figure 11: Bus timing tBPC

4.6 Timing for soft control and status functions

Timing for SFP-DD soft control and status functions are described in Table 4. Squelch and disable timings are defined in Table 5.

Table 4- Timing for SFP-DD soft control and status functions

Parameters	Symbol	Min	Max	Unit	Conditions
MgmtInitDuration	Max MgmtInit Duration		2000	ms	Time from power on[1] to hot plug or rising edge of reset until completion of the MgmtInit State
ResetL Assert Time	t_reset_init	10		µs	Minimum pulse time on the ResetL signal to initiate a module reset.
IntL Assert Time	ton_IntL		200	ms	Time from occurrence of condition triggering IntL until Vout:IntL=Vol
IntL Deassert Time	toff_IntL		500	µs	Time from clear on read[2] operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS, TXFault and other flag bits.
Rx LOS Assert Time	ton_los		200	ms	Time from Rx LOS condition present to Rx LOS bit set (value = 1b), LOS signal asserted and IntL asserted.
Rx LOS Assert Time (optional fast mode)	ton_losf		1	ms	Time from Rx LOS state to Rx LOS bit set (value = 1b) and LOS signal asserted IntL asserted.
TXFault Assert Time	ton_TxFault		200	ms	Time from TXFault state to TXFault bit set (value=1b) and IntL asserted.
Flag Assert Time	ton_flag		200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.
Mask Assert Time	ton_mask		100	ms	Time from mask bit set (value=1b)[3] until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask		100	ms	Time from mask bit cleared (value=0b)[3] until associated IntL operation resumes
DataPathDeinit Max Duration	DataPathDeinit_MaxDuration				See SFP-DD MIS Table 7-39
DataPathDeinit Max Duration	DataPathInit_MaxDuration				See SFP-DD MIS Table 7-39
ModulePwrDn Max Duration	ModulePwrDn_MaxDuration				See SFP-DD MIS Table 7-48
Data Path TX Turn On Max Duration	DataPathTxTurnOn_MaxDuration				See SFP-DD MIS Table 7-48
Data Path TX Turn Off Max Duration	DataPathTxTurnOff_MaxDuration				See SFP-DD MIS Table 7-48

Notes:
1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified in Table 8.
2. Measured from low to high SDA edge of the Stop condition of the read transaction.
3. Measured from low to high SDA edge of the Stop condition of the write transaction.
4. Rx LOS condition is defined at the optical input by the relevant standard.

Table 5- I/O Timing for Squelch & Disable

Parameters	Symbol	Max	Unit	Conditions
Rx Squelch Assert Time	ton_Rxsq	100	ms	Time from loss of Rx input signal until the squelched output condition is reached, see 4.7.1.
Rx Squelch Deassert Time	toff_Rxsq	10	s	Time from resumption of Rx input signals until normal Rx output condition is reached, see 4.7.1.
Tx Squelch Assert Time	ton_Txsq	400	ms	Time from loss of Tx input signal until the squelched output condition is reached, see 4.7.2.
Tx Squelch Deassert Time	toff_Txsq	10	s	Time from resumption of Tx input signals until normal Tx output condition is reached, see 4.7.2.
Tx Disable Assert Time	ton_txdis	100	ms	Time from the stop condition of the Tx Disable write sequence [1] until optical output falls below 10% of nominal
Tx Disable Assert Time (optional fast mode)	ton_txdisf	3	ms	Time from Tx Disable bit set (value = 1b)[1] until optical output falls below 10% of nominal
Tx Disable Deassert Time	toff_txdis	400	ms	Time from Tx Disable bit cleared (value = 0b)[1] until optical output rises above 90% of nominal
Tx Disable Deassert Time (optional fast mode)	toff_txdisf	10	ms	Time from Tx Disable bit cleared (value = 0b)[1] until optical output rises above 90% of nominal
Rx Output Disable Assert Time	ton_rxdis	100	ms	Time from Rx Output Disable bit set (value = 1b)[1] until Rx output falls below 10% of nominal
Rx Output Disable Deassert Time	toff_rxdis	100	ms	Time from Rx Output Disable bit cleared (value = 0b)[1] until Rx output rises above 90% of nominal
Squelch Disable Assert Time	ton_sqdis	100	ms	This applies to Rx and Tx Squelch and is the time from bit set (value = 0b)[1] until squelch functionality is disabled.
Squelch Disable Deassert Time	toff_sqdis	100	ms	This applies to Rx and Tx Squelch and is the time from bit cleared (value = 0b)[1] until squelch functionality is enabled

Notes:
1. Measured from LOW to HIGH SDA signal transition of the STOP condition of the write transaction.

4.7 High Speed Electrical Specifications

For detailed electrical specifications see the appropriate specification, e.g. IEEE Std 802.3-2018 Annex 83E, 86A, and 120E; IEEE Std 802.3cd clause 136 and Annex 136A; FC-PI-6 and FC-PI-7; OIF-CEI-28G-VSR and OIF-CEI-56G-VSR or the InfiniBand specifications.

Partial or complete squelch specifications may be provided in the appropriate specification. Where squelch is not fully defined by the appropriate specification, the recommendations given in clause 4.7.1 and 4.7.2 may be used.

4.7.1 RD0+, RD0-, RD1+, RD1-

RD(n)+/- are SFP-DD module receiver data outputs. Rx(n)+/- are AC-coupled 100 Ohm differential lines that should be terminated with 100 Ohm differentially at the Host ASIC(SerDes). The AC coupling is inside the SFP-DD module and not required on the Host board. When properly terminated, the differential voltage swing shall be less than or equal to 900 mVpp or the relevant standard, whichever is less.

Output squelch for loss of optical input signal, hereafter RX Squelch, is required and shall function as follows. In the event of the Rx input signal on any optical port becoming equal to or less than the level required to assert LOS, then the receiver output(s) associated with that Rx port shall be squelched. A single Rx optical port can be associated with more than one Rx output as shown in Table 9. In the squelched state output impedance levels are maintained while the differential voltage amplitude shall be less than 50 mVpp.

In normal operation the default case has RX Squelch active. Rx Squelch can be deactivated using Rx Squelch Disable through the 2-wire serial interface.

4.7.2 TD0+, TD0-, TD1+, TD1-

TD(n)+/- are SFP-DD module transmitter data inputs. They are AC-coupled 100 Ohm differential lines with 100 Ohm differential terminations inside the SFP-DD optical module. The AC coupling is implemented inside the SFP-DD optical module and not required on the Host board.

Output squelch for loss of electrical signal, hereafter TX Squelch, is an optional function. Where implemented it shall function as follows. In the event of the differential, peak-to-peak electrical signal amplitude on any electrical input channel becoming less than 70 mVpp, then the transmitter optical output associated with that electrical input channel shall be squelched and the associated TxLOS flag set. If multiple electrical input channels are associated with the same optical output channel, the loss of any of the incoming electrical input channels causes the optical output channel to be squelched.

For applications, e.g. Ethernet, where the transmitter off condition is defined in terms of average power, squelching by disabling the transmitter is recommended and for applications, e.g. InfiniBand, where the transmitter off condition is defined in terms of OMA, squelching the transmitter by setting the OMA to a low level is recommended.

In module operation, where TX Squelch is implemented, the default case has TX Squelch active. TX Squelch can be deactivated using TX Squelch Disable through the 2-wire serial interface. TX Squelch is an optional function. If TX squelch is implemented, the disable squelch must be provided.

4.8 Rate Select Hardware Control

The module provides 4 inputs Speed1, Speed2, Speed1DD and Speed2DD that can optionally be used for rate selection as defined in Table 6. Speed1, Speed1DD specifies the highest rate advertised by the channels. Speed2, Speed2DD specifies a lower speed for each channel. Speed1 controls the receive path signaling rate capability for the channel 1 receive path. Speed1DD controls the receive path signaling rate capability for the channel 2 receive path. Similarly, Speed2 controls the transmit path signaling rate capability for channel 1 and Speed2DD controls the transmit path signaling rate capability for the channel 2 transmit path.

The rate select functionality can also be controlled by software as defined by the SFP-DD management specification.

The Rate select Hardware Control is intended to be compatible with Fibre Channel 64GFC rate select methodology.

Table 6- Rate Select Hardware Control

Parameters	State	Conditions
Speed1, Speed1DD	Low	RX signaling rate of 14 GBd
	High	RX signaling rate of 28 GBd
Speed2, Speed2DD	Low	TX signaling rate of 14 GBd
	High	TX signaling rate of 28 GBd

4.9 Power Requirements

The power supply has four designated pins, VccT, VccT1 VccR, VccR1 in the connector. Power is applied concurrently to VccT, VccR in the row for channel 1 and concurrently to VccT1, VccR1 in the row for channel 2.

A host board together with the SFP-DD module(s) forms an integrated power system. The host supplies stable power to the module. The module limits electrical noise coupled back into the host system and limits inrush charge/current during hot plug insertion.

All power supply requirements in Table 8 shall be met at the maximum power supply current. No power sequencing of the power supply is required of the host system since the module sequences the contacts in the order of ground, supply and signals during insertion.

4.9.1 Power Classes and Maximum Power Consumption

There are multiple power classes as defined in Table 7. Since different classes of modules exist with pre-defined maximum power consumption limits, it is necessary to avoid exceeding the system power supply limits and cooling capacity when a module is inserted into a system designed to only accommodate lower power modules. It is recommended that the host identify the power class of the module before allowing the module to go into high power mode.

Power levels associated with classifications of modules are shown in Table 7.

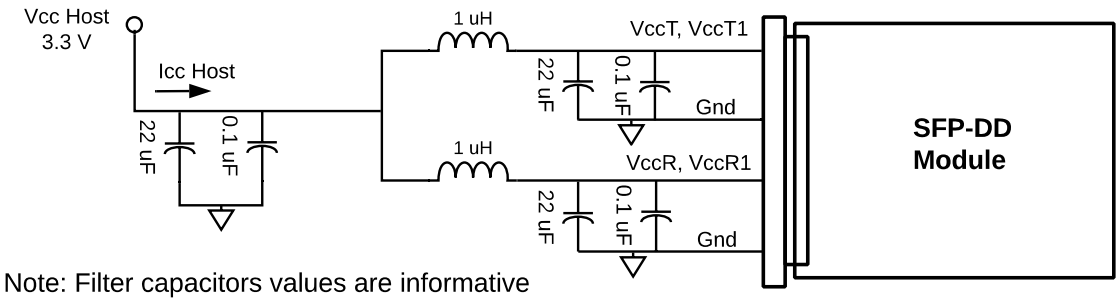
Table 7- Power Classification

Power Class	Max Power (W)
1	1.0
2	1.5
3	2.0
4	3.5
5	5.0
6	reserved
7	reserved
8	See management register for maximum power consumption.

In general, the higher power classification levels are associated with higher data rates and longer reaches. The system designer is responsible for ensuring that the maximum case temperature does not exceed the case temperature requirements.

4.9.2 Host Board Power Supply Filtering

The host board should use the power supply filtering equivalent to that shown in Figure 12.



Note: Filter capacitors values are informative and vary depending on applications.

Note: VccT, VccT1 may be connected to VccR, VccR1 provided the applicable derating of the maximum current limit is used.

Figure 12: Recommended Host Board Power Supply Filtering

Any voltage drop across a filter network on the host is counted against the host DC set point accuracy specification. Inductors with DC Resistance of less than 0.1 Ohm should be used in order to maintain the required voltage at the Host Card Edge Connector. It is recommended that the 22 μF capacitors each have an equivalent series resistance of 0.22 ohms.

The specifications for the power supply are shown in Table 8. The limits in Table 8 apply to the combined current that flows through all inductors in the power supply filter (represents ICC host in Figure 12). An example test method for measuring inrush current can is Keysight Technologies application brief 5991-2778EN.pdf.

4.9.3 Module Power Supply Specification

In order to avoid exceeding the host system power capacity, upon hot-plug, power cycle or reset, all SFP-DD modules shall power up in Low Power Mode if LPMode is asserted. If LPMode is not asserted the module will proceed to High Power Mode without host intervention. Figure 13 shows waveforms for maximum instantaneous, sustained and steady state currents for Low Power and High Power modes. Specification values for maximum instantaneous, sustained and steady state currents at each power class are given in Table 8.

Table 8- Power Supply specifications, Instantaneous, sustained and steady state current limits

Parameter	Symbol	Min	Nom	Max	Unit
Power supply voltages VccTx, VccTx1, VccRx, VccRx1 including ripple, droop and noise below 100 kHz[1]		3.135	3.3	3.465	V
Host RMS noise output 10 Hz-10 MHz				25	mV
Module RMS noise output 10 Hz - 10 MHz				15	mV
Module power supply noise tolerance 10 Hz - 10 MHz (peak-to-peak)	$PSNR_{mod}$			66	mV
Module inrush - instantaneous peak duration	T_ip			50	µs
Module inrush - initialization time	T_init			500	ms
Low Power Mode[2]					
Power Consumption	P_lp		.5		W
Instantaneous peak current at hot plug	Icc_ip_lp	-	200		mA
Sustained peak current at hot plug	Icc_sp_lp	-	165		mA
Steady state current	Icc_lp		See Note 4		mA
High Power Class 1 module					
Power Consumption	P_1		1.0		W
Instantaneous peak current	Icc_ip_1	-	400		mA
Sustained peak current	Icc_sp_1	-	330		mA
Steady state current	Icc_1		See Note 4		mA
High Power Class 2 module					
Power Consumption	P_2		1.5		W
Instantaneous peak current	Icc_ip_2	-	600		mA
Sustained peak current	Icc_sp_2	-	495		mA
Steady state current	Icc_2		See Note 4		mA
High Power Class 3 module					
Power Consumption	P_3		2.0		W
Instantaneous peak current	Icc_ip_3	-	800		mA
Sustained peak current	Icc_sp_3	-	660		mA
Steady state current	Icc_3		See Note 4		mA
High Power Class 4 module					
Power Consumption	P_4		3.5		W
Instantaneous peak current	Icc_ip_4	-	1400		mA
Sustained peak current	Icc_sp_4	-	1155		mA
Steady state current	Icc_4		See Note 4		mA
High Power Class 5 module					
Power Consumption	P_5		5.0		W
Instantaneous peak current	Icc_ip_5	-	2000		mA
Sustained peak current	Icc_sp_5	-	1650		mA
Steady state current	Icc_5		See Note 4		mA
High Power Class 8 module					
Power Consumption	P_8[3]				W
Instantaneous peak current	Icc_ip_8	-	-	P_8/2.5	A
Sustained peak current	Icc_sp_8	-	-	P_8/3.03	A
Steady state current	Icc_8	-	-	4	A

Notes:
1. Measured at VccT, VccR, VccT1, and VccR1.
2. Host designers are responsible for handling 1.5W Low Power Mode SFP(INF-8074i)/SFP+(SFF-8431) legacy modules as appropriate in their system.
3. User must read management register for maximum power consumption.
4. The module must stay within its declared power class.

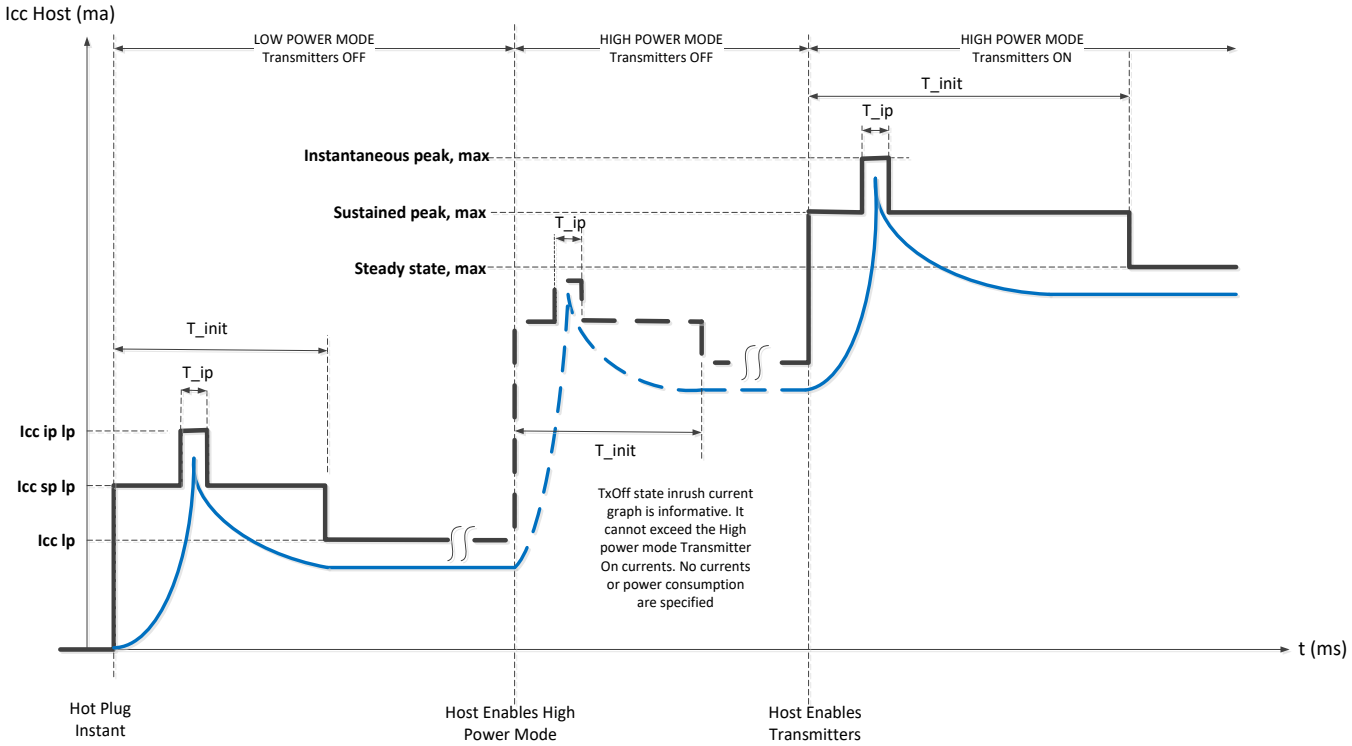


Figure 13: Instantaneous and sustained peak currents for Icc Host (see Fig. 6)

4.9.4 Host Board Power Supply Noise Output

The host shall generate an effective weighted integrated spectrum RMS noise less than the value in Table 8 when tested by the methods of SFF-8419, see A.1.1.

4.9.5 Module Power Supply Noise Output

The SFP-DD module shall generate less than the value in Table 8 when tested by the methods of SFF-8419, see A.1.2. Note: The series resister value may need to be reduced for high power modules.

4.9.6 Module Power Supply Noise Tolerance

The SFP-DD module shall meet all requirements and remain fully operational in the presence of a sinusoidal tolerance signal of amplitude given by Table 8, swept from 10 Hz to 10 MHz according to the methods of SFF-8419, see A.1.1. This emulates the worst case noise output of the host.

4.10 ESD

Where ESD performance is not otherwise specified, e.g. in the InfiniBand specification, the SFP-DD module shall meet ESD requirements given in EN61000-4-2, criterion B test specification when installed in a properly grounded cage and chassis. The units are subjected to 15 kV air discharges during operation and 8 kV direct contact discharges to the case. All the SFP-DD module and host pins including high speed signal pins shall withstand 1000 V electrostatic discharge based on Human Body Model per ANSI/ESDA/JEDEC JS-001.

5. Optical Port Mapping and Optical Interfaces

5.1 Electrical data input/output to optical port mapping

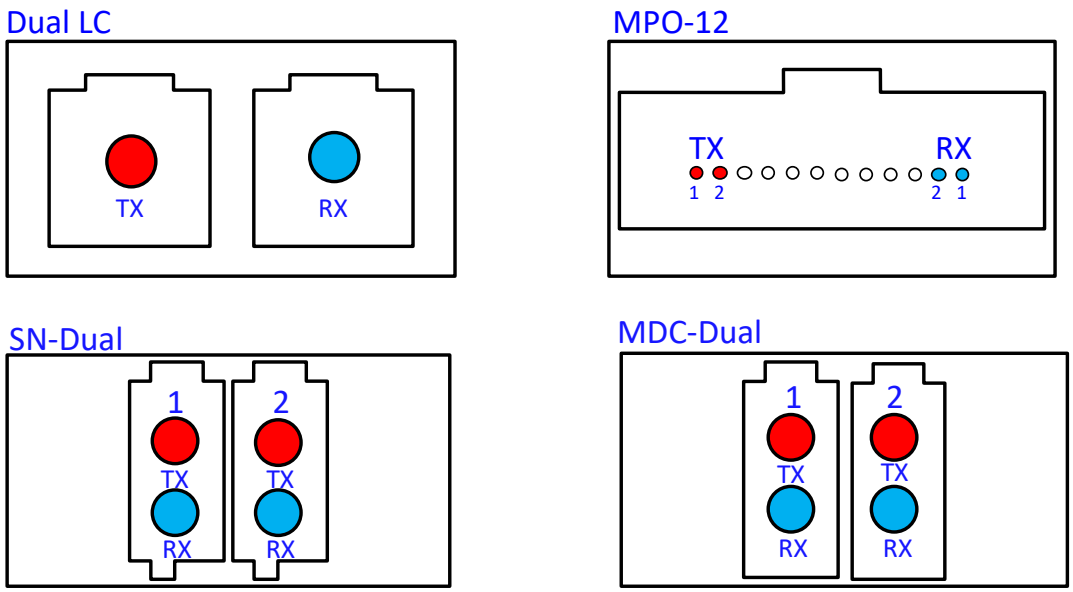
Table 9 defines the mapping of electrical TX data inputs to optical ports. The mapping of the RX optical ports to electrical RX outputs is symmetric. Note that there is no defined mapping of electrical input/output to optical wavelengths for WDM applications.

Table 9- Electrical data input to Optical Port Mapping

Electrical Data Input Reference	LC, SN, MDC	SN, MDC, MPO-12
	1 TX fiber	2 TX fibers
TD0+/-	TX-1	TX-1
TD1+/-		TX-2

5.2 Optical Interface

Four examples of the SFP-DD optical interface port are a male MPO receptacle (see Figure 24), a dual LC (see Figure 16), a SN receptacle (see Figure 17), or a MDC receptacle (see Figure 18). The recommended location and numbering of the optical ports for each of the Media Dependent Interfaces is shown in Figure 14.



Note: The transmit and receive optical lanes shall occupy the positions depicted here when looking into the MDI receptacle with the connector keyway feature on top.

Figure 14: Optical Media Dependent Interface port assignments

5.2.1 MPO Optical Cable connections

The optical plug and receptacle for the MPO-12 connector is specified in TIA-604-5, IEC 61754-7 and shown in Figure **15**. Note: Two alignment pins are present in each receptacle.

Aligned keys are used to ensure alignment between the modules and the patchcords. The optical connector is orientated such that the keying feature of the MPO receptacle is on the top.

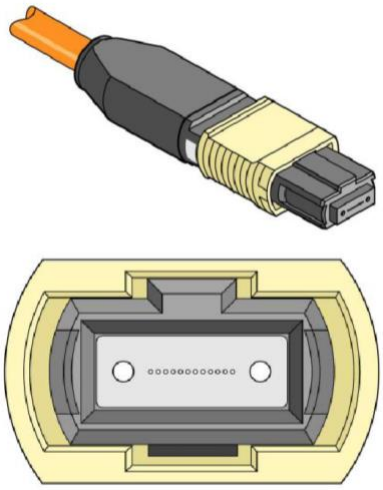


Figure 15**: MPO-12 Single Row optical patch cord and module receptacle**

5.2.2 Dual LC Optical Cable connection

The Dual LC optical patchcord and module receptacle is specified in TIA-604-10, IEC 61754-20 and shown in Figure 16.

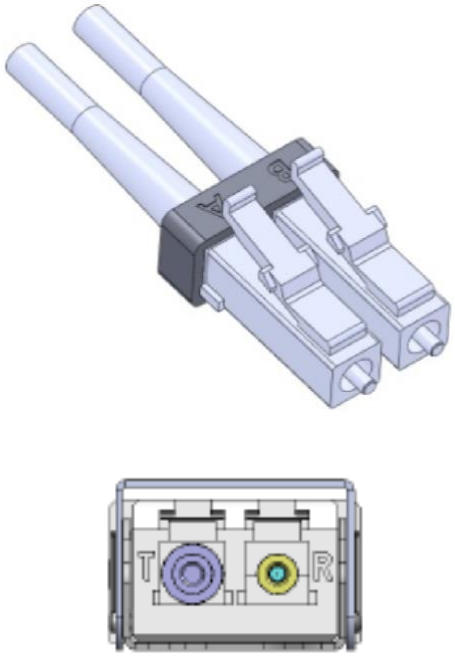


Figure 16: Dual LC optical patchcord and module receptacle

5.2.3 SN Optical Cable connections

The SN optical connector and receptacle for SFP-DD module is specified in SN-60092019 and shown in Figure 26. The top key and offset bottom key are used to ensure alignment between the modules and the patch cords.

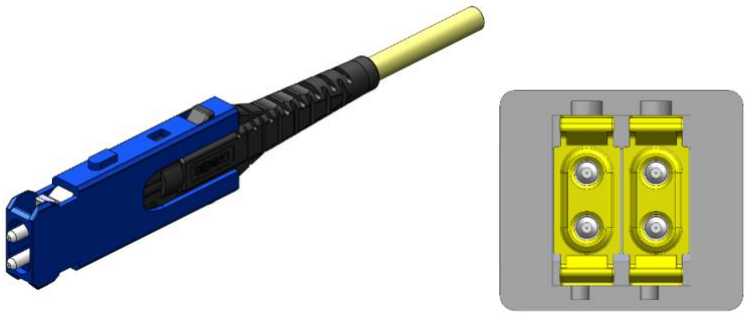


Figure 17: SN optical connector plug and two-port module receptacle

5.2.4 MDC Optical Cable connections

The MDC optical plug and receptacle for a SFP-DD module is specified in USC-11383001 and shown in Figure 27. The optical connector is orientated such that the keying feature of the MDC receptacle is on the top.

Figure 18: MDC optical connector plug and two-port module receptacle

5.3 Module Color Coding and Labeling

If provided, color coding shall be on an exposed feature of the SFP-DD module (a feature or surface extending outside of the bezel). Color code are outside the scope of this specification.

Each SFP-DD module shall be clearly labeled. The complete labeling need not be visible when the SFP-DD module is installed and the bottom of the device is the recommended location for the label. Labeling shall include:

- Appropriate manufacturing and part number identification
- Appropriate regulatory compliance labeling
- A manufacturing traceability code.

The label should also include clear specification of the external port characteristics such as:

- Optical wavelength
- Required fiber characteristics
- Operating data rate
- Interface standards supported
- Link length supported.

The labeling shall not interfere with the mechanical, thermal or EMI features.

6. Mechanical and Board Definition

6.1 Introduction

The cages and modules specifications defined in this chapter are illustrated in Figure 19 (press fit cage) and Figure 20 (pluggable module). All Pluggable modules and direct attach cable plugs must mate to the connectors and cages defined in this specification. (See SFF-8432 for details) Heat sink/clip thermal designs are application specific and not specifically defined by this specification. The SFP-DD module and cage support both a pull tab and a bail latch solution. Details on bail latch retention and extraction specifications can be found in SFF-8432.

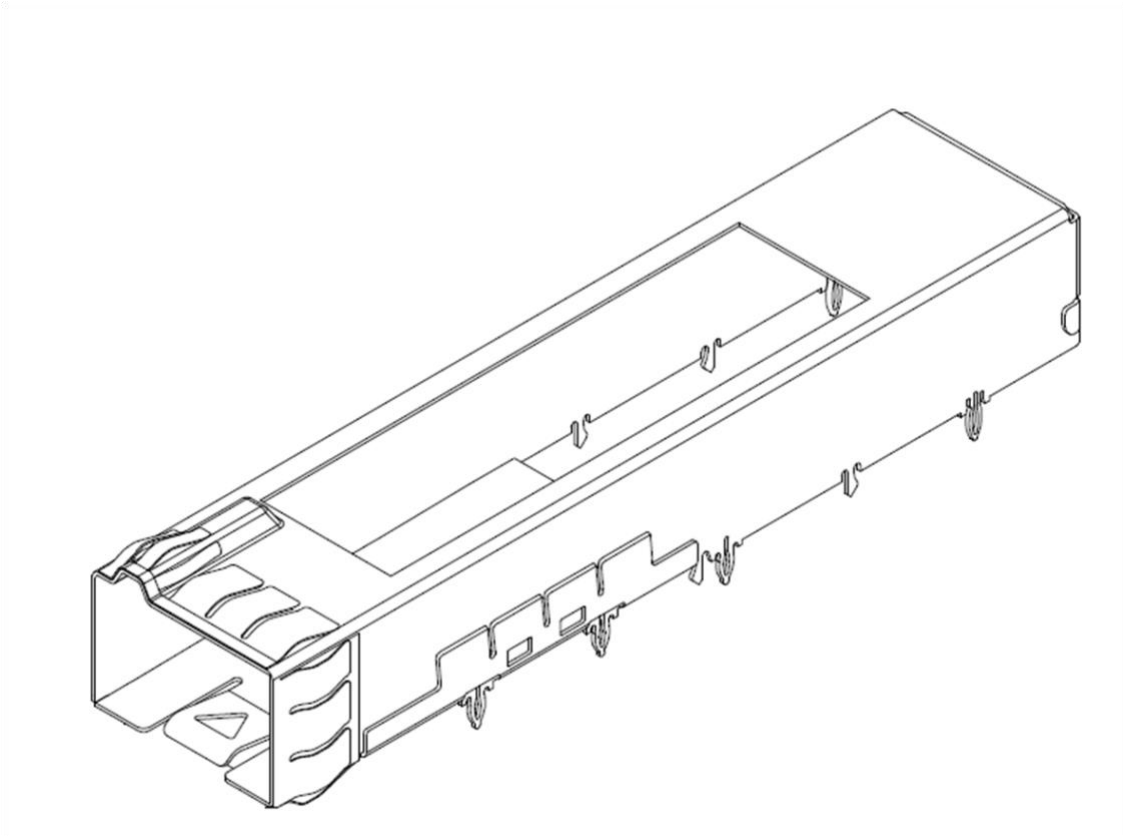
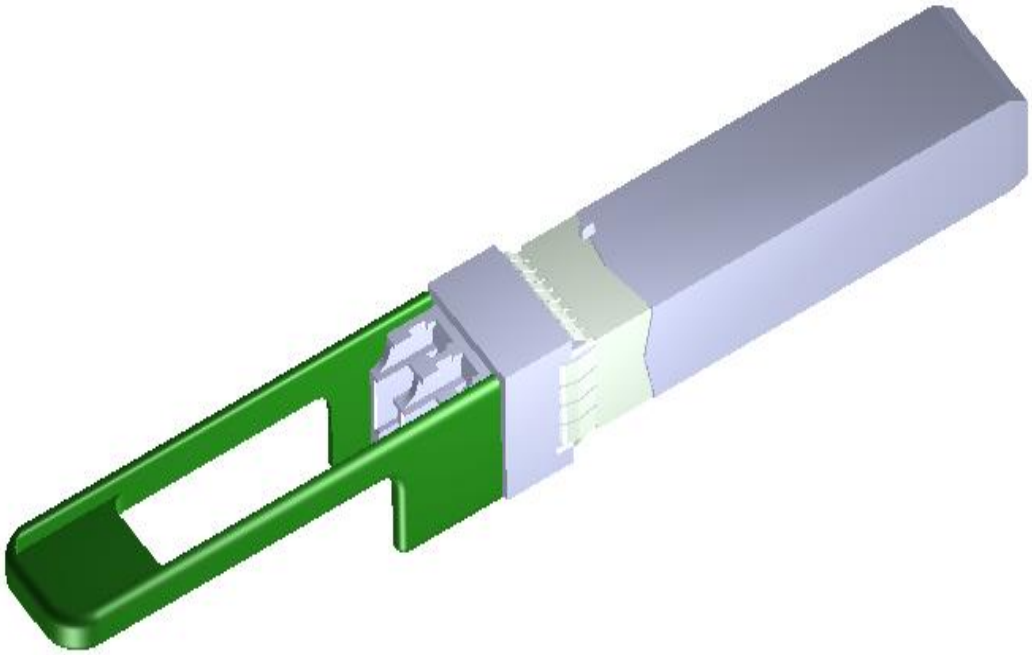
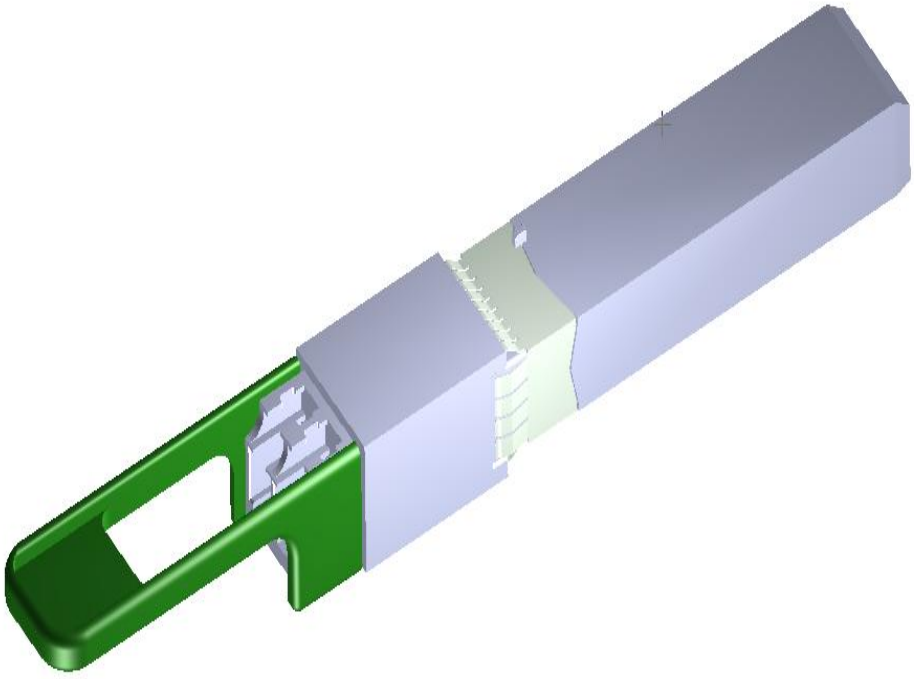


Figure 19: Press fit cage



Type 1 module



Type 2 module

Figure 20: Modules

Table 10- Datum Description

Datum	Description
A	Width Of module
B	Bottom surface of module
C	Leading edge of signal contact pads on module paddle card
D	Hard stop on module
E	Host board thru hole to accept primary cage press fit pin
F	Hard stop on cage
G	Bottom surface of bezel cutout
K	Host board thru hole #1 to accept connector guidepost
L	Host board thru hole #2 to accept connector guidepost
P	Vertical center line of internal surface of cage
S	Seating plane of cage on host board
Z	Top surface of host board
AA	Center line of module paddle card width
BB	Top surface of module paddle card
CC	Center line of connector slot width
DD	Seating plane of connector on host board

6.2 Cage, Connector, Module Alignment

The alignment of the cage, connector and module are shown in Figure 21.

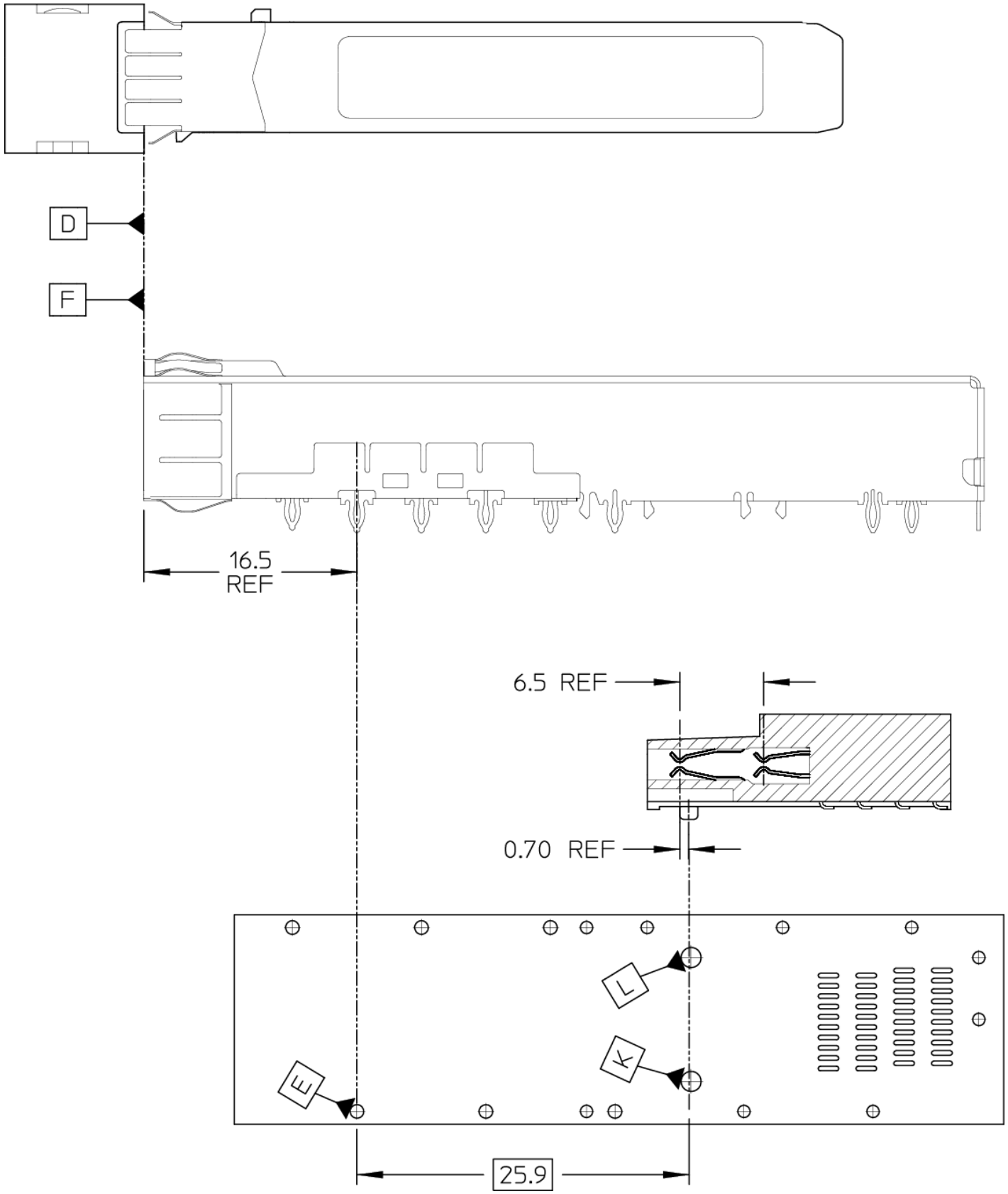
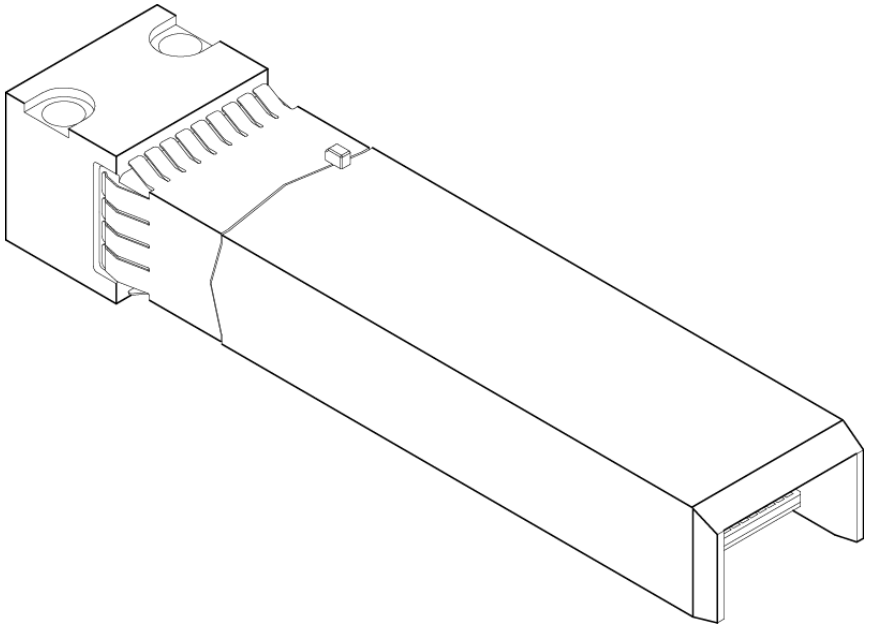


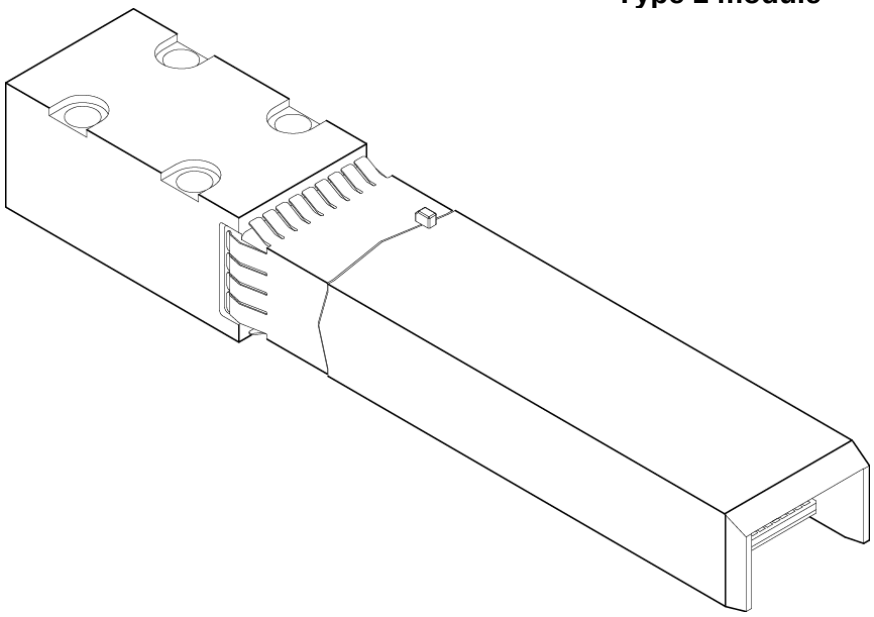
Figure 21: Cage, Connector alignment

6.3 Module Mechanical Dimensions

The mechanical outline for the SFP-DD module and direct attach cables is shown in Figure 22. The module shall provide a means to self-lock with the cage upon insertion. The module package dimensions are defined in Figure 23. The dimensions that control the size of the module that extends outside of the cage are listed as maximum dimensions per Note 4 in Figure 23.



Type 1 module



Type 2 module

Figure 22: Type 1 and Type 2 Modules

NOTES APPLY TO MODULE DRAWINGS :

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2009

2. SHARP CORNERS AND EDGES ARE NOT ALLOWED. ROUND OFF ALL EDGES AND CORNERS.

3 RECOMMENDED MAXIMUM. MODULE LENGTH EXTENDING OUTSIDE OF CAGE. OTHER LENGTHS ARE APPLICATION SPECIFIC.

4 INDICATED OUTLINE DEFINES MAXIMUM ENVELOP OUTSIDE THE CAGE. THE SURFACES OF THE MAXIMUM ENVELOP MAY BE CONTACTED BY AN ADJACENT MODULE EMI SPRINGS DURING INSERTION AND EXTRACTION OF THE MODULE FROM THE CAGE. THE SURFACES SHALL NOT HAVE ANY SHAPES OR MATERIALS THAT CAN DAMAGE THE ADJACENT MODULE EMI SPRINGS OR BE DAMAGED THEMSELVES BY THE SPRINGS.

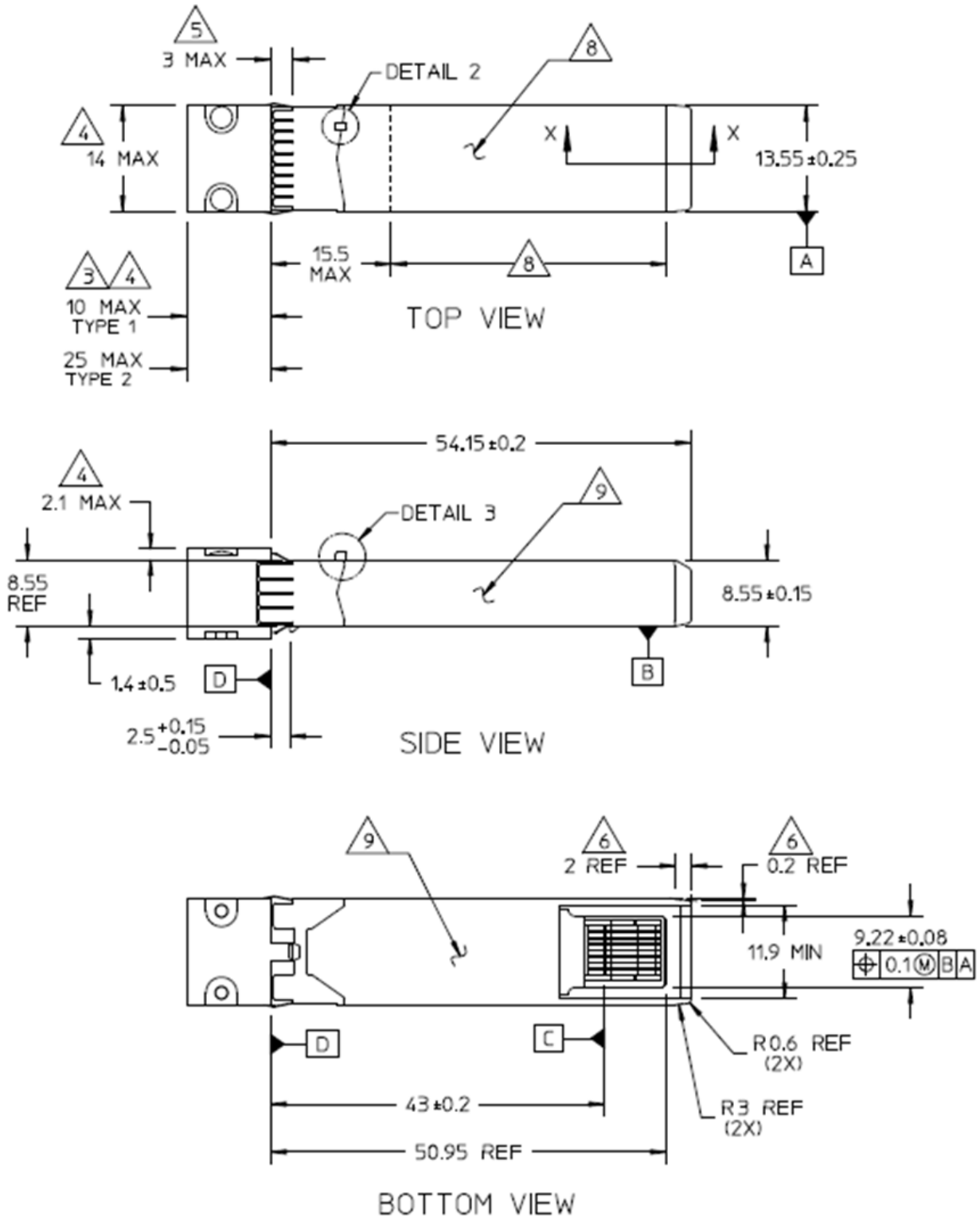
5 DIMENSIONS DEFINES EMI SPRING CONTACT POINT WITH MODULE CAGE.

6 LEAD-IN CHAMFER DIMENSION MEASURED FROM TSC (THEORETICAL SHARP CORNER).

7 BLOCKING RIB FEATURE TO PREVENT SFP-DD MODULE FROM MATING INTO LEGACY SFP CONNECTOR.

8 FLATNESS SPECIFICATION APPLIES OVER THE ENTIRE HEAT SINK AREA. REFER TO SECTION 5.4 TABLE 9FOR FLATNESS REQUIREMENTS.

9 PRODUCT LABEL ON BOTTOM AND/OR SIDES TO BE FLUSHED OR RECESSED BELOW EXTERNAL SURFACES. LABEL(S) SHALL NOT INTERFERE WITH THE MECHANICAL, THERMAL, OR EMC PROPERTIES.


5
3 MAX
DETAIL 2
8
4
14 MAX
X
X
13.55±0.25
15.5
MAX
8
A
3
4
10 MAX
TYPE 1
25 MAX
TYPE 2
TOP VIEW
54.15±0.2
4
2.1 MAX
DETAIL 3
9
8.55
REF
8.55±0.15
1.4±0.5
D
B
2.5 +0.15 −0.05
SIDE VIEW
9
6
2 REF
6
0.2 REF
11.9 MIN
9.22±0.08
0.1 M B A
D
C
R0.6 REF
(2X)
43±0.2
R3 REF
(2X)
50.95 REF
BOTTOM VIEW

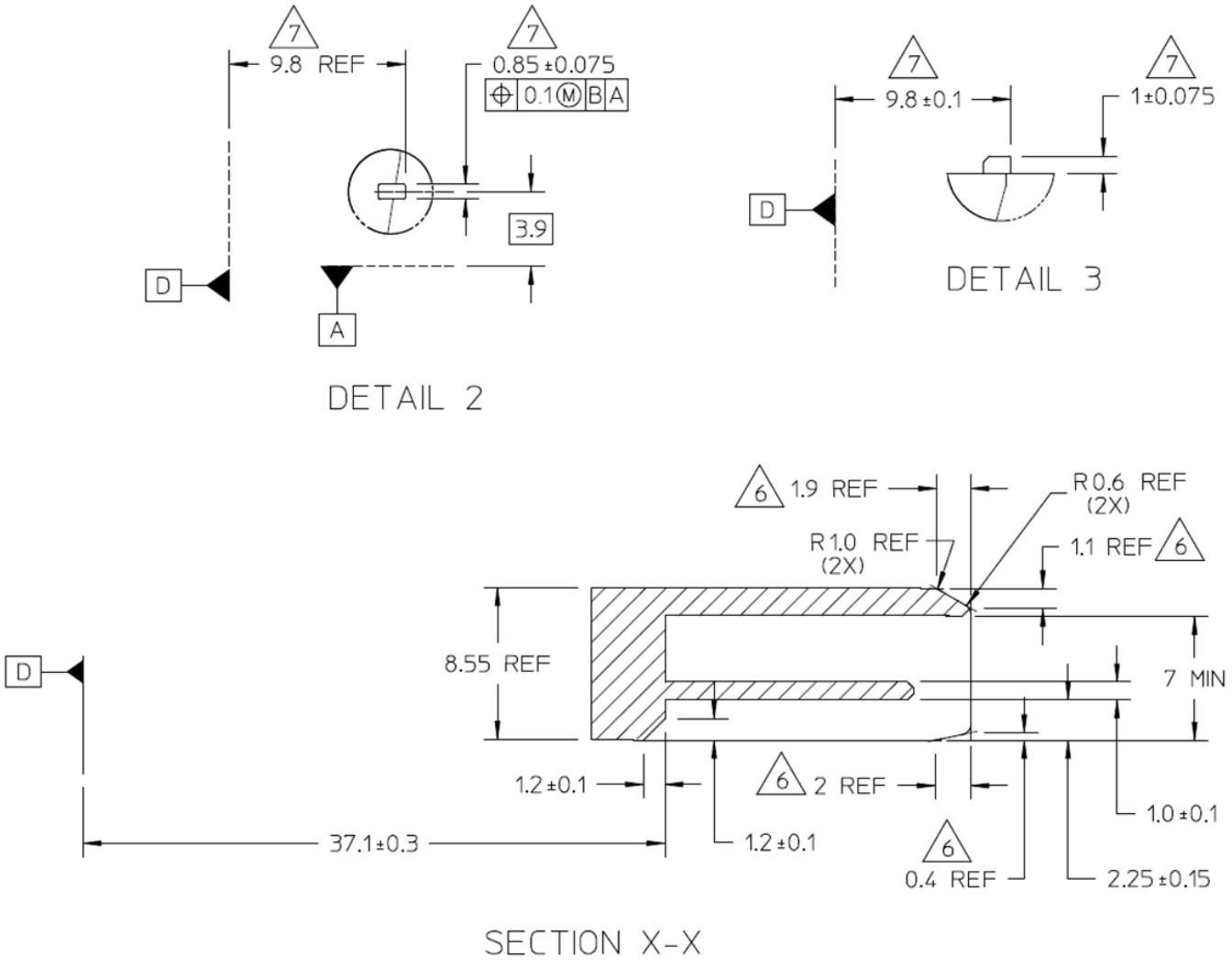


Figure 23: Detailed dimensions of module

6.4 Module Flatness and Roughness

Module flatness and roughness are specified to improve module thermal characteristics when used with a riding heat sink. Relaxed specifications are used for lower power modules to reduce cost. The module flatness and roughness specifications apply to the specified heat sink contact area as specified in Figure 23. Specifications for Module flatness and surface roughness are shown in Table 11.

Table 11- Module flatness specifications

Power Class	Module Flatness (mm)	Surface Roughness (Ra,µm)
1	0.075	1.6
2	0.075	1.6
3	0.075	1.6
4	0.075	1.6
5	0.050	0.8
6	reserved	reserved
7	reserved	reserved
8	0.050	0.8

6.5 Module paddle card dimensions

NOTES APPLY TO MODULE PADDLE CARD :

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2009
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. NO SOLDER MASK WITHIN 0.05 MM OF ALL DEFINED CONTACT PAD EDGES
4. NO SOLDER MASK BETWEEN END CONTACTS AND THE SIDES OF THE PADDLE CARD
5. DATUM C IS ESTABLISHED WITH DATUM TARGET POINTS AT THE LEADING EDGE OF THE OUTER MOST SIGNAL CONTACTS PADS TO BE RE-ESTABLISHED ON EACH SIDE
6. DIMENSION APPLIES FROM THE FIRST SET OF SIGNAL PADS TO THE SECOND SET OF SIGNAL PADS
7. DIMENSION AND TOLERANCE APPLIES TO ALL PADS ON BOTH TOP AND BOTTOM SIDE OF THE PADDLE CARD
8. A ZERO GAP IS ALLOWED FOR A CONTINUOUS PAD OPTION
9. APPLIES TO ALL SIGNAL PAD TO PRE-WIPE PAD SPACING
10. PRE-WIPE PADS (SHADED AREA) ON MODULE CARD HOST SIDE ARE OPTIONAL
11. PRE-WIPE PADS (UNSHADED AREA) ARE REQUIRED EXCEPT IN CONTINUOUS POWER AND GROUND PAD DESIGNS
12. PADDLE CARD THICKNESS IS MEASURED OVER PADS VIAS MUST NOT BE PROUD OF THE PAD SURFACE
13. MINIMUM DIMENSION REQUIRED FOR MATING SEQUENCE BETWEEN SIGNAL AND GROUND PADS
14. MINIMUM DIMENSION REQUIRED FOR MATING SEQUENCE BETWEEN SIGNAL AND POWER PADS
15. COMPONENT KEEP OUT AREA MEASURED FROM DATUM C
16. A SINGLE SPLIT IN THE PRE-WIPE SIGNAL PAD IS OPTIONAL, AND IF IMPLEMENTED, THE RESULTING 2 PADS SHALL BE SEPARATED WITH A GAP OF 0.13 ± 0.05
17. PRE-WIPE PADS ENSURE ADEQUATE WIPE REQUIRED TO PROVIDE A RELIABLE ELECTRICAL INTERCONNECT WHILE MINIMIZING SIGNAL INTEGRITY STUB EFFECTS
18. CONTACT PAD PLATING
    0.38 MICROMETERS MINIMUM GOLD OVER
    1.27 MICROMETERS MINIMUM NICKEL
    ALTERNATE CONTACT PAD PLATING
    0.05 MICROMETERS MINIMUM GOLD OVER
    0.30 MICROMETERS MINIMUM PALLADIUM OVER
    1.27 MICROMETERS MINIMUM NICKEL

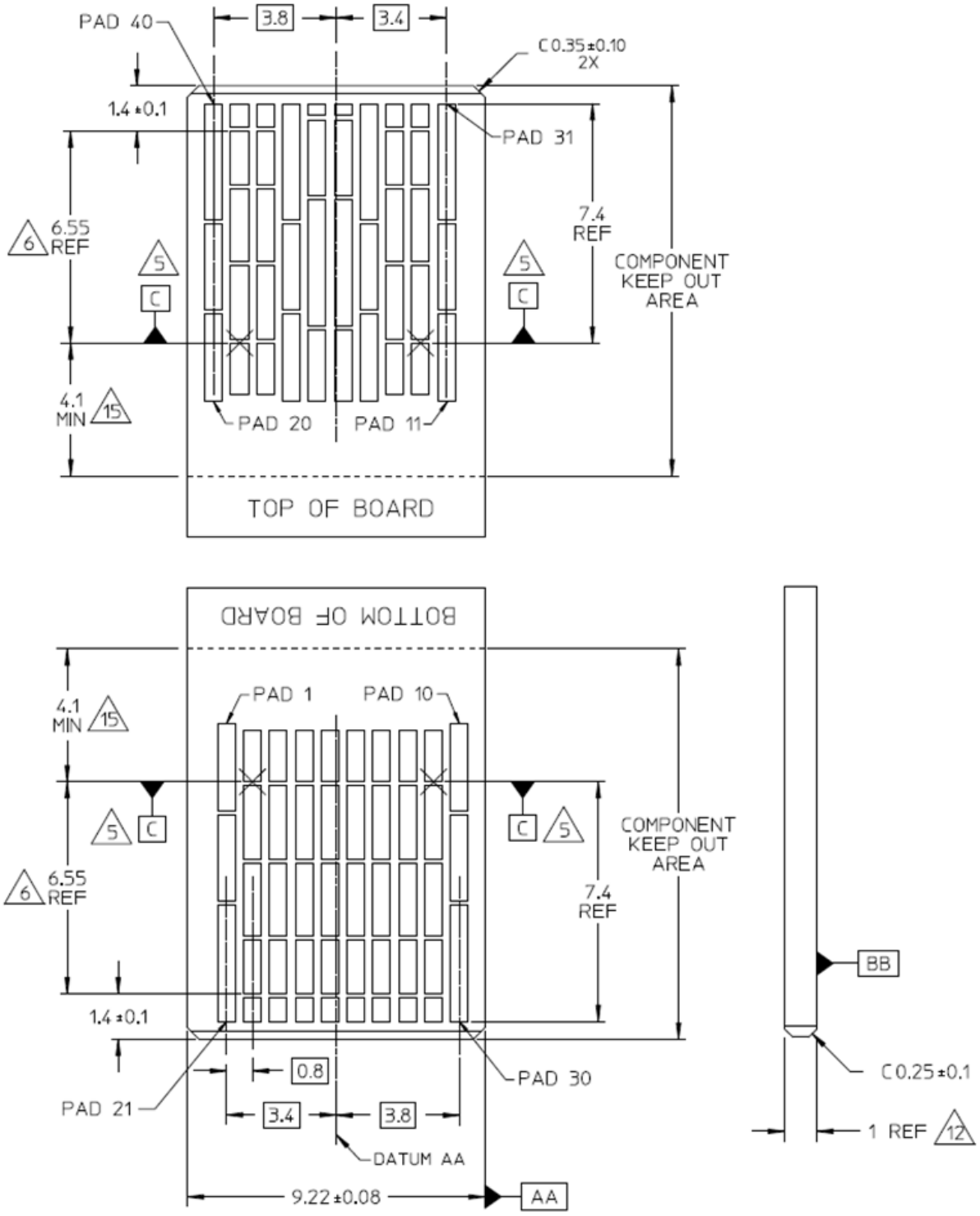


Figure 24: Module paddle card dimensions

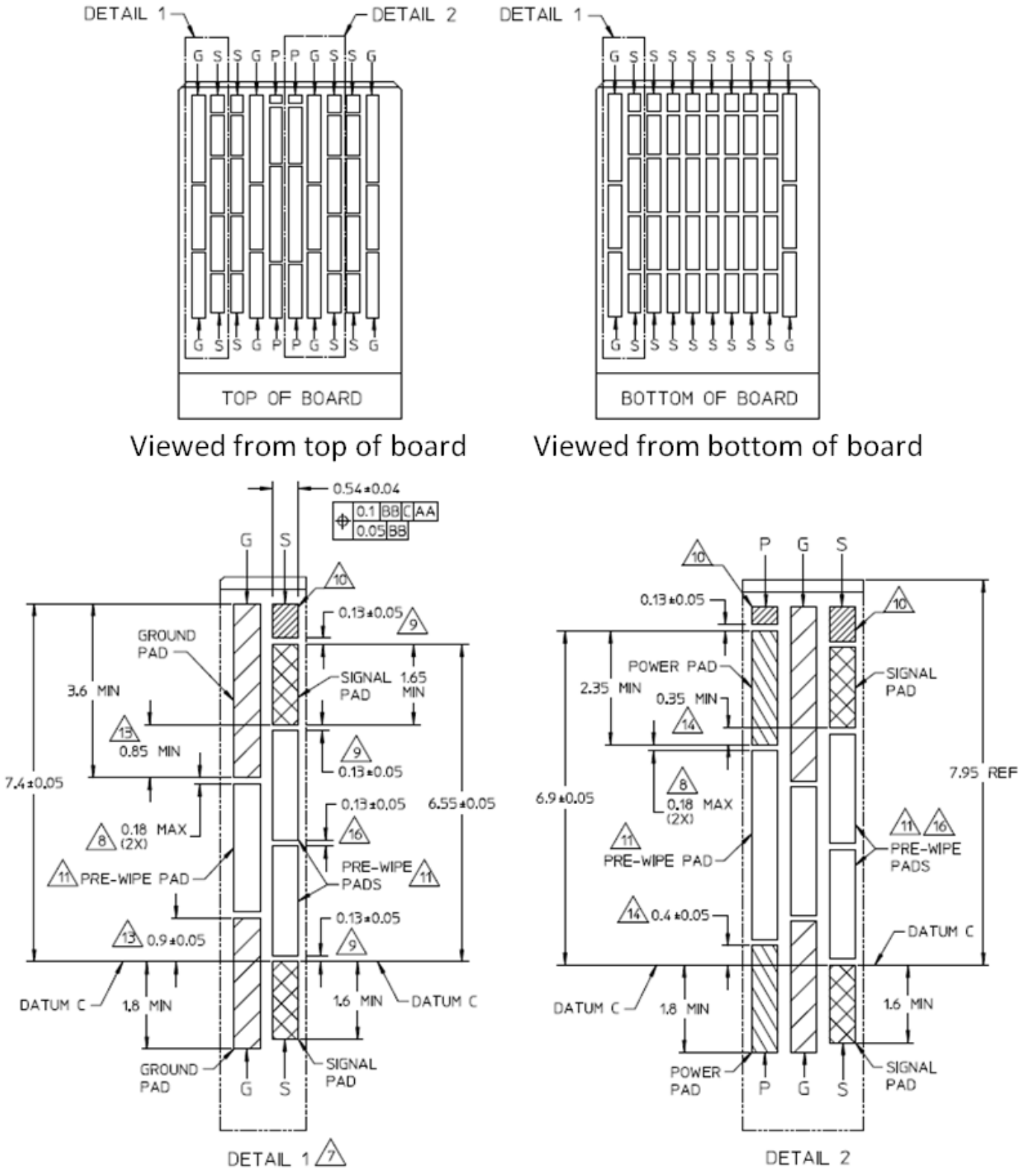


Figure 25: Module pad dimensions

6.6 Module Extraction and Retention Forces

The requirements for insertion forces, extraction forces and retention forces are specified Appendix A. The SFP-DD cage and module are designed to ensure that excessive force applied to a cable does not damage the SFP-DD cage or host connector. If any part is damaged by excessive force, it should be the cable or media module and not the cage or host connector which is part of the host system. Examples of module retention mechanisms are found in SFF-8432 Figures 4-4 through 4-7. The contact pad plating shall meet the requirements are given in 6.5.

6.7 Press fit Cage Mechanical

The SFP-DD Cage is shown in Figure 26 with detailed drawings in Figure 27. Recommendations for the cage bezel opening are shown in Figure 29.

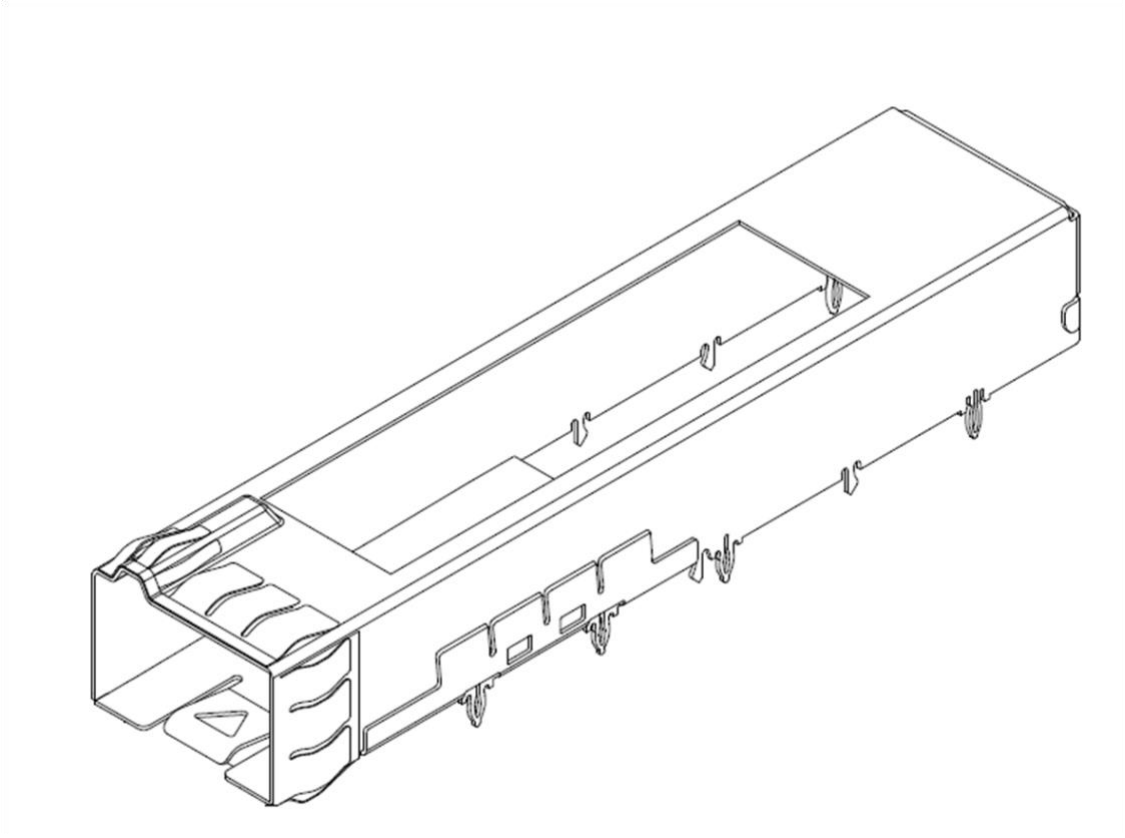


Figure 26: Press Fit 1x1 Cage

NOTES APPLY TO 1 X N CAGE DRAWINGS :

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2009

2 DATUM S IS DEFINED BY THE SEATING SURFACE ON THE HOST BOARD

3 DIMENSIONS FROM INSIDE SURFACES OF CAGE

4 SIZE AND SHAPE OF CAGE PINS SHALL BE DEFINED BY EACH SUPPLIER BASED UPON THE PCB FOOTPRINT LAYOUT

5 APPLIES TO 1.05 MM PCB HOLE DIAMETER

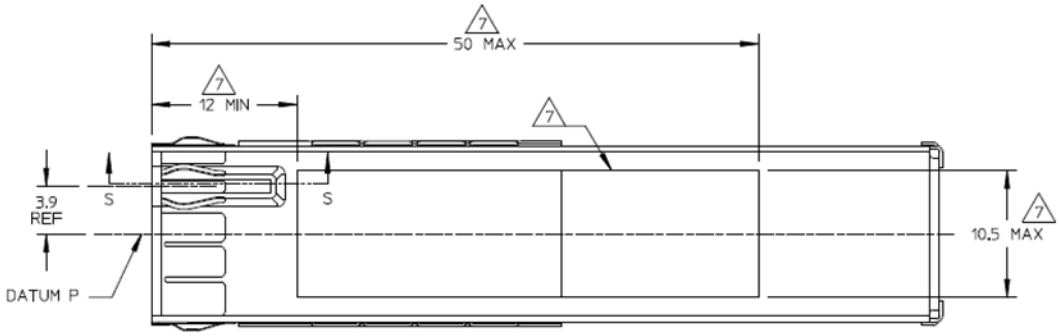
6 APPLIES TO 0.95 MM PCB HOLE DIAMETER

7 CUTOUT OPENING FOR HEAT SINK IS OPTIONAL

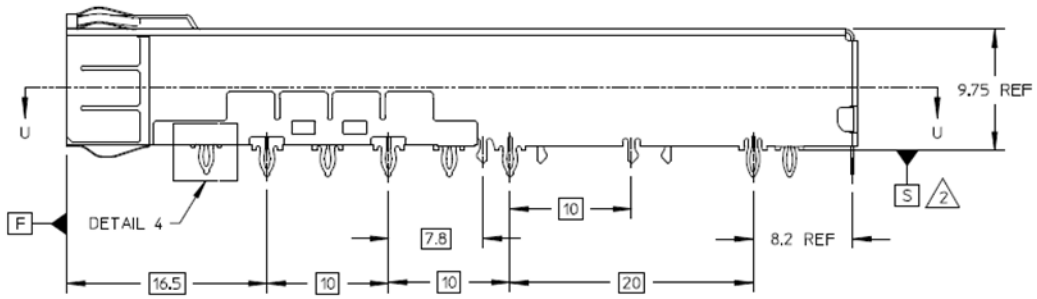
8 MAXIMUM ENVELOPE DIMENSION INCLUDES BACK COVER FOLDING TABS AND BOTTOM COVER ATTACHMENT FEATURES

9 APPLIES TO ALL RADAII SURFACES BETWEEN POINTS A AND B

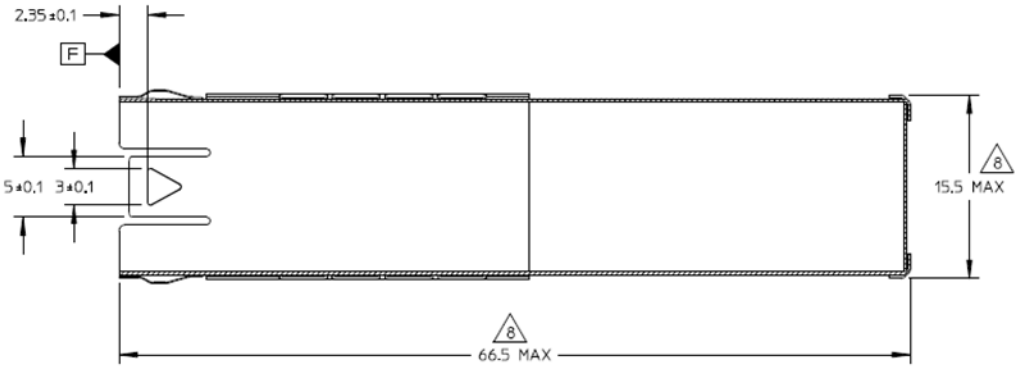
10 APPLIES TO ALL FLAT SURFACES BETWEEN POINTS A AND B



TOP VIEW



RIGHT VIEW



SECTION U-U

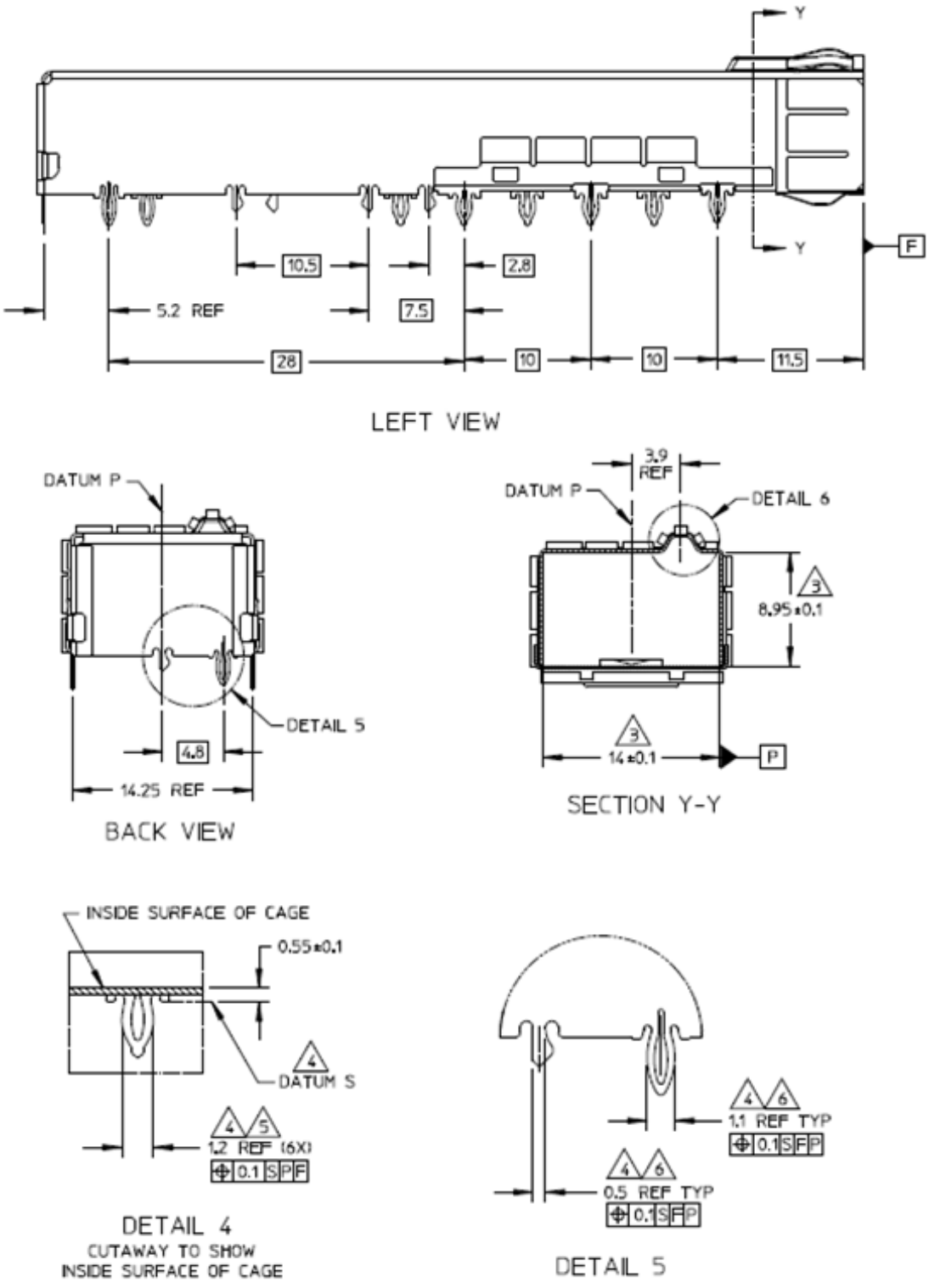


Figure 27: Press Fit 1x1 Cage Design

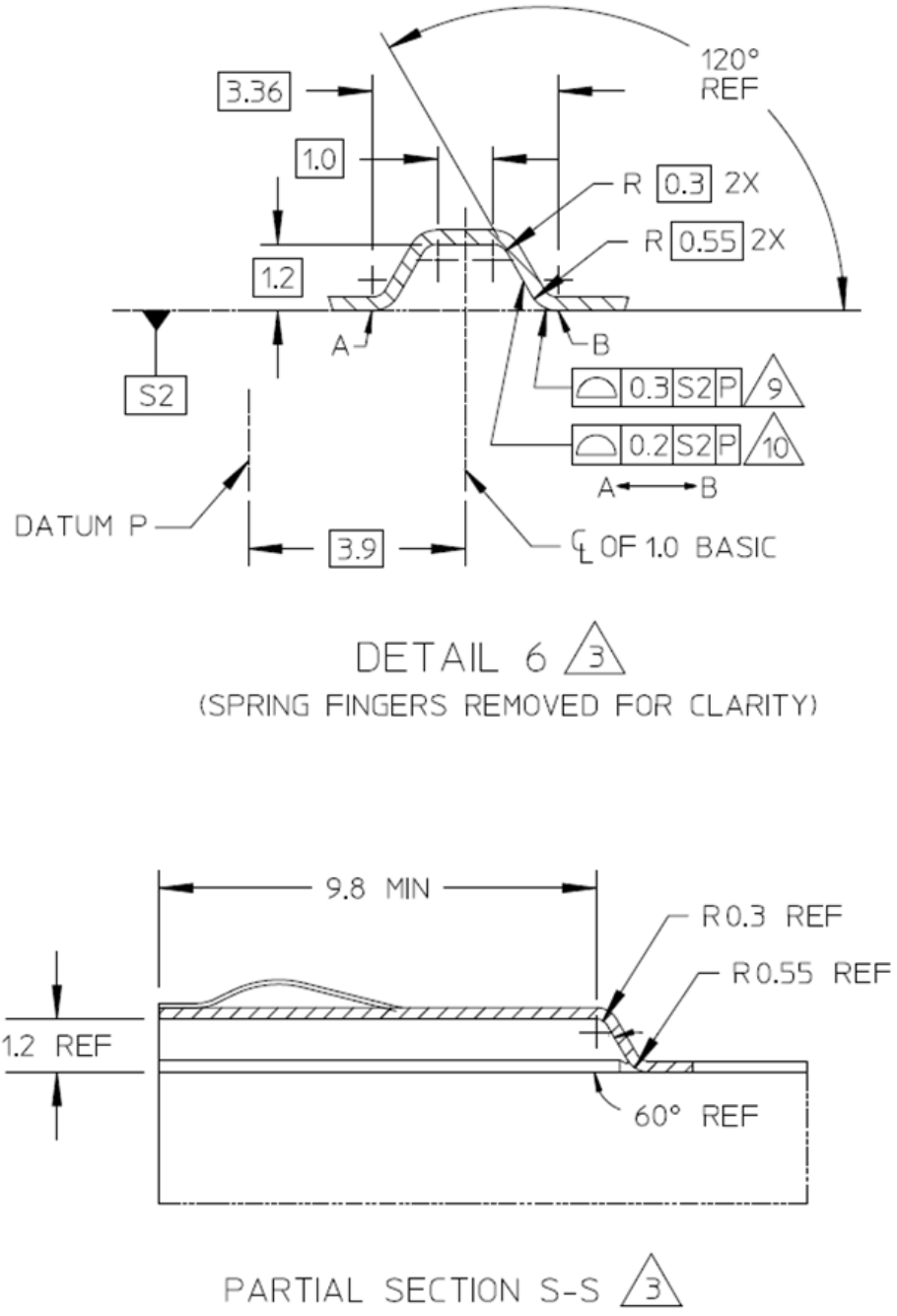


Figure 28: Press Fit Cage Detail

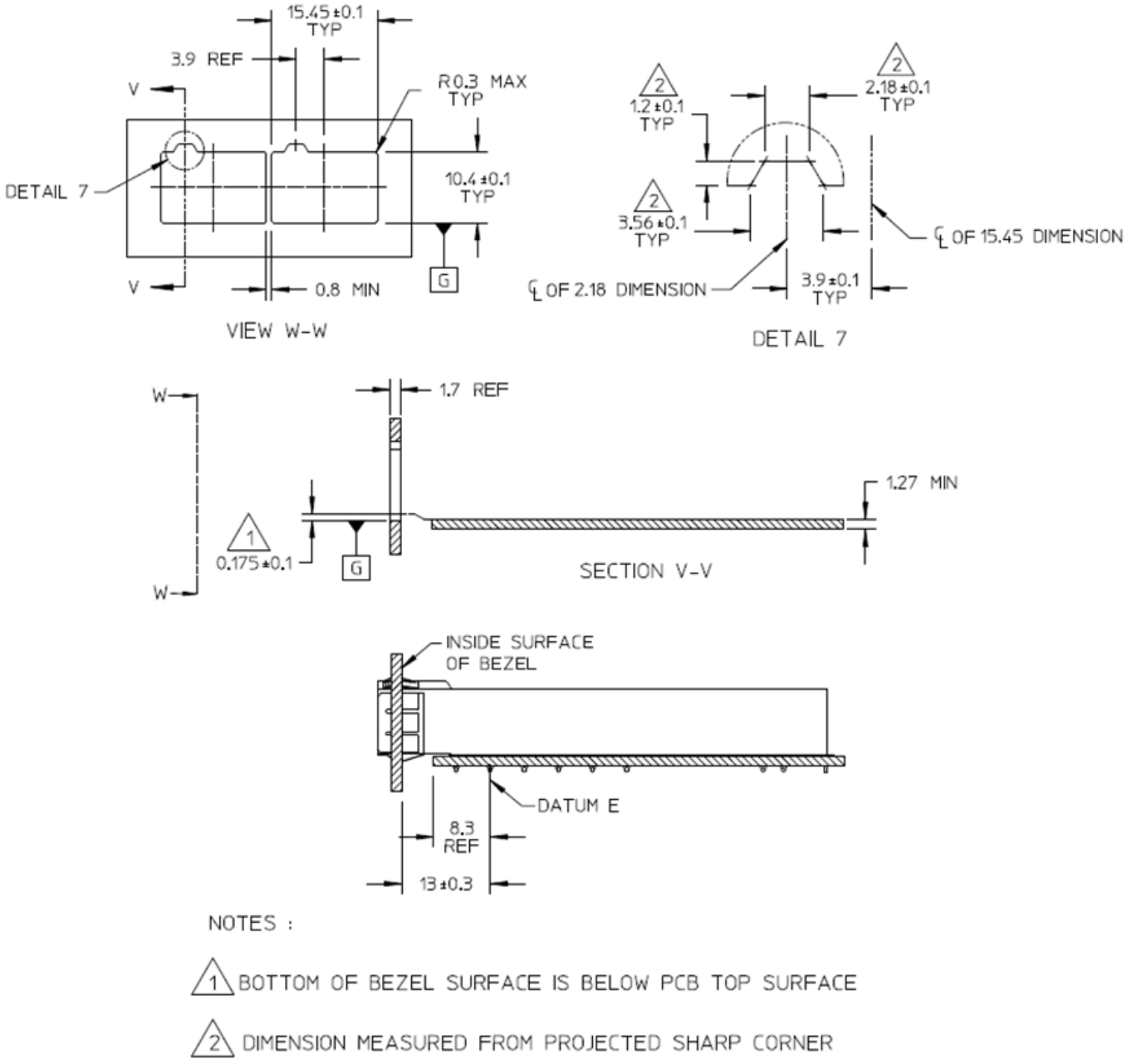


Figure 29: 1 x n bezel opening

6.8 SMT Electrical Connector Mechanical

The SFP-DD Connector is a 40-contact, right angle connector. The SMT connector is shown in Figure 30 with detailed drawings in Figure 31.

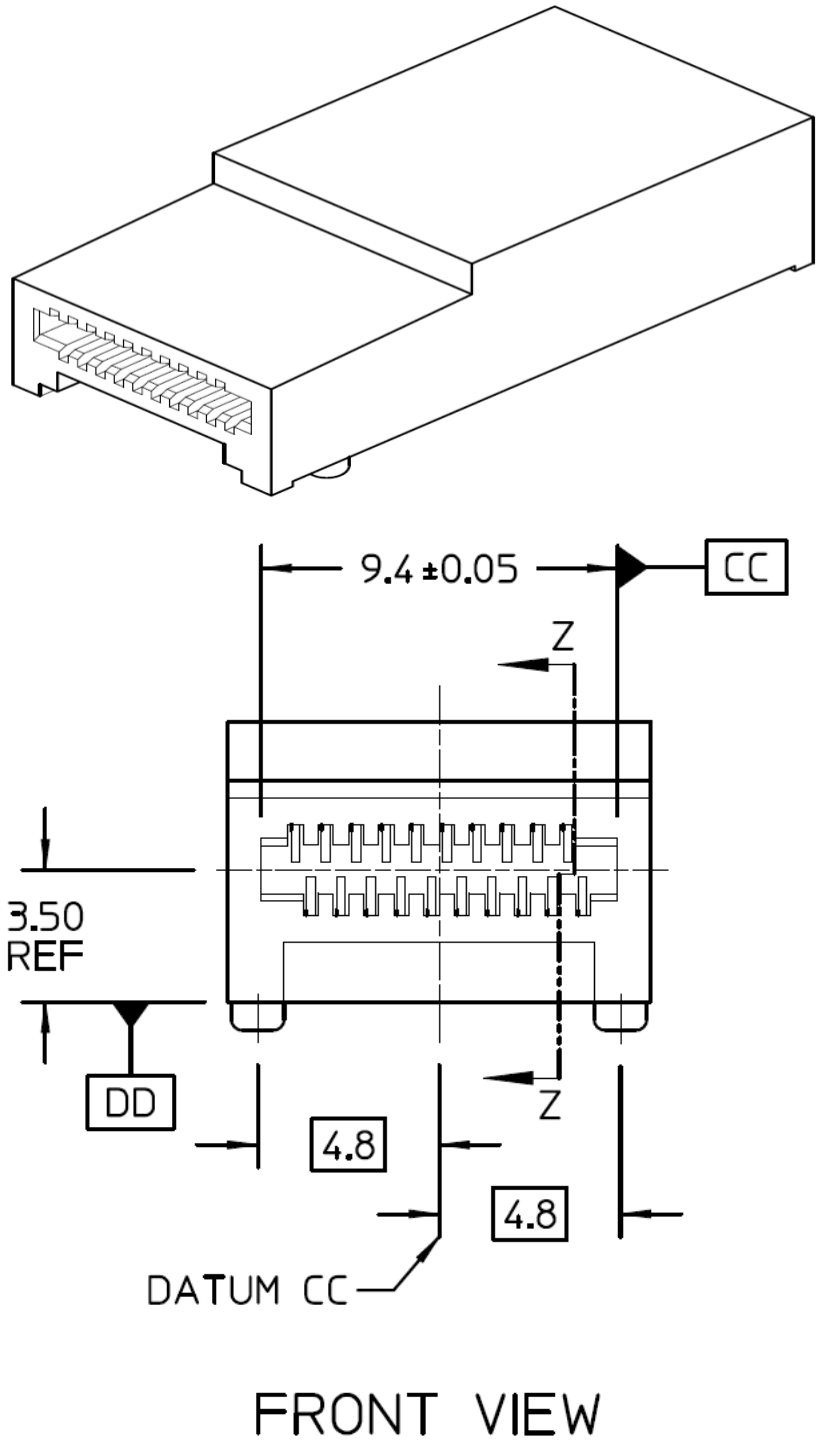
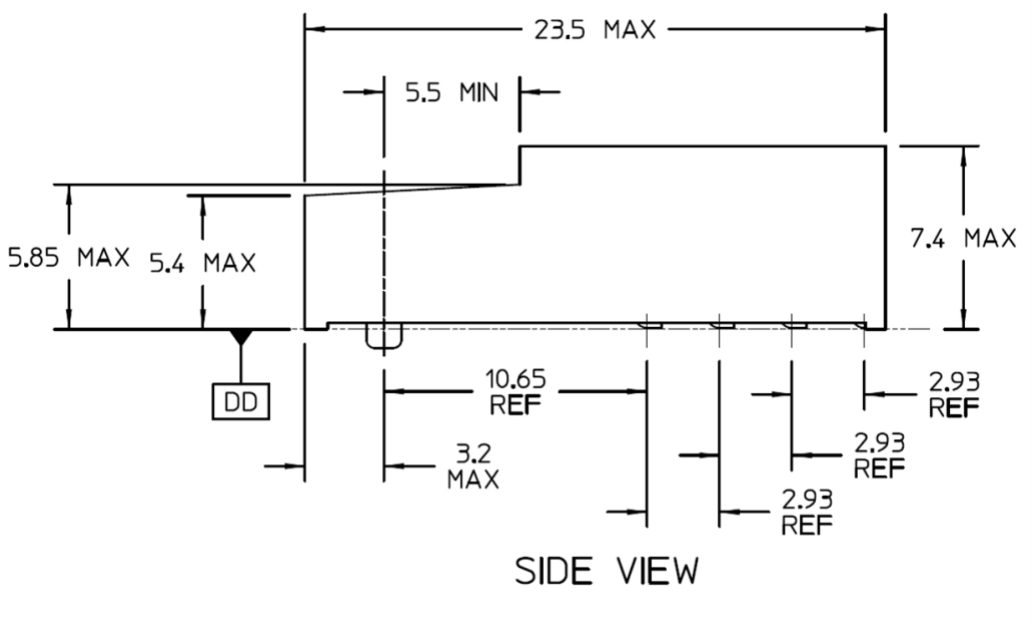
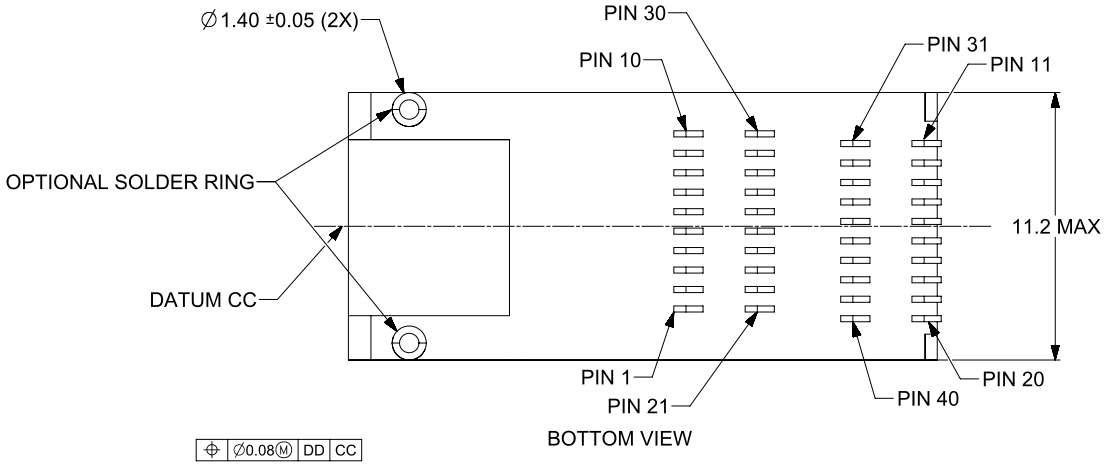


Figure 30: SMT connector


23.5 MAX
5.5 MIN
5.85 MAX
5.4 MAX
7.4 MAX
DD
10.65 REF
3.2 MAX
2.93 REF
2.93 REF
2.93 REF
SIDE VIEW


∅1.40 ±0.05 (2X)
PIN 30
PIN 10
PIN 31
PIN 11
OPTIONAL SOLDER RING
DATUM CC
11.2 MAX
PIN 1
PIN 21
PIN 40
PIN 20
BOTTOM VIEW
⌖ ∅0.08Ⓜ DD CC

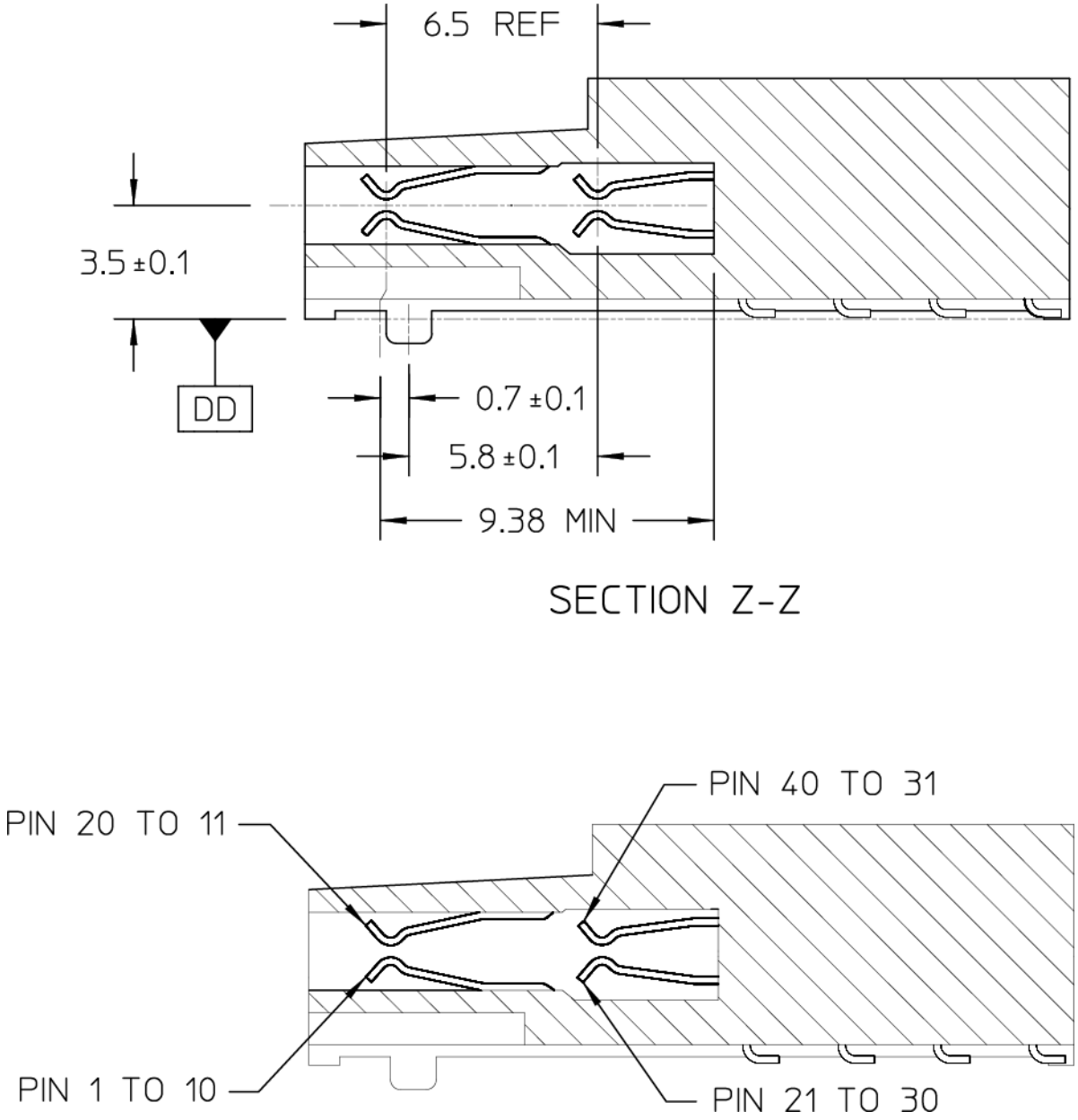
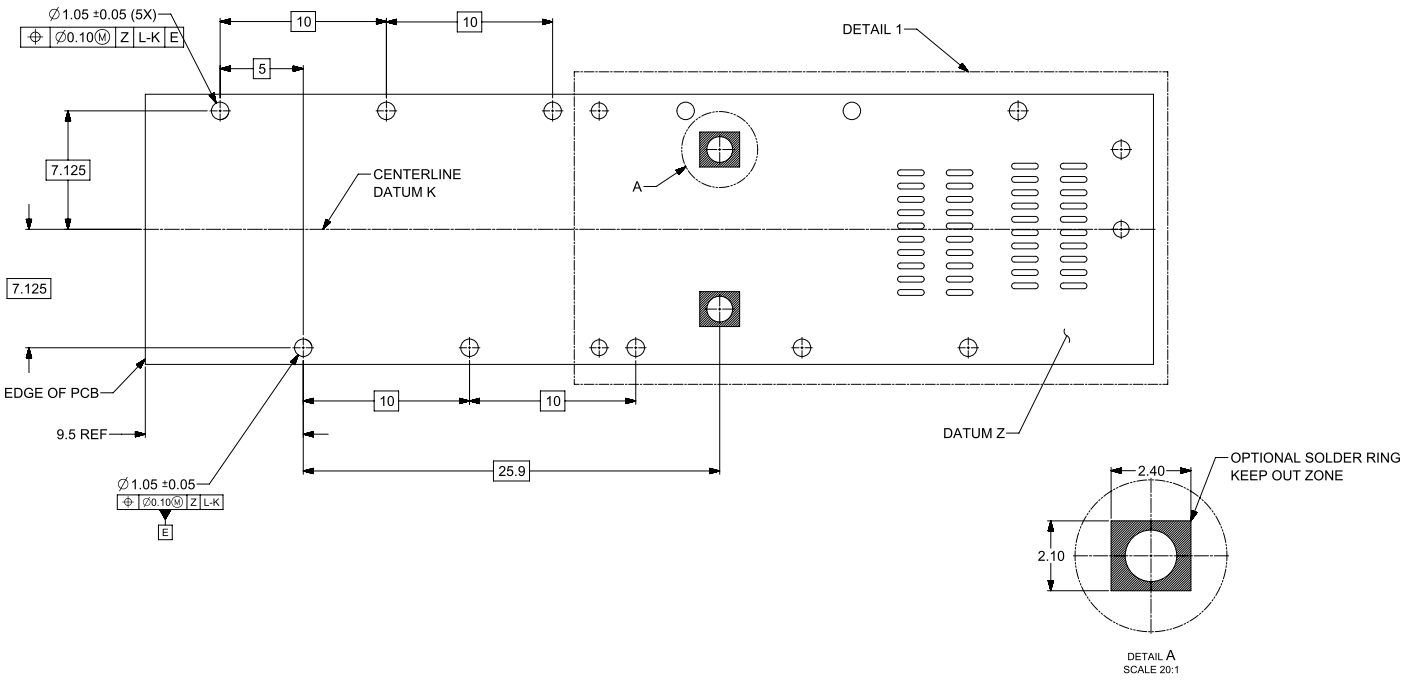


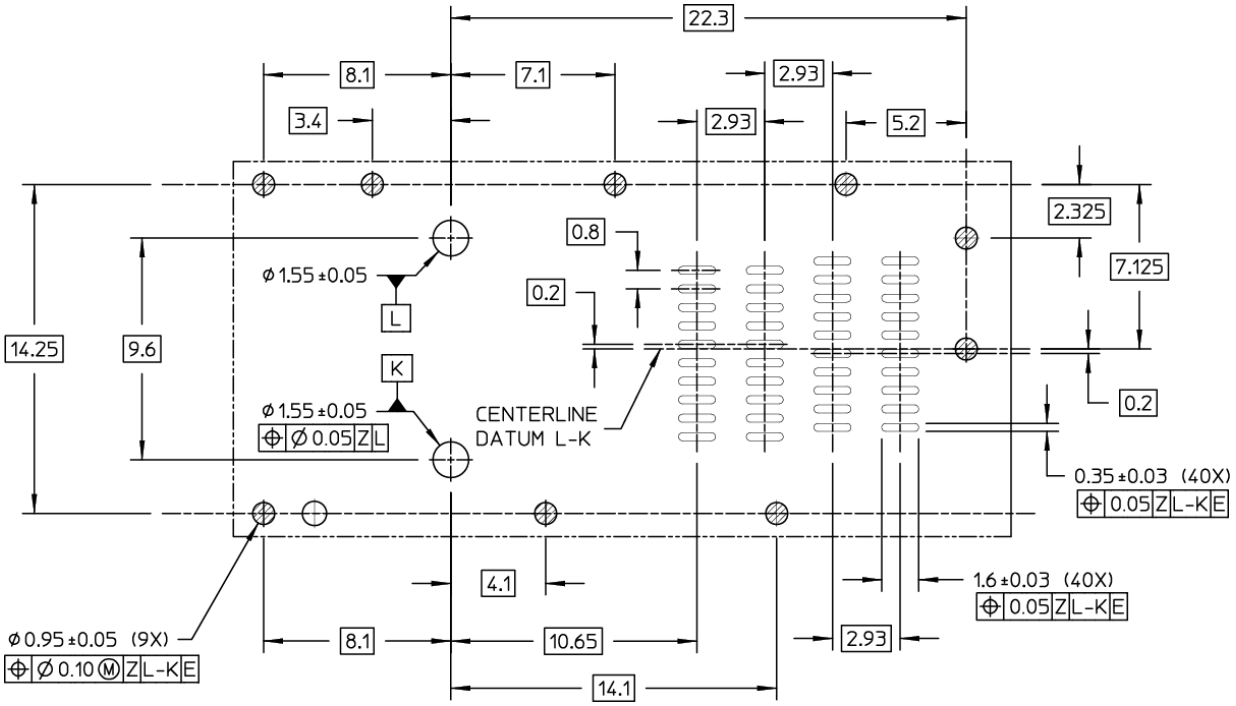
Figure 31: 1x1 Connector Design and Host PCB Pin Numbers

6.8.1 SMT connector and cage host PCB layout

A typical host board mechanical layout for attaching the SFP-DD SMT Connector and press fit Cage System is shown in Figure 32. Location of the pattern on the host board is application specific.

To achieve 25-50 Gbps performance pad dimensions and associated tolerances must be adhered to and attention paid to the host board layout.





DETAIL 1

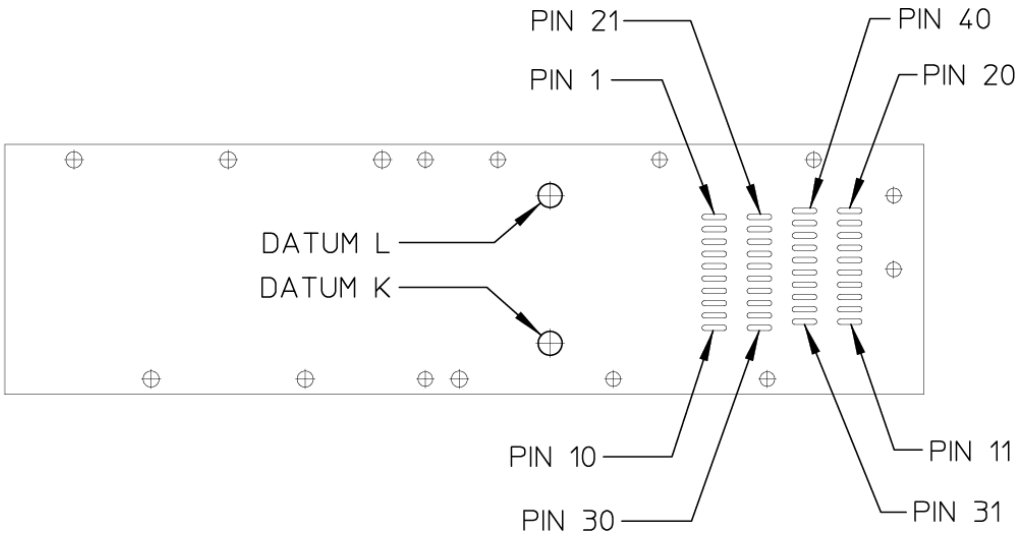


Figure 32: Host PCB Mechanical Layout

7. Environmental and Thermal

7.1 Thermal Requirements

The SFP-DD module shall operate within one or more of the case temperatures ranges defined in Table 12. The temperature ranges are applicable between 60 m below sea level and 1800 m above sea level, (Ref. NEBS GR-63) utilizing the host systems designed airflow.

Table 12- Temperature Range Class of operation

Class	Case Temperature Range
Standard	0°C through 70°C
Extended	-5°C through 85°C
Industrial	-40°C through 85°C

SFP-DD is designed to allow for up to 48 modules; stacked, ganged and/or belly-to-belly in a 1U 19" rack, with the appropriate thermal design for cooling/airflow.

Appendix A Normative Module and Connector Performance Requirements

A.1 Performance Tables

EIA-364-1000 (TS-1000) shall be used to define the test sequences and procedures for evaluating the connector system described in this document. Where multiple test options are available, the manufacturer shall select the appropriate option where not previously specified. The selected procedure should be noted when reporting data. If there are conflicting requirements or test procedures between EIA-364 procedures and those contained within this document, this document shall be considered the prevailing authority. Unless otherwise specified, procedures for sample size, data, and collection to be followed as specified in EIA-364-1000. See EIA-364-1000 Annex B for objectives of tests and test groups.

This document represents the minimum requirements for the defined product. Additional test conditions and evaluations may be conducted within the defined EIA-364-1000 sequences. More extreme test conditions and failure criteria may be imposed and still meet the requirements of this document.

Table 13 summarizes the performance criteria that are to be satisfied by the connector described in this document. Most performance criteria are validated by EIA-364-1000 testing, but this test suite leaves some test details to be determined. To ensure that testing is repeatable, these details are identified in Table 14. Finally, testing procedures used to validate any performance criteria not included in EIA-364-1000 are provided in Table 15.

Table 13- Form Factor Performance Requirements

Performance Parameters	Description/ Details	Requirements
Mechanical/ Physical Tests		
Plating Type	Plating type on connector contacts	Precious (refer to 6.5 for plating details)
Surface Treatment	Surface treatment on connector contacts; if surface treatment is applied, Test Group 6 is required	Manufacturer to specify
Wipe length	Designed distance a contact traverses over a mating contact surface during mating and resting at a final position. If less than 0.127 mm, test group 6 is required	Manufacturer to specify
Rated Durability Cycles	The expected number of durability cycles a component is expected to encounter over the course of its life	Connector/ cage: 100 cycles Module: 50 cycles
Mating Force[1]	Amount of force needed to mate a module with a connector when latches are deactivated	SFP module: 18 N MAX SFP-DD module: 40 N MAX
Unmating Force[1]	Amount of forced needed to separate a module from a connector when latches are deactivated	SFP module: 12.5 N MAX SFP-DD module: 30 N MAX
Latch Retention[1]	Amount of force the latching mechanism can withstand without unmating	SFP module: 90 N MIN SFP-DD module: 90 N MIN
Cage Latch Strength[1]	The amount of force that the cage latches can hold without being damaged.	100 N MIN
Cage Retention to Host Board[1]	Amount of force a cage can withstand without separating from the host board	SFP module: 18 N MAX SFP-DD module: 40 N MAX
Environmental Requirements		
Field Life	The expected service life for a component	10 years
Field Temperature	The expected service temperature for a component	65°C
Electrical Requirements		
Current	Maximum current to which a contact is exposed in use	0.5 A per signal contact MAX 1.0 A per power contact MAX
Operating Rating Voltage	Maximum voltage to which a contact is exposed in use	30 V DC per contact MAX

Note:
1. These performance criteria are not validated by EIA-364-1000 testing, see Table 15 for test procedures and pass/fail criteria.

Table 14 describes the details necessary to perform the tests described in the EIA-364-1000 test sequences. Testing shall be done in accordance with EIA-364-1000 and the test procedures it identifies in such a way that the parameters/ requirements defined in Table 13 are met. Any information in this table supersedes EIA-364-1000.

Table 14- EIA-364-1000 Test Details

Performance Parameters	Description/ Details	Requirements
Mechanical/ Physical Tests		
Durability (preconditioning)	EIA-364-09 To be tested with connector, cage, and module. Latches may be locked out to aid in automated cycling.	No evidence of physical damage
Durability[1]	EIA-364-09 To be tested with connector, cage, and module. Latches may be locked out to aid in automated cycling.	No visual damage to mating interface or latching mechanism
Environmental Tests		
Cyclic Temperature and Humidity	EIA-364-31 Method IV omitting step 7a Test Duration B	No intermediate test criteria
Vibration	EIA-364-28 Test Condition V Test Condition Letter D Test set-up: Connectors may be restrained by a plate that replicates the system panel opening as defined in this specification. External cables may be constrained to a non-vibrating fixture a minimum of 8 inches from the module. For cabled connector solutions: Wires may be attached to PCB or fixed to a non-vibrating fixture.	No evidence of physical damage -AND- No discontinuities longer than 1 µs allowed
Mixed Flowing Gas	EIA-364-65 Class II See Table 4.1 in EIA-364-1000 for exposure times Test option Per EIA-364-1000 option 3	No intermediate test criteria
Electrical Tests		
Low Level Contact Resistance[2]	EIA-364-23 20 mV DC Max, 100 mA Max To include wire termination or connector-to-board termination	20 mΩ Max change from baseline
Dielectric Withstanding Voltage	EIA-364-20 Method B 300 VDC minimum for 1 minute Applied voltage may be product / application specific	No defect or breakdown between adjacent contacts -AND- 1 mA Max Leakage Current

Notes:

1. If the durability requirement on the connector is greater than that of the module, modules may be replaced after their specified durability rating.
2. The first low level contact resistance reading in each test sequence is used to determine a baseline measurement. Subsequent measurements in each sequence are measured against this baseline.

Table 15 describes the testing procedures necessary to validate performance criteria not validated by EIA-364-1000 testing. The tests are to be performed in such a way that the parameters/ requirements defined in Table 13 are met.

Table 15- Additional Test Procedures

Tests	Test Descriptions and Details	Pass/ Fail Criteria's
Mechanical/ Physical Tests		
Mating Force[1]	EIA-364-13 Mating/ unmating rate 12.7 mm/min To be tested with cage, connector, and module. Latching mechanism deactivated (locked out).	Refer to Table 13 -AND- No physical damage to any components
Unmating Force[1]		
Latch Retention[1]	EIA-364-13 Mating/ unmating rate 12.7 mm/min To be tested with cage, connector, and module. Latching mechanism engaged (not locked out).	
Latch Strength	An axial load applied using a static load or ramped loading to the specified load. To be tested with cage, connector, and module or module representative tool without heat sinks Latching mechanism engaged (not locked out).	
Cage Retention to Host Board	Tested with module, module analog, or fixtures mated to cage. Pull cage in a direction perpendicular to the board at a rate of 25.4 mm/min to the specified force.	No physical damage to any components -AND- Cage shall not separate from board
Electrical Tests		
Current	EIA-364-70 Method 3, 30-degree temperature rise Contacts energized: All signal and power contacts energized simultaneously	Refer to Table 13 for current magnitude

Note:
1. Values listed in Table 13 apply with or without the presence of a riding heat sink.

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