ZYNQ-EAME ULTRASCALE 0

DESIGN BY soceame.wordpress.com DESIGNED IN SPAIN

Version 0:

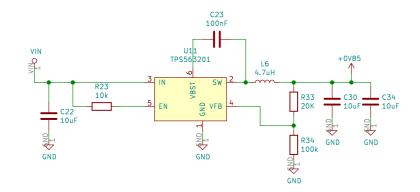


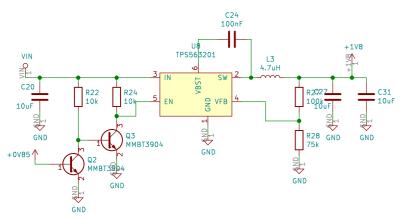
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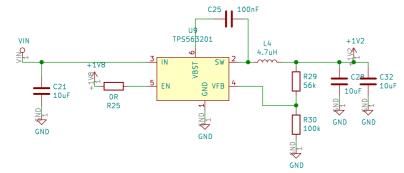
github.com/DRubioG/Zynq-eame/Zynq-eame_UltraScale_0

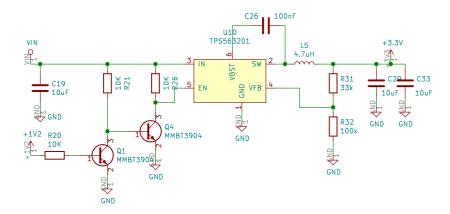
	soceame.wordpress.com		
	Sheet: / File: Zynq-eame_UltraScale_0.sch		
Title: Zynq-eame UltraScale 0			
	Size: A3 Date:	Rev:	
	KiCad E.D.A. kicad (5.1.4)-1	ld: 1/6	
	7	0	

VIN -> 0V85, 1V8, 1V2, 3V3

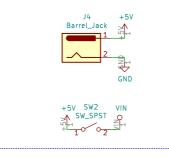




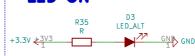




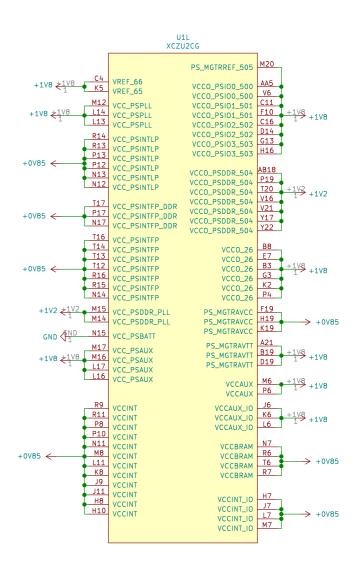
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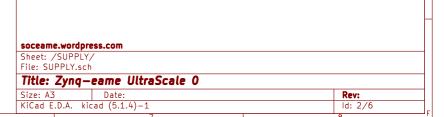


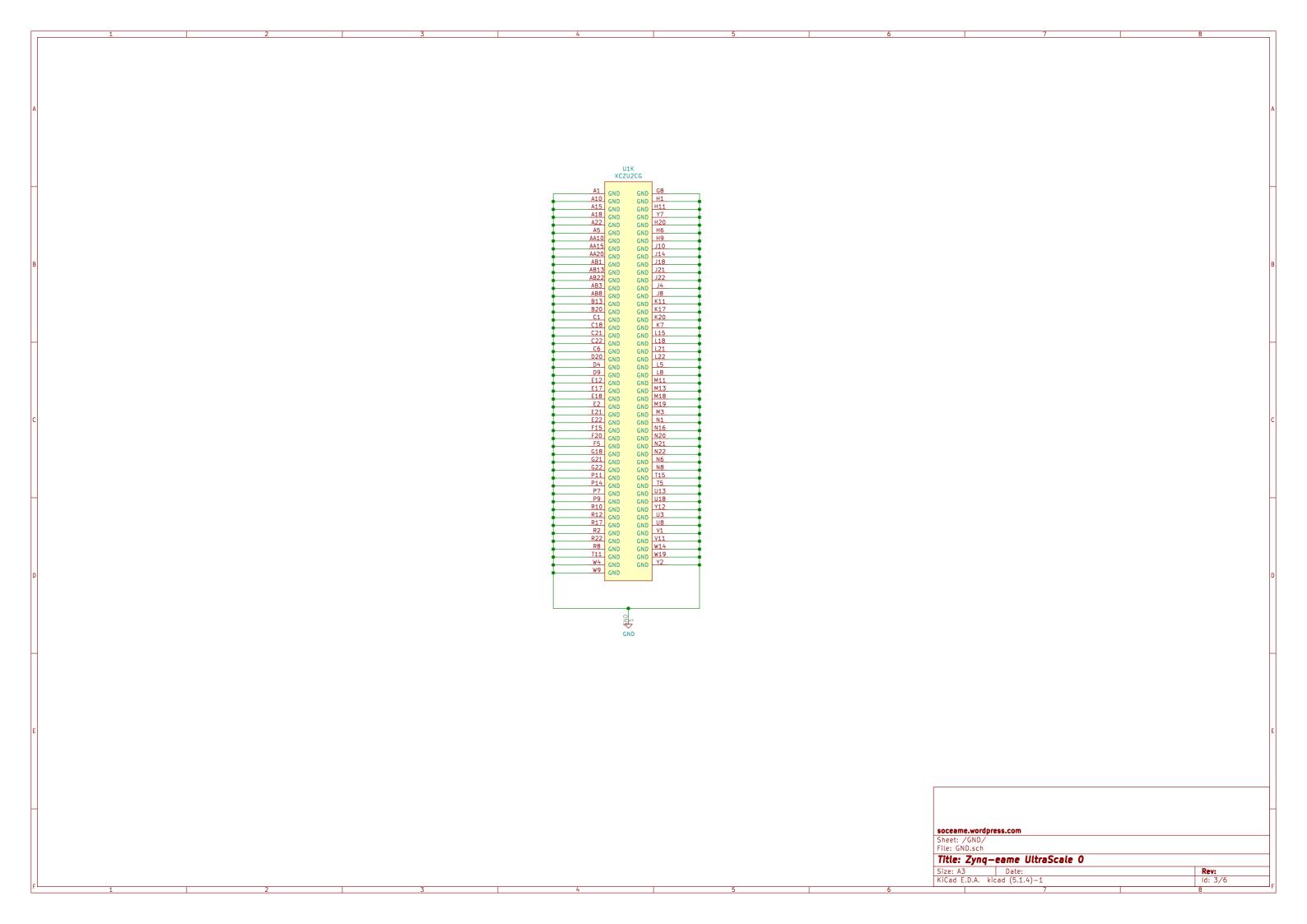
LED ON



XCZU2CG





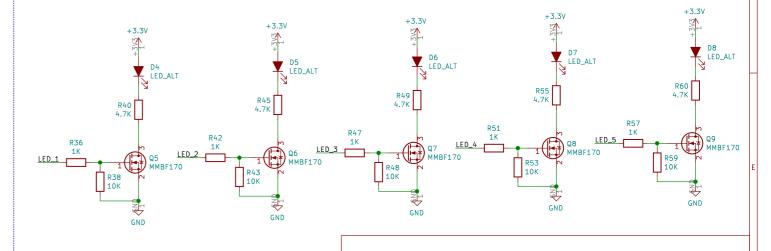


U1D XCZU2CG

U1B XCZU2CG

U1C XCZU2CG

LEDS



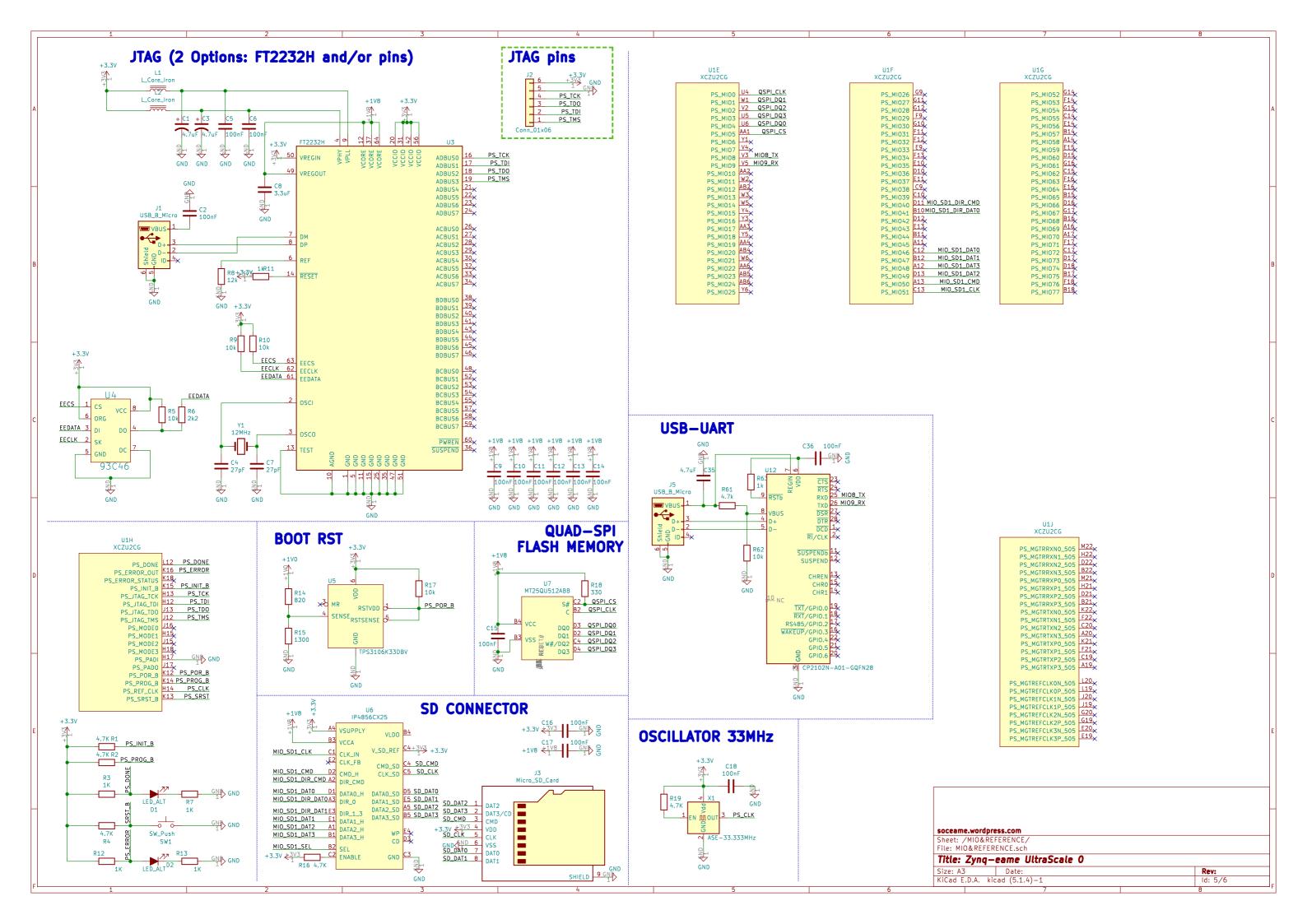
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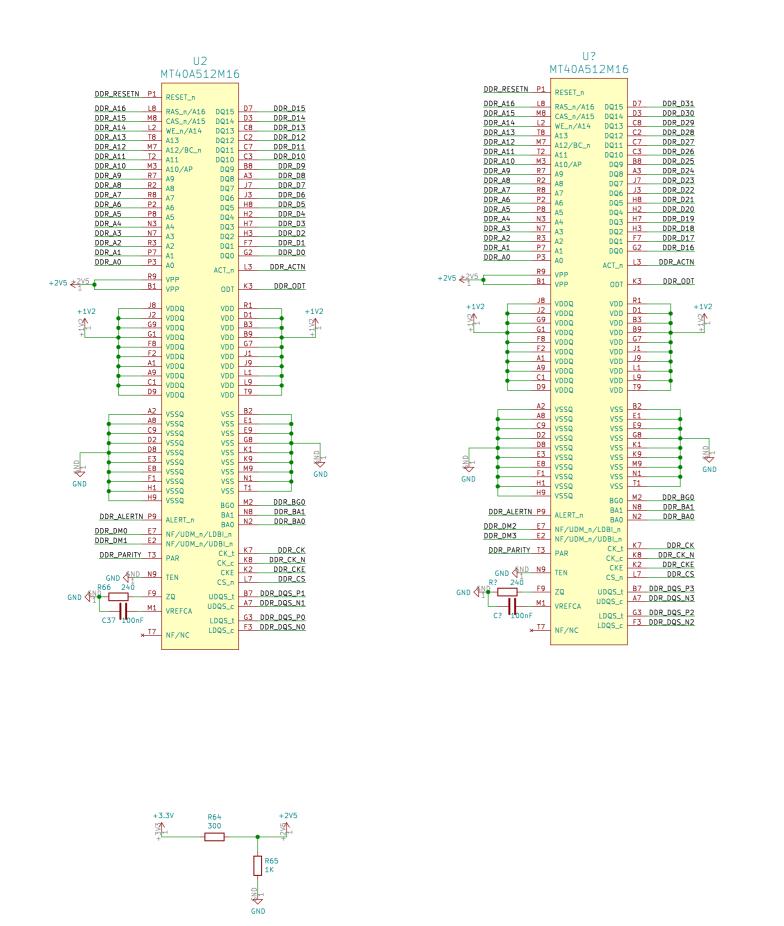
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Title: Zynq-eame UltraScale 0

 Size: A3
 Date:
 Rev:

 KiCad E.D.A. kicad (5.1.4)-1
 Id: 4/6





U1I XCZU2CG PS_DDR_DQ71
PS_DDR_DQ69
PS_DDR_DQ68
PS_DDR_DQ66
PS_DDR_DQ66
PS_DDR_DQ65
PS_DDR_DQ65
PS_DDR_DQ64
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PS_DDR_DQ27
PS_DDR_DQ21
PS_DDR_DQ31
PS_DDR_DQ31 DDR_A16 Y16 PS_DDR_A16
DDR_A15 AA16 PS_DDR_A15
DDR_A14 AA17 PS_DDR_A14
AA17 AA19 DDR D31 DDR_D30 DDR_A13 AA19 .5 DDR D29 S_DDR_A13 DDR_A12 AA18 DDR_D28 .5 <u>DDR_D27</u> .5 <u>DDR_D26</u> DDR_A11 AA21 S DDR A11 DDR_A10 Y21 DDR_A9 Y18 5 DDR_D25 S DDR A9 DDR_A8 W17 5 DDR_D24 S_DDR_A8 S_DDR_A7 DDR A6 Y20 DDR D22 S_DDR_A6 DDR_A5 AB16 DDR_D21 DDR_A4 AB21 DDR_D20 S DDR A4 DDR_D19 DDR_A3 AB19 DDR_A2 AB17 DDR_D18 S DDR 42 DDR_A1 AB20 DDR_D17 PS_DDR_DQ16
PS_DDR_DQ15
PS_DDR_DQ15
PS_DDR_DQ14
AA14 DDR_A0 AA22 PS_DDR_A0 DDR_D15 DDR_D14 DDR D13 DDR_D12 DDR_BA1 V17 PS_DDR_BA1 DDR_BA0 U17 PS_DDR_BA0 5 DDR_D11 .5 DDR_D10 DDR_BG0 W18 PS_DDR_BG1 PS_DDR_BG0 DDR D8 DDR_D7 DDR_RESETN T18 PS_DDR_RAM_RST_N DDR_CK V20 PS_DDR_CK0 DDR_CK_N W20
PS_DDR_CK_N0 XV19 PS_DDR_CK_N1
U22 PS_DDR_CKE0 DDR_CKE XU21 PS_DDR_CKE1
V22 PS_DDR_CS_N0
PS_DDR_CS_N1 DDR_CS PS_DDR_DQS_P8
PS_DDR_DQS_P8
PS_DDR_DQS_P3
PS_DDR_DQS_N3
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PS_DDR_DQS_N0 DDR_ODT W22 PS_DDR_ODT1 PS_DDR_ODT0 DDR_ACTN U15 DDR_ALERTN T21 PS_DDR_ACT_N PS_DDR_ALERT_N DDR_PARITY U19 PS_DDR_PARITY T19 PS_DDR_ZQ GND GND

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Sheet: /DDR/
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Title: Zynq—eame UltraScale 0

Size: A3 Date: Rev:
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