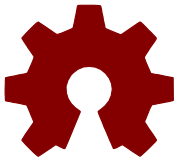


Version 0:

- SoC: XC7Z010-CLG400
- ALIMENTACIONES
 - SoC: XC7Z010-CLG400 (GND & VCC)
 - TPS563201 x4
 - TPS3106K33DBV (DELAY RST)
- MEMORIA RAM
 - SoC: XC7Z010-CLG400 (DDR)
 - RAM: MTK41K256M16TW-107:P x2
- ENTRADAS Y SALIDAS
 - SoC: XC7Z010-CLG400 (BANK 34 & 35)
 - TP0125016
 - HDMI CONNECTOR
 - LEDS
 - BUTTONS
 - SWITCHES
- REFERENCIAS Y MIOs
 - SoC: XC7Z010-CLG400 (MIO, NC & REFERENCE)
 - JTAG (FT2232H &93C46)
 - CP2102N (UART)
 - SD CONNECTOR
 - S25FL128S (QUAD-SPI FLASH MEMORY)
 - OSCILLATOR 33.333MHz

DESIGNED BY: SoC-eame
DESIGNED IN SPAIN



soceame.wordpress.com

Sheet: Alimentaciones



File: alimentaciones.sch

Sheet: Memoria RAM



File: DDR.sch

Sheet: Entradas y Salidas



File: ent_sal.sch

Sheet: Referencias y MIOs



File: referencia.sch

Zynq-eame 0

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VIN -> 1V0, 1V8, 3V3 & 1V35

The first three diagrams show the conversion of VIN to +1V0, +1V8, and +1V35 respectively. The fourth diagram shows the conversion to VCCO_34. All converters are based on the TPS563201 IC.

Voltage Input

Delay RST

LED ON

XC7Z010

U5I XC7Z010-BUENO

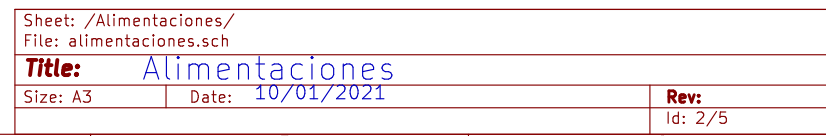
M7	GND_1	GND_30	P13
G12	GND_2	GND_31	K15
M13	GND_3	GND_32	M1
G16	GND_4	GND_33	N4
N8	GND_5	GND_34	N14
H7	GND_6	GND_35	A8
N12	GND_7	GND_36	R20
H9	GND_8	GND_37	A18
P7	GND_9	GND_38	W2
H11	GND_10	GND_39	B1
P11	GND_11	GND_40	L12
H13	GND_12	GND_41	B11
P17	GND_13	GND_42	M11
H19	GND_14	GND_43	C4
R12	GND_15	GND_44	N10
J2	GND_16	GND_45	C14
T3	GND_17	GND_46	P9
J8	GND_18	GND_47	K11
T13	GND_19	GND_48	R8
J12	GND_20	GND_49	D17
U16	GND_21	GND_50	I7
K5	GND_22	GND_51	E10
V19	GND_23	GND_52	V9
K7	GND_24	GND_53	E20
W12	GND_25	GND_54	Y5
C9	GND_26	GND_55	F3
Y15	GND_27	GND_56	L8
K13	GND_28	GND_57	F7
U6	GND_29	GND_58	L18
		GND_59	G10

U5H XC7Z010-BUENO

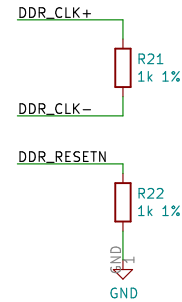
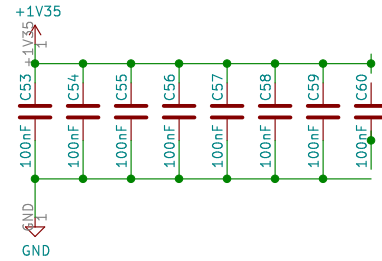
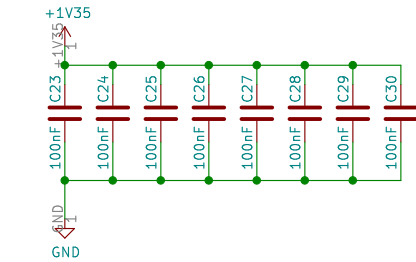
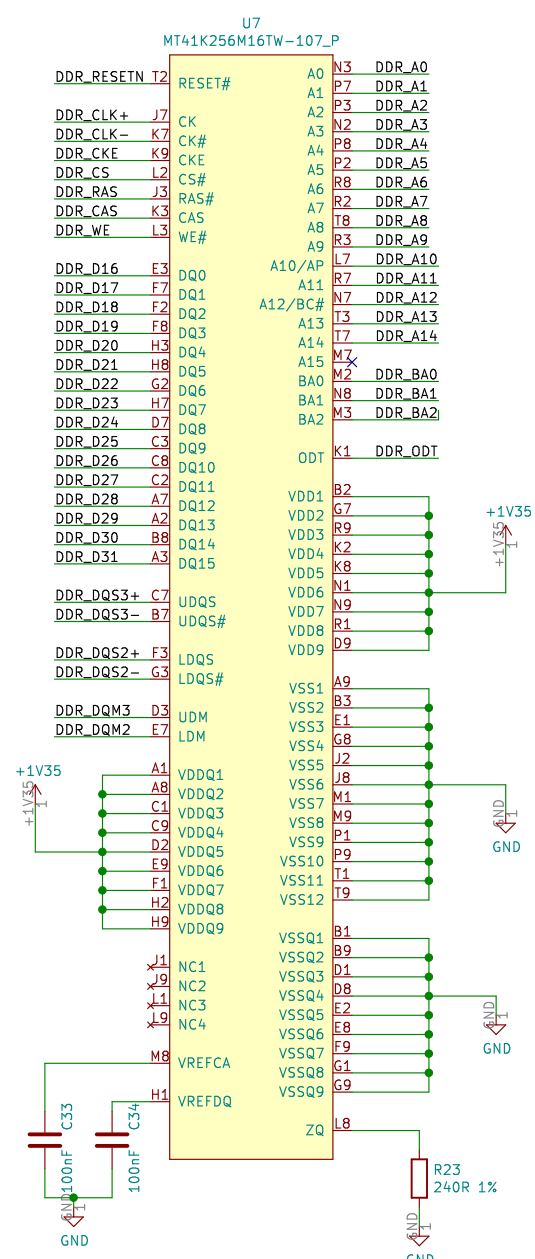
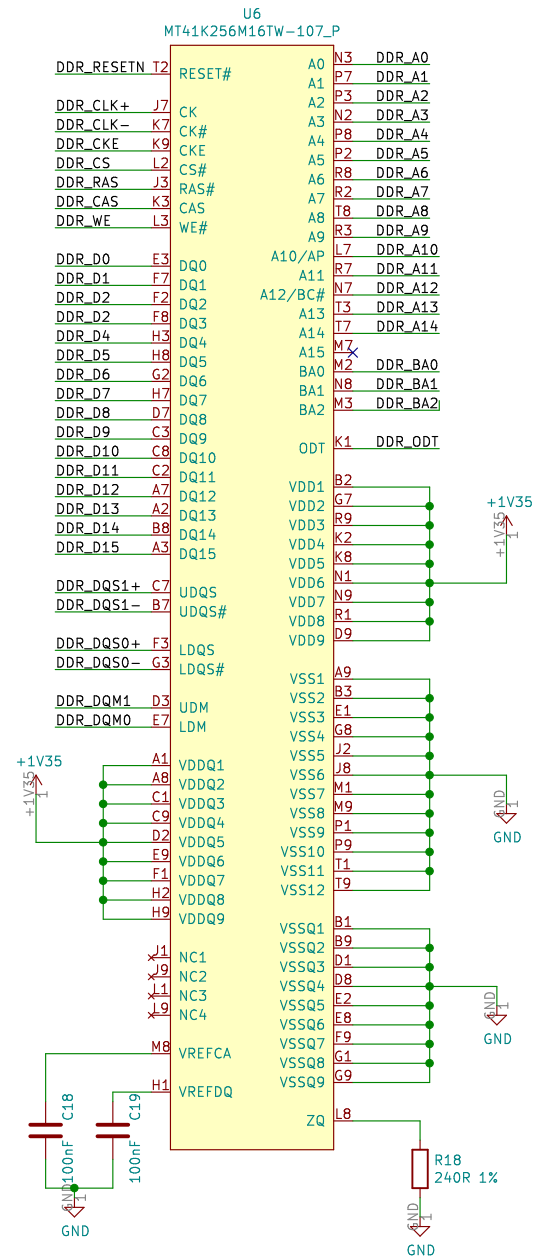
D2	VCCO_DDR_502_1	VCCO_0	K6
A3	VCCO_DDR_502_2		
H4	VCCO_DDR_502_3	VCCO_13_1	U11
V4	VCCO_DDR_502_4	VCCO_13_2	W7
P2	VCCO_DDR_502_5	VCCO_13_3	T8
R5	VCCO_DDR_502_6	VCCO_13_4	Y10
L3	VCCO_DDR_502_7		
F5	VCCO_DDR_502_8	VCCO_34_1	R15
G1	VCCO_DDR_502_9	VCCO_34_2	N19
U1	VCCO_DDR_502_10	VCCO_34_3	T18
H10	VCCBRAM_1	VCCO_34_4	Y20
G11	VCCBRAM_2	VCCO_34_5	W17
		VCCO_13_6	V14
B6	VCCO_MIO0_500_1	VCCO_35_1	F18
D7	VCCO_MIO0_500_2	VCCO_35_2	J17
		VCCO_35_3	K20
F15	VCCO_MIO1_501_1	VCCO_35_4	M16
B16	VCCO_MIO1_501_2	VCCO_35_5	C19
D12	VCCO_MIO1_501_3	VCCO_35_6	H14
A13	VCCO_MIO1_501_4		
P8	VCCPINT_1	VCCAUX_1	R9
R7	VCCPINT_2	VCCAUX_2	N11
J7	VCCPINT_3	VCCAUX_3	L11
L7	VCCPINT_4	VCCAUX_4	N9
N7	VCCPINT_5	VCCAUX_5	P10
G7	VCCPINT_6	VCCAUX_6	J11
F8	VCCPAUX_1	VCCINT_1	L13
K8	VCCPAUX_2	VCCINT_2	N13
M8	VCCPAUX_3	VCCINT_3	M12
H8	VCCPAUX_4	VCCINT_4	R13
G9	VCCPAUX_5	VCCINT_5	G13
		VCCINT_6	J13
		VCCINT_7	K12
		VCCINT_8	H12
		VCCINT_9	P12
G8	VCCPLL		
		VCCBATT_0	F11

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The schematic diagram illustrates the power supply connection. A J5 Barrel Jack is connected to a +5V source and GND. The +5V line passes through an ON_OFF1 SW_SPST switch before reaching the VIN pin of the DC-DC converter.



MT41K256M16TW-107:P x2



XC7Z010

