ZYNQ-EAME ULTRASCALE 0

DESIGN BY soceame.wordpress.com
DESIGNED IN SPAIN

OPEN HARDWARE

Version 0:

Sheet: SUPPLY
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Sheet: GND
File: GND.sch

Sheet: DDR
File: DDR.sch

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File: MIO&REFERENCE.sch

github.com/DRubioG/Zynq-eame/Zynq-eame_UltraScale_0

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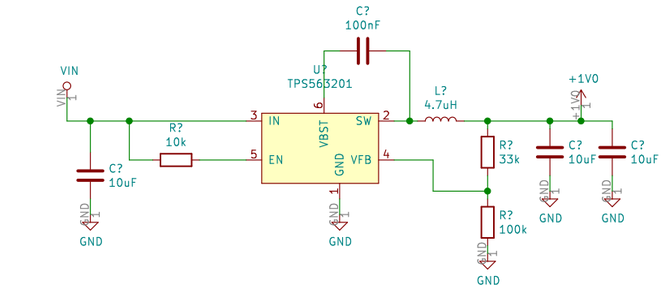
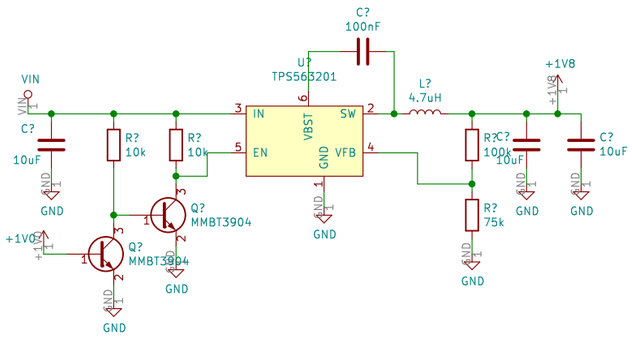
Sheet: /
File: Zynq-eame_UltraScale_0.sch

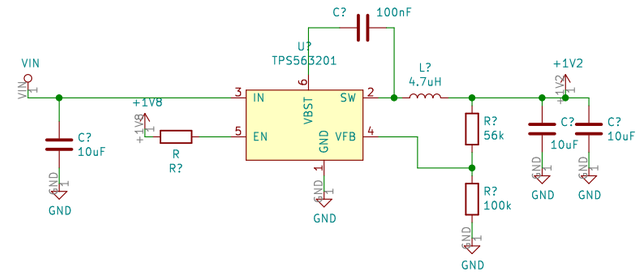
Title: Zynq-eame UltraScale 0

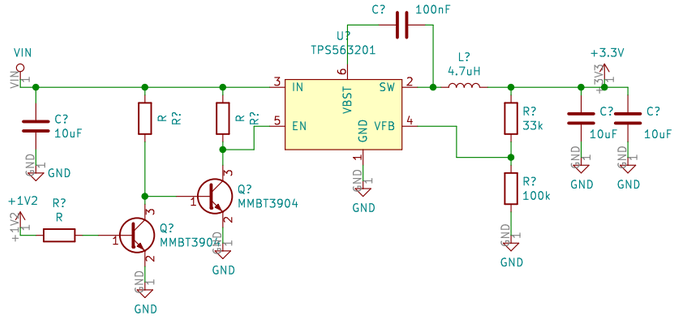
Size: A3	Date:	Rev:
KiCad E.D.A. kicad (5.1.4)-1		Id: 1/6

VIN -> 1V0, 1V8, 1V2, 3V3

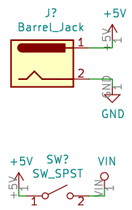






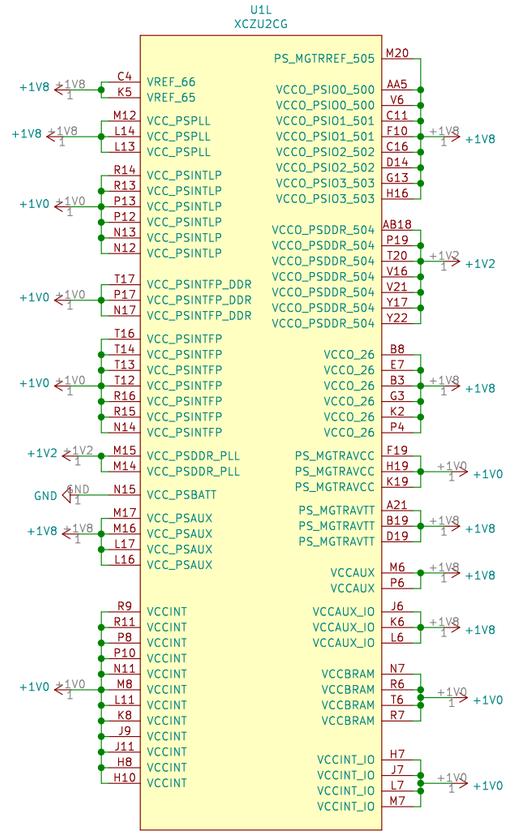


SUPPLY



LED ON

XCZU2CG



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Sheet: /SUPPLY/
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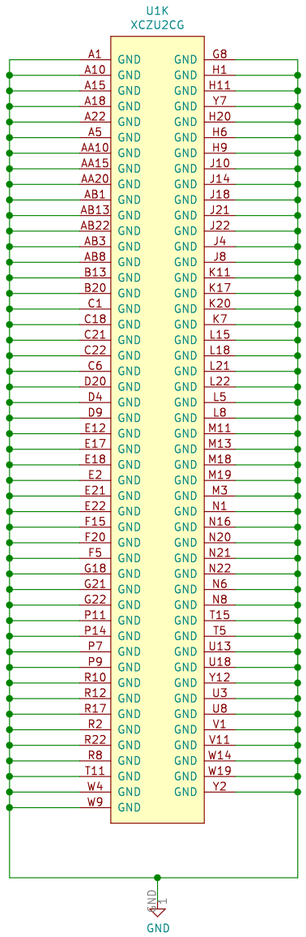
Title: Zynq-eame UltraScale 0

Size: A3	Date:	Rev:
KiCad E.D.A. kicad (5.1.4)-1		Id: 2/6



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Size: A3	Date:	Rev:
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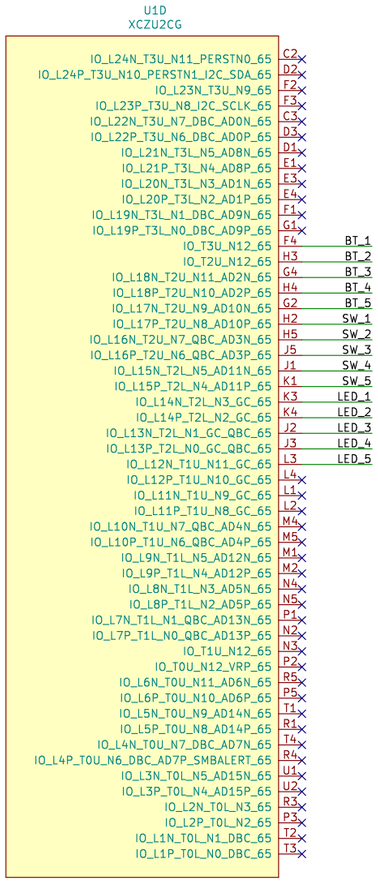

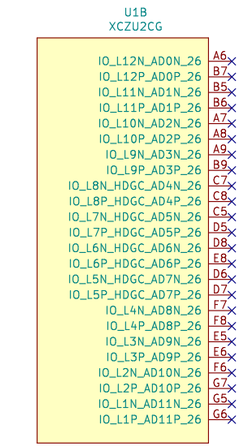

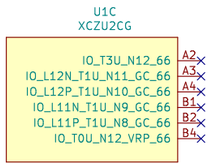

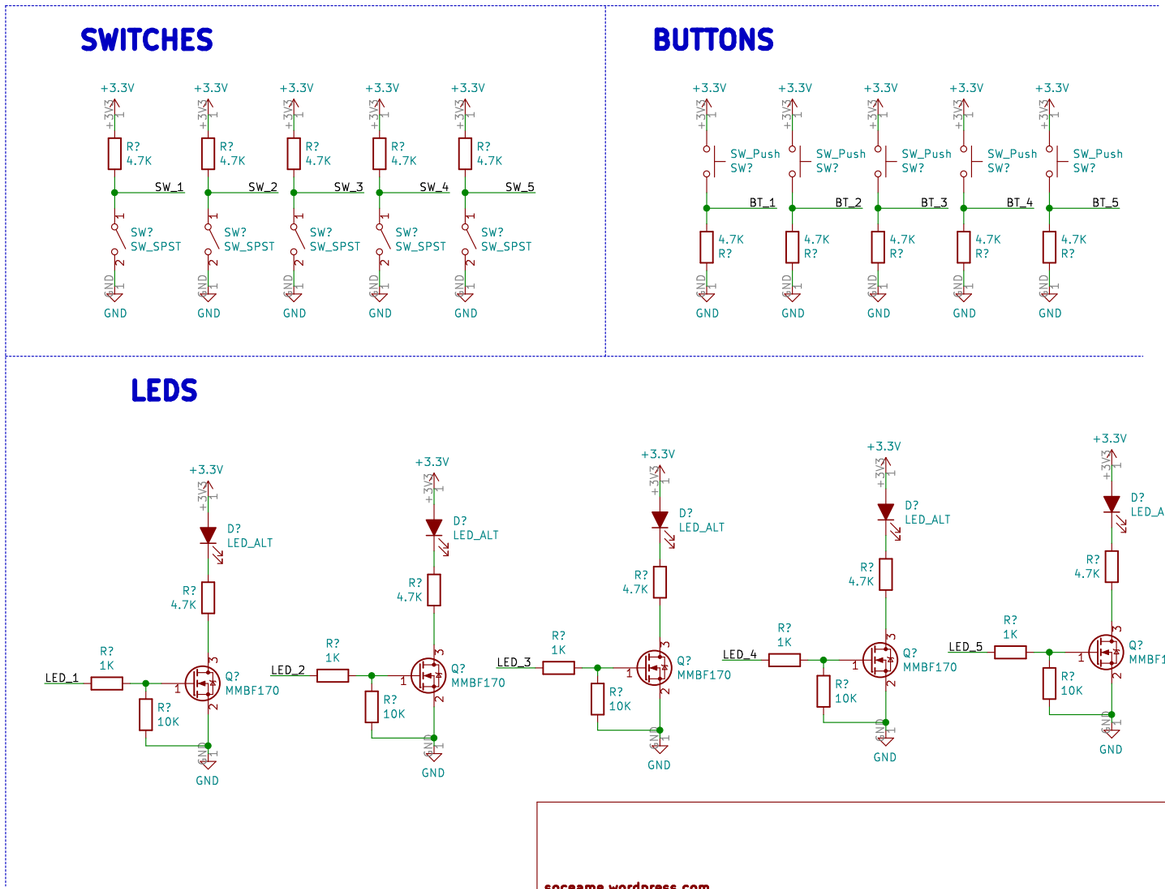

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Sheet: /PINOUT/
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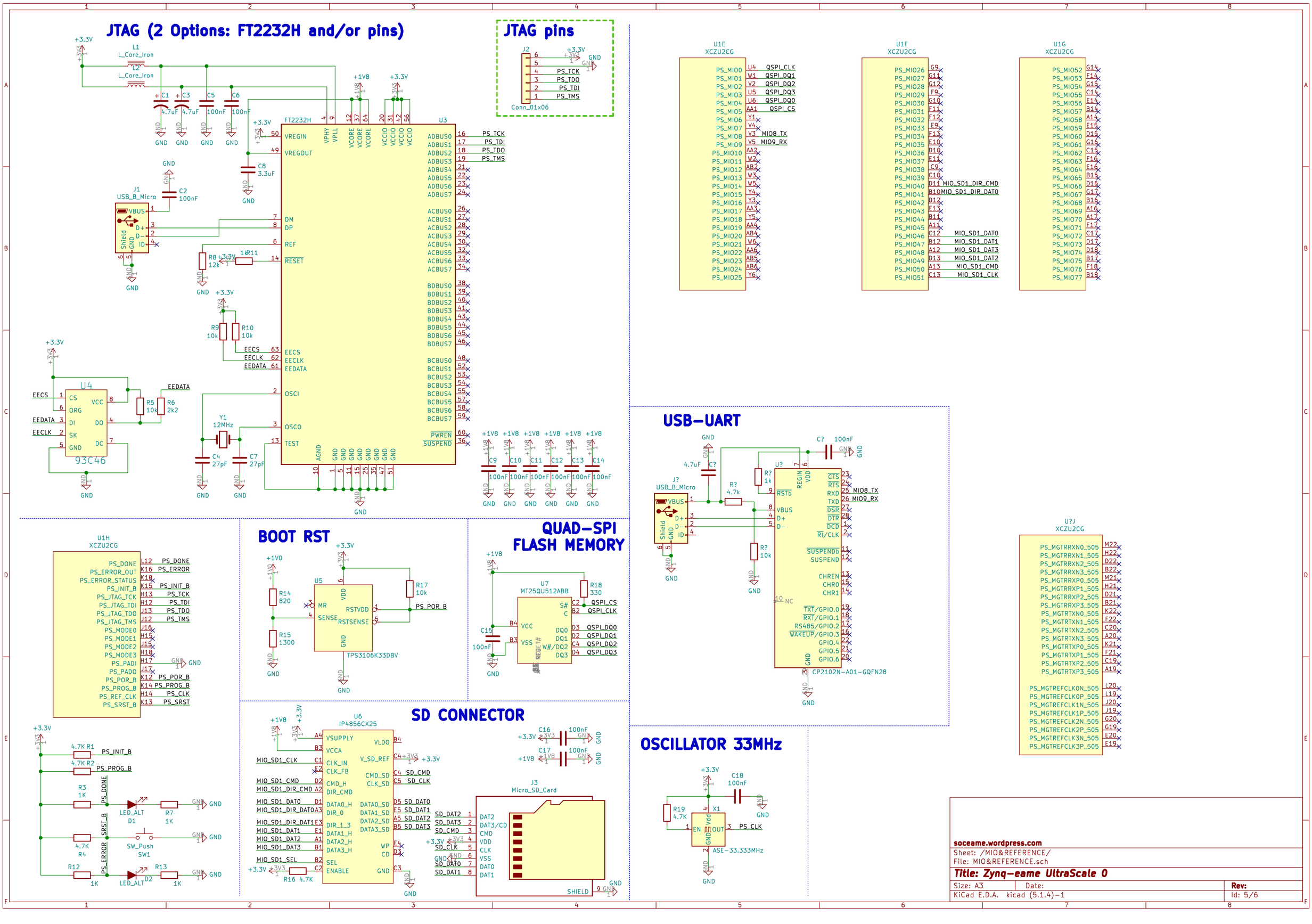
Title: Zynq-eame UltraScale 0

Size: A3	Date:	Rev:
KiCad E.D.A. kicad (5.1.4)-1		Id: 4/6


JTAG (2 Options: FT2232H and/or pins)
JTAG pins
J2
Conn_01x06
PS_TCK
PS_TDO
PS_TDI
PS_TMS
GND
+3.3V
L1
L_Core_Iron
L2
L_Core_Iron
C1 4.7uF
C3 4.7uF
C5 100nF
C6 100nF
+1V8
FT2232H
U3
VREGIN
VREGOUT
VPHY
VPLL
VCORE
VCORE
VCORE
VCCIO
VCCIO
VCCIO
VCCIO
C8 3.3uF
J1
USB_B_Micro
VBUS
D+
D-
ID
Shield
GND
C2 100nF
DM
DP
REF
RESET
R8 12k
1kR11
ADBUS0
ADBUS1
ADBUS2
ADBUS3
ADBUS4
ADBUS5
ADBUS6
ADBUS7
ACBUS0
ACBUS1
ACBUS2
ACBUS3
ACBUS4
ACBUS5
ACBUS6
ACBUS7
BDBUS0
BDBUS1
BDBUS2
BDBUS3
BDBUS4
BDBUS5
BDBUS6
BDBUS7
BCBUS0
BCBUS1
BCBUS2
BCBUS3
BCBUS4
BCBUS5
BCBUS6
BCBUS7
PWREN
SUSPEND
R9 10k
R10 10k
EECS
EECLK
EEDATA
OSCI
OSCO
TEST
Y1 12MHz
C4 27pF
C7 27pF
AGND
C9 100nF
C10 100nF
C11 100nF
C12 100nF
C13 100nF
C14 100nF
U4
93C46
CS
ORG
DI
SK
GND
VCC
DO
DC
R5 10k
R6 2k2
U1E
XCZU2CG
PS_MIO0
PS_MIO1
PS_MIO2
PS_MIO3
PS_MIO4
PS_MIO5
PS_MIO6
PS_MIO7
PS_MIO8
PS_MIO9
PS_MIO10
PS_MIO11
PS_MIO12
PS_MIO13
PS_MIO14
PS_MIO15
PS_MIO16
PS_MIO17
PS_MIO18
PS_MIO19
PS_MIO20
PS_MIO21
PS_MIO22
PS_MIO23
PS_MIO24
PS_MIO25
QSPI_CLK
QSPI_DQ1
QSPI_DQ2
QSPI_DQ3
QSPI_DQ0
QSPI_CS
MIO8_TX
MIO9_RX
U1F
XCZU2CG
PS_MIO26
PS_MIO27
PS_MIO28
PS_MIO29
PS_MIO30
PS_MIO31
PS_MIO32
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PS_MIO39
PS_MIO40
PS_MIO41
PS_MIO42
PS_MIO43
PS_MIO44
PS_MIO45
PS_MIO46
PS_MIO47
PS_MIO48
PS_MIO49
PS_MIO50
PS_MIO51
MIO_SD1_DIR_CMD
MIO_SD1_DIR_DAT0
MIO_SD1_DAT0
MIO_SD1_DAT1
MIO_SD1_DAT3
MIO_SD1_DAT2
MIO_SD1_CMD
MIO_SD1_CLK
U1G
XCZU2CG
PS_MIO52
PS_MIO53
PS_MIO54
PS_MIO55
PS_MIO56
PS_MIO57
PS_MIO58
PS_MIO59
PS_MIO60
PS_MIO61
PS_MIO62
PS_MIO63
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PS_MIO67
PS_MIO68
PS_MIO69
PS_MIO70
PS_MIO71
PS_MIO72
PS_MIO73
PS_MIO74
PS_MIO75
PS_MIO76
PS_MIO77
USB-UART
J?
USB_B_Micro
C? 100nF
4.7uF C?
R? 1k
R? 4.7k
R? 10k
U?
CP2102N-A01-GQFN28
REGIN
VDD
RSTb
VBUS
D+
D-
NC
SUSPENDb
SUSPEND
CHREN
CHR0
CHR1
TXT/GPIO.0
RXT/GPIO.1
RS485/GPIO.2
WAKEUP/GPIO.3
GPIO.4
GPIO.5
GPIO.6
RI/CLK
DCD
DSR
DTR
RTS
CTS
RXD
TXD
MIO8_TX
MIO9_RX
U1H
XCZU2CG
PS_DONE
PS_ERROR_OUT
PS_ERROR_STATUS
PS_INIT_B
PS_JTAG_TCK
PS_JTAG_TDI
PS_JTAG_TDO
PS_JTAG_TMS
PS_MODE0
PS_MODE1
PS_MODE2
PS_MODE3
PS_PADI
PS_PADO
PS_POR_B
PS_PROG_B
PS_REF_CLK
PS_SRST_B
BOOT RST
U5
TPS3106K33DBV
MR
SENSE
VDD
RSTVDD
RSTSENSE
GND
R14 820
R15 1300
R17 10k
PS_POR_B
+1V0
QUAD-SPI FLASH MEMORY
U7
MT25QU512ABB
S#
C
VCC
VSS
DQ0
DQ1
W#/DQ2
DQ3
RESET#
R18 330
C15 100nF
QSPI_CS
QSPI_CLK
QSPI_DQ0
QSPI_DQ1
QSPI_DQ2
QSPI_DQ3
U2J
XCZU2CG
PS_MGTRRXN0_505
PS_MGTRRXN1_505
PS_MGTRRXN2_505
PS_MGTRRXN3_505
PS_MGTRRXP0_505
PS_MGTRRXP1_505
PS_MGTRRXP2_505
PS_MGTRRXP3_505
PS_MGTRTXN0_505
PS_MGTRTXN1_505
PS_MGTRTXN2_505
PS_MGTRTXN3_505
PS_MGTRTXP0_505
PS_MGTRTXP1_505
PS_MGTRTXP2_505
PS_MGTRTXP3_505
PS_MGTREFCLK0N_505
PS_MGTREFCLK0P_505
PS_MGTREFCLK1N_505
PS_MGTREFCLK1P_505
PS_MGTREFCLK2N_505
PS_MGTREFCLK2P_505
PS_MGTREFCLK3N_505
PS_MGTREFCLK3P_505
SD CONNECTOR
U6
IP4856CX25
VSUPPLY
VCCA
CLK_IN
CLK_FB
CMD_H
DIR_CMD
DATA0_H
DIR_0
DIR_1_3
DATA1_H
DATA2_H
DATA3_H
SEL
ENABLE
VLDO
V_SD_REF
CMD_SD
CLK_SD
DATA0_SD
DATA1_SD
DATA2_SD
DATA3_SD
WP
CD
J3
Micro_SD_Card
DAT2
DAT3/CD
CMD
VDD
CLK
VSS
DAT0
DAT1
SHIELD
SD_DAT2
SD_DAT3
SD_CMD
SD_CLK
SD_DAT0
SD_DAT1
C16 100nF
C17 100nF
R16 4.7K
OSCILLATOR 33MHz
R19 4.7K
C18 100nF
X1
EN
GND
Vdd
OUT
ASE-33.333MHz
PS_CLK
4.7K R1
4.7K R2
PS_INIT_B
PS_PROG_B
R3 1K
4.7K R4
R12 1K
R7 1K
R13 1K
LED_ALT D1
LED_ALT D2
SW_Push SW1
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Sheet: /MIO&REFERENCE/
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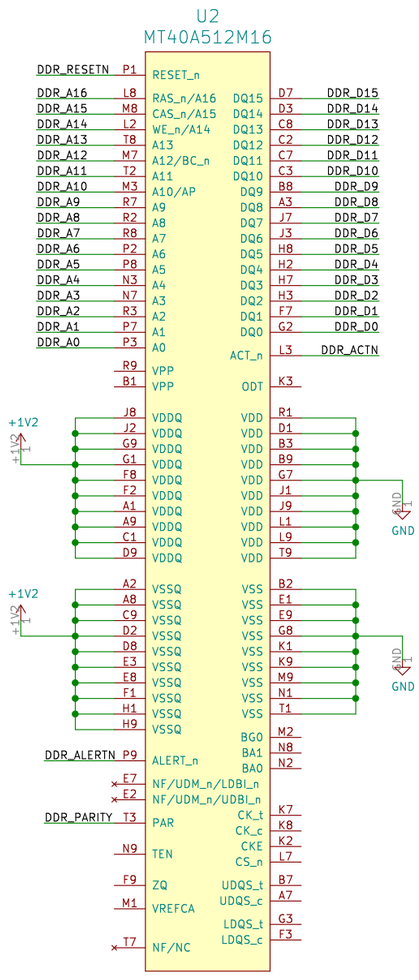

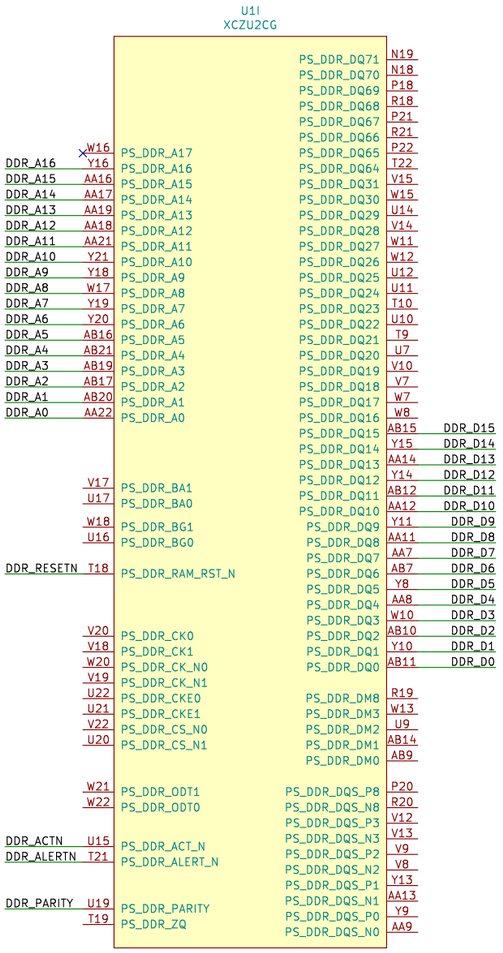

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