Hardware Interrupts

On AVR Microcontrollers

A little background

Polling

vs

Interrupts

What actually happens?

Interrupt Service Routine (ISR)
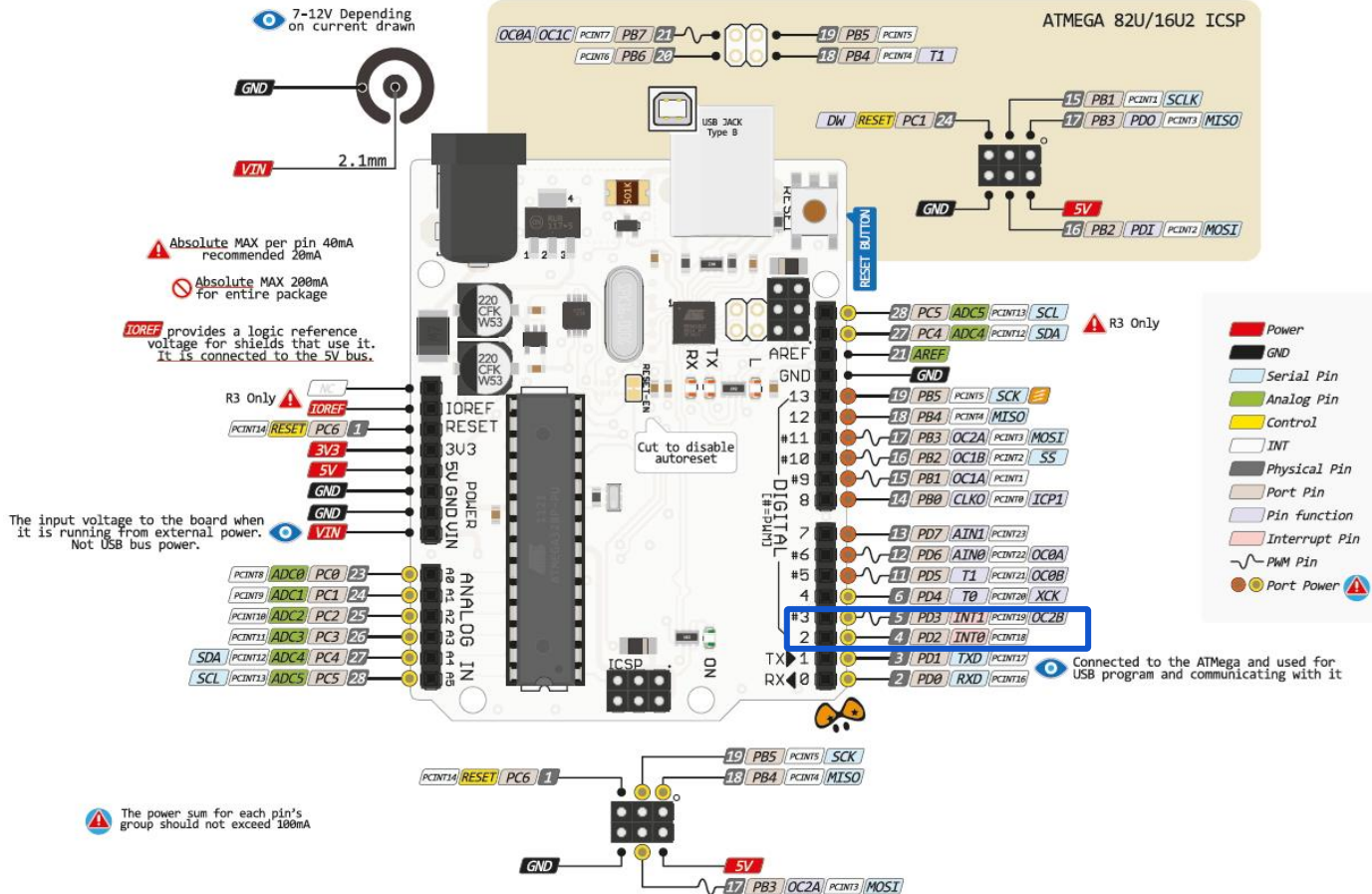
Steps:

1. Save data (where?)
2. Jump to ISR
3. Execute ISR
4. Return

Setup: Which interrupt?

Bit	7	6	5	4	3	2	1	0	
0x1D (0x3D)	–	–	–	–	–	–	INT1	INT0	**EIMSK**
Read/Write	R	R	R	R	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Setup: What triggers the interrupt?

Bit		7	6	5	4	3	2	1	0	
(0x69)		–	–	–	–	ISC11	ISC10	ISC01	ISC00	EICRA
Read/Write		R	R	R	R	R/W	R/W	R/W	R/W	
Initial Value		0	0	0	0	0	0	0	0	

ISCx1	ISCx0	DESCRIPTION
0	0	Low level of INTx generates an interrupt request
0	1	Any logic change on INTx generates an interrupt request
1	0	The falling edge of INTx generates an interrupt request
1	1	The rising edge of INTx generates an interrupt request

ISC Bit Settings