Government College of Engineering, Amravati

(An Autonomous Institute of Government of Maharashtra)

Fourth Semester B.Tech. (Information Technology)

Summer – 2018

Course Code: ITU401

Course Name: Digital Integrated Circuits

Time: 2 hr. 30min. **Max. Marks: 60**

Instructions to Candidate

1) All questions are compulsory.
2) Assume suitable data wherever necessary and clearly State the assumptions made.
3) Diagrams/sketches should be given wherever necessary.
4) Use of logarithmic table, drawing instruments and non-programmable calculators is permitted.
5) Figures to the right indicate full marks.

1. Attempt Any TWO

a. Explain Bipolar transistor characteristics of TTL, ECL, MOS and CMOS families? **6**

b. Minimize the following expression using K-Map and realize using NAND gates only. **6**
$F(A,B,C,D,E)=\sum m(0,2,5,7,8,9,10,11,18,21,24,25,26,31)+d(1,6,16,22)$

c. What are the different attributes of array? Explain unconstrained array types and unconstrained array ports. **6**

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2. **Attempt Any TWO**

a. Explain the classification of VHDL types with the help of diagram? Describe type qualification and type conversion. 6

b. Reduce the following expression to an indicated number of literals. 6
i) F(W,X,Y,Z) = W'X(Z'+Y'Z)+X(W+W'YZ) to a one literal
ii) F(X,Y,Z) = X'Y'+XYZ+X'Y to a three literals

c. Realize following Boolean function using multilevel NAND and NOR gates only. 6
F(P,Q,R,S,T,U,V,W) = PQ+R(S+T+U)+V+W

3. **Attempt**

a. Minimize following function using tabulation method and find prime implicants & essential prime implicants. 6
F(W,X,Y,Z) =∑m (0,1,3,4,6,7,8,9,10,11,13,15)

b. Write down the design procedure for combinational logic design? Design combinational circuit whose input is a 4-bit binary number and whose output is 4-bit Gray Code. 6

4. **Solve Any TWO**

a. Convert following Boolean expression into standard and canonical form and simplify by using K-Map. 6
F(A,B,C,D) = AD+ABC+B+D'

b. Design combinational circuit whose input is a 4-bit number and whose output is the 2's complement of the input number. 6

c. Write down the steps for Flip-flop interconvert ion? Justify whether it is possible to obtain S-R Flip-flop from J-K FF. 6

5. **Solve**

a. A sequential circuit has 3D Flip-flops A, B, C and one input X .it is described by the following Flip-flop function. 8
$D_A = (BC'+B'C)X+(BC+B'C')X'$
$D_B = A$
$D_C = B$
i) Derive the state table for circuit.
ii) Draw two state diagrams one for X=0 and other for X=1.

b. What do you mean by Ripple counter? Write down steps for designing the counter? Design 3 bit synchronous counter using J-K Flip-flop. 4