Government College of Engineering, Amravati
(An Autonomous Institute of Government of Maharashtra)

Fifth Semester B. Tech.
(Electronics and Telecommunication)

Winter – 2016

Course Code: ETU501

Course Name: Linear Integrated Circuits and Applications

Time: 2 hr. 30 min. **Max. Marks: 60**

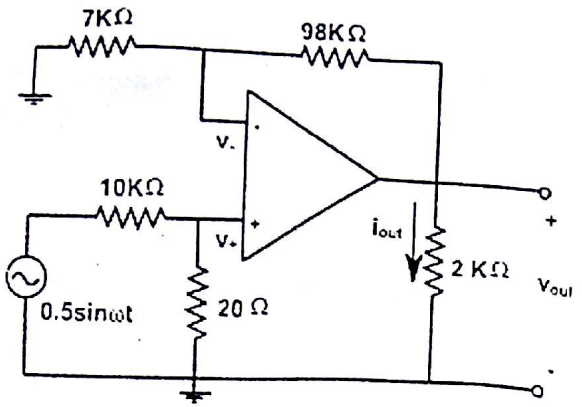
Instructions to Candidate

1) All questions are compulsory; solve any two sub-questions from Q1 and Q5.
2) Assume suitable data wherever necessary and clearly state the assumptions made.
3) Diagrams/sketches should be given wherever necessary.
4) Use of logarithmic table, drawing instruments and non-programmable calculators is permitted.
5) Figures to the right indicate full marks.

1. a) Define input offset voltage and input offset current, and explain the effect of each on the dc output voltage of an op-amp circuit. 06

b) Discuss the need for a level shifting stage between the input and output stages of an op-amp. Show how this can be done without introducing attenuation. 06

c)



Find v_{out} and i_{out} for the circuit shown in fig.1. The input voltage is sinusoidal with amplitude of 0.5 V. 06

2. a) Define common mode input, common mode gain, common mode rejection ratio, and power supply rejection ratio. 04

b) Sketch a lead compensation circuit. Explain its operation and show how it affects the frequency and phase response graphs of an op-amp. 04

c) Explain Miller effect and show how it can be used to stabilize an op-amp circuit. 04

3. a) Sketch the output waveforms produced by triangular and rectangular waveform inputs to an op-amp differentiating circuit. Explain each waveform, show the type of distortion that occurs and explain how distortion can be minimized. 06

b) Illustrate a zener diode peak clipper circuit with an adjustable output voltage limit. Explain the circuit operation, and write the equations for the upper and lower limits of output voltage. 06

4. a) Show how a triangular waveform generator can be modified for duty cycle and frequency adjustment. 04

b) Design an op-amp monostable multivibrator without any triggering circuit, to produce a ±11V, 1ms output pulse. 04

c) How the UTP and LTP of a non-inverting Schmitt trigger circuit may be modified by using diodes. 04

5. a) Design a Butterworth second-order high-pass filter circuit to have a cutoff frequency of 600Hz. Use the selected component values to determine the actual cutoff frequency. 06

b) Draw the circuit diagram for a monostable multivibrator using a 555 timer. Sketch the circuit waveforms, and referring to the 555 functional block diagram explains the circuit operation. 06

c) Show how a 555 square wave generator can be converted into a voltage controlled oscillator. Explain the effect on output waveform duty cycle. 06

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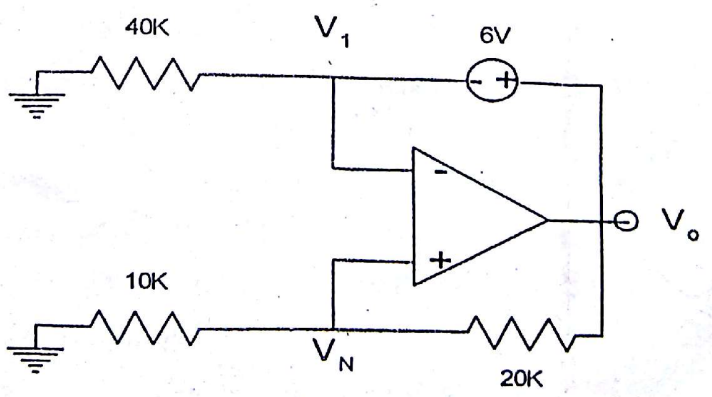
1. a) Find V_1, V_N and V_0 for the circuit as shown in below. **04**

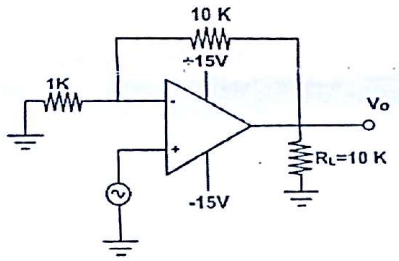


b) Why is the Widlar source said to have good power supply insensitivity? Justify **04**

c) A 100 PF capacitor has a maximum charging current of 150 μA. What is the slew rate and power bandwidth? **04**

2. a) Briefly explain the frequency response of op-amp. Give the frequency compensation techniques adopted in operational amplifiers. **06**

b) Design an input offset voltage compensating network for the circuit shown in below as Vin = 5 mV. Draw the complete circuit diagram. **06**



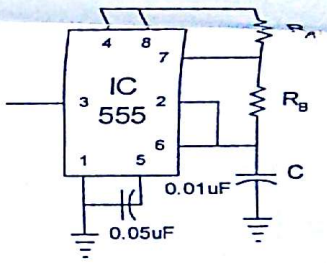
3. a) In a practical integrator circuit assume $R_1 = 10k\Omega$, $R_f = 100k\Omega$ and $C_f = 10nF$, determine the lower frequency limit of integration and output response for the inputs a) sine-wave b) square-wave and c) step input **06**

b) Explain with a circuit the working of V to I converter with floating load. Where can we use it? **06**

4. a) Design a triangular wave generator such that frequency of oscillation is 4 kHz and $V_{out(pp)}$ = 10.8V. The op-amp saturation voltage is ± 15V. **06**

b) Which is the filter that possesses ripple pass and flat stop band? Explain the response of second order butterworth filter. **06**

5. a) An IC 555 has typical pin connections with components is shown in fig, it is desired to generate a square pulse of 10 kHz. Evaluate values of R_A and R_B if the capacitor C has the value of 0.01 μF for the configuration chosen. If necessary you can suggest modification in the external circuit configuration. **06**



b) Explain working of PLL using appropriate block diagram and explain any one application of the same. **06**

c) Explain with functional block diagram the operation of 566 voltage controlled oscillator. Also determine the maximum and minimum output frequencies. **06**

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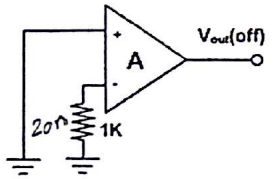
1. a) How can we improve CMRR? Explain. Why does an op-amp have high common mode rejection ratio. **04**

b) An inverting amplifier is implemented with $R_1 = 1\ k\Omega$ and $R_f = 100\ k\Omega$. Find the percentage change in the closed loop gain. A is the open loop gain changes from 2×10^5 V/V to 5×10^4 V/V. **04**

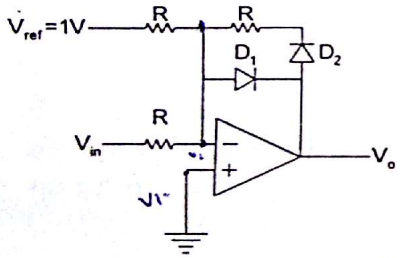
c) What is the differential input voltage for the given circuit $I_{in(off)} = 20$ nA and $V_{in(off)} = 0$. If $A = 10^5$, what does the output offset voltage? **04**



2. a) List the parameters that are important for ac applications and what problem can occur with a steep gain roll-off in an op-amp? **06**

b) What do you mean by slew rate limiting frequency? Calculate slew rate and maximum possible frequency of the input voltage that can be applied to get undistorted output for the parameters as I_{CQ}=10μA and C_C=33 nF and peak value for input voltage is 15V. **06**

3. a) Neatly sketch and label the dc transfer characteristic (i.e.V_0 vs V_{in}) for the circuit shown in below as V_{in} varies from -3V to +3V. Assume ideal op-amp, and the diodes have a forward voltage of 0.65V and zero incremental resistance. **06**



b) Design a differentiator to differentiate an input signal that varies in frequency from 10.5 H_Z to about 1000 H_Z. If a sine wave of 1V peak at 1 kHz is applied to the differentiator, draw its output waveform. **06**

4. a) Derive the expression for output frequency and gain of phase shift oscillator. Why negative feedback is used in RC phase shift oscillator. **06**

b) Design a noninverting Schmitt trigger circuit to obtain ±100mV crossover voltages. Its saturated output voltages are ±10V. Choose suitable component values. **06**

5. a) Draw the block diagram of Astable multivibrator using 555 timer and derive an expression for its frequency of oscillation. **06**

b) Derive the expression for capture range for PLL where a simple RC network is used as a LPF. **06**

c) Draw the functional diagram of IC 555 Timer. Explain with a circuit diagram how it can be connected for monostable operation. **06**