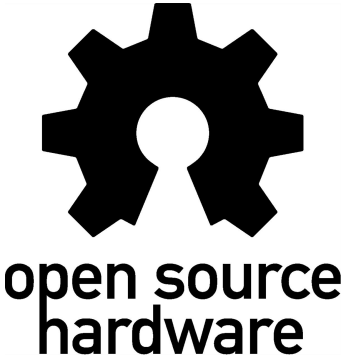
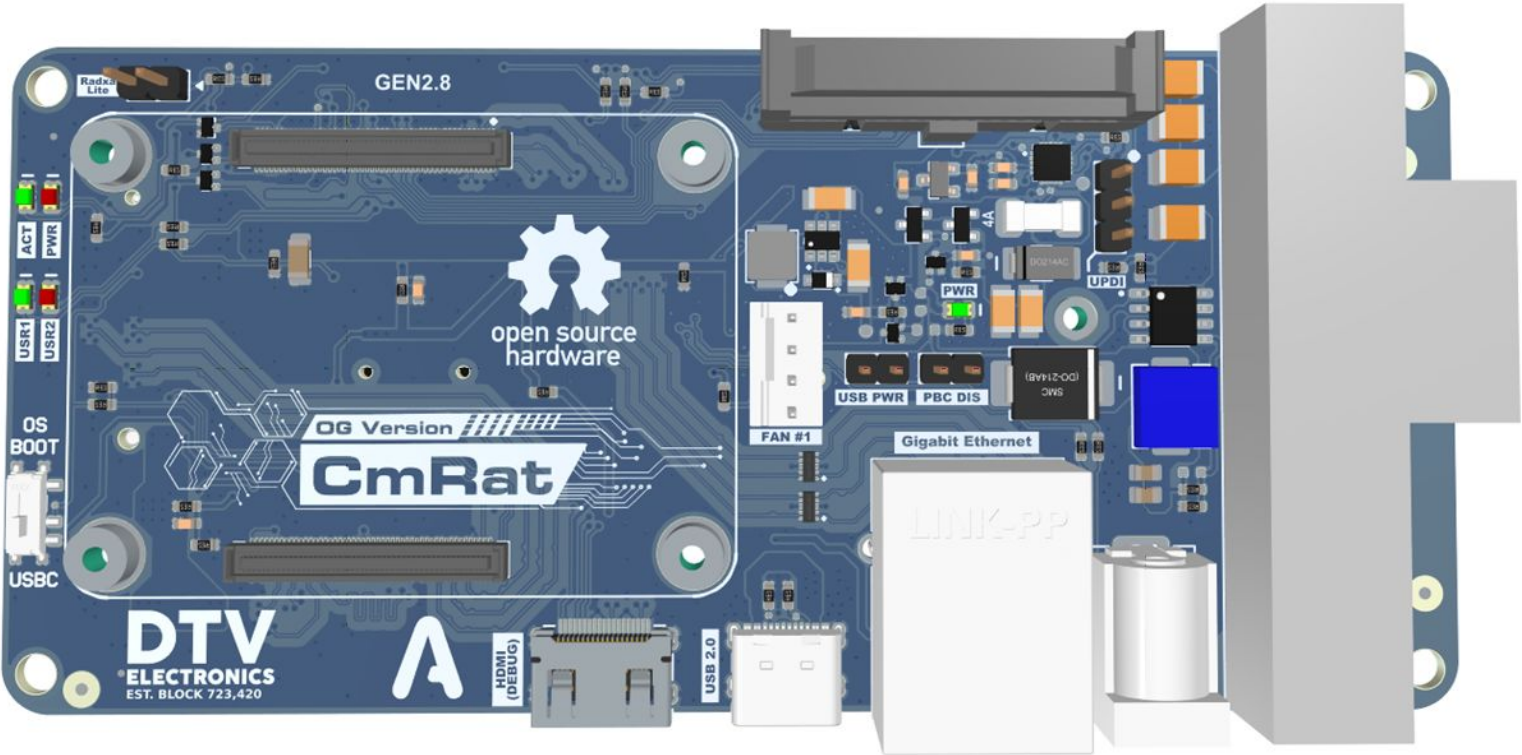
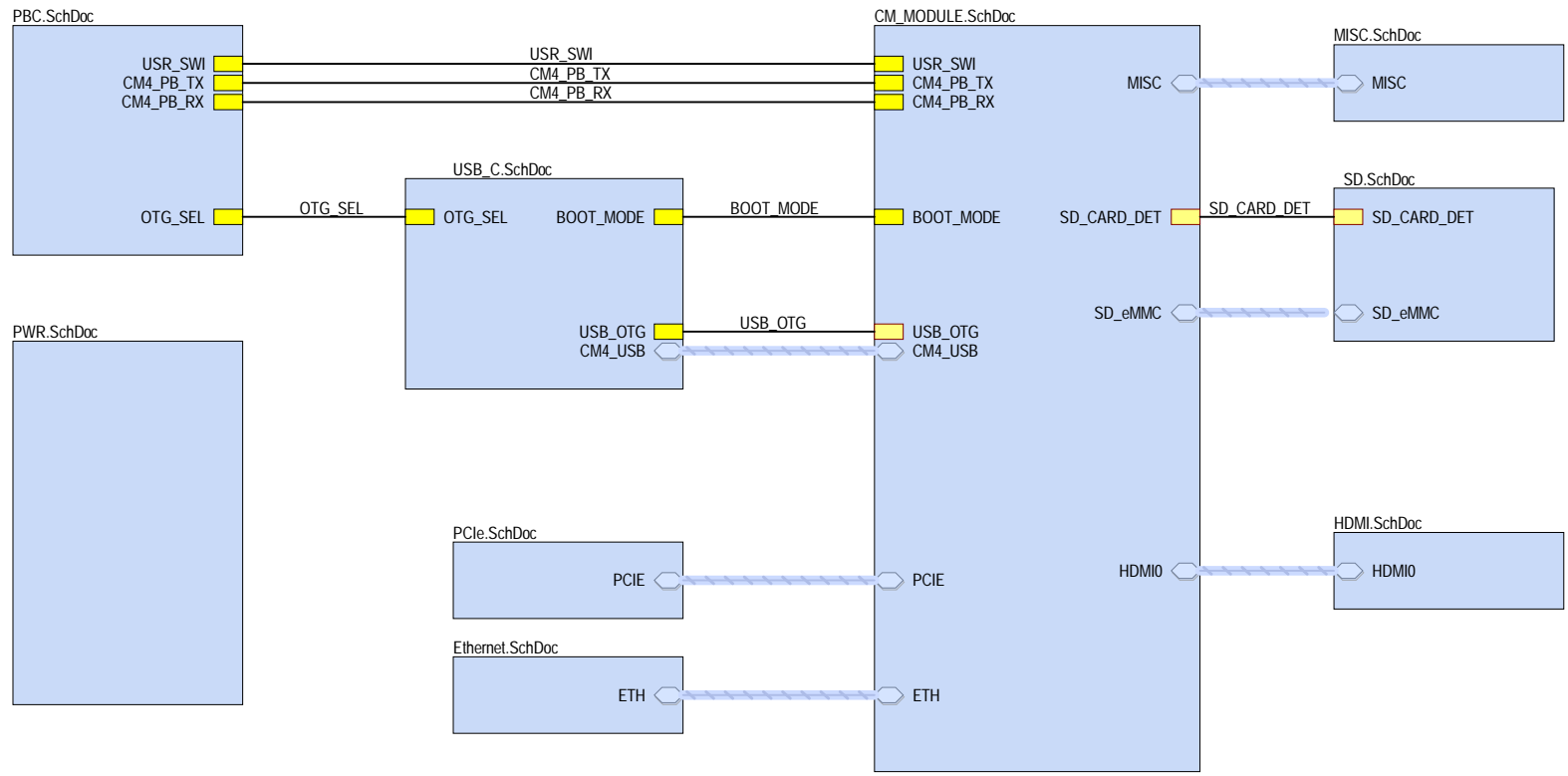


CMRat Computer (GEN2.8)

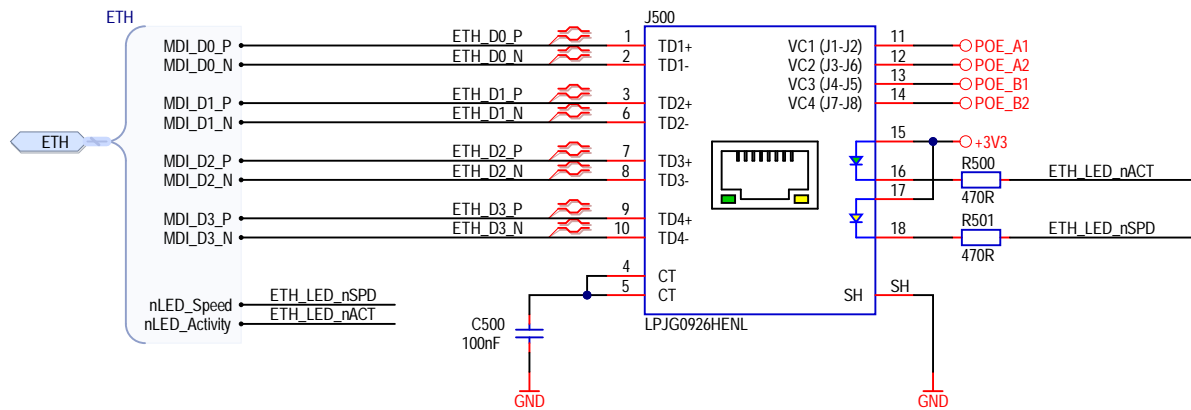
Cannot open file G:\Mój dysk\Praca\Kaico\GFX\MiXXjugo.png. File does not exist.



Title		A
COVER PAGE.SchDoc		
Project:	CMRat Computer	
Variant:	FULL	Version V2.8

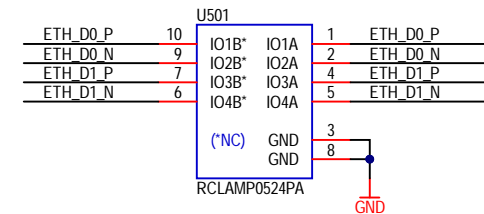
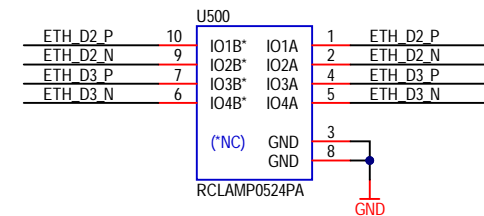


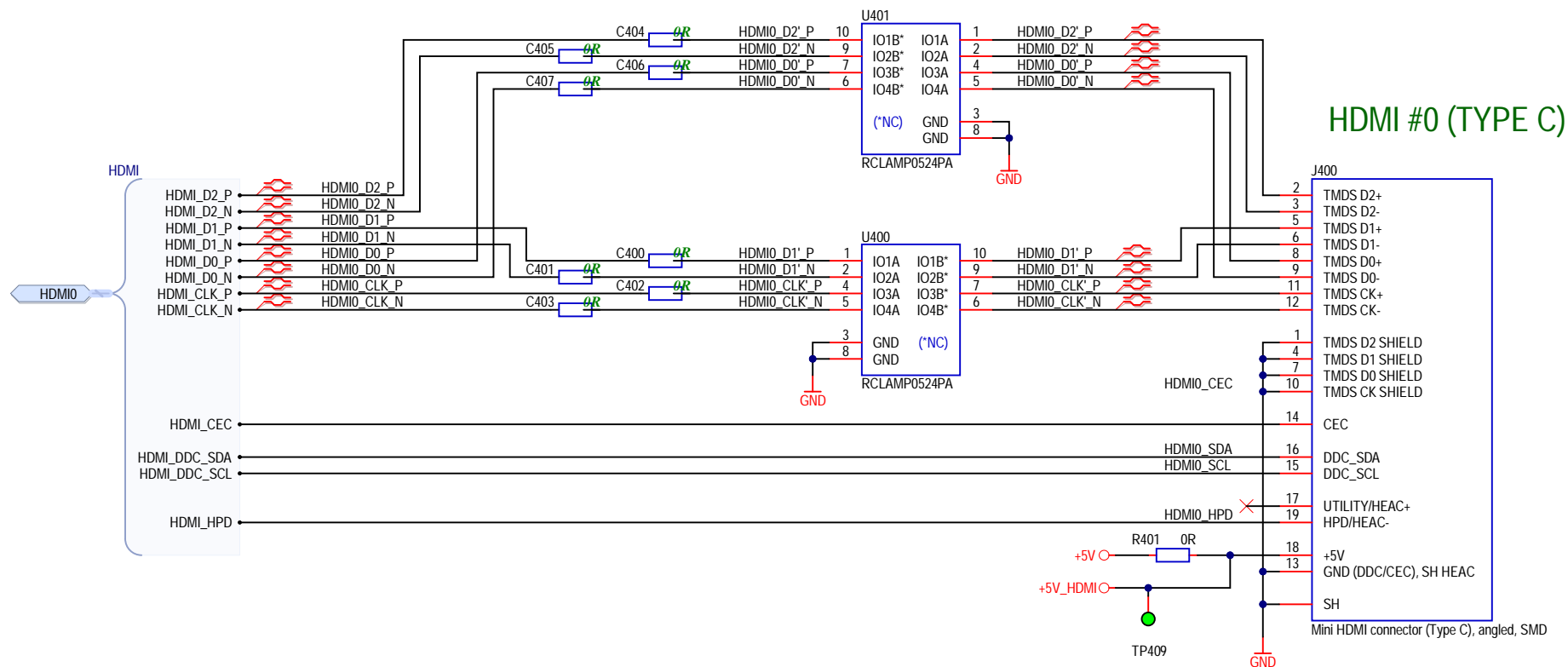
100/1000M ETH + POE/POE+



BOM:

RJ45 connector: 100/1000M RJ45, Tab-down, G/Y LEDs, PoE/PoE+:
Link-PP, LPJG0926HENL
Link-PP, LPJG4926HENL
HULYN, HRK1-1B71PG5-36A1BB-1R
TRXCOM, TRJG0926HENL





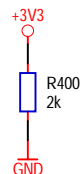
BOM:

HDMI #0 connector:
XKB Connectivity, MPN = A71-05H4-111N1
Würth Elektronik, MPN = 685119136923
Description: Type C (Mini), 19 pins, 0.4mm pitch, angled, SMD.

3V3 LOAD

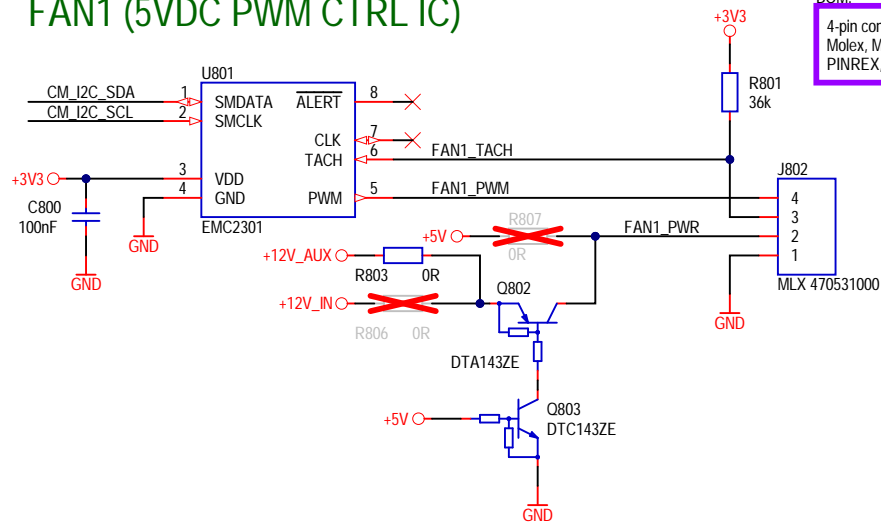
SCH:

Extra load on the 3V3 power rail to fix the HDMI issue with 5V LED.



Title	HDMI.SchDoc	A
Project:	CMRat Computer	
Variant:	FULL	
		Version V2.8

FAN1 (5VDC PWM CTRL IC)



BOM:
4-pin connector (2.54mm pitch):
Molex, MPN = 47053-1000.
PINREX, MPN = 744-81-04TW30.

M2.5 STEEL SPACERS

MECH800
M2.5, L = 3.0mm

MECH801
M2.5, L = 3.0mm

MECH802
M2.5

MECH804
M2.5, L = 3.0mm

MECH805
M2.5, L = 3.0mm

MECH806
M2.5

BOM:
SMT Steel Spacer with internal Thread M2.5, L = 3.0mm:
Use Wurth Elektronik, MPN = 977 403 015 1.

PCB MARKING

FID800
Fiducial

FID801
Fiducial

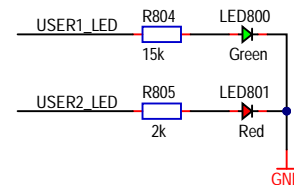
FID802
Fiducial

FID803
Fiducial

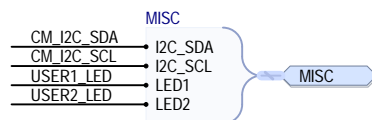
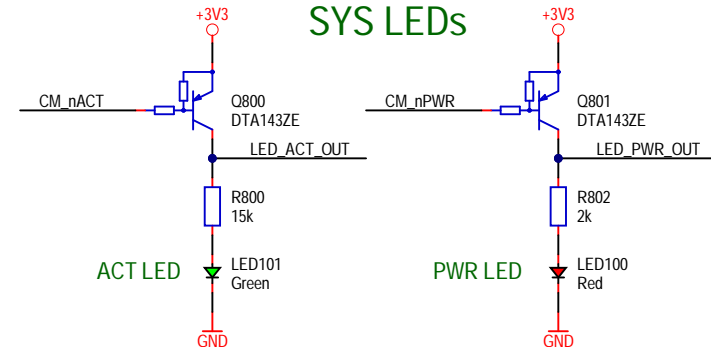
FID804
Fiducial

FID805
Fiducial

USER LEDs



SYS LEDs



PCB801
LAYER INDICATOR
PCB_LAYER_STACKUP

Title	MISC.SchDoc	A
Project:	CMRat Computer	
Variant:	FULL	
		Version V2.8

The schematic diagram illustrates the PBC interface and user switch circuitry. It is divided into two main sections: PBC INTERFACE and USER SWITCH.

PBC INTERFACE:

- +5V:** Connected to R700 (2k) and R705 (2k). R700 is connected to ADC_5V0_CM4. R705 is connected to GND.
- +3V3:** Connected to R701 (2k) and R706 (20k). R701 is connected to ADC_3V3_CM4. R706 is connected to GND.
- +3V3_PCIE:** Connected to R702 (2k) and R707 (20k). R702 is connected to ADC_3V3_PCIE. R707 is connected to GND.

USER SWITCH:

- +3V3_PBC:** Connected to R703 (15k) and R704 (470R). R703 is connected to MCU_USR_SWI. R704 is connected to USR_SWI.
- MCU_USR_SWI:** Connected to R703 (15k) and C700 (100nF). C700 is connected to GND.
- USR_SWI:** Connected to R704 (470R) and USR_SWI.
- CM4_BOOT:** Connected to R710 (2k) and OTG_SEL.
- OTG_SEL:** Connected to R710 (2k) and OTG_SEL.

CM4 PB RX and TX:

- CM4_PB_RX:** Connected to R708 (2k) and CM4_PB_RX.
- CM4_PB_TX:** Connected to R709 (2k) and CM4_PB_TX.

TESTPOINTS (DEBUG)

The diagram illustrates the test points for debug on a PBC_DBG line. A horizontal line represents the PBC_DBG signal. A green circle, representing a test point, is located on this line. To the right of the green circle is the label TP923. Below the PBC_DBG line, there are two columns of test points. The left column lists test points for MCU_UPDI, MCU_PWR_SWI, MCU_USR_SWI, PWR_MOS, HW_VERO, and HW_VER1. The right column lists test points for ADC_3V3_CM4, ADC_3V3_PCIE, PBC_TXD, PBC_RXD, and CM4_BOOT. Each test point is represented by a blue circle with a red dot in the center, and a horizontal line connects it to the PBC_DBG line. The test points are arranged in two columns, with the left column containing six test points and the right column containing five test points.

MCU_UPDI	TP906	ADC_3V3_CM4	TP913
MCU_PWR_SWI	TP907	ADC_3V3_PCIE	TP914
MCU_USR_SWI	TP908	PBC_TXD	TP915
PWR_MOS	TP909	PBC_RXD	TP918
HW_VERO	TP910	CM4_BOOT	TP919
HW_VER1	TP911		

PUSH-BUTTON CONTROLLER

MCU

MCU UPDI 19 PA0 (RESET/UPDI) PB0 14 PBC_RFU GPIO RFU
 ADC_5V0_CM4 20 PA1 PB1 13 RTC_INT GPIOINT RFU
 ADC_3V3_CM4 21 PA2 PB2 12 PBC_TXD USART0-TXD
 ADC_1V8_CM4 22 PA3 (EXTCLK) PB3 11 PBC_RXD USART0-RXD
 ADC_3V3_PCIE 5 PA4 PB4 10 IR_RX GPIOINT RFU
 ADC_5V0_USB 6 PA5 PB5 9 PBC_DBG GPIOCLKOUT
 HW_VER0 7 PA6 PC0 15 MCU_USR_SWI GPIO
 HW_VER1 8 PA7 PC1 16 MCU_PWR_SWI GPIO
 PC2 17 CM4_BOOT GPIO
 PC3 18 STAT_LED GPIO RFU

VDD 4 +3V3_PBC
 GND 3
 EP GND

ATTINY806

HARDWARE VERSION

+3V3_PBC R711 DNP HW_VER1
 +3V3_PBC R712 DNP HW_VER0
 R713 1k
 R714 1k
 GND

HW_VER = 0000_0000 => BitPiRat (0000) + GEN2.1 (0000)


MCU ISP (UPDI)

J901 HDR 1x3
 1 +3V3_PBC
 2 ISP_UPDI
 3 GND
 R716 100R
 R715 15k
 MCU_UPDI

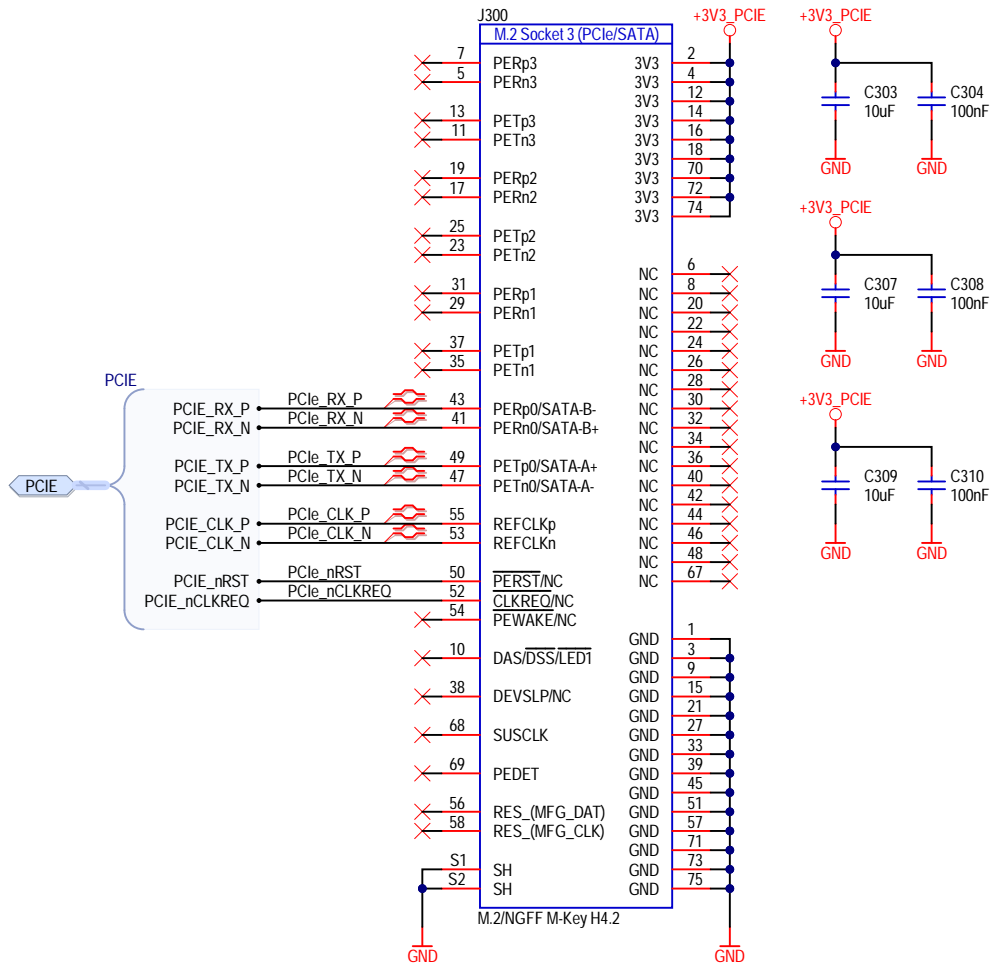
3.3V/300mA LDO

+5V_FUS U701 VIN VOUT +3V3_PBC
 C703 10uF 1 GND
 C704 10uF 2 GND
 AP2210N-3.3

HW_VER = 0000_0000 => BIHPiRat (0000) + GEN2.1 (0000)

Title	PBC.SchDoc	
Project:	CMRat Computer	Version
Variant:	FUJIL	V2.8

M.2 Socket 3 (M-Key) PCIe x1



BOM:

M.2 connector (NGFF), M-Key:
H2.3 -> Lotes, MPN = APC10146-P001A
H3.2 -> Lotes, MPN = APC10079-P002A
H4.2 -> Lotes, MPN = APC10107-P001A
H4.8 -> Lotes, MPN = APC10113-P001A
H3.2 -> TE Connectivity, MPN = 1-2199119-5
H4.2 -> TE Connectivity, MPN = 1-2199230-5

TESTPOINTS (DEBUG)

PCIE_nRST TP300
PCIE_nCLKREQ TP301
+3V3_PCIE TP303
+3V3_PCIE TP304

STAND-OFF HEIGHT TABLE

Connector Height Descriptor	L1
H2.3	0.35 ± 0.03
H2.5	0.55 ± 0.03
H2.8	0.80 ± 0.03
H3.2	1.45 ± 0.03
H4.2	2.45 ± 0.03

MECH301
M2.5, L = 2.5mm

SCR300
M2.5

~~MOD300~~
~~MOD_SSD_NGFF~~

Title	PCle.SchDoc	A
Project:	CMRat Computer	
Variant:	FULL	
		Version
		V2.8

