Department of Electronics and Communication Engineering

Vasavi College of Engineering (Autonomous)

ACCREDITED BY NAAC WITH 'A++' GRADE

IBRAHIMBAGH,HYDERABAD-500031

CERTIFICATE

This is to certify that the Theme based Project titled **"Implementation of PCIe Protocol on Zynq Ultrascale FPGA'**

submitted by

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Students of Electronics and Communication Engineering Department,Vasavi College of Engineering in partial fulfillment of the requirement of the award of the Degree of Bachelor of Engineering in Electronics and Communication Engineering is a record of the bonafide work carried out by them during the academic year 2023-2024.

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1.INTRODUCTION TO PCIe

Ever wondered how your computer manages to run all it's cool stuff so smoothly? Well, that's where PCIe (Peripheral Component Interconnect Express) comes into play – think of it like a super-fast road system inside your computer. This special road isn't for cars, though; it's for crucial parts like graphics cards and storage to talk to each other at lightning speed.

PCI Express (PCIe), or Peripheral Component Interconnect Express, is a high-speed serial computer expansion bus standard used for connecting various hardware devices to a computer. It is commonly used to connect graphics cards, network cards, storage devices, and other peripherals to the motherboard.We will discuss about this in more detail.

PCI Express was introduced to overcome the limitations of the original PCI bus, which operated at 33 MHz and 32 bits with a peak theoretical bandwidth of 132 MB/s. It uses a shared bus topology, where bus bandwidth is divided among multiple devices, to enable communication among the different devices on the bus. Over time, devices have evolved and become more bandwidth-hungry. As a result, bandwidth across the PCI bus has become limited due to these bandwidth-hungry devices starving other devices on the same shared bus.

2.Literature Survey

1)S. Monika. et.al.[12] in January 2014'. This paper implements the DC balanced 8B/10B coding in Super speed USB which employ a very fast FPGA from Xilinx family is proposed. Using the look-up table and memory with fast technique made this design efficient to be implemented. The Scrambling and descrambling modules are added in the above modules. This work can be extended by connecting this total module in between Link layer and Physical analog layer of USB 3.0architecture. Also the work can be extended to do the FPGA implementation by using SPARTAN 3E or Virtex V XILINX FPGA's. The Design of Physical layer coding can be rigorously tested if soft cores of link layer, physical analog layer are available.

2)SatishK.Dhawan worked on PCI Express-A New High Speed Serial Data Bus. It is a very high speed dualsimplex, point to point serial differential low voltage interconnect. The signaling rate is 2.5 Gbit per second, with 8/10 bit encoding to embed the clock in the data stream. On the transmit side parallel data is shifted out serially and on the receive side serial data is shifted into registers for parallel data output. The data is shifted serially at 2.5GHZ to the printed circuit board traces or to the cable segment [5].

3)Hemant Kumar Soni,[11]et.al. The aim of this paper is to design and verify the physical layer implementation by using ISE 8.1 from Xilinx and Spartan 3 FPGA to reduce the cost and hardware.PCS is the sub layer of the physical layer of PCI Express 1.0. The major constituents of this layer are transmitter and receiver. Transmitter comprises of 8b/10b encoder. The Primary purpose of this scheme is to embed a clock into the serial bit stream of transmitter lanes with advancement in the design by reducing the utilized hardware resources within FPGA . No clock is

transmitted along with the serial data bit stream. This eliminates EMI noise and provides DC balance.

3.Problem Statement

Our Project aims to implement the PCIe Protocol on the Zynq Ultrascale FPGA board. To Implement PCIe on the FPGA board,it involves integrating a PCIe IP core, designing a required hardware logic and developing necessary software drivers.Also It is thoroughly tested and the implementation ensures it meets the performance and compatibility requirements. This project will enhance the Zedboard's capabilities, enabling it to interface with high-speed PCIe devices and expanding its application potential in high-performance computing and data transfer applications.

4.Problem Approach

Implementation of PCIe protocol requires, understanding of the different layers and versions of the PCIe Protocol. It is also important to study the architecture of the Zedboard focusing on the availability of programmable logic and I/O resources. To implement this protocol a sequence of steps are to be followed.They are:

1)Design of System Architecture:
We design the overall system architecture, including how the PCIe interface will connect to the Zynq Processing System (PS) and Programmable Logic (PL).

2)IP Core Selection:
In this selection of IP Core for the FPGA board, we are using i.e. Zynq Ultrascale Board.We have taken the Ultra scale + PCIe integrated block IP which is already present in the IP catalog of the FPGA board in the Vivado.

3)Hardware Design:
It involves IP Core Configuration,We Configure the PCIe IP core in Vivado to match the required PCIe specification. The parameters like lane width, data rate, and addressing are selected as required and we also write an application-level software to test and demonstrate the PCIe interface. This software will perform data transfer operations and verify the correctness and performance of the PCIe link.

4)Simulation and Verification:
a)Create Testbenches:
We Develop testbenches to simulate the PCIe hardware design and use these to verify functionality, timing, and correctness of data transfers.
b)Run Simulations:

Perform extensive simulations to ensure that the design meets all functional and timing requirements. Validate error handling and any other redundant cases.

5)Hardware Implementation:

a)Synthesize and Implement:
We use Vivado to synthesize and implement the design on the Zynq Ultrascale board. Also ensures that the design fits within the FPGA resources and meets timing constraints.

b)Generate Bitstream:
Bit stream file is generated to program the FPGA Board.

5.Features of PCIe

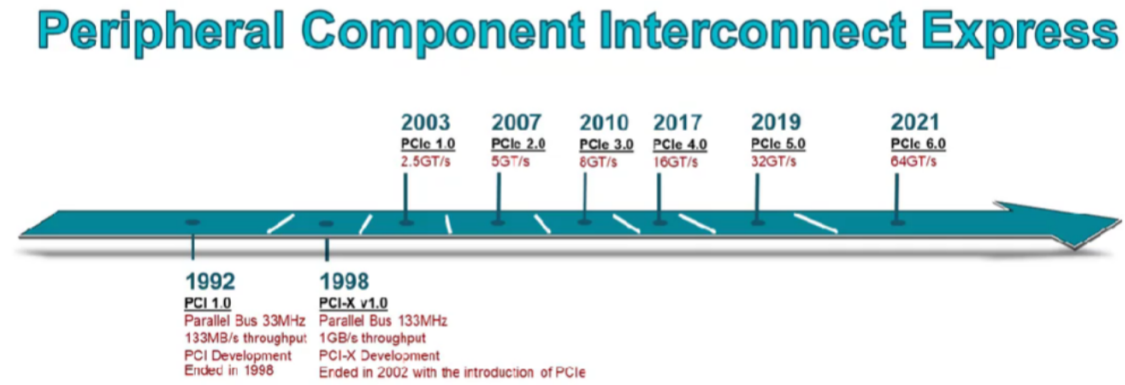
The features of PCIe (Peripheral Component Interconnect Express)makes it a widely used interface for connecting various components in modern computers. Some of its key features include:

1)PCIe follows a Point to Point topology between the CPU and the endpoint devices, which means each device connected via PCIe has a direct, dedicated lane to the CPU or a dedicated PCIe controller.

2)PCIe offers a high-speed data transfer rates, with each lane providing data rates of up to several gigabytes per second.As PCIe follows Serial Communication for the data transfer,in this serial communication there is no chance for electromagnetic interference of various paths,in turn there is no question of metastability,which is responsible for faster data rates in PCIe.

3)PCIe is scalable, allowing for flexible configurations with varying numbers of lanes (x1, x4, x8, x16, etc.). This scalability enables it to accommodate different bandwidth requirements for various devices.

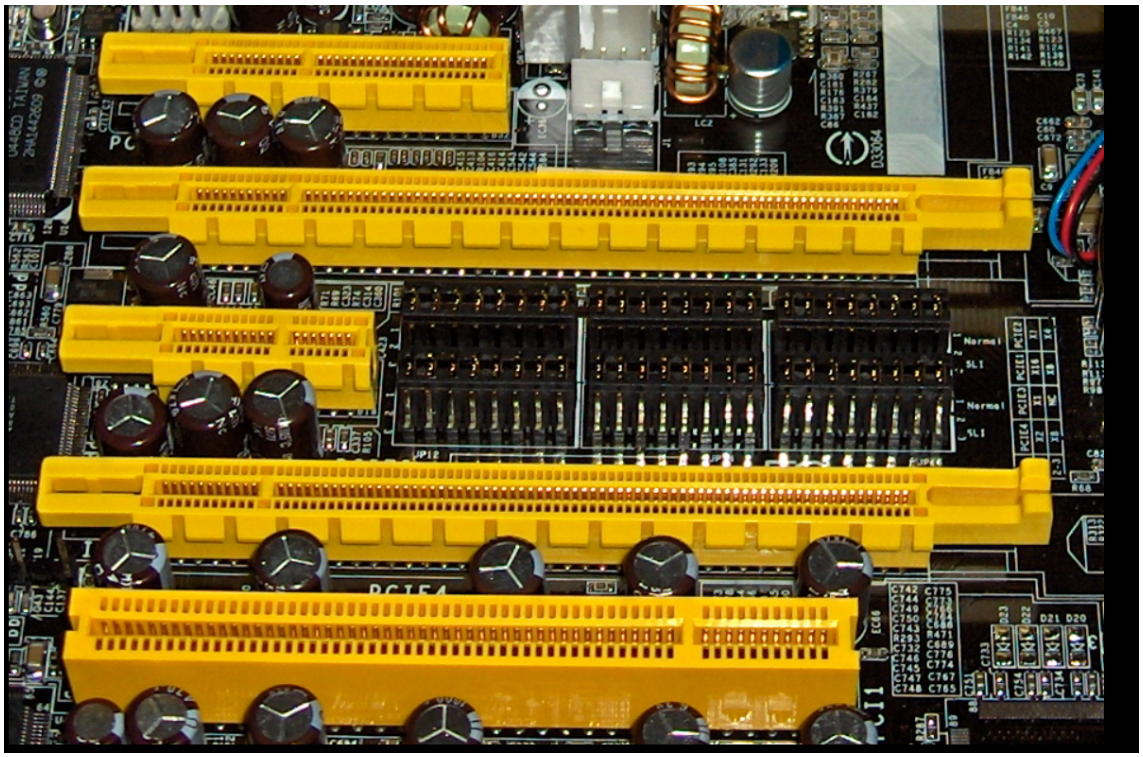
4)PCIe is backward compatible with older versions, allowing newer devices to work with older PCIe slots and vice versa. This is the reason why we have both Legacy endpoint and PCIe endpoint,in which Legacy endpoints are the endpoints which were dealt by the older versions of the PCIe and are backward compatible with the Present existing PCIe.



The below table give the information about the data throughputs of the PCIe over the various generations:

Generation	Year of Release	Data Transfer Rate	Bandwidth x1	Bandwidth x16
PCIe 1.0	2003	2.5 GT/s	250 MB/s	4.0 GB/s
PCIe 2.0	2007	5.0 GT/s	500 MB/s	8.0 GB/s
PCIe 3.0	2010	8.0 GT/s	1 GB/s	16 GB/s
PCIe 4.0	2017	16 GT/s	2 GB/s	32 GB/s
PCIe 5.0	2019	32 GT/s	4 GB/s	64 GB/s
PCIe 6.0	2021	64 GT/s	8 GB/s	128 GB/s

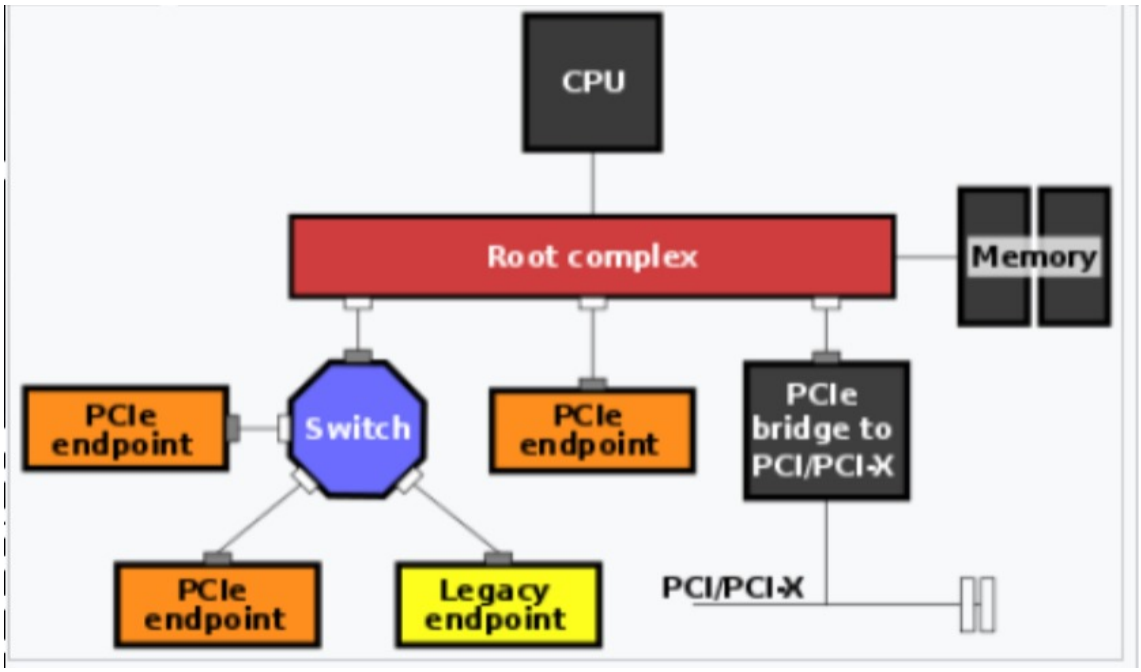
Iamge of PCIe ,with different lane widths



6.Topology of PCIe

In the context of PCIe (Peripheral Component Interconnect Express), topology refers to the way in which the PCIe lanes and devices are arranged and connected to each other and to the central processing unit (CPU) or a PCIe switch.
The toplogy of the PCIe include Root complex,PCIe Switch,PCIe endpoint, Legacy endpoint and various other buses and devices as shown below:

The detailed explanation of each element present in the topology of the PCIe mentioned as :
Root Complex (RC): This is the primary interface between the CPU and the PCIe endpoints. The root complex initiates transactions and manages communication with the various PCIe endpoints. Both



the data transfer from the CPU and receiving data to CPU takes place through this root complex.

Switches: Switches acts as the logical assembly of multiple virtual PCI-to-PCI Bridges.PCIe switches function similarly to network switches,allowing multiple devices to be connected and communicate through the root complex but it cannot split the data packets receiving from the root complex. Switches help to expand the number of available PCIe lanes and manage traffic between multiple devices.

Endpoints: These are the devices that connect to the PCIe bus, such as graphics cards, SSDs, network cards, and other peripheral devices. Each endpoint communicates with the root complex or through switches using dedicated lanes.There are two types of Endpoints named legacy endpoint and PCIe endpoint.

Legacy endpoint:A legacy endpoint is a device that was

originally designed for older versions of PCIe,such as PCI(Peripheral Component Interconnect), but has been adapted to work with the PCIe interface. These devices may not support all the advanced features of PCIe and might operate at lower performance levels compared to native PCIe endpoints.That is why we have this type of endpoints.

PCIe Endpoint:A PCIe endpoint is a device that is natively designed to interface with the PCIe protocol. These devices utilize the full capabilities of PCIe, including its advanced features and high-speed data transfer rates.

Lanes: PCIe communication occurs over lanes, which consist of pair of differential signals — one for sending data and one for receiving data. Lanes can be configured in different widths (x1, x4, x8, x16, etc.), with more lanes providing higher data transfer rates.

Links: A PCIe link is the connection between two PCIe devices, such as between an endpoint and the root complex or between two switches.The combination of all the lanes is called as a link.

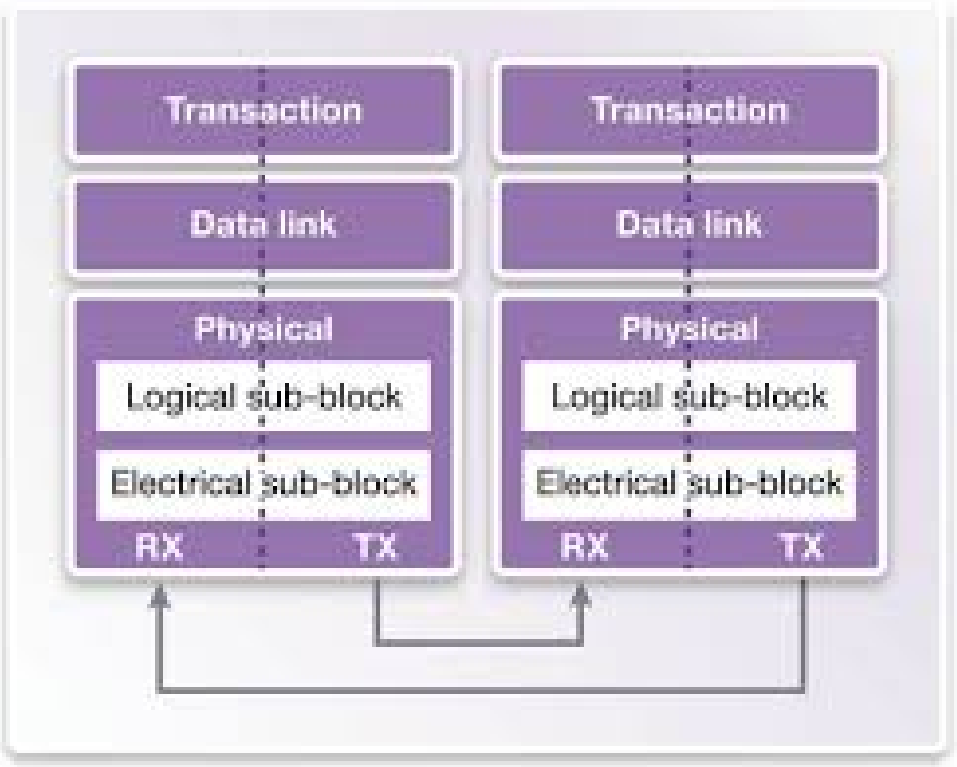
Ports: These are the connection points on the root complex, switches, and endpoints where PCIe devices can be connected. There are different types of ports, such as root ports, downstream ports (on switches), and upstream ports (on endpoints).

Topology Configuration: The overall configuration of how these elements are interconnected defines the topology. In a typical setup,the root complex connects directly to some endpoints via dedicated lanes.The root complex connects to switches, which in turn connect to additional endpoints, effectively expanding the number of devices that can be connected. This structured and efficient topology allows PCIe to provide high-speed, low-latency, and reliable connections for a wide range of

computing and peripheral devices.

7) Different Layers in PCIe

PCIe (Peripheral Component Interconnect Express) is structured into three main layers, the Transaction Layer, the Data Link Layer, and the Physical Layer. Each layer has distinct responsibilities and works together to ensure efficient communication between devices.



Transaction Layer:

The purpose of this layer is to manage the creation,

transmission, and reception of packets (transactions) that communicate data and control information between PCIe devices.The function of this layer is to create Packets,which Forms request and response packets for data transfer operations.It also manages credits and ensures that data flow is regulated to prevent buffer overflow or underflow. It maps high-level memory requests to specific addresses on the bus.

2)Data Link Layer:

The purpose of the data link layer is to ensure reliable data transfer between two directly connected PCIe devices by managing error detection and correction. This layers performs Error Detection and Correction by using a Cyclic Redundancy Check (CRC) to detect errors in transmitted data and requests retransmission if errors are found.It sends acknowledgments (ACKs) and negative acknowledgments (NAKs) to confirm successful receipt or request retransmission of packets.Finally,Prepares data packets for transmission by adding necessary headers and footers.

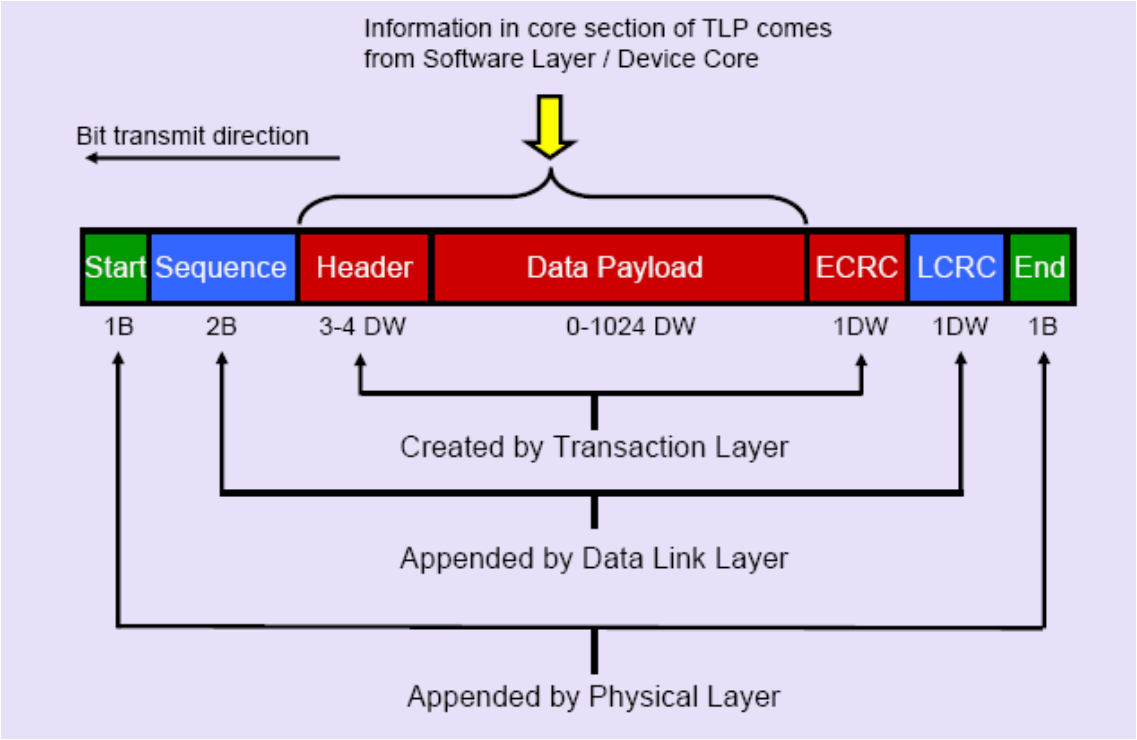
3) Physical Layer:

The purpose of this layer is to manage the actual physical transmission of data over the PCIe interconnect.The Functions include:

It defines the electrical characteristics of the signals, such as voltage levels and timing.

It Manages the configuration of PCIe lanes (x1, x4, x8, x16, etc.) and handles the transmission of data across these lanes.

It Uses encoding schemes like 8b/10b (for PCIe 1.x and 2.x) or 128b/130b (for PCIe 3.0 and later) to ensure data integrity during transmission.

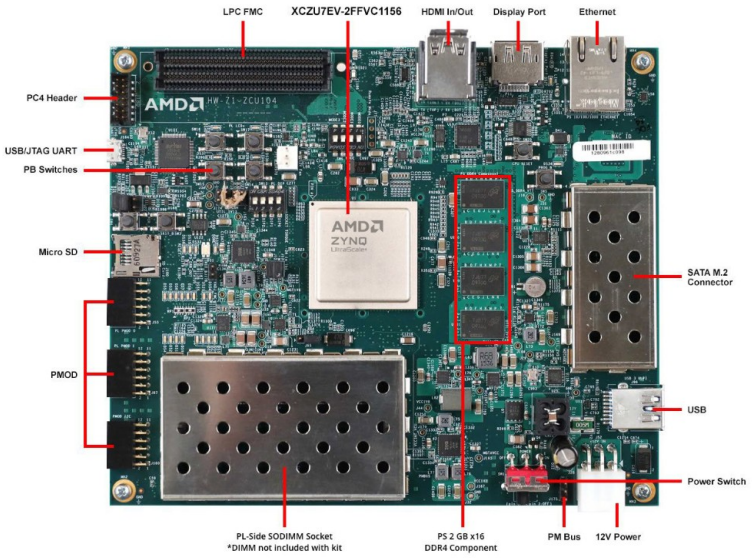


Together, these three layers facilitate efficient, reliable, and high-speed communication between PCIe devices, enabling them to perform complex data transfers and operations with minimal latency and high throughput.

8. Architecture of the Zynq Ultrascale Board

The Zynq UltraScale+ MPSoC by Xilinx combines a high-performance processing system (PS) with a programmable logic (PL) fabric in a single chip architecture. The PS includes ARM Cortex-A53 application processors, Cortex-R5 real-time processors, and optional graphics processing units (GPUs) for diverse processing capabilities. The PL offers FPGA fabric for customizable hardware acceleration, interfacing with the PS through high-bandwidth AXI interconnects. It boasts a rich set of peripherals,

including DDR memory controllers, high-speed connectivity options like PCIe and USB 3.0, and multimedia interfaces for display applications. Advanced security features, dynamic power management, and support for ARM TrustZone ensure secure and efficient operation across various applications, making it an ideal solution for embedded systems, networking, and high-performance computing.



10.Procedure and Observation

Creating a New project in the vivado by selecting the required language i.e. verilog and target board as the Zynq Ultrascale Board we start our project.
Then Going to the IP catalog present in the Vivado We select the Ultrascale+PCI Express Integrated Block Ip core.Clicking on it,gives us a developed IP Block of PCIe protocol.
By right clicking on the developed folder in the design of the vivado and using the Open IP example design we

generate the required design sources, input output ports,and the files to integrate the protocol on to the board.
Finally we develop the testbench to test and verify our design and run the design.
The observations after running the design is that the packets are continuously transmitted and received until they are completed.There are ports such as even clock,odd clock, system clock,Transmit data, recieve data.....
After the whole data packet completes its transaction there is a message in the console that the transmission and receiving the data is completed successfully with a random data.

10.Future Work

In this Theme based project of implementation of PCIe protocol on FPGA board,we have selected already available PCIe IP core which is available in the IP catalog of Zynq Ultrascale board in the vivado. Furtherly, we want to write the RTL code for this Protocol implementation in verilog.

Also a deep understanding of the three layers, Transaction layer,Datalink layer and Physical layer is necessary.So we decided to go through each layer of the PCIe deeply and code each layer in verilog and establish a link between them and want to design the IP catalog, which we used now on our own and implement the PCIe protocol on Zynq UltraScale FPGA board.

11.Conclusions

The successful implementation of PCIe on the Zynq Ultrascale Board represents enhancing the board's functionality and connectivity by incorporating PCIe.The FPGA Board gains the ability to communicate with PCIe-compatible peripherals, opening up a wide range of applications including high-speed data transfer, storage, and networking. This project requires an approach by combining hardware design and FPGA programming. Through hardware design, FPGA logic implementation, and software integration, the PCIe interface is implemented with efficiency, reliability, and performance optimization in mind. Thorough testing ensure that the PCIe implementation meets functional requirements and performance criteria, providing a solid foundation for future development and experimentation. Overall, the successful integration of PCIe significantly elevates the Zynq Ultrascale FPGA board versatility and utility, making it a more powerful and adaptable platform for embedded systems prototyping and development.

12.References

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2)https://www.udemy.com/course/pci-express-development-with-fpga/?amp

3)PCI Express® Base Specification Revision 5.0 Version 1.0

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