
**Department of Electronics and Communication Engineering**

**Vasavi College of Engineering (Autonomous)**

ACCREDITED BY NAAC WITH 'A++' GRADE

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# CERTIFICATE

This is to certify that the Mini Project titled **"IMPLEMENTATION OF PCIE SIDEBAND SIGNALS"** submitted by

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Students of Electronics and Communication Engineering Department,Vasavi College of Engineering in partial fulfillment of the requirement of the award of the Degree of Bachelor of Engineering in Electronics and Communication Engineering is a record of the bonafide work carried out by them during the academic year 2022-2023.

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HOD-ECE

# INDEX

# 1.INTRODUCTION TO PCIe

Ever wondered how your computer manages to run all its cool stuff so smoothly? Well, that's where PCIe (Peripheral Component Interconnect Express) comes into play – think of it like a super-fast road system inside your computer. This special road isn't for cars, though; it's for crucial parts like graphics cards and storage to talk to each other at lightning speed.

PCI Express (PCIe), or Peripheral Component Interconnect Express, is a high-speed serial computer expansion bus standard used for connecting various hardware devices to a computer. It is commonly used to connect graphics cards, network cards, storage devices, and other peripherals to the motherboard.We will discuss about this in more detail.

PCI Express was introduced to overcome the limitations of the original PCI bus, which operated at 33 MHz and 32 bits with a peak theoretical bandwidth of 132 MB/s. It uses a shared bus topology, where bus bandwidth is divided among multiple devices, to enable communication among the different devices on the bus. Over time, devices have evolved and become more bandwidth-hungry. As a result, bandwidth across the PCI bus has become limited due to these bandwidth-hungry devices starving other devices on the same shared bus.

## 2.Literature Survey

Literature Survey gives the research work related to this project done by several scholars ,scientists,reasearchers.Some of the reasearch work on this Project is:

1)The introduction by Jean-Marc Verdiell, Eric Zbinden, Raymond Lee, and Benjamin Troxell of the Samtec Optical Group discusses the evolution of PCI Express (PCIe) as the dominant bus standard for computer I/O since its introduction in 2004. The second generation (Gen2) of PCIe allows transfer rates of 5GT/s on up to 16 lanes, resulting in 80 Gb/s bandwidth with low latency. The upcoming third generation (Gen3) will further increase the speed to 8GT/s, providing an aggregate 128 Gb/s on x16 links.

2)The team, consisting of Jean-Marc Verdiell, Eric Zbinden, Raymond Lee, and Benjamin Troxell, has successfully demonstrated PCIe optical connections over fiber at distances of up to 300m. The optical connections offer several advantages in avionics applications, including high bandwidth, low weight, immunity to electromagnetic interference (EMI), and ruggedness of the electrical connector interface. This suggests that PCIe Active Optical Cables are well-suited for avionics environments where these attributes are crucial for reliable and high-performance connectivity

3) The authors, Odile Liboiron-Ladouceur from McGill University, Howard Wang, and Keren Bergman from Columbia University, describe the implementation of a power-efficient and low-latency edge node PCI-Express interface connected to a Wavelength Division Multiplexing (WDM) optical packet switched network. The focus of the report is on assessing scalability within the constraints imposed by the PCI-Express jitter

specification on packet propagation. The work aims to demonstrate a viable and efficient integration of PCI-Express with an optical packet switched network, considering power consumption, latency, and scalability aspects.

## 3.Problem Statement

As PCIe Gen3 and Gen4 standards redefine the landscape of high-speed data transfer, the conventional electrical transmission of Sideband Signals, including PERST,PRFCLK,POWER On, and WAKE, faces limitations in terms of signal integrity and susceptibility to electromagnetic interference.

The Challenge is to convert these critical signals into a serialized bitstream and transmit them optically via optic channels, addressing the demands for increased bandwidth and improved performance. This report aims to explore the methodologies, challenges, and outcomes associated with this transition, ensuring seamless integration within the PCIe architecture while adhering to the stringent standards of PCIe Gen3 and Gen4.

## 4.Approach

1. Study PCIe Sideband Signals: Begin with an in-depth exploration of PCIe sideband signals, dissecting their roles and functions in the context of data transfer and system management within PCIe Gen3 and Gen4 architectures.

2. Transceiver Selection: Identify and select optical transceivers compatible with PCIe Gen3 and Gen4 specifications. Ensure that the chosen transceivers align with the required data rates and protocols, emphasizing

their capability to maintain signal integrity.

3. Requirements Definition: Clearly outline the specific requirements for the optical transceivers, taking into account the unique characteristics of PCIe sideband signals. This includes stipulating data rates, protocol support, and any additional features critical for integration.

4. Mapping Strategy: Develop a robust strategy to map PCIe sideband signals to an optical medium. This involves serialization methods and considerations for seamless compatibility with selected optical transceivers while adhering to PCIe Gen3 and Gen4 standards.

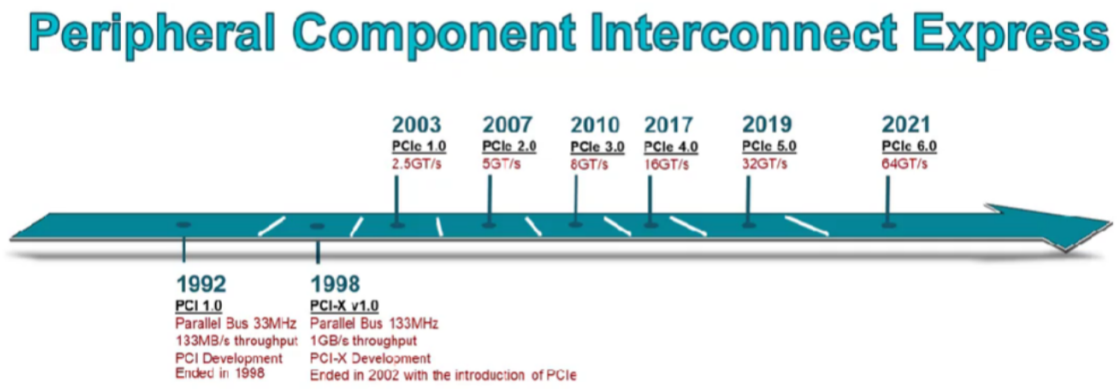
5. Signal Transmission Implementation: Implement the mapped PCIe sideband signals for transmission over the chosen optical transceivers. Rigorously test the efficiency of signal transmission, focusing on factors such as signal integrity, latency, and reliability.

6. Integration Testing: Integrate the optical transmission system into the PCIe Gen3 and Gen4 architecture. Conduct thorough compatibility testing to ensure a smooth integration that aligns seamlessly with the existing PCIe infrastructure.

## 5.Evolution of PCIe

The evolution of PCI Express (PCIe) signifies a revolutionary leap in interconnect technology, surpassing its predecessors, PCI and PCI-X. PCIe introduces a high-bandwidth, low pin count, and serial communication approach, departing from the parallel communication used in older standards. This shift enables higher data transfer rates and improved efficiency. PCIe boasts a smaller physical footprint with a reduced I/O pin count, making it suitable for space-constrained systems. Furthermore, it exhibits superior scalability for bus devices, accommodating a diverse range of peripherals. The addition of Advanced Error Reporting (AER) enhances reliability by providing detailed error detection and reporting mechanisms. In essence, PCIe's evolution addresses the growing demands of modern computing with a focus on speed, efficiency, and adaptability.

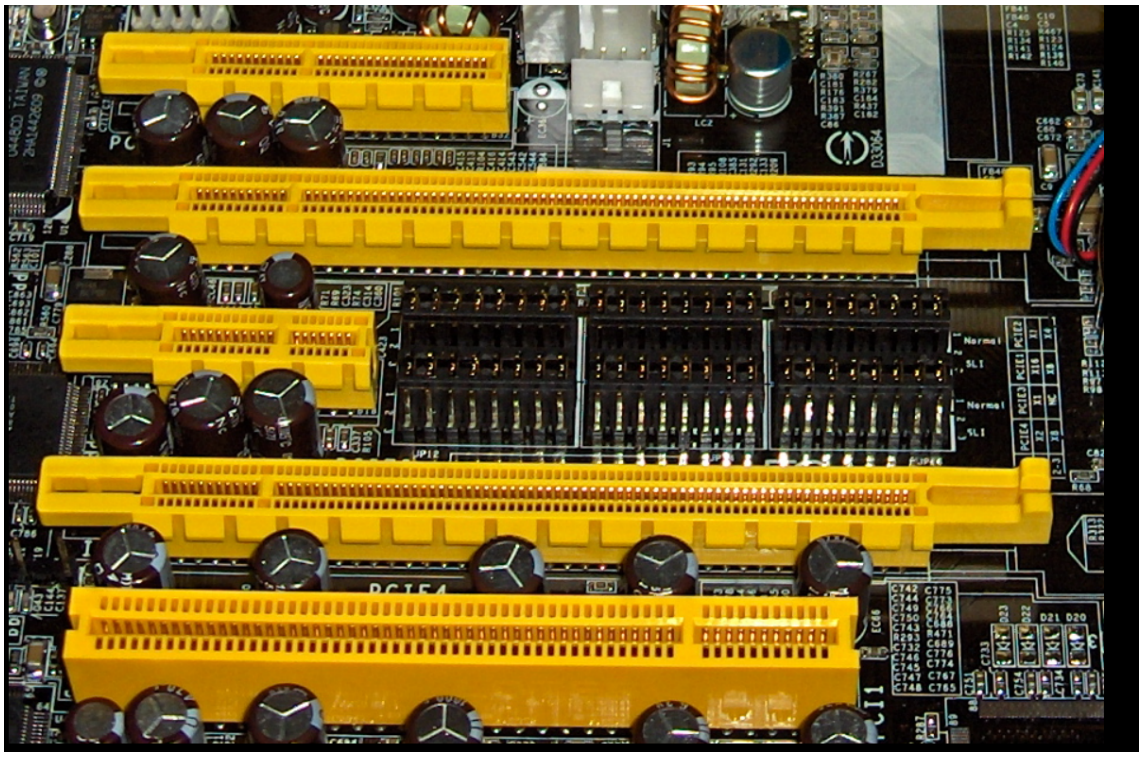
The below table give the information about the data throughputs of the PCIe over the various generations:

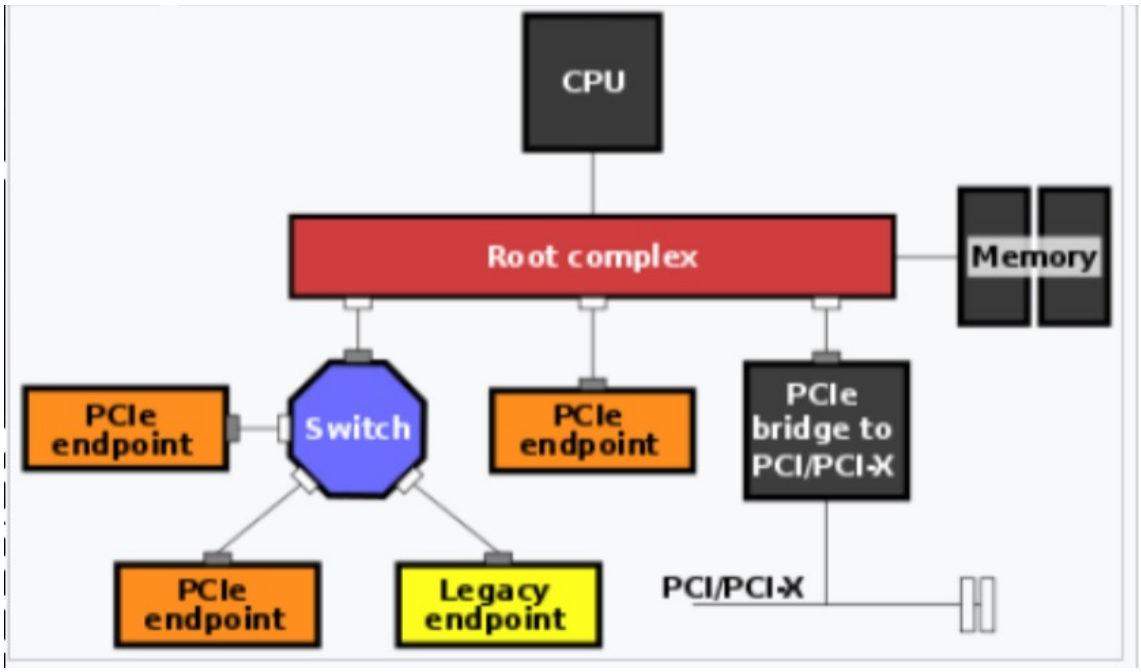



| Generation | Year of Release | Data Transfer Rate | Bandwidth x1 | Bandwidth x16 |
|---|---|---|---|---|
| PCIe 1.0 | 2003 | 2.5 GT/s | 250 MB/s | 4.0 GB/s |
| PCIe 2.0 | 2007 | 5.0 GT/s | 500 MB/s | 8.0 GB/s |
| PCIe 3.0 | 2010 | 8.0 GT/s | 1 GB/s | 16 GB/s |
| PCIe 4.0 | 2017 | 16 GT/s | 2 GB/s | 32 GB/s |
| PCIe 5.0 | 2019 | 32 GT/s | 4 GB/s | 64 GB/s |
| PCIe 6.0 | 2021 | 64 GT/s | 8 GB/s | 128 GB/s |

## PCIe

Architecture of the PCIe:






## 6.Sideband signals in PCIe:

In the context of PCIe, "sideband signals" refer to additional signals or communication channels that run alongside the main data lanes. These sideband signals are used for various purposes, including control, management, and monitoring of the PCIe link.

Some of the other sideband signals mentioned of PCIe are :
1.SMDATA (Sideband Management Data)
2.SMCLK (Sideband Management Clock)
3.TCK (Test Clock)
4.TDI (Test Data In)
5.TDO (Test Data Out)
6.TMS (Test Mode Select)
7.TRST (Test Reset)

## 4 Signaling

Each component of PCIe communication (except for redrivers) have the following control signals: PERST, WAKE, CLKREQ, and REFCLK. These signals work to generate high-speed signals and communicate with other PCIe devices. Figure 4-1 shows the diagram of PCIe devices with the control signals. This diagram shows that all of the control signals except REFCLK are active low signals.

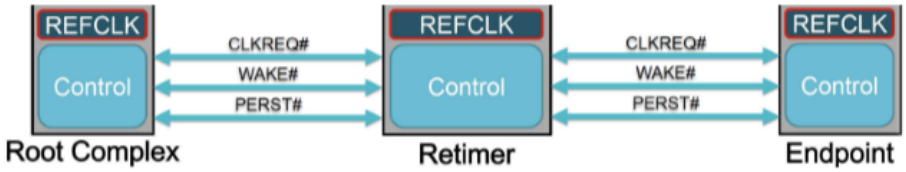



**Figure 4-1. PCIe Control Signals**

### 4.1 PERST

PERST is referred to as a fundamental reset. PERST should be held low until all the power rails in the system and the reference clock are stable. A transition from low to high in this signal usually indicates the beginning of link initialization. In Figure 4-1, it is referred as "PERST#."

### 4.2 WAKE and CLKREQ

WAKE and CLKREQ signals are both used for transitioning to and from low power states. WAKE signal is an active-low signal that is used to return the PCIe interafce to an active state when in a low-power state. CLKREQ signal is also an active-low signal and is used to request the reference clock. In Figure 4-1, these are referred as "WAKE#" and "CLKREQ#", respectively.

### 4.3 REFCLK

A REFCLK, or reference clock signal, is a prerequisite for a PCIe device to begin data transmission. This 100 MHz reference clock signal is used by the PCIe device to generate the high-speed PCIe data within the link and is shared by the PCIe devices within the link. In Figure 4-1, it is referred as "REFCLK."

## 5 Link Training

When all devices are powered and have a reference clock provided, a PCIe device starts the link training process. The link training process consists of receiver detection (Rx detect), polling, and configuration. After this process, PCIe devices are connected from the endpoint to the root complex.

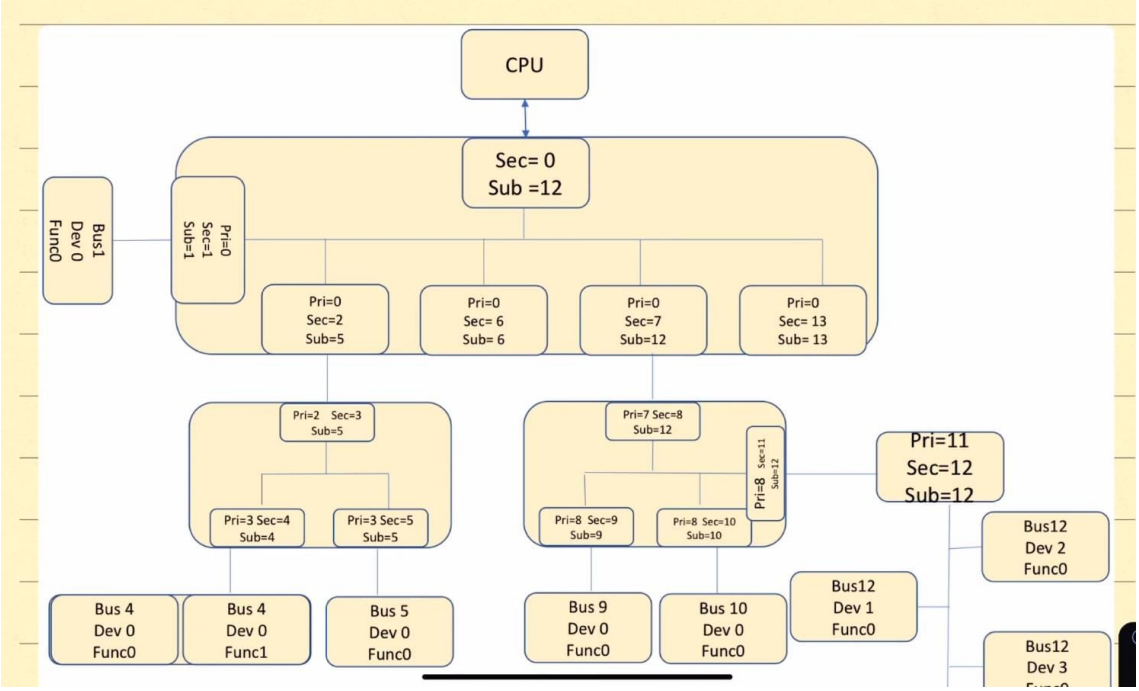
PCIe consists of both high speed signals and sideband signals. Where Side Band Signals are mainly used for power supply, controlmangament, coordination between the PCIe devices. High speed signals are responsible for transferring the actual user data between PCIe devices. But for enumeration we require all the side Band signals and a set of High speed signals. These signals which are responsible for the enumeration should be converted into optical signals.

| Pin | Side B | Side A | Description |
|---|---|---|---|
| 1 | +12 V | PRSNT1# | Must connect to farthest PRSNT2# pin |
| 2 | +12 V | +12 V | Main power pins |
| 3 | +12 V | +12 V | |
| 4 | Ground | Ground | |
| 5 | SMCLK | TCK | SMBus and JTAG port pins |
| 6 | SMDAT | TDI | |
| 7 | Ground | TDO | |
| 8 | +3.3 V | TMS | |
| 9 | TRST# | +3.3 V | |
| 10 | +3.3 V aux | +3.3 V | Aux power & Standby power |
| 11 | WAKE# | PERST# | Link reactivation; fundamental reset [23] |
| Key notch | | | |
| 12 | CLKREQ#[24] | Ground | Clock Request Signal |
| 13 | Ground | REFCLK+ | Reference clock differential pair |
| 14 | HSOp(0) | REFCLK− | Lane 0 transmit data, + and − |
| 15 | HSOn(0) | Ground | |
| 16 | Ground | HSIp(0) | Lane 0 receive data, + and − |
| 17 | PRSNT2# | HSIn(0) | |
| 18 | Ground | Ground | |

## 7.Enumeration

It is the process of detecting all the PCIe devices connected to the host bridge and their location,where the particular device is located by assigning address to

device.




The CPU begins by configuring the host bridge and setting the Sub Bus number to 255. Subsequently, it employs a Depth First Search (DFS) algorithm to systematically explore the PCI Express (PCIe) device hierarchy. The traversal starts from the 0th PCIe device and proceeds to the last PCIe endpoint until the desired endpoint is reached.
During this exploration, the CPU initiates transactions and reads critical information such as the Vendor ID and head register for each device encountered. These readings help the CPU make determinations about the nature of each device, discerning between multifunction and single-function devices and identifying whether they are endpoints or bridges.

This meticulous process ensures a comprehensive detection and configuration of all PCIe devices connected to the bus. The extended access mechanism configuration is employed to set up the system effectively, ensuring that each device is correctly identified and configured for optimal functionality within the PCIe architecture.

## 8.Future Work

The prototype design involves combining PCIe sideband signals and high-speed signals at the transmitter, transmitting them through a single channel, and demultiplexing at the receiver. Steps include developing a system for signal combination, implementing single-channel transmission using optical fiber, designing interfaces for transmitter and receiver, selecting components, rigorous testing and optimization, ensuring compliance with PCIe standards, and considering scalability. Thorough documentation is essential for understanding functionality, limitations, and recommendations for further improvements. This detailed process establishes a foundation for achieving seamless integration and advancements in PCIe signal processing technologies.

## 9.Conclusions

In conclusion, the evolution of PCIe represents a groundbreaking leap in interconnect technology, surpassing its predecessors with high bandwidth, low pin count, and serial communication. The shift to a serial approach allows for enhanced data transfer rates and efficiency, making PCIe adaptable to modern computing demands. Sideband signals play a crucial role in PCIe, serving various purposes alongside the main data lanes, ensuring effective control, management, and coordination among devices. The enumeration process in PCIe facilitates the detection and location of connected devices, providing addresses for optimal system configuration. Looking ahead, the prototype design, focused on combining sideband and high-speed signals for transmission and demultiplexing, holds promise for advancing PCIe signal processing technologies. By emphasizing scalability, compliance with standards, and thorough documentation, this design sets the stage for seamless integration and future enhancements in PCIe architectures.

## 10.References

1)Texas Instruments, High-Speed Layout Guidelines for Signal Conditioners and USB Hubs

2)Design and Implementation of a Data Transfer

3)Protocol Via Optical Fiber Shizu Minami, Jan Hoffmann, Nikolaus Kurz, and Wolfgang Ott https://www.renesas.com/us/en/products/interface/pci-express-solutions

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