HO CHI MINH CITY UNIVERSITY OF TECHNOLOGY

OFFICE FOR INTERNATIONAL STUDY PROGRAM

SEMESTER: 251

LAB 6 REPORT

INSTRUCTOR:

MR. PHAM CONG THAI

Student Name	ID
Trần Lê Tuấn Anh	2452089
Ngô Đức Anh	2452054
Nguyễn Thành Trường An	2452020

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Workload and Team Contribution

No.	Name	Student ID	Workload	Contribution
1	Trần Lê Tuấn Anh	2452089	Report, 2.3.1 , 2.3.2	100%
2	Nguyễn Thành Trường An	2452020	4. , 5.1	100%
3	Ngô Đức Anh (nhóm trưởng)	2452054	3.1 , 3.2 , 5.2	100%

1. Introduction

In the Bipolar Junction Transistor tutorials, we saw that the output Collector current of the transistor is proportional to input current flowing into the Base terminal of the de- vice, thereby making the bipolar transistor a **CURRENT** operated device (Beta model) as a smaller current can be used to switch a larger load current.

The Field Effect Transistor, or simply FET however, uses the voltage that is applied to their input terminal, called the Gate to control the current flowing through them resulting in the output current being proportional to the input voltage. As their operation relies on an electric field (hence the name field effect) generated by the input Gate voltage, this then makes the Field Effect Transistor a **VOLTAGE** operated device.

The Field Effect Transistor has one major advantage over its standard bipolar transistor cousins, in that their input impedance, (Rin) is very high, (thousands of Ohms), while the BJT is comparatively low. This very high input impedance makes them very sensitive to input voltage signals, but the price of this high sensitivity also means that they can be easily damaged by static electricity.

2. Junction Field Effect Transistor

We saw previously that a bipolar junction transistor is constructed using two PN-junctions in the main current carrying path between the Emitter and the Collector terminals. The Junction Field Effect Transistor (JUGFET or JFET) has no PN-junctions but instead has a narrow piece of high resistant semiconductor material forming a "Channel" of either N- type or P-type silicon for the majority carriers to flow through with two ohmic electrical connections at either end commonly called the Drain and the Source, respectively.

Before analysing the circuit using JFET, students are proposed to characterize the I-V curve of a JFET in PSPICE (named JbreakN in the Favourite list), to determine IDSS and VP, which are two parameters for a JFET. The circuit bellow is required to implement in PSPICE:

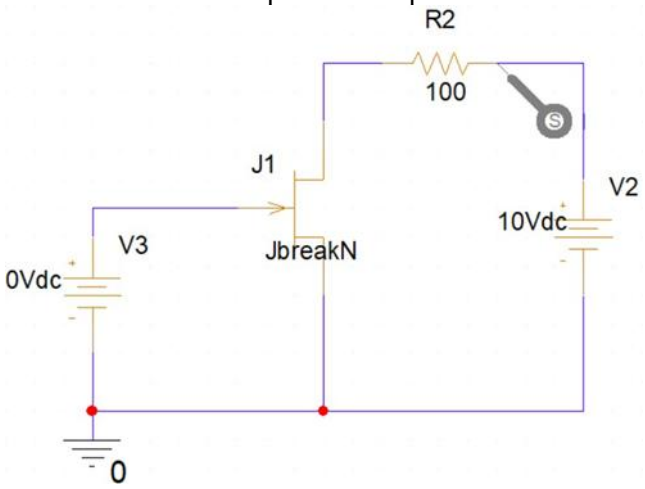


Figure 2.1: JFET circuit in PSPICE

2.1 DC Sweep simulation

In the first simulation, a DC sweep for input source V3 is perform, varying from -3V to 0V to verify the **active region**. The simulation profile is suggested as follows:

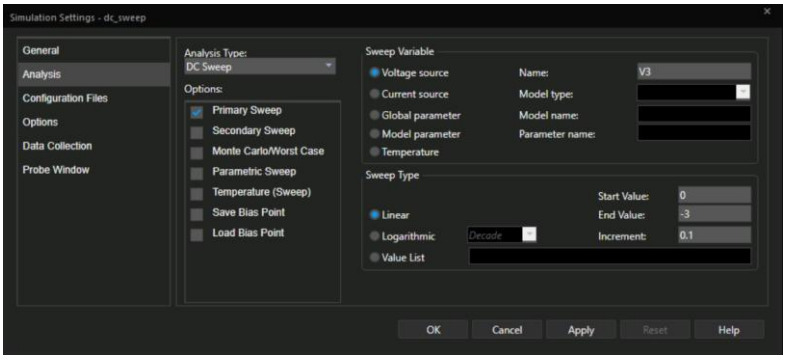


Figure 2.2: DC Sweep simulation profile

The simulation results are presented in the following figure:

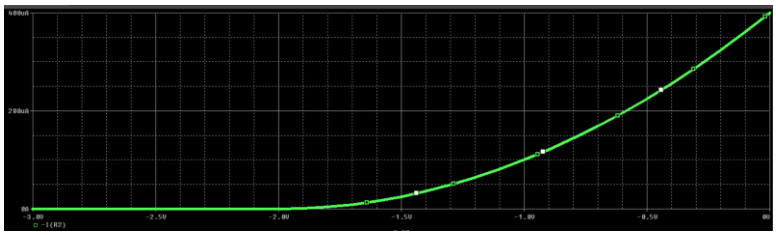


Figure 2.3: Simulation results for sweeping V3 from -3V to 0V

The simulation results confirm that **IDSS = 400mA** and **VP = -2V** for a typical JFET device in PSPICE.

2.2 Nested DC Sweep simulation

In this simulation, more details for the I-V characteristics are performed. Instead of vary- ing the source V3, V2 can be also varied in a nested DC Sweep simulation.

Firstly, for the primary DC sweep source, which is set to V2, is configured as follows:

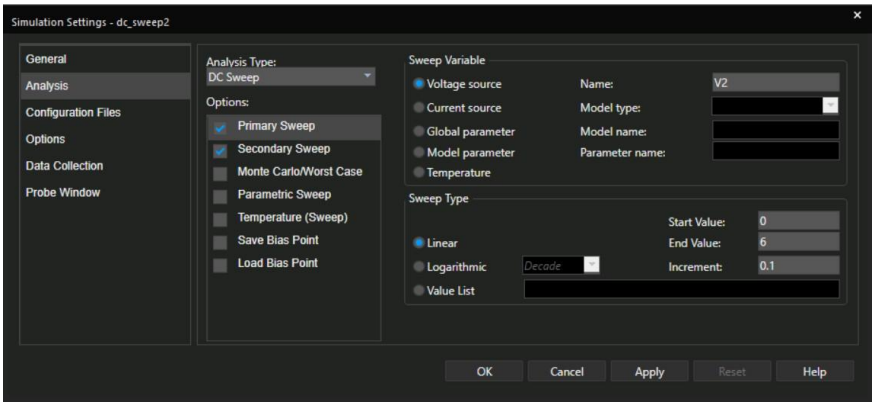


Figure 2.4: Primary dc sweep source V2

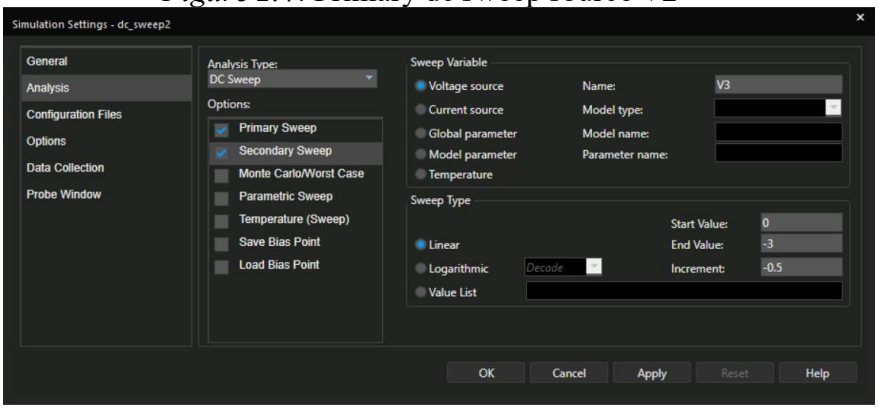


Figure 2.5: Primary dc sweep source V3

Secondly, the secondary DC sweep source, which is set to V3, is configured as follows: The simulation results are shown as the figure bellow:

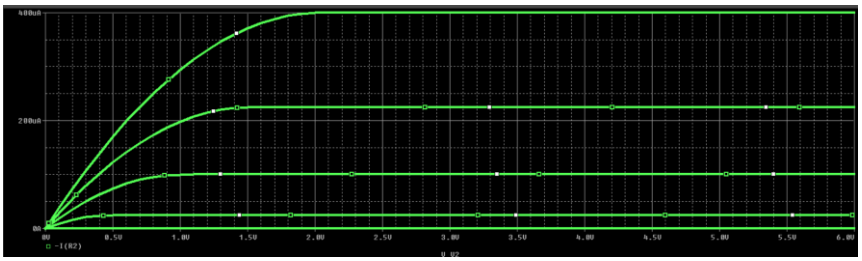


Figure 2.6: Simulation results with JFET

This figure also confirm that IDSS = 400mA and VP = -2V (the lowest curve is -1.9V). In this simulation, the ohmic region and saturation region are indicated better.

2.3 Exercises

2.3.1 Self bias configuration

This is the first configuration for a JFET, when the Gate pin is connected to the Ground. A typical circuit is presented as follows:

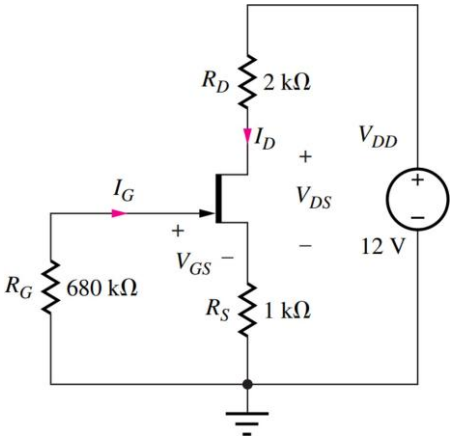
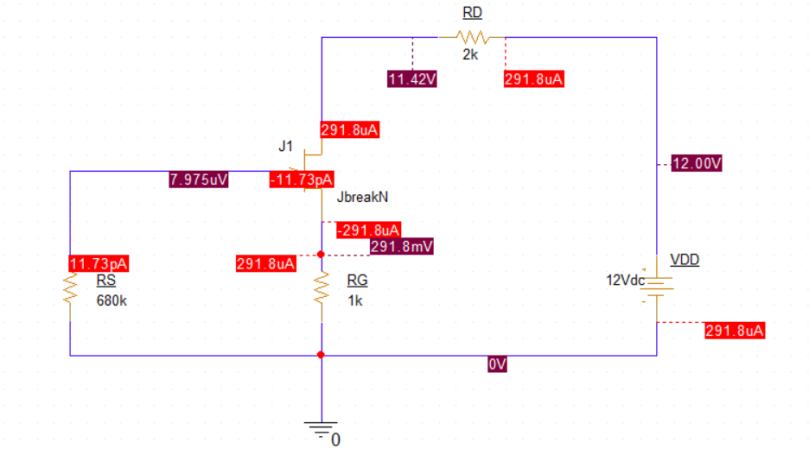


Figure 2.7: Self bias configuration

Students are proposed to implement this circuit in PSPICE with the JFET is JbreakN. The simulation results in PSPICE (**bias configuration**) are presented here. Moreover, a short explanations are required in this report to explain the value of ID and VGS.



Bias simulation

Explanation of V_{GS}

Since the JFET Gate current is negligible ($I_G \approx 0$), there is no voltage drop across the Gate resistor (R_G). Thus,

$V_G = 0V$.

The Source voltage is generated by the current flowing through R_S(1 kΩ):

$$V_S = I_D . R_S = 291{,}8\mu A . 1k\Omega \approx 0{,}292V$$

Therefore, the Gate-to-Source voltage is:

$$V_{GS} = V_G - V_S = 0 - 0{,}292 = -0{,}292V$$

Verification of I_D

Using the JFET parameters found in previous steps ($I_{DSS} = 400\mu A$ and $V_P = -2V$), we verify the current using Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = 400\mu A \times \left(1 - \frac{-0{,}292}{-2}\right)^2 \approx 291{,}6\mu A$$

Conclusion:

The theoretical calculation closely matches the simulation result (291,8 µA).

2.3.2 Voltage divider configuration

The proposed schematic for this configuration is presented as follows:

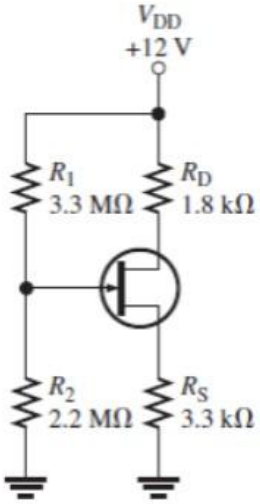
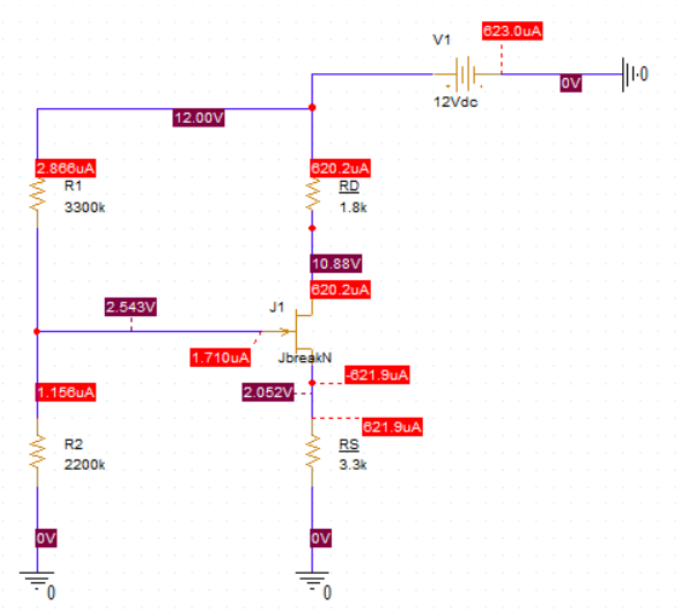


Figure 2.8: Voltage divider configuration

Students are proposed to implement this circuit in PSPICE with the JFET is JbreakN. The simulation results in PSPICE (**bias configuration**) are presented here. Moreover, a short explanations are required in this report to explain the value of ID and VGS.



Bias simulation

Analysis of Gate Voltage (V_G)

Theoretically, for an ideal JFET where input impedance is infinite ($I_G = 0$), the Gate voltage is determined purely by the voltage divider formed by $R_1$and R_2:

$$V_{G(theory)} = V_{DD} \cdot \frac{R_2}{R_1 + R_2} = 12V \cdot \frac{2{,}2M\Omega}{3{,}3M\Omega + 2{,}2M\Omega} = 12V \cdot 0{,}4 = 4{,}8V$$

However, the simulation shows $V_G = 2.543V$.

Reason:

The difference is caused by the Gate current (I_G). The simulation indicates a current of approximately $1.7\mu A$flowing into the Gate

($I_{R1} - I_{R2} = 2{,}866\mu A - 1{,}156\mu A$).

Because $R_1$and R_2have very high resistance (Mega-ohms), even this small current causes a significant voltage drop, pulling $V_G$down from 4.8V to 2.543V.

Analysis of $V_{GS}$and I_D

Using the simulation values:

$$V_{GS} = V_G - V_S = 2{,}543V - 2{,}052V = +0{,}491V$$

Since $V_{GS} > 0$, the Gate-Source junction is forward-biased (acting like a conducting diode). This explains why:

- There is a leakage current entering the Gate ($I_G \neq 0$).
- The Drain current ($620{,}2\mu A$) exceeds the device's saturation current ($I_{DSS} \approx 400\mu A$), as the forward bias enhances the channel conductivity beyond its normal depletion-mode limits.

3. Metal Oxide Semiconductor FET

As well as the Junction Field Effect Transistor (JFET), there is another type of Field Effect Transistor available whose Gate input is electrically insulated from the main current car- rying channel and is therefore called an Insulated Gate Field Effect Transistor.

The most common type of insulated gate FET which is used in many different types of electronic circuits is called the Metal Oxide Semiconductor Field Effect Transistor or MOS- FET for short.

The IGFET or MOSFET is a voltage controlled field effect transistor that differs from a JFET in that it has a “Metal Oxide” Gate electrode which is electrically insulated from the main semiconductor n-channel or p-channel by a very thin layer of insulating material usually silicon dioxide, commonly known as glass.

3.1 Depletion-mode MOSFET

The Depletion-mode MOSFET, which is less common than the enhancement mode types. This device is very similar to JFET, except that the maximum current saturation is ob- tained at VGS > 0. The circuit used to verify IDSS and VP for DFET is presented as follows:

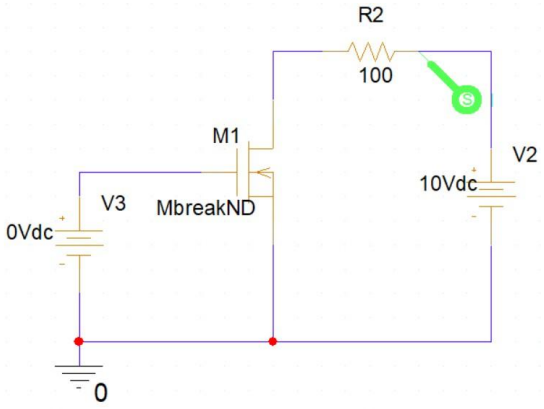


Figure 2.9: DFET verification in PSPICE

The device for a common DFET is MbreakND. After a dc sweep simulation when V3 varies from -5V to 0V, the results are shown bellow:

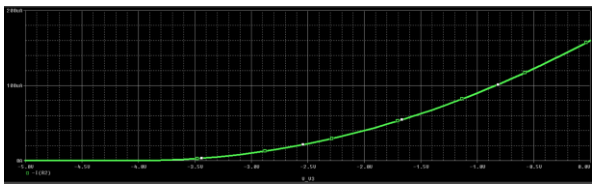


Figure 2.10: Simulation results with DFET

From this simulation results, it is confirmed that IDSS = 160mA and VP = -4V for DFET.

Students are proposed to implement the circuit bellow:

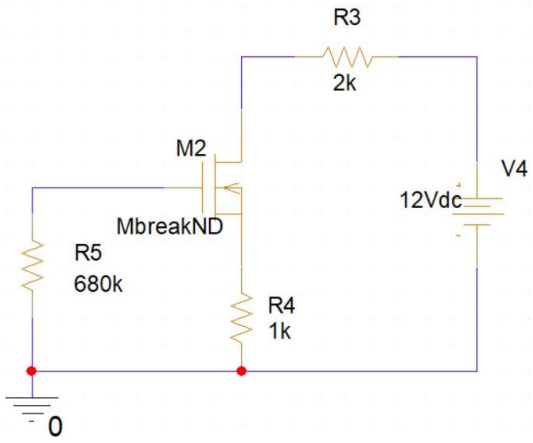
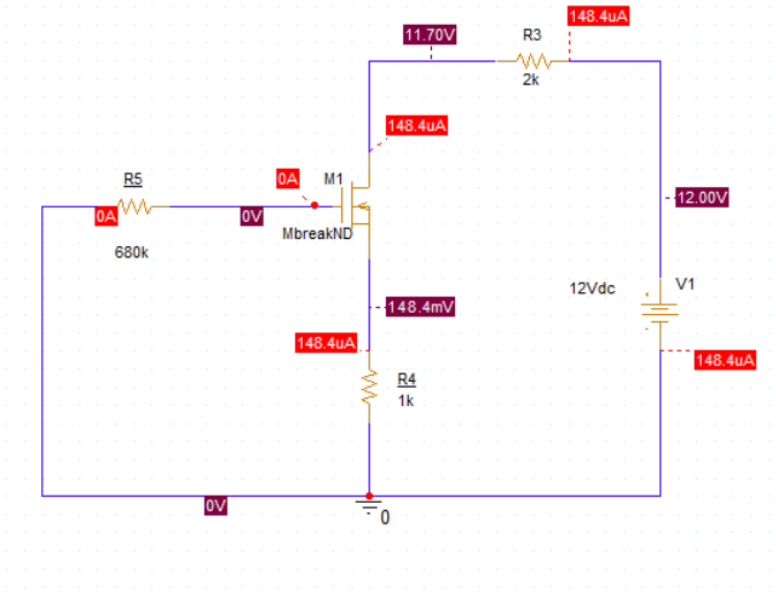


Figure 2.11: Self bias configuration for DFET

Only the bias configuration is required to executed. Please capture the simulation results with current and voltage information on the circuit. Finally, explain these values by theory calculations.



Bias simulation

Device Parameters (I_{DSS} and V_P)

According to the "DC Sweep simulation" section for the Depletion-mode MOSFET (Figure 2.10 in the lab manual):

- **Pinch-off Voltage (V_P)**: -4 V.
- **Saturation Current (I_{DSS})**: The manual text states **160 mA**, but the simulation graph in Figure 2.10 clearly shows the current in micro-amps (µA), peaking around **160 µA**.
  Given that our current simulation result is **148,4 µA**, it is physically consistent to assume the correct parameter is

$$I_{DSS} = 160\ \mu A.$$

Theoretical Verification

In a self-bias configuration for a Depletion MOSFET:

- The Gate current is zero ($I_G \approx 0$), so there is no voltage drop across $R_G = 680k\Omega$. Thus:

$$V_G = 0\ V$$

- The Source voltage is determined by the source resistor $R_S = 1k\Omega$:

$$V_S = I_D . R_S = 148{,}4\mu A . 1k\Omega = 0{,}1484V$$

- The Gate-to-Source voltage:

$$V_{GS} = V_G - V_S = -0{,}1484V$$

Applying Shockley's Equation:

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

Substituting the values ($I_{DSS} = 160\mu A$, $V_{GS} = -0{,}1484V$, $V_P = -4V$):

$$I_D = 160\mu A\left(1-\frac{-0{,}1484}{-4}\right)^2$$
$$= 160\mu A \times (1 - 0{,}0371)^2$$
$$= 160\mu A \times (0{,}9629)^2$$
$$= 160\mu A \times 0{,}9272 \approx 148{,}35\mu A$$

Conclusion:

The theoretical calculation (**148,35 µA**) matches the simulation result (**148,4 µA**) almost perfectly, confirming the circuit operation and the device parameters ($I_{DSS} = 160\mu A$, $V_P = -4V$).

3.2 Enhancement-mode MOSFET

The more common Enhancement-mode MOSFET or eMOSFET. The device is normally "OFF" (non-conducting) when the gate bias voltage, VGS is equal to zero. For the n- channel enhancement MOS transistor a drain current will only flow when a gate voltage (VGS) is applied to the gate terminal greater than the threshold voltage (VTH) level in which conductance takes place making it a transconductance device. In other words, for an n-channel enhancement mode MOSFET: +VGS turns the transistor "ON", while a zero or -VGS turns the transistor "OFF". Thus the enhancement-mode MOSFET is equivalent to a "normally-open" switch.

The reverse is true for the p-channel enhancement MOS transistor. When VGS = 0 the de- vice is "OFF" and the channel is open. The application of a negative (-ve) gate voltage to the p-type eMOSFET enhances the channels conductivity turning it "ON". Then for an p- channel enhancement mode MOSFET: +VGS turns the transistor "OFF", while -VGS turns the transistor "ON".

The validation of an EFET in PSPICE is presented bellow. The typical EFET in PSPICE is **MbreakN** device.

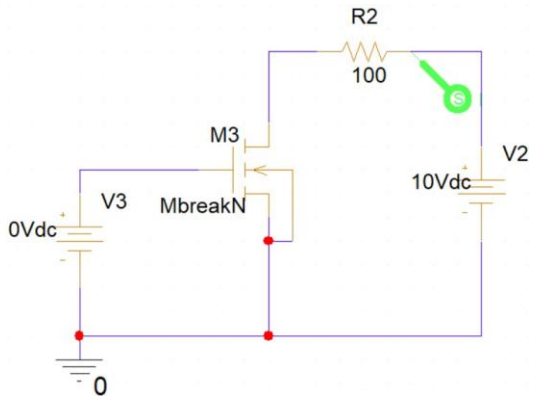


Figure 2.12: EFET validation

A dc sweep simulation with V3 can be performed. The simulation results with V3 varies from -1V to 5V are presented as following:

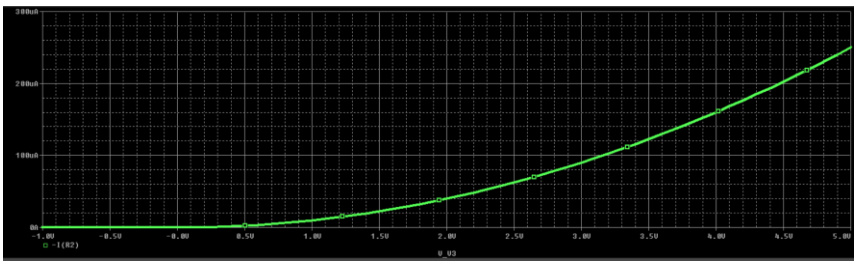


Figure 2.13: Simulation results with EFET

4. MOSFET Application

This part presents some applications using MOSFETs and most of them are EFETs. Stu- dents are proposed to implement the schematic and then, validate in PSPICE.

4.1 MOSFET as a switch

In this circuit arrangement an Enhancement-mode N-channel MOSFET is being used to switch a simple lamp "ON" and "OFF" (**could be replace by an resistor to simulate in PSPICE**).

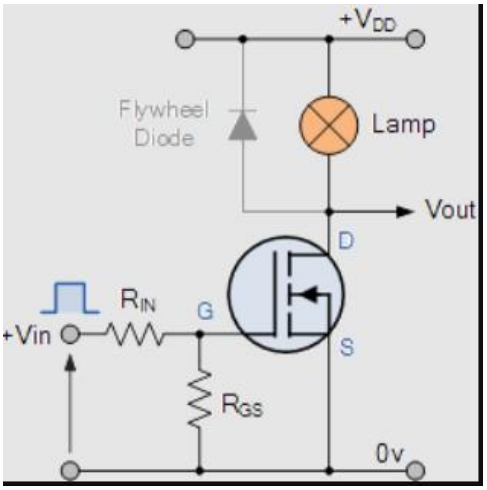
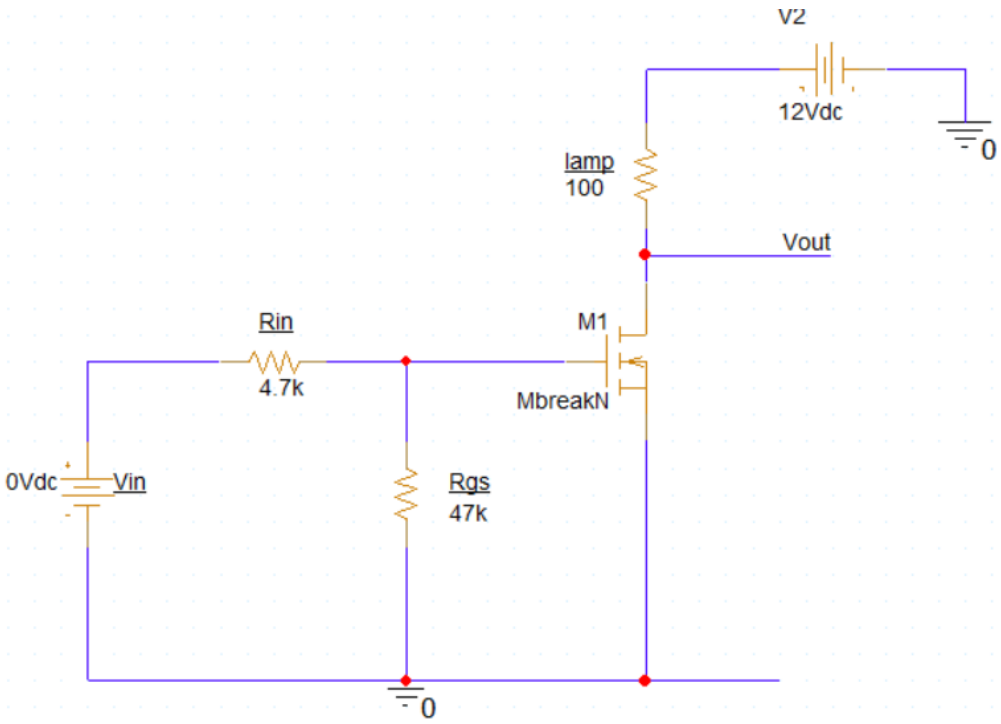


Figure 2.14: EFET is used as a switch

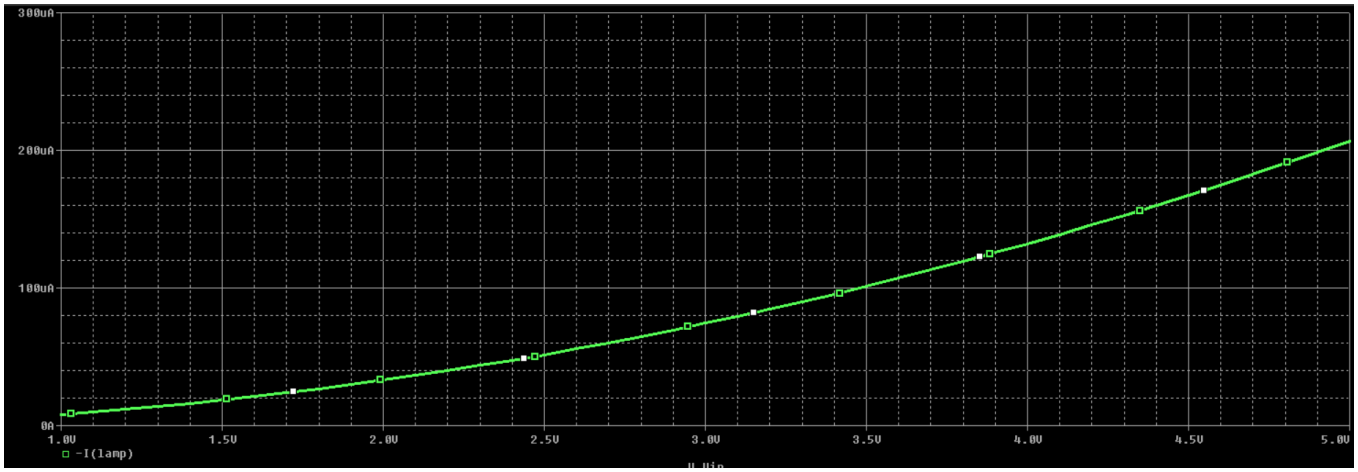
The gate input voltage VGS is taken to an appropriate positive voltage level to turn the device and therefore the lamp load either "ON", (VGS = +ve) or at a zero voltage level that turns the device "OFF", (VGS = 0V).

If the resistive load of the lamp was to be replaced by an inductive load such as **a coil, solenoid or relay** a "flywheel diode" would be required in parallel with the load to protect the MOSFET from any self generated back-emf.

Students are proposed to simulation this circuit with RIN = 4.7k and RGS = 47k and VIN is the TTL level (0V and 5V). The power supply for VDD can be set to 12V or 24V. Shortly explain the current passing through the load (a resistance 100Ohm replaced for the Lamp in the circuit). - Schematic in PSPICE:



- Simulation:



Current through the 100Ω load

When VIN = 5 V, the MOSFET gate reaches about 4.5 V, which is enough to turn the MOSFET ON.
In this state, the MOSFET behaves almost like a closed switch, so the load current is determined mainly by the supply voltage and the 100Ω resistor:

. If VDD = 12 V:

$$I \approx 0.12\ A = 120mA$$

. If VDD = 24 V:

$$I \approx 0.24\ A = 240mA$$

When VIN = 0 V, the gate voltage becomes 0 V, the MOSFET turns OFF, and only a tiny leakage current flows.
Therefore, the load current is essentially 0 A.

4.2 MOSFET Motor Controller [Optional]

Because the motor is an inductive load, a standard flyback diode is connected across it to safely discharge any back-EMF produced when the MOSFET switches the motor **OFF**. A clamping network—made from a diode in series with a zener diode—can also be added to improve switching speed and provide better control over peak reverse voltage and the drop-out time.

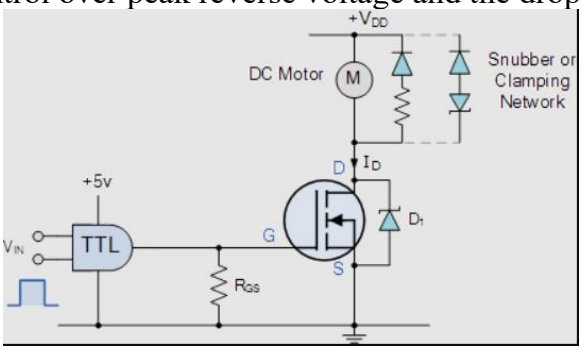


Figure 2.15: Simple motor controller using EFET

For extra protection, an additional silicon or zener diode (D1) may be placed across the MOSFET's channel when driving inductive devices such as motors, relays, or solenoids. This helps suppress voltage spikes and electrical noise, giving the MOSFET enhanced protection if needed. The resistor RGS acts as a pull-down resistor, ensuring the TTL control signal is pulled back to 0V when the MOSFET is turned **OFF**.

4.3 Complementary MOSFET Motor Controller [Optinal]

The two MOSFETs are arranged to form a bidirectional switch using a dual power supply, with the motor connected between the common drain node and ground. When the input signal is LOW, the P-channel MOSFET turns ON because its gate-to-source junction is negatively biased, causing the motor to rotate in one direction using only the positive +VDD supply.

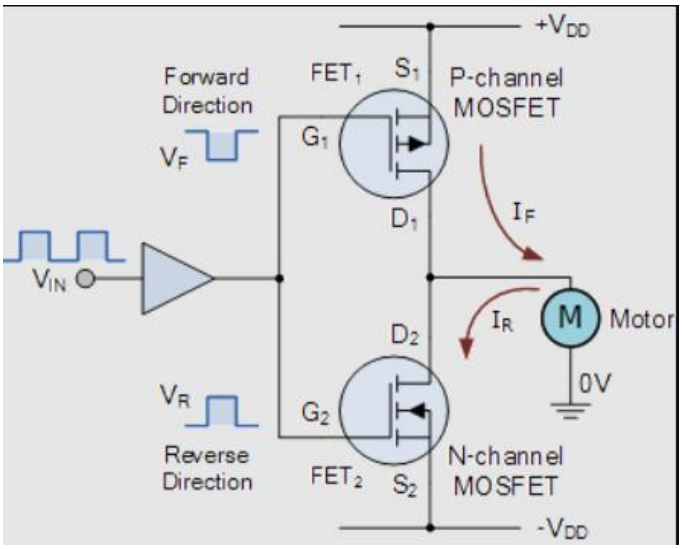


Figure 2.16: Full Motor controller with N and P channel EFET

When the input goes HIGH, the P-channel MOSFET turns OFF and the N-channel MOSFET turns ON due to its positively biased gate-to-source junction. The motor now spins in the opposite direction because the voltage across it is reversed and it is powered from the negative –VDD supply.
Thus, the P-channel MOSFET switches the positive supply to drive the motor forward (high-side switching), while the N-channel MOSFET switches the negative supply to drive the motor in reverse (low-side switching).

5. Altium Designer

5.1Button Input

Pushbuttons or switches connect two points in a circuit when you press them. In a system, button is a traditional input method. The figure bellow is an example of a simple button, which is the target of this exercise:

Figure 2.17: An example of a button

The schematic of this circuit is proposed as follows:

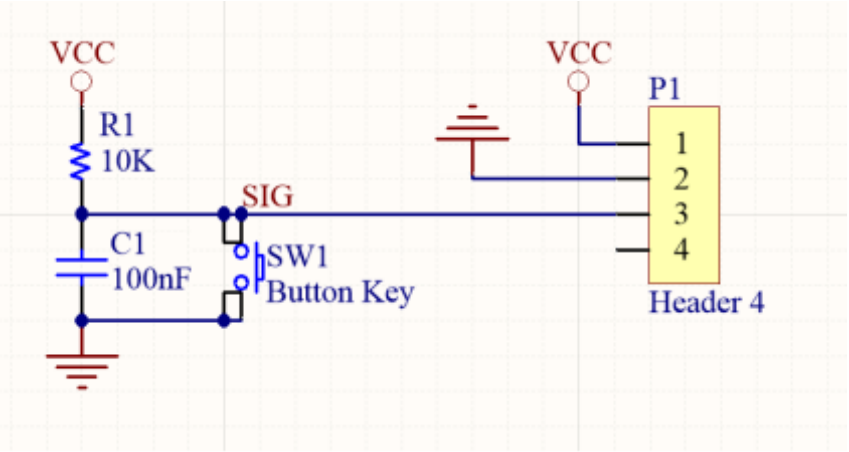
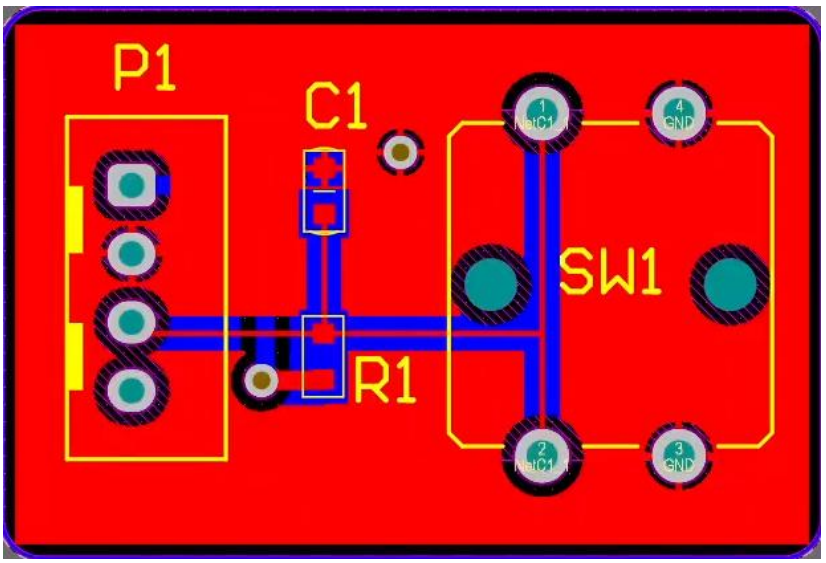


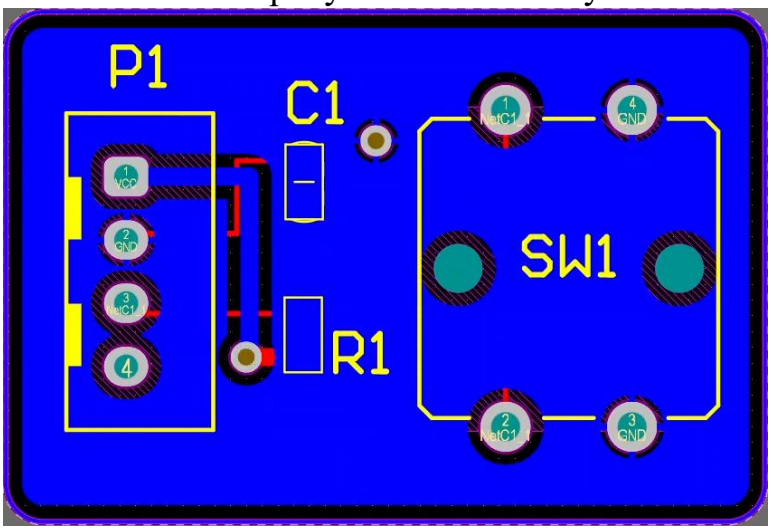
Figure 2.18: Button schematic in Altium

Students are proposed to implement the circuit in Altium Designer. The manual can be found in the same playlist with other manual videos. Please capture the screen to present the schematic as well as the layout of your PCB.

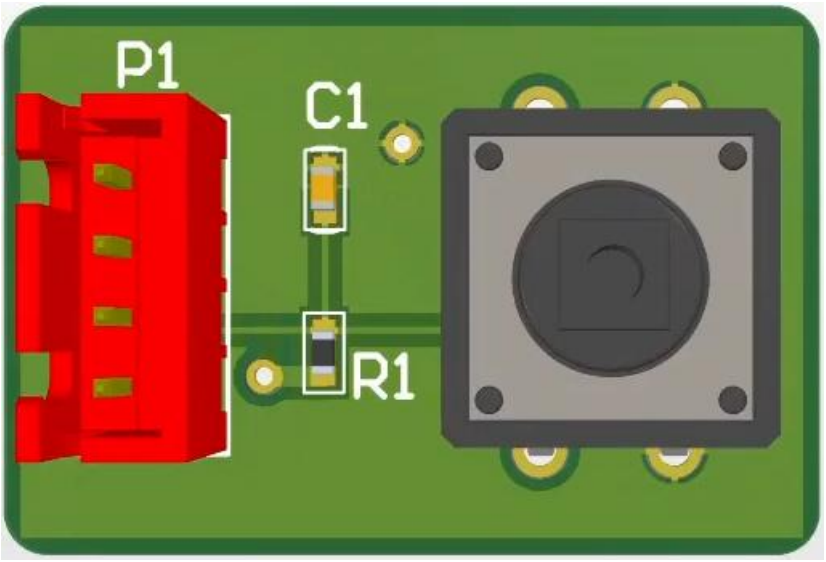
- PCB Layout:



The top layer of the PCB layout



The bottom layer of the PCB layout



5.2 ADC Input

The second type of the input signal is the ADC input value, which is a kind of sensing de- vice. In this sensor part, we use two opamps which are packed in one IC LM358. IC LM3 includes two opamps. A photoresistor (also known as a light-dependent resistor, LDR, or photo-conductive cell) is use to measure the light intensitive. It is a passive component that decreases resistance with respect to receiving luminosity (light) on the component's sensitive surface. An example of this module can be found in the figure bellow:

Figure 2.19: An example of a light sensor

The schematic of this circuit is proposed as follows, which is based on a voltage follower circuit:

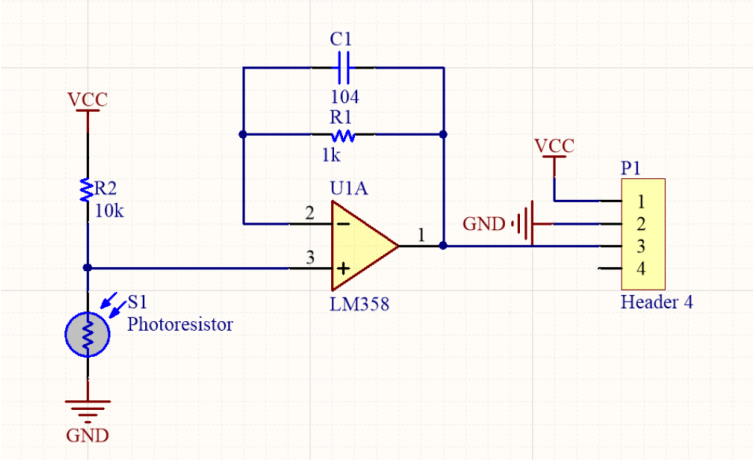
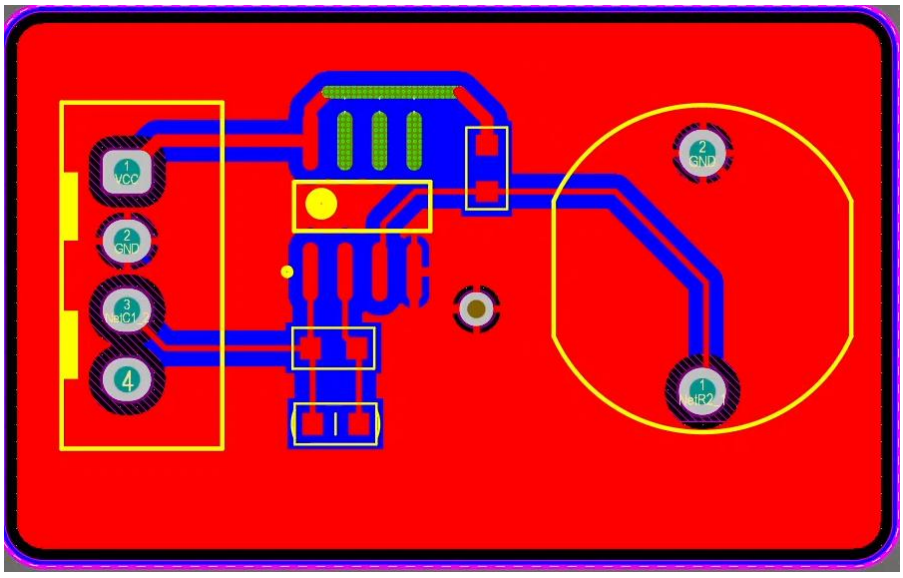


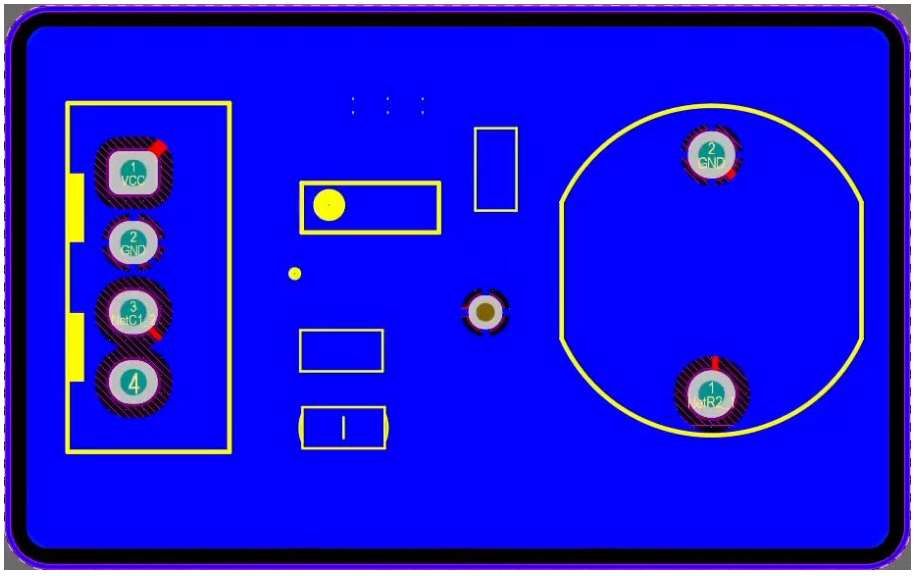
Figure 2.20: Light sensor schematic in Altium

Students are proposed to implement the circuit in Altium Designer. The manual can be found in the same playlist with other manual videos. Please capture the screen to present the schematic as well as the layout of your PCB.

- PCB Layout:



The top layer of the PCB layout



The bottom layer of the PCB layout