HO CHI MINH CITY UNIVERSITY OF TECHNOLOGY

OFFICE FOR INTERNATIONAL STUDY PROGRAM

SEMESTER: 251

LAB 5 REPORT

INSTRUCTOR:

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Class ID: CC04

Ho Chi Minh city, November 27, 2025

Workload and Team Contribution

No.	Name	Student ID	Workload	Contribution
1	Trần Lê Tuấn Anh	2452089	Report, 3.1 , 3.3	100%
2	Nguyễn Thành Trường An	2452020	3.2 , 3.4 , 3.6 , 4.1	100%
3	Ngô Đức Anh (nhóm trưởng)	2452054	3.5 , 3.7 , 4.2	100%

1. Introduction

Operational Amplifiers, also known as Op-amps, are basically a voltage amplifying device designed to be used with components like capacitors and resistors, between its in/out terminals. They are essentially a core part of analog devices. Feedback components like these are used to determine the operation of the amplifier. The amplifier can perform many different operations, giving it the name Operational Amplifier.

One key to the usefulness of these little circuits is in the engineering principle of feedback, particularly negative feedback, which constitutes the foundation of almost all automatic control processes. The principles presented in this section, extend well beyond the immediate scope of electronics. It is well worth the electronics student's time to learn these principles and learn them well.

Operational amplifiers can have either a closed-loop operation or an open-loop opera- tion. The operation (closed-loop or open-loop) is determined by whether or not feedback is used. Without feedback the operational amplifier has an open-loop operation. This open-loop operation is practical only when the operational amplifier is used as a coop- erator (a circuit which compares two input signals or compares an input signal to some fixed level of voltage). As an amplifier, the open-loop operation is not practical because the very high gain of the operational amplifier creates poor stability. (Noise and other unwanted signals are amplified so much in open-loop operation that the operational am- plifier is usually not used in this way.) Therefore, most operational amplifiers are used with feedback (closed-loop operation).

2. Closed Loop Operation

Operational amplifiers are used with degenerative (or negative) feedback which reduces the gain of the operational amplifier but greatly increases the stability of the circuit. In the closed-loop configuration, the output signal is applied back to one of the input terminals. This feedback is always degenerative (negative). In other words, the feedback signal al- ways opposes the effects of the original input signal. One result of degenerative feedback is that the inverting and non-inverting inputs to the operational amplifier will be kept at the same potential.

Closed-loop circuits can be of the inverting configuration or non-inverting configuration.

2.1 Non inverting configuration

The typical circuit for this configuration is shown in the figure bellow:

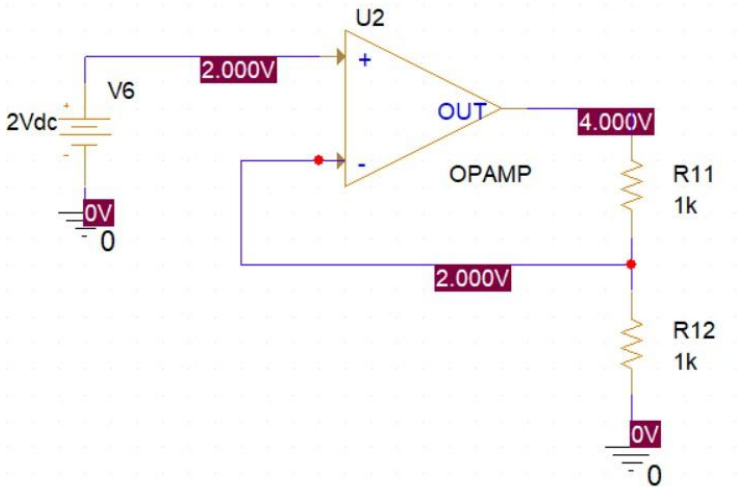


Figure 1.1: Non inverting configuration

The new component, named also OPAMP (Operational Amplifier) is easily found in the favorite list of the PSPICE.

In order to explain the 4V at the ouput, it is obviously that $V(+) = V(-) = 2V$ in a closed loop configuration. Therefore, from a resistor bridge at the output, $V_{OUT} = 4V$.

2.2 Inverting configuration

In this configuration, the output is connected directly to a pin of the opamp as follow:

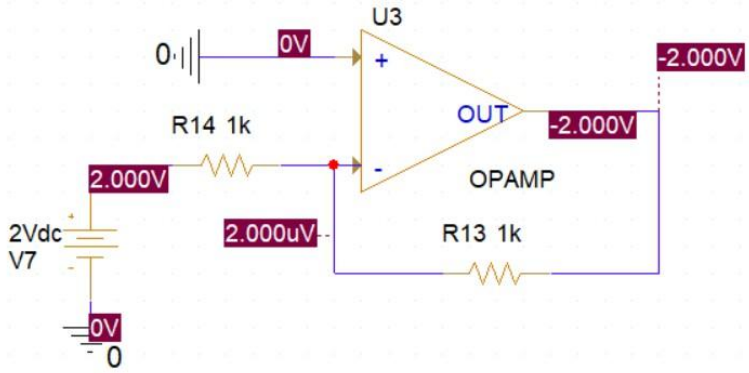


Figure 1.2: Inverting configuration

As the output voltage is negative, which is inverted to the input, the name of this circuit is the invert connection. Students are proposed to perform calculations to confirm the output, which is $-2V$.

3. Exercise and Report

3.1 Voltage Follower

Voltage follower is one of the simplest uses of an operational amplifier, where the output voltage is exactly same as the input voltage applied to the circuit. In other words, the gain of a voltage follower circuit is unity. The connections are proposed as follows:

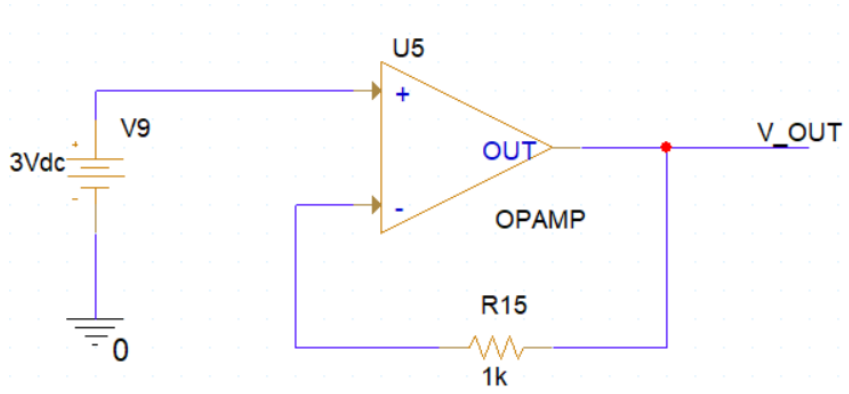
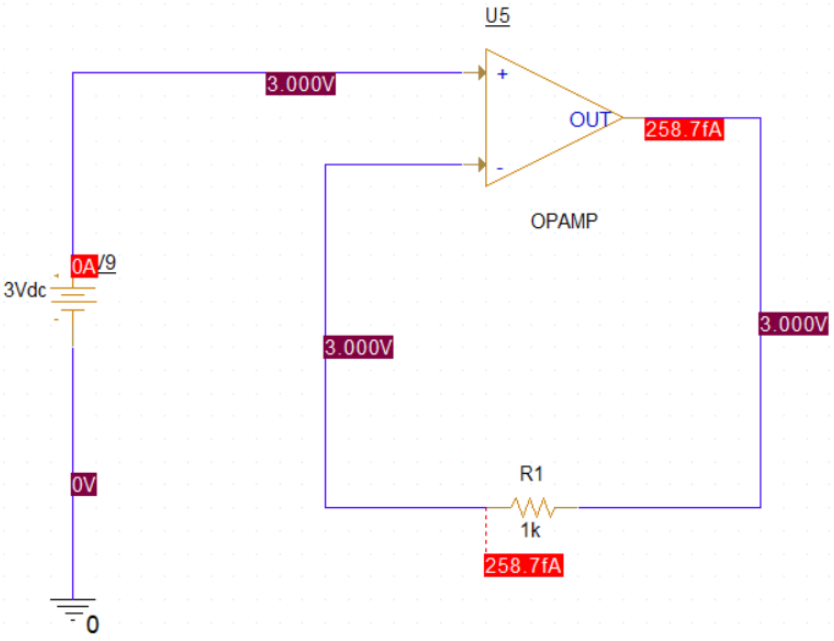


Figure 1.3: Opamp follower circuit

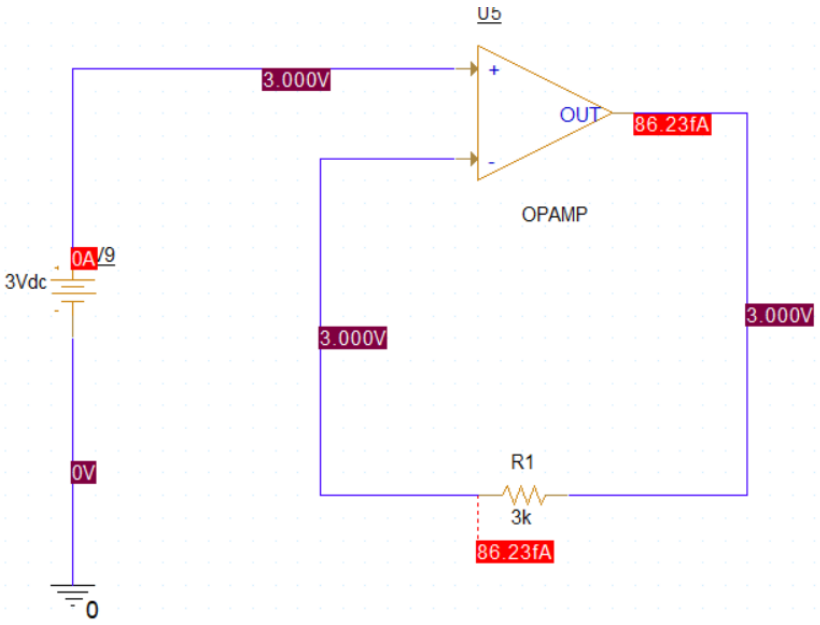
A voltage follower has low output impedance and extremely high input impedance, and this makes it a simple and effective solution to problematic impedance relationships. If a high-output-impedance sub-circuit must transfer a signal to a low-input-impedance sub-circuit, a voltage follower placed between these two sub-circuits will ensure that the full voltage is delivered to the load.

Students are propose to run the simulation with bias mode to confirm that $V_{OUT} = V(+)$. The feedback resistance is also required to change.

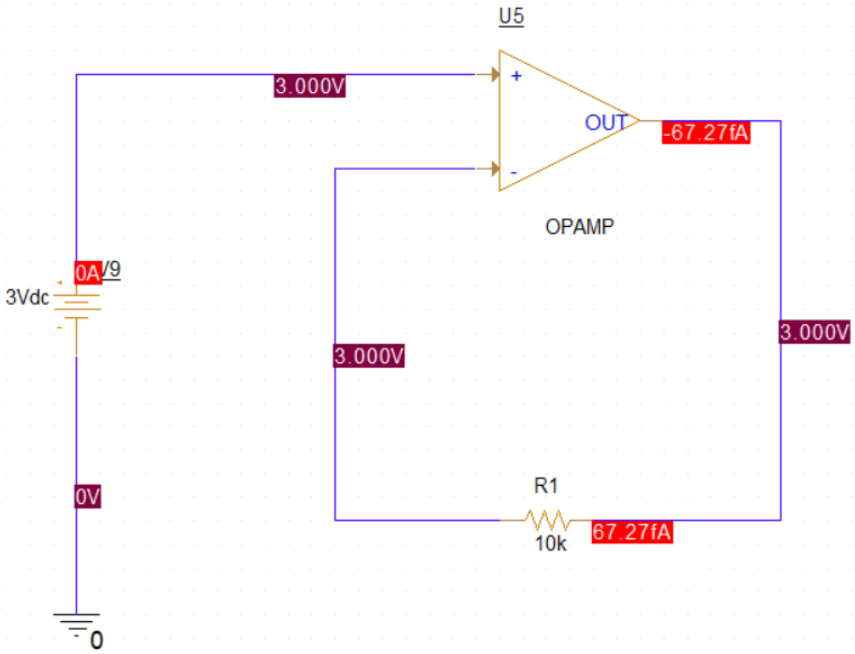
Your calculations are presented here to prove $V_{OUT} = V(+)$ with any value of R15.



The bias point simulation when feedback resistance is 1k Ω



The bias point simulation when feedback resistance is 3k Ω



The bias point simulation when feedback resistance is 10k Ω

Step-by-Step Explaination:

1. **Analyze the current through R_{15}:** In the Voltage Follower circuit, the resistor R_{15} connects the Output pin directly to the Inverting Input pin (-). Since the input impedance of the op-amp is extremely high, the current entering the inverting terminal is zero ($I_{-} = 0$). Therefore, the current flowing through the feedback resistor R15 is also zero: $I_{-R15} = I_{-} = 0$
2. **Apply Ohm's Law to R_{15}:** The voltage drop across the resistor R_{15} is calculated as: $V_{drop} = I_{-R15} \times R_{15}$ Substituting the current from Step 1: $V_{drop} = 0\ A \cdot R_{15} = 0\ V$
3. **Determine the Output Voltage:** Since the voltage drop across R_{15} is 0V, the electric potential at the Output pin (V_{OUT}) is exactly the same as the potential at the Inverting Input pin (V_{-}): $V_{OUT} = V_{-}$
4. **Apply the Virtual Short Rule:** Due to the negative feedback mechanism, the op-amp ensures that: $V_{-} = V_{+}$
5. **Final Conclusion:** Combining the results from Step 3 and Step 4: V.OUT = V_minus = V_{+} Therefore: $V_{OUT} = V_{+}$

3.2 High-Current Voltage Follower

The voltage follower's low output impedance makes it a good circuit for driving current into a low-impedance load, but it's important to remember that most op-amps are not designed to deliver large output currents. The most basic circuit for buffering an op-amp's output current is the following:

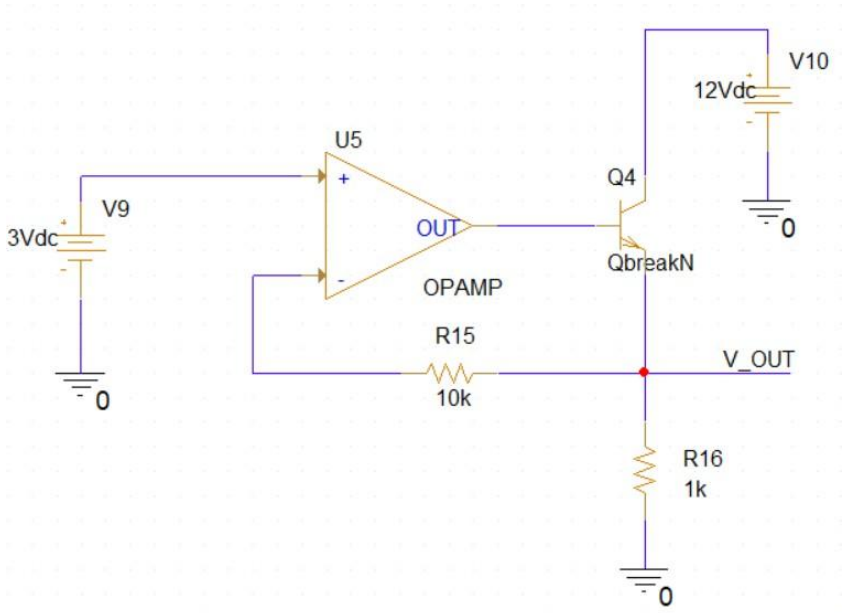
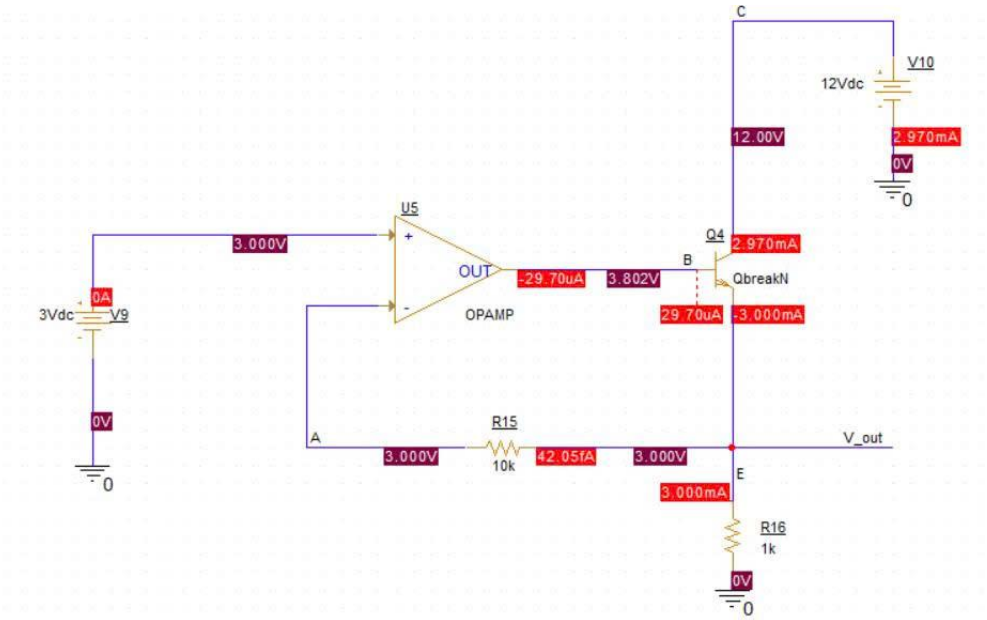


Figure 1.4: Opamp follower circuit

The voltage at the positive pin of the Opamp is copied to V_{OUT} . In this schematic, R16 is used to simulate a load device, which can be a motor or an high power LED. However, in this case, there is a high current can pass the load.

Students are proposed to run the simulation with bias configuration, capture the results and place them in the report.

Finally, your computations go here to explain the results.



The bias point simulation

Assumption: $V_E = 3\,V$, $R_{16} = 1000\,\Omega$ and transistor DC current gain $\beta = 100$(so $\alpha = \frac{\beta}{\beta+1}$)

– **Node voltages:**

$$V_{(+)} = V_{(-)} = V_E = 3\,V$$

– **Emitter current I_E:**

$$I_E = \frac{V_E - 0}{R_{46}} = \frac{3-0}{1000} = 0{,}003A = 3\,mA$$

– **Collector current I_C using $\alpha = \frac{\beta}{\beta+1} = \frac{100}{101}$:**

$$I_C = \alpha I_E = \frac{100}{101}.3\,mA = 2{,}97\,mA$$

– **Base current I_B:**

$$I_B = I_E - I_C = 3\,mA - 2{,}97\,mA = 0{,}03\,mA = 30\,\mu A$$

– **Op-amp output (base) voltage:**

$$V_B = V_E + V_{BE} \approx 3 + 0{,}7 = 3{,}7\,V$$

3.3 Voltage Follower with Gain

This basic circuit is not limited to the unity-gain configuration. As with a non-buffered op-amp, you can insert resistors into the feedback path to create overall gain from the input to the load voltage. Here is the non-unity-gain version of the circuit:
Students are proposed to implement this circuit on PSPICE with input is 2V and the gain is 3. The voltage supply for the load side is 12VDC. Value of R_{LOAD} is 1K.

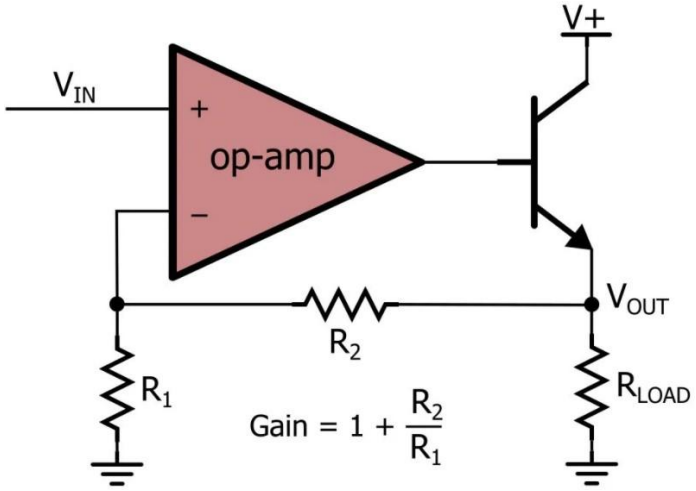
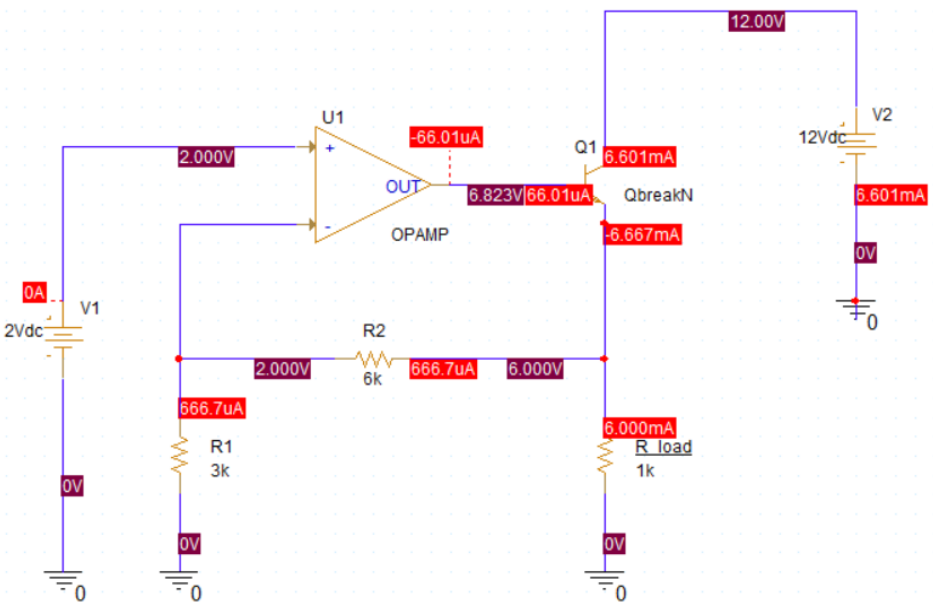
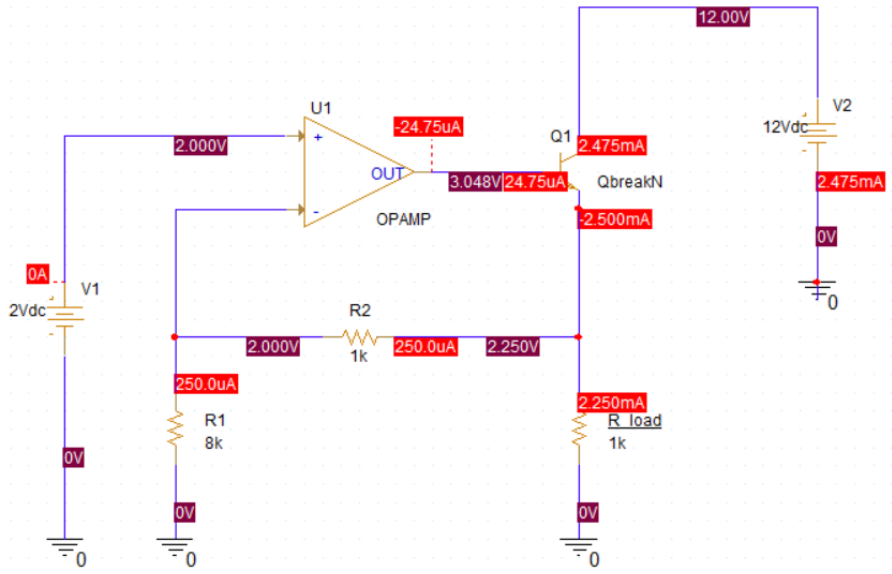


Figure 1.5: Opamp follower with gain for the output

The simulation results in PSPICE (bias configuration) are presented here. Moreover, a short explanations are required in this report to explain the gain of the output follower voltage.

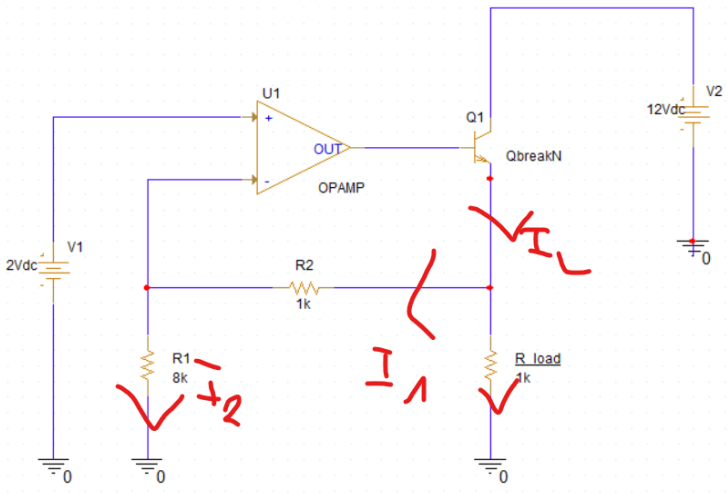


The bias point simulation when R_1 = 3(kΩ) and R_2 = 6(kΩ)



The bias point simulation when R_1 = 8(kΩ) and R_2 = 1(kΩ)

Explaination:



Assumptions for an Ideal Op-Amp:
The current flowing into the input terminals is negligible ($I_+ = I_- \approx 0$).
The voltage at the inverting input tracks the non-inverting input ($V_- = V_+ = V_{in} = 2V$).
Nodal Analysis at the Inverting Input:
Since no current enters the Op-Amp, the current flowing through the feedback resistor (R_2) must equal the current flowing through the ground resistor (R_1).

$$i_{feedback} = i_{ground}$$
$$\Leftrightarrow \quad \frac{V_{out} - V_{in}}{R_2} = \frac{V_{in} - 0}{R_1}$$

Rearranging the equation to solve for V_{out}:

$$V_{out} = V_{in} \cdot (1 + \frac{R_2}{R_1})$$

Result:
With a required gain of 3 and an input of 2V:

$$V_{out} = 2V \cdot 3 = 6V$$

3.4 Summing Amplifier

Students are proposed to implement following schematic in PSPICE and run the simula- tion with R1 = 1K, R2 = 2K, R3 = 5K, Rf = 9K, Ri = 1K. There inputs are V1 = 1V, V2 = 2V and V3 = 3V. This circuit is a non inverting summing configuration using opamp.

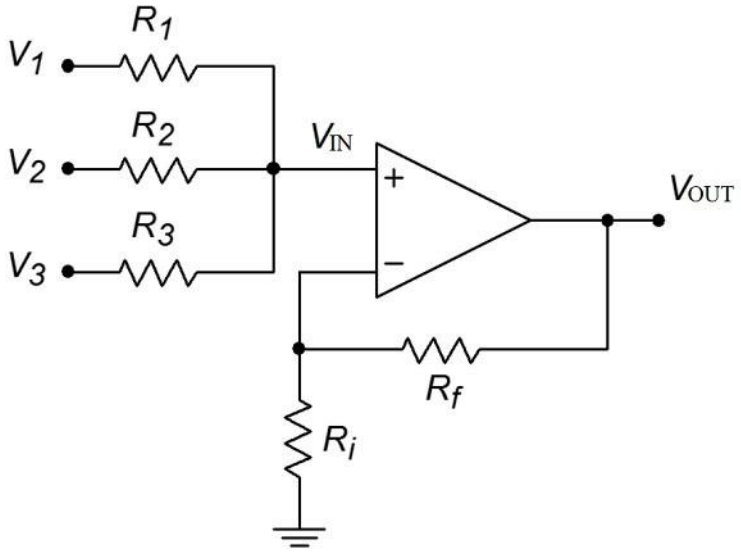
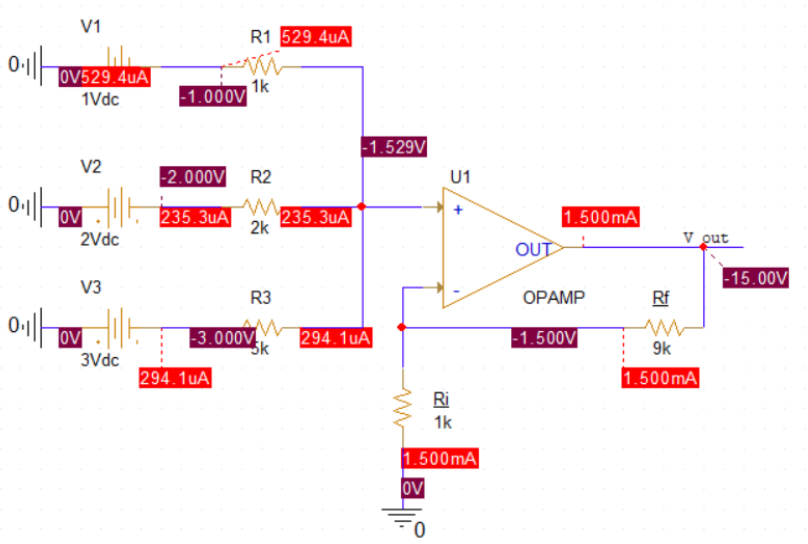


Figure 1.6: Non inverse summing using OPAMP

Students are proposed to design the schematic and place the results in this report.

Your image goes here



Your calculations go here to explain the value of V_{OUT}

Nodal Analysis at Non-Inverting Input V_+:

Using Kirchhoff's Current Law (KCL) at the non-inverting node, where the sum of currents entering the node is zero:

$$\frac{V_1 - V_+}{R_1} + \frac{V_2 - V_+}{R_2} + \frac{V_3 - V_+}{R_3} = 0$$

Substituting the given values ($V_1 = 1V,\ V_2 = 2V,\ V_3 = 3V\ and\ R_1 = 1k, R_2 = 2k, R_3 = 5k$):

$$\frac{1 - V_+}{1000} + \frac{2 - V_+}{2000} + \frac{3 - V_+}{5000} = 0$$

Solving for V_+:

$$10(1 - V_+) + 5(2 - V_+) + 2(3 - V_+) = 0$$

$$26 - 17V_+ = 0 \Rightarrow V_+ = \frac{26}{17} \approx 1.529V$$

The circuit operates as a non-inverting amplifier with respect to the combined input voltage V_+.The gain is determined by the feedback resistor ($R_f = 9k$)and the ground resistor ($R_i = 1k$).

$$V_{out} = \left(1 + \frac{R_f}{R_i}\right) \cdot V_+$$

$$V_{out} = \left(1 + \frac{9000}{1000}\right) \cdot 1.529$$

$$V_{out} = 10 \cdot 1.529 = 15.29V$$

System of Equations Setup

Let I_1, I_2, I_3denote the currents flowing from Node A (Non-inverting input) towards the sources V_1, V_2, V_3respectively. We establish the following system of equations based on Ohm's Law and Kirchhoff's Current Law (KCL) at Node A:

$$\begin{cases} V_A - V_1 = 1000I_1 \\ V_A - V_2 = 2000I_2 \\ V_A - V_3 = 5000I_3 \\ I_1 + I_2 + I_3 = 0 (\text{Since } I_{OpAmp} \approx 0) \end{cases}$$

Substituting the known voltage values ($V_1 = 1V, V_2 = 2V, V_3 = 3V$):

$$\begin{cases} V_A - 1 = 1000I_1 \Rightarrow I_1 = \dfrac{V_A - 1}{1000} \\ V_A - 2 = 2000I_2 \Rightarrow I_2 = \dfrac{V_A - 2}{2000} \\ V_A - 3 = 5000I_3 \Rightarrow I_3 = \dfrac{V_A - 3}{5000} \end{cases}$$

Solving for Node Voltage (V_A)

Substitute the current expressions into the KCL equation ($I_1 + I_2 + I_3 = 0$):

$$\frac{V_A - 1}{1000} + \frac{V_A - 2}{2000} + \frac{V_A - 3}{5000} = 0$$

Multiplying the entire equation by 10,000 to clear denominators:

$$10(V_A - 1) + 5(V_A - 2) + 2(V_A - 3) = 0$$
$$10V_A - 10 + 5V_A - 10 + 2V_A - 6 = 0$$
$$17V_A = 26$$
$$\Rightarrow V_A \approx 1.529 \text{ V}$$

Calculating Currents (Optional Verification)

$$I_1 = (1.529 - 1)/1000 = 529 \text{ µA}$$
$$I_2 = (1.529 - 2)/2000 = -235.5 \text{ µA}$$
$$I_3 = (1.529 - 3)/5000 = -294.2 \text{ µA}$$

(Note: The negative signs indicate currents $I_2$and I_3actually flow towards Node A.)

Final Output Calculation (V_{OUT})

Because of the Op-Amp's negative feedback property, the voltage at the inverting input (V_B) equals the non-inverting input (V_A):

$$V_B = V_A = 1.529 \text{ V}$$

The current Iflowing through the ground resistor ($R_i = 1\text{k}\Omega$) is:

$$I = \frac{V_B - 0}{R_i} = \frac{1.529}{1000} = 1.529 \text{ mA}$$

The output voltage is the sum of the voltage at B and the voltage drop across the feedback resistor ($R_f = 9\text{k}\Omega$):

$$V_{OUT} = V_B + I \times R_f$$
$$V_{OUT} = 1.529 + (1.529 \times 10^{-3} \times 9000)$$
$$V_{OUT} = 1.529 + 13.761 = 15.29 \text{ V}$$

Conclusion:

This calculated value matches the simulation result perfectly.

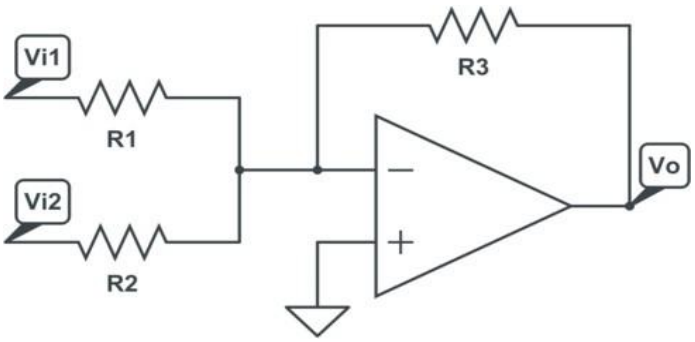
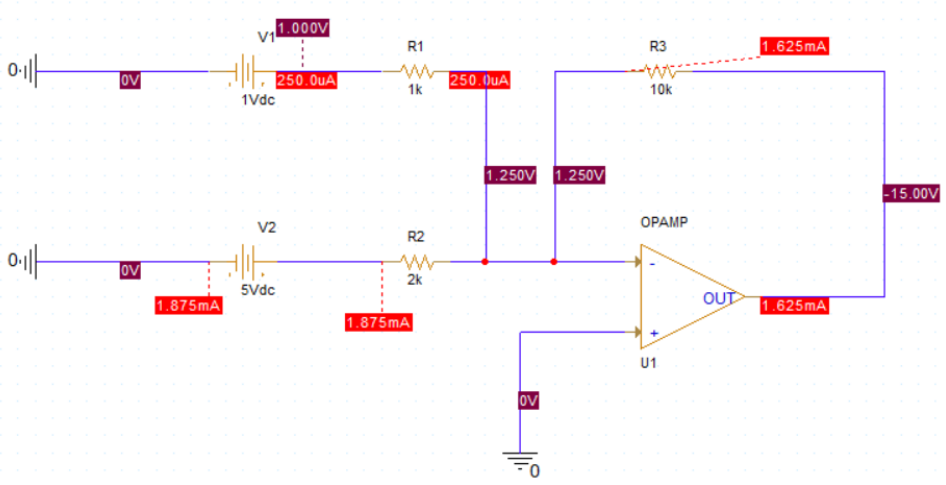


Figure 1.7: Inverse summing using OPAMP

The second type of the summing amplifier is proposed as follows:

Students are proposed to do the same steps above, with R1 = 1K, R2 = 2K, R3 = 10K and V1 = 1V, V2 = 5V.



Theoretical Calculation

Using Kirchhoff's Current Law at the inverting node (Virtual Ground, $V_A = V_B \approx 0V$):

The total current I flowing from the inputs is:

$$I = I_1 + I_2 = \frac{V_1 - V_A}{R_1} + \frac{V_2 - V_A}{R_2}$$

$$I = \frac{1 - 0}{1000} + \frac{5 - 0}{2000} = 1mA + 2.5mA = 3.5mA$$

The output voltage is determined by the feedback resistor $R_3 = 10k\Omega$:

$$V_{OUT} = V_B - (I \times R_3)$$

$$V_{OUT} = 0 - (3.5 \times 10^{-3} \times 10000) = -35V$$

Comparison with Simulation Results

The calculated theoretical value is -35V. However, the simulation result shows a much smaller magnitude (approx. -11V to -12V).

Explanation: This discrepancy occurs because the Op-Amp is in Saturation.

In a realistic scenario (and in simulation), the output voltage of an Op-Amp is limited by its power supply rails (typically $\pm 12V$ in this lab). Since the theoretical required output (-35V) exceeds the negative supply rail, the Op-Amp output is clipped near the negative supply voltage. Consequently, the negative feedback loop is broken, and the virtual ground condition $V_A \approx 0V$ is no longer maintained.

3.5 Low Pass Filter

Low pass filter is a filter which passes all frequencies from 0Hz (DC current) to upper cut-off frequency f_H and rejects any signals above this frequency. A picture to demonstrate a low pass filter behavior is shown in the figure bellow:

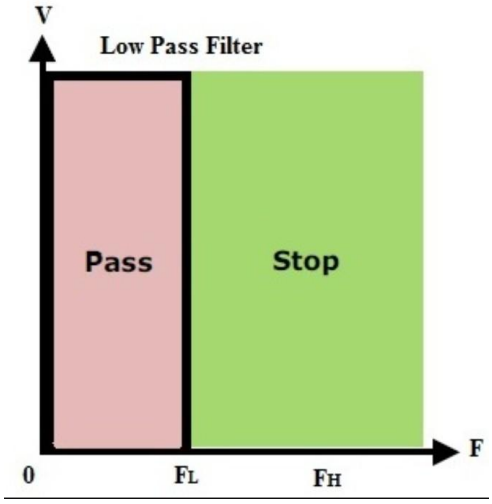


Figure 1.8: Low pass filter principles

Similar to the closed loop configuration, there also 2 types of low pass filter, including the inverting and non-inverting low pass filter. The figure bellow is an inverting low pass filter. The cut-off frequency is determined by this equation:

$$f_H = \frac{1}{2\pi R_2 C}$$

By applying the value of $R2 = 10KOhm$ and $C = 1nF$, the cut-off frequency is around $16K$ Hz. In order to see the results, students are proposed to run the AC Sweep simula- tion profile (**Linear Type, Start and Stop frequency are 1Hz and 50kHz, 200 points**), as follows:

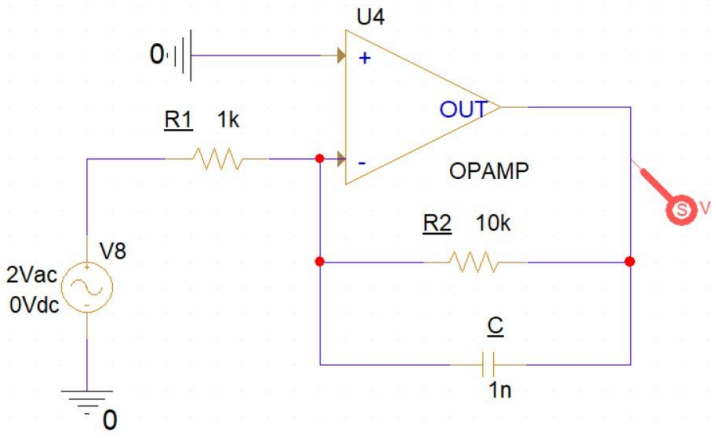


Figure 1.9: Inverting low pass filter

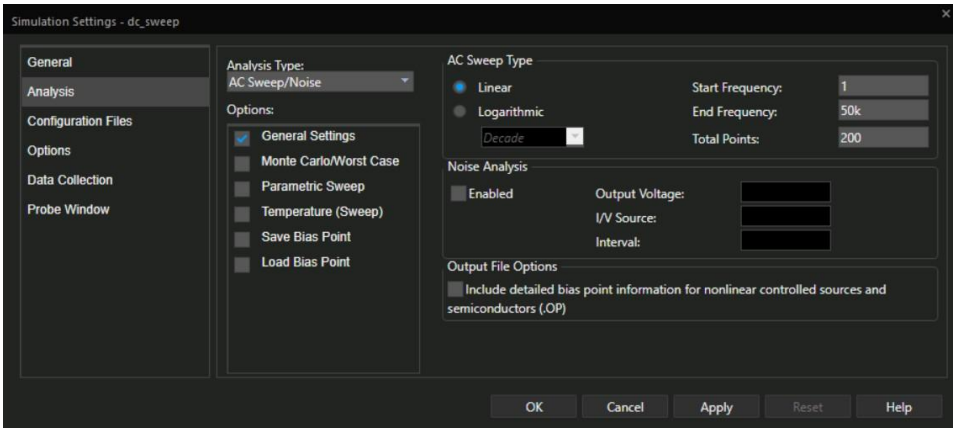


Figure 1.10: AC Sweep simulation profile

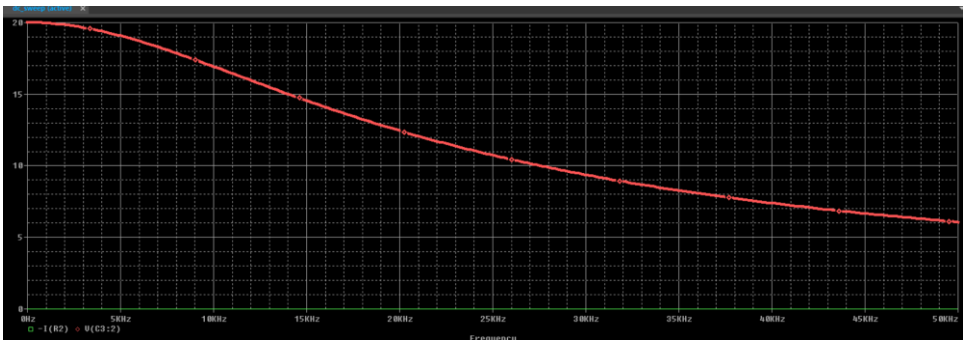


Figure 1.11: Simulation results

The final results can be archived like the figure bellow:
It is said that the cut-off frequency point having the gain reduced 3dB. The gain at 0Hz is 10 (input voltage is 2V and output voltage is 20V), or $20log\,(10) = 20dB$, meanwhile, the gain at 16kHz is 7 (input voltage is 2V and output voltage is 14V), or $20log\,(7) = 16.9$.

The second type of a low pass filter, the non-inverting configuration, is presented as follows:

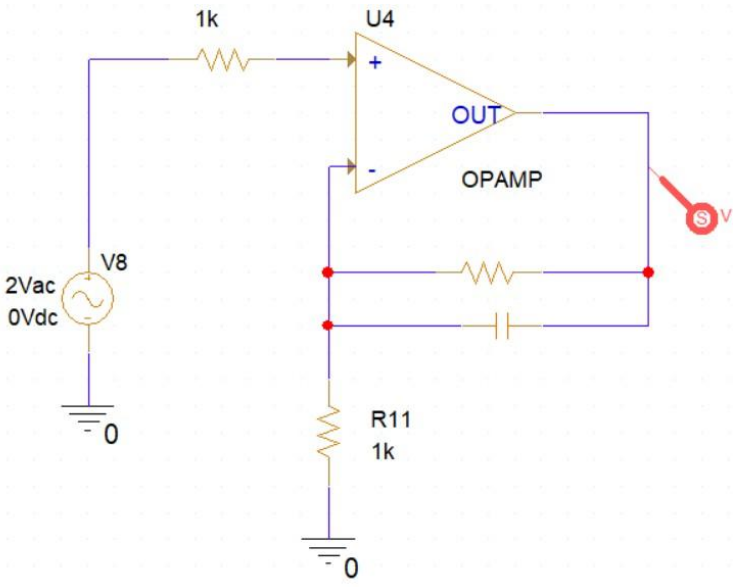


Figure 1.12: Non-inverting low pass filter

Students are proposed to calculate the value of R and C to have the amplifier factor equal to 10 and the cut-off frequency is the same as the previous example. The simulation result with AC Sweep mode is required to plot in this report as well.

Gain design (non-inverting amplifier)
For a non-inverting op-amp

$$A_v = 1 + \frac{R_f}{R_g}$$

Require $A_v = 10$. Choose $R_g = 1k\Omega$(convenient value).

$$10 = 1 + \frac{R_f}{1k\Omega} \Rightarrow R_f = 9k\Omega$$

Cut-off frequency:
The capacitor $C$is placed in parallel with the feedback resistor R_f. The feedback network seen by $C$is the parallel of $R_f$and R_g.

$$R_{eq} = \frac{R_f.R_g}{R_f + R_g} = \frac{9k.1k}{9k + 1k} = 900\Omega$$

The corner frequency (–3dB point) for this single-pole active low-pass is

$$f_c = \frac{1}{2\pi R_{eq} C}$$

Solve for Cgiven $f_c = 16kHz$

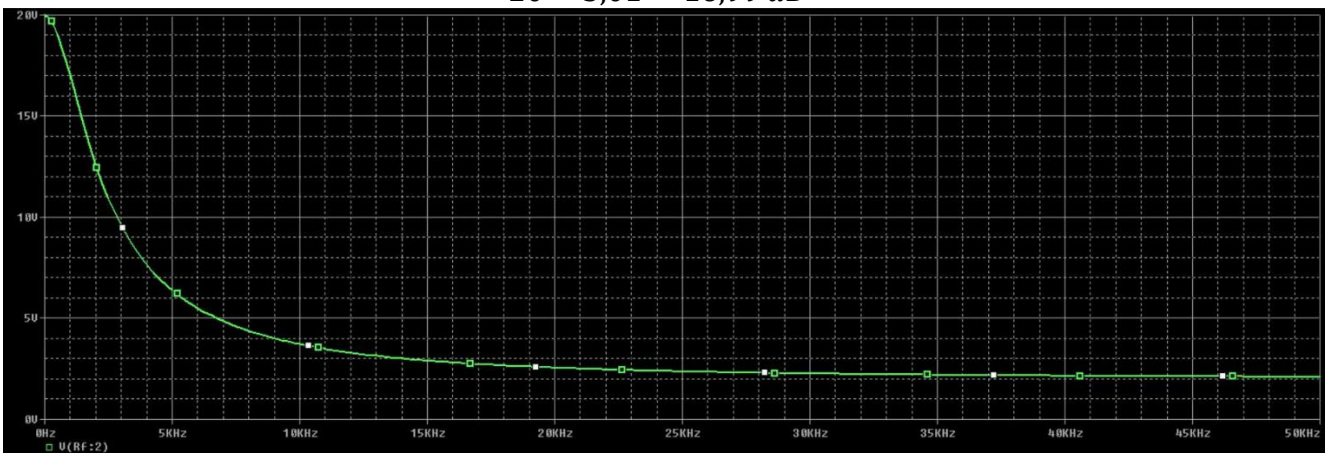
$C=\frac{1}{2\pi fcReq1}=2\pi.16000.9001\approx 11{,}05nF$

dB and gain remarks:

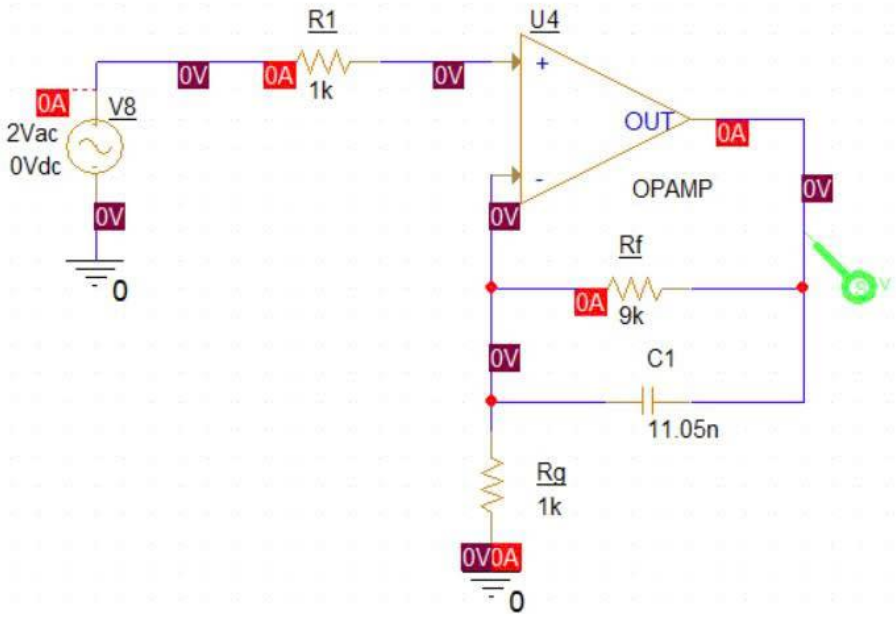
– Low-frequency gain magnitude = 10 → $20\log_{10}(10) = 20\ dB$

– At the cut-off the magnitude is $\frac{1}{\sqrt{2}}$ of the low-frequency gain, so in dB it is

$$20 - 3{,}01 \approx 16{,}99\ dB$$



The AC Sweep result

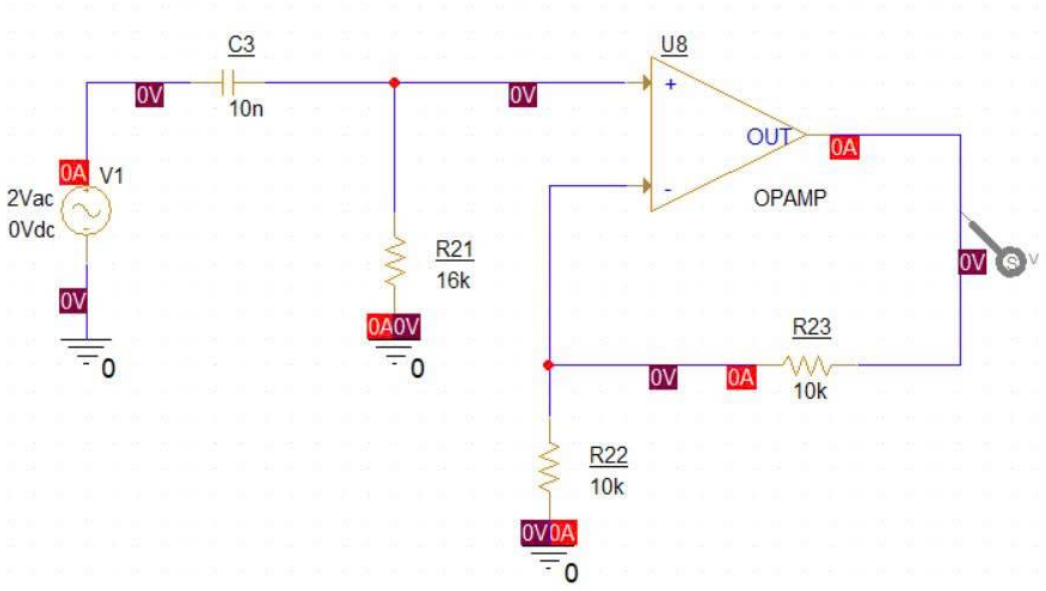


The Bias Circuit Result

3.6 High Pass Filter

In contrast to the low pass filter, there is a high pass filter, which can be referred from this link: https://www.allaboutcircuits.com/video-tutorials/op-amps-low-pass-and-high-pass-active-filters/

Students are proposed to implement a high pass filter in PSPICE and explain the behaviors of your high pass filter.



Active high pass filter with amplification.

Cut-off frequency.
The cut-off frequency of a high-pass RC filter is given by:

$$f_c = \frac{1}{2\pi RC}$$

Rearranging to find R:

$$R = \frac{1}{2\pi C f_c}$$

Substituting values:

$$R = \frac{1}{2\pi . 10^{-10} . 1000} \approx 15{,}92\ k\Omega$$

Or $R \approx 16\ k\Omega$
Amplifier Gain.
The pass-band gain is:

$$A_s = 2$$

For a non-inverting op-amp:

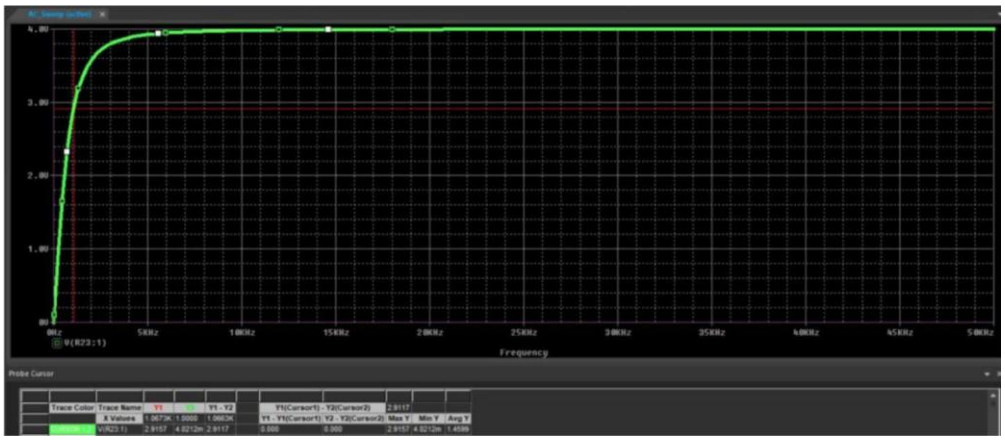
$$A_s = 1 + \frac{R_{23}}{R_{22}}$$

Setting $A_s = 2$:

$$2 = 1 + \frac{R_{23}}{R_{22}} \Rightarrow R_{22} = R_{23}$$

Therefore,
We can both choose
$R_{22} = R_{23} = 10\ k\Omega$
The AC sweep results shows that:

- Low–frequency signals are heavily attenuated
- The output amplitude rises around 1 kHz
- The gain stabilizes at about 2x in the high–frequency region



The AC sweep result

3.7 Comparator with Hysteresis (Schmitt Trigger)

The two resistors R1 and R2 act only as a "pure" attenuator (voltage divider). The input loop acts as a simple series voltage summer that adds a part of the output voltage in series to the circuit input voltage. This series positive feedback creates the needed hysteresis that is controlled by the proportion between the resistances of R1 and the whole resis- tance (R1 and R2). The effective voltage applied to the op-amp input is floating so the op-amp must have a differential input.

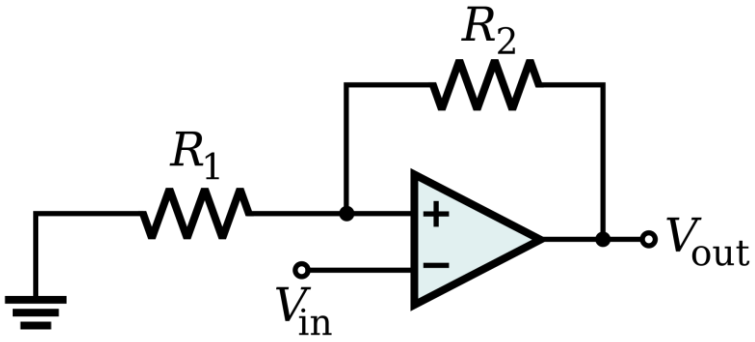


Figure 1.13: Inverting Schmitt trigger op-amp must have a differential input.

The circuit is named inverting since the output voltage always has an opposite sign to the input voltage when it is out of the hysteresis cycle (when the input voltage is above the high threshold or below the low threshold). However, if the input voltage is within the hysteresis cycle (between the high and low thresholds), the circuit can be inverting as well as non-inverting. The output voltage is undefined and it depends on the last state so the circuit behaves like an elementary latch.

In PSPice, this trigger is implemented as follows, with 3 voltage markers:

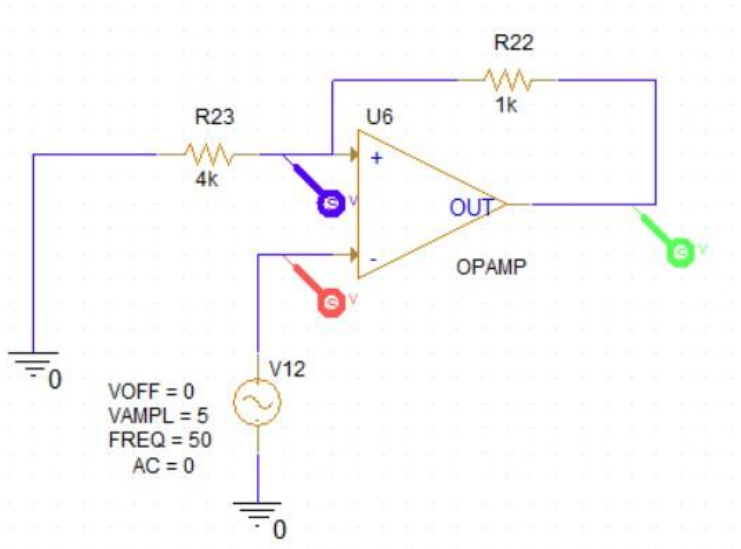


Figure 1.14: Schmitt trigger in PSPICE

The OPAMP device is modified in the **Properties** windows (right click on the component and chose Edit Properties or double click on the component), in order to set the VPOS and VNEG to +5V and -5V, as follows:
The simulation profile in this exercise is the **Time Domain**, and is configured as follows: Finally, the simulation results can be archived as follows:
Students are proposed to explain the signal at the output of the opamp. Why the signal is toggled at +4V and -4V.

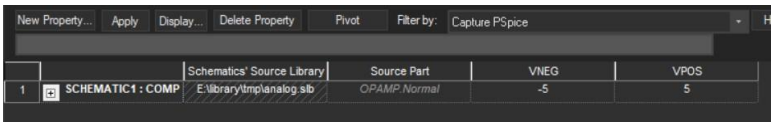


Figure 1.15: Schmitt trigger in PSPICE

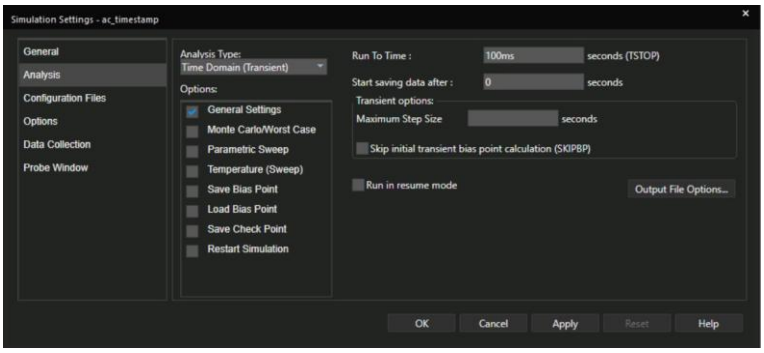


Figure 1.16: Simulation profile

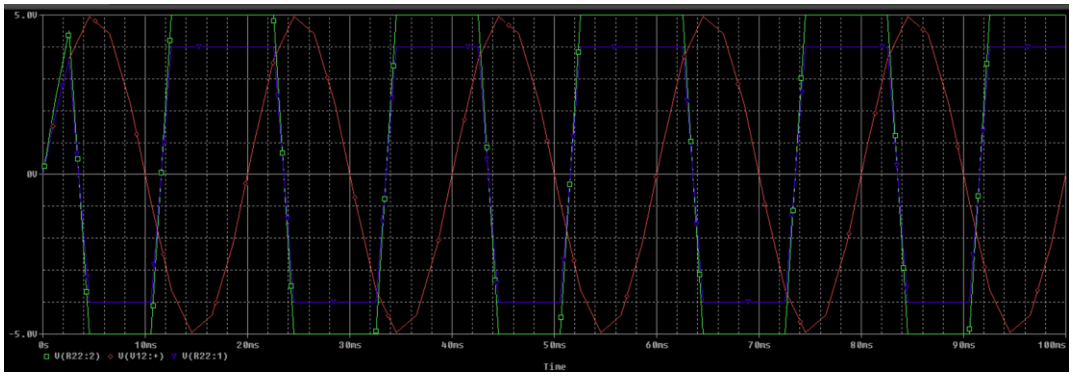
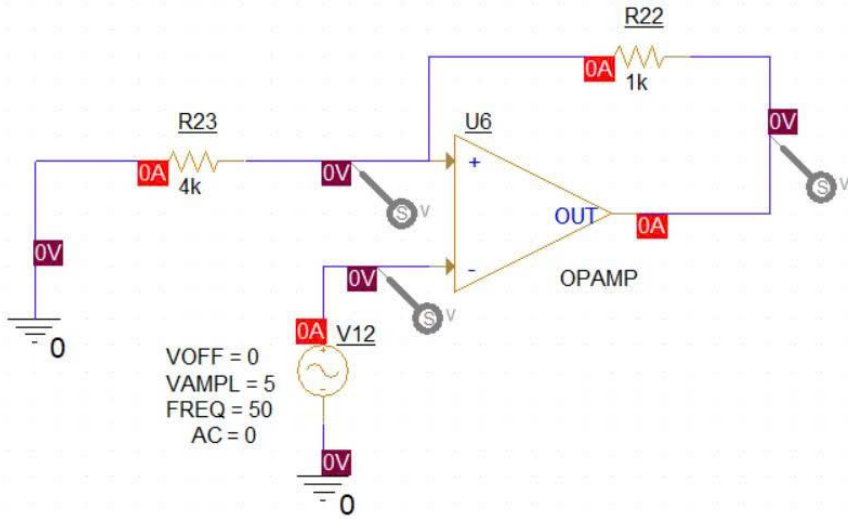
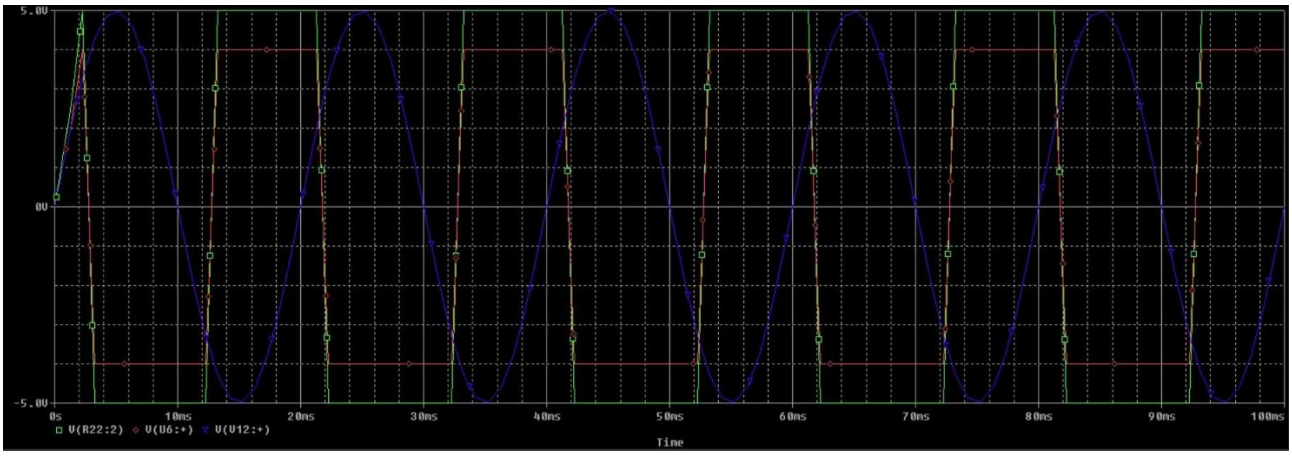


Figure 1.17: Schmitt trigger simulation results



Bias simulation



Explanation:
The input network functions as a basic series voltage adder, combining part of the output voltage with the input voltage so the signal switches between +4 V and –4 V.
This form of series positive feedback produces the required hysteresis, and its amount is determined by the ratio of R1 to the total resistance.

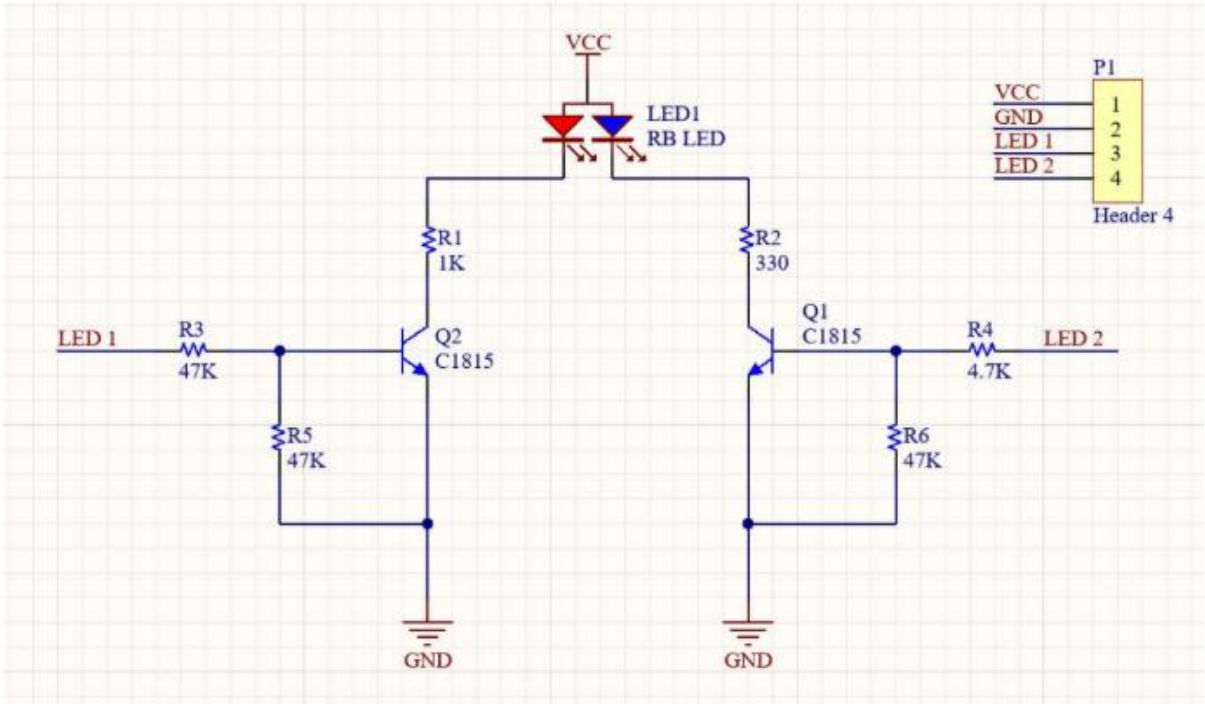
4. Altium Designer

4.1 LED Driver

In this project, we will show how to build a simple LED driver circuit. A simple driver based on BJT is proposed in this section.

4.1.1 Schematic design

The manual for the schematic is posted in this link:
https://www.youtube.com/watch?v=ftiX8peTsiw
Students are proposed to design the schematic and place the results in this report.

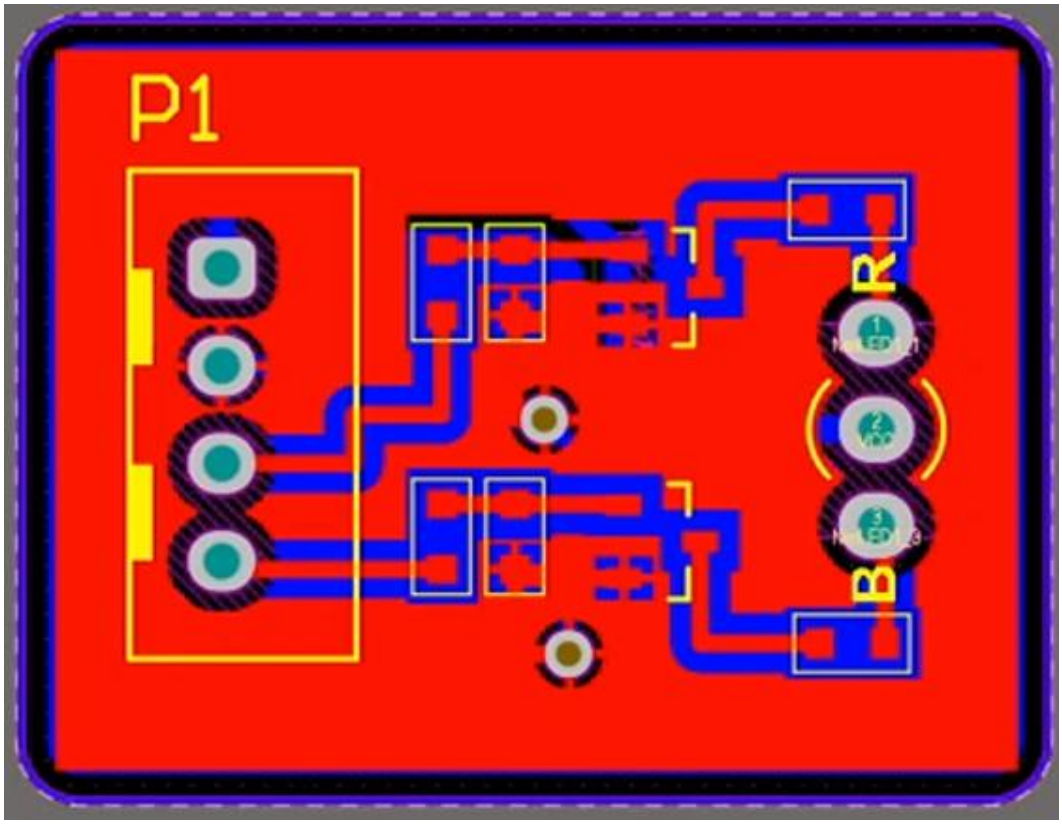


The schematic design of the LED Driver

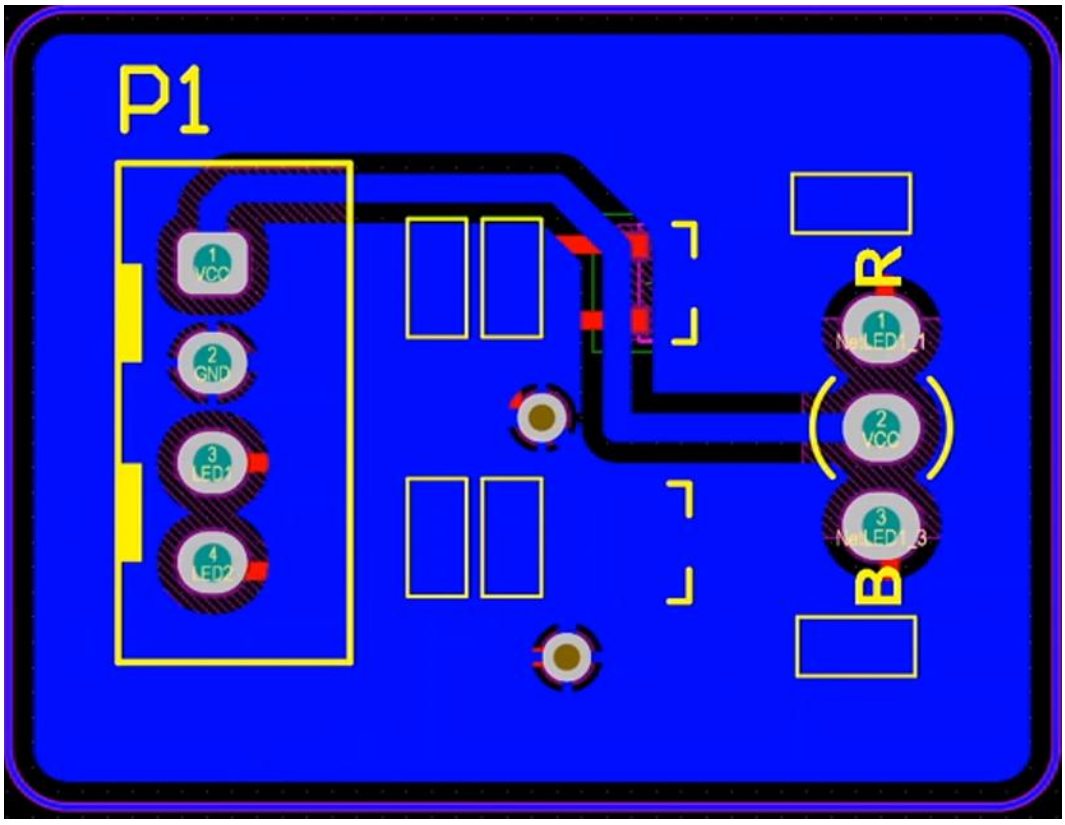
4.1.2 PCB layout

The manual for PCB layout is posted in this link:

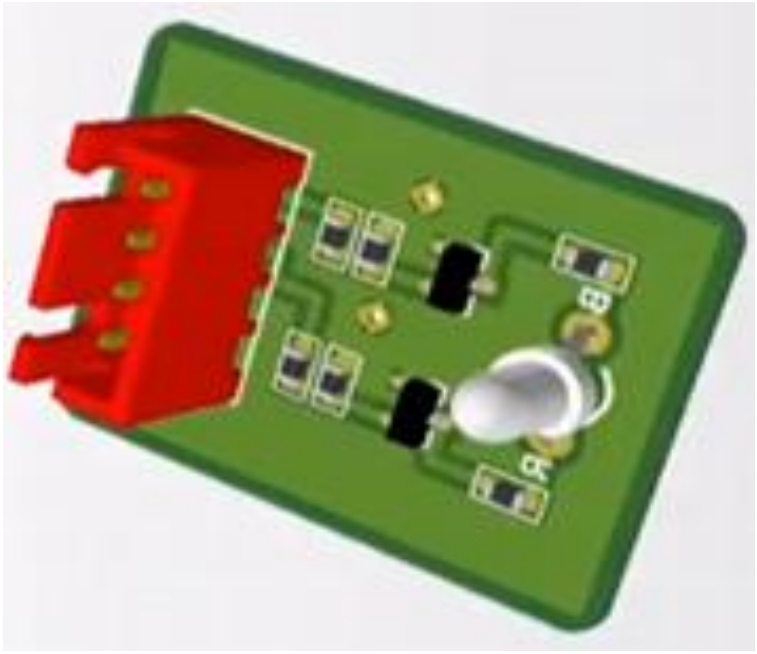
https://www.youtube.com/watch?v=btpAoh3nmBU



The top layer of the PCB layout



The bottom layer of the PCB layout



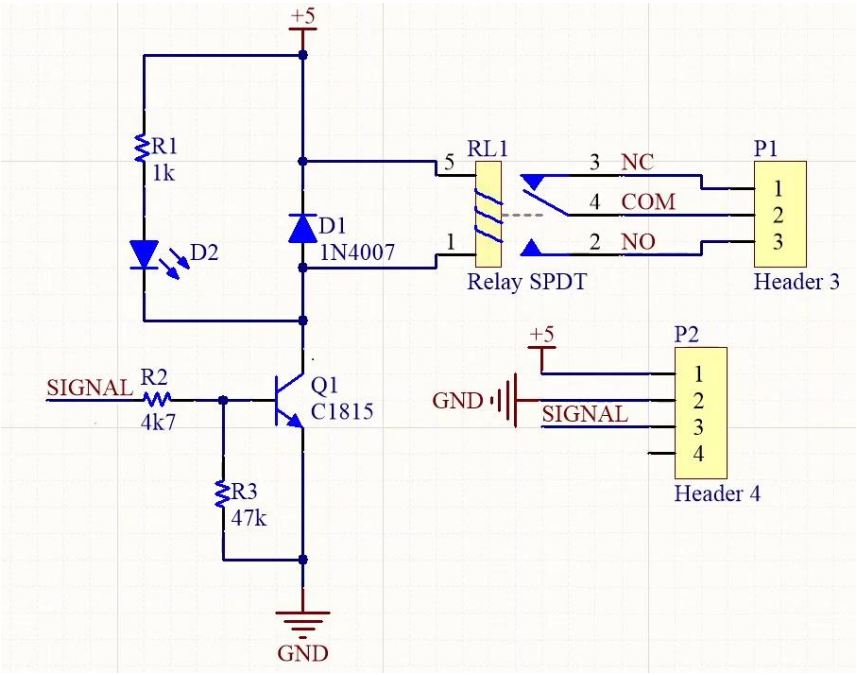
The LED Driver in 3D

4.2 Relay Controller

4.2.1 Schematic design

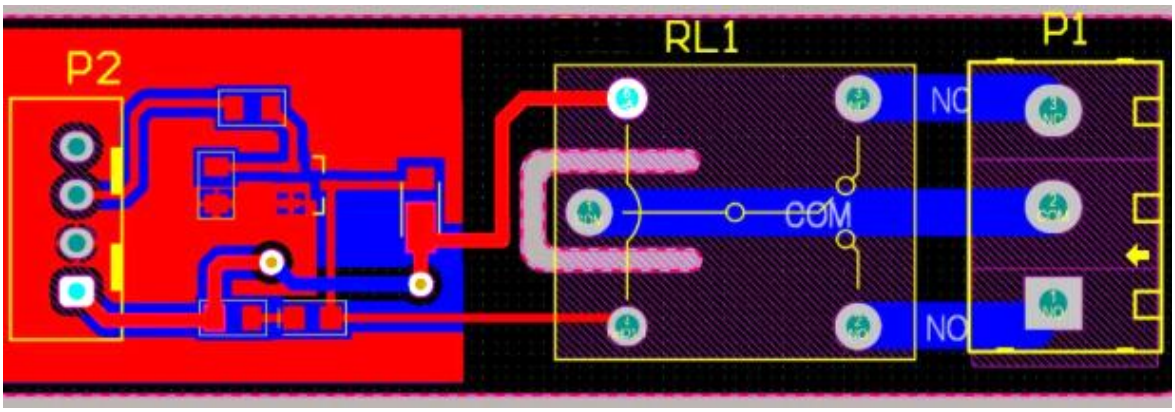
The manual for the schematic is posted in this link:
https://www.youtube.com/watch?v=VcO_F97ydFM

Students are proposed to design the schematic and place the results in this report.

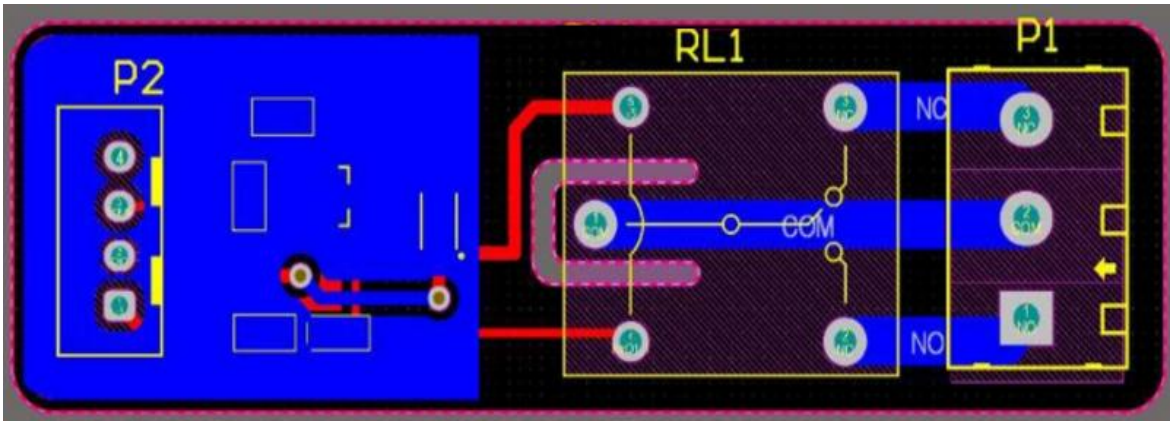


The schematic design of the Relay Controller

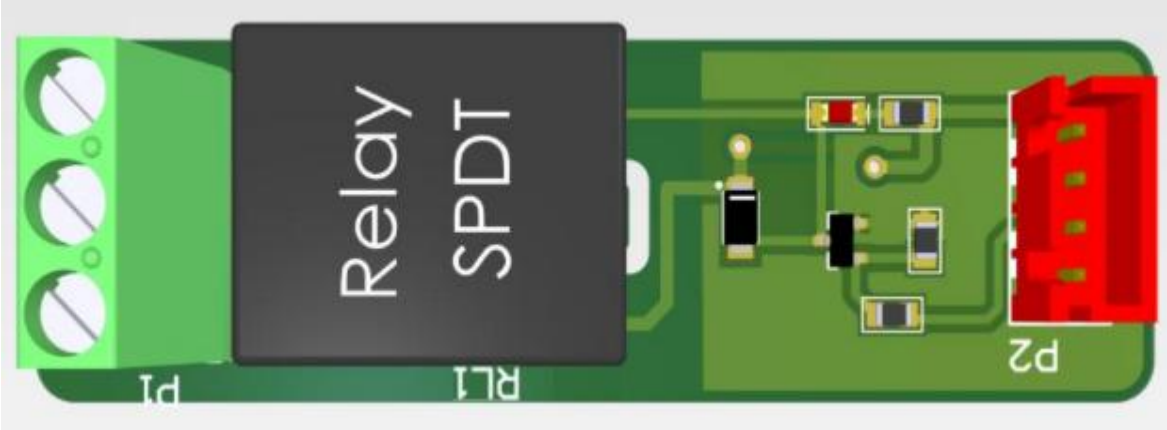
4.2.2 PCB layout



The top layer of the PCB layout



The bottom layer of the PCB layout



The Relay Controller in 3D