HO CHI MINH CITY UNIVERSITY OF TECHNOLOGY

OFFICE FOR INTERNATIONAL STUDY PROGRAM

SEMESTER: 251

LAB 3 REPORT

INSTRUCTOR:

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Class ID: CC04

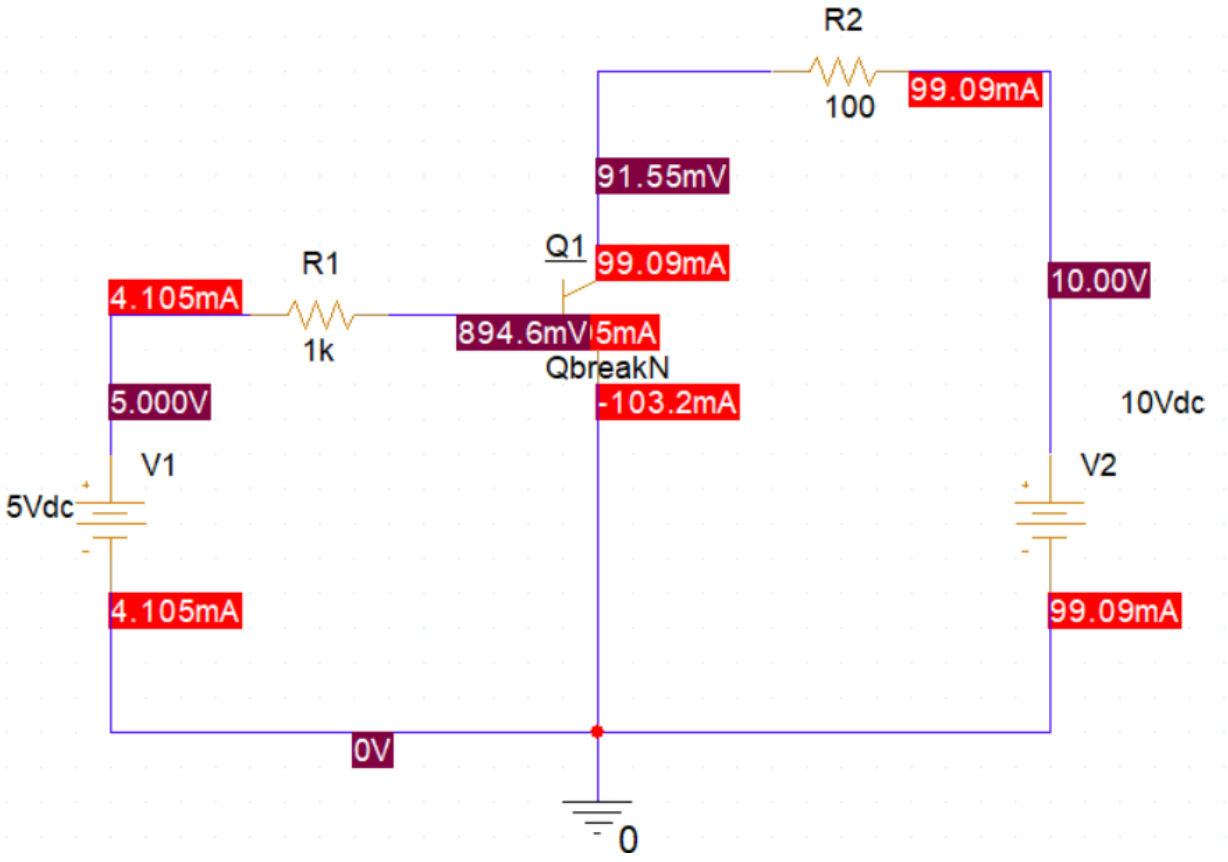
Ho Chi Minh city, October 30, 2025

Workload and Team Contribution

No.	Name	Student ID	Workload	Contribution
1	Trần Lê Tuấn Anh	2452089	3.1, 3.4, 3.8, report	100%
2	Nguyễn Thành Trường An	2452020	3.2, 3.5, 3.7, 3.10, 3.11	100%
3	Ngô Đức Anh (team leader)	2452054	3.3, 3.6, 3.9, 3.12, 3.13	100%

3.1 BJT in Saturation Mode

Change the value of **R1 to 1k** and run the simulation again. Capture the simulation results and explain the values of I_B ,I_C ,V_{CE} . The default transistor gain is $\beta = 100$, and the saturated voltage $V_{CE(Sat)} = 0.65V$ and $V_{BE} = 0.7V$.



The results in PSpice are explained as follows:

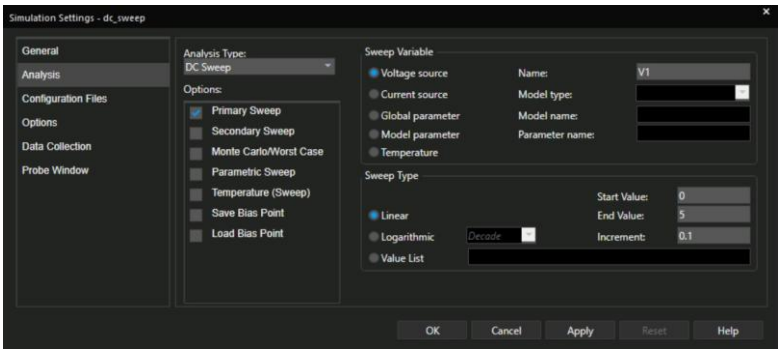
- According to the Ohm's Law, $I_B = \frac{V_{BB} - V_{BE}}{R_1} = \frac{5-0,7}{1000} = 4,3\ mA$
- It is assumed that the transistor is in linear (or active) mode, $I_C = \beta . I_B = 100.4,3.10^{-3} = 0,43\ A$
- Finally, in order to confirm the assumption above, $V_{CE} = V_{CC} - I_C . R2 = 10 - 0,43.100 = -33\ V$

Since $V_{CE} < 0$, our assumption is not correct. The transistor stays in saturation mode. Therefore, I_C is determined as follows:

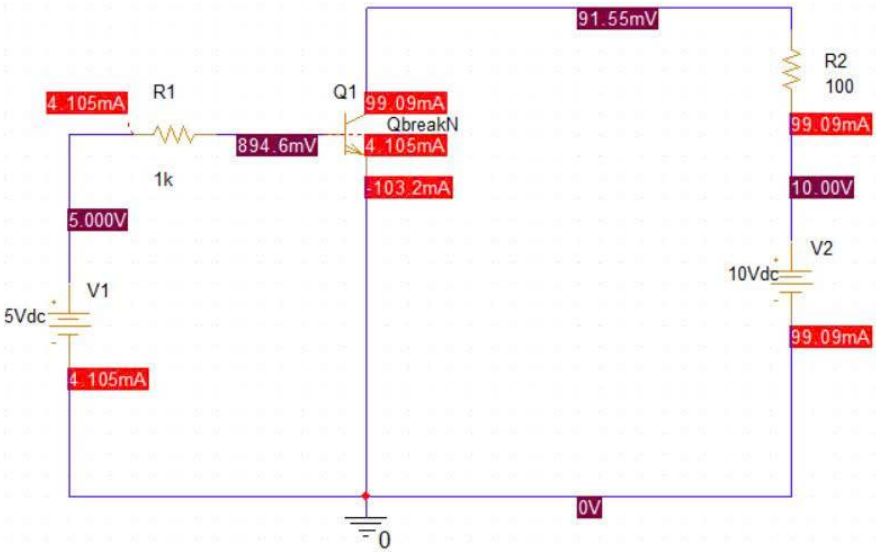
$$I_C = \frac{(V_{CC} - V_{CE(Sat)})}{R2} = \frac{10 - 0,65}{100} = 0,0935\ A$$

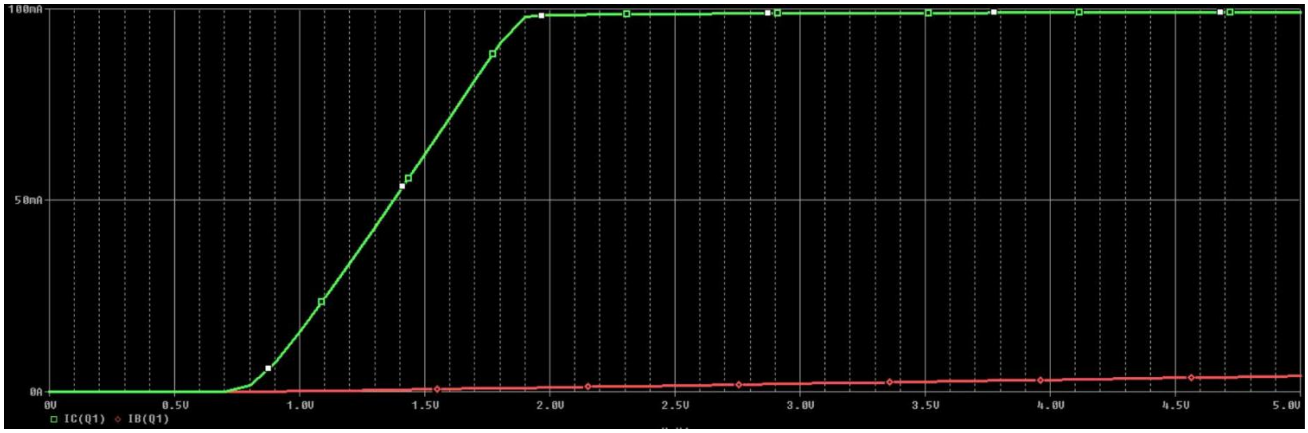
3.2 DC Sweep Simulation

The schematic in the first exersice with **R1 = 1k** is re-used in this exercise. However, a DC- Sweep simulation mode is performed with V1 is varied from 0V to 5V (0.1V for the step), as follows:



Run the simulation and trace for the current I_C according to the value of V1. Capture your screen and plot it in the report. Please increase the width of the curve.





Collector current in saturation (limited by R_2 and $V_{CE\,(sat)}$):

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_2} = \frac{10 - 0{,}65}{100} = 9{,}35 \cdot 10^{-2} = 93{,}5\,mA$$

Base current required (assuming β = 100) to produce that collector current:

$$I_B = \frac{I_{C(sat)}}{\beta} = \frac{93{,}5\,mA}{100} = 0{,}935\,mA$$

The base voltage V_1 that yields that base current through R_1 = 1 kΩ:

$$V_1 = I_B \cdot R_1 + V_{BE} = 0{,}935\,mA \cdot 1000\,\Omega + 0{,}7\,V = 1{,}635\,V$$

3.3 BJT used as a Switch

For a given BJT circuit, determine R_1 and R_2 to have IC saturated at 50mA. In this saturation mode, $V_{CE(Sat)}$ is 30mV. Assume that V_{BE} = 0.7V and the current gain β = 100.

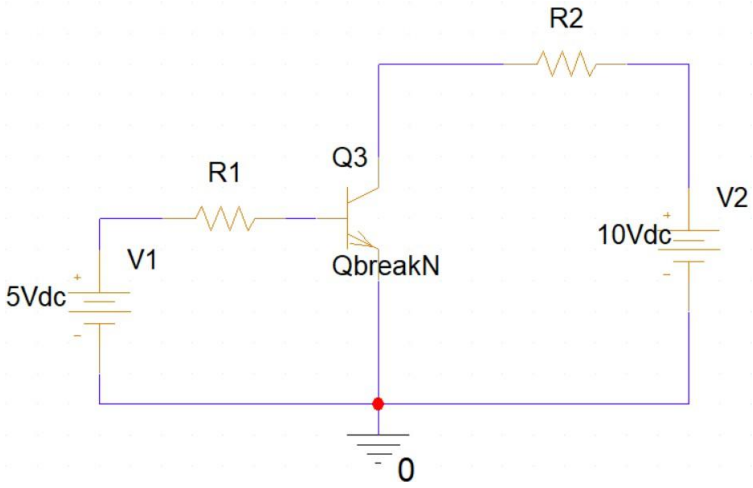
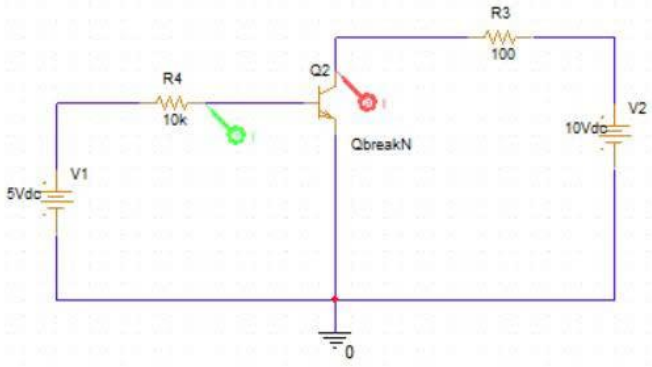
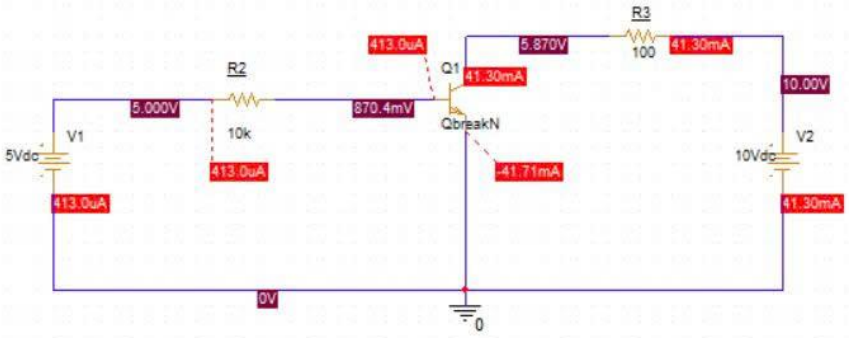


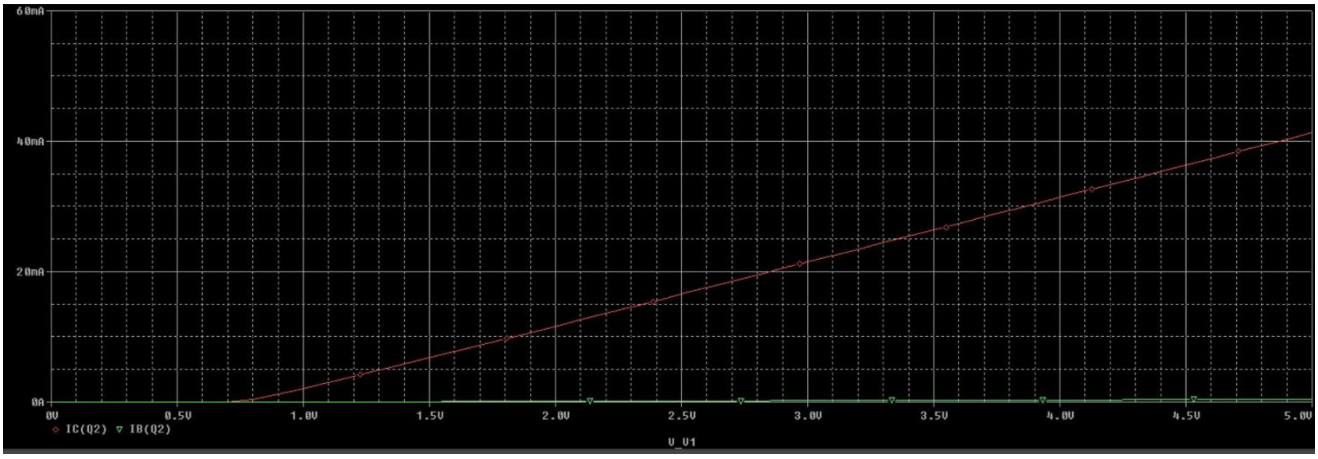
Figure 1.5: *BJT used as switch in saturation mode*

Present your solution to determine R1 and R2. Perform the simulation in PSpice to confirm the results. Capture the screen in PSpice and present in the report.



Here is the result circuit and simulation:





Explaination:

$$I_{C(Sat)} = \frac{V_{CC} - V_{CE(Sat)}}{R_2}$$

$$\Rightarrow 50.10^{-3} = \frac{10 - 30.10^{-3}}{R_2}$$

$$R_2 = 199{,}4\Omega$$

We have: $I_B = \frac{V_{BB}-V_{BE}}{R_1} \Leftrightarrow \frac{I_C}{B_{DC}} = \frac{V_{BB}-V_{BE}}{R_1} \Leftrightarrow \frac{50.10^{-3}}{100} = \frac{5-0{,}7}{R_1} \Rightarrow R_1 = 8600\Omega$

3.4 Drive a device with an NPN BJT

This exercise has a 5V logic output (the V_{ter} in Figure 1.6) that can source up to 10m A of current without a severe voltage drop and stand a maximum current of 20mA. If the logic terminal sources a current larger than 20mA, it would be damaged. Or, if it sources a current larger than 10 A, the V_{ter} voltage will drop to less than 4V . We should avoid this drop in many cases. However, this logic terminal has to be used to drive an electrical component with an equivalent internal resistance of 5 ohms (the LOAD in Figure 1.6) and requires a current of at least 300m A and not exceeding 500m A to function normally. Given that we have an NPN transistor with the current gain β equals 100, the maximum I_C current is 400m A, and the barrier potential at the BE junction is V_{BE} = 0.7V , select a resistor available in the market to replace the resistor R_B revealed in Figure 1.6. to make the circuit function well. After that, perform a simulation to double-check your selection.

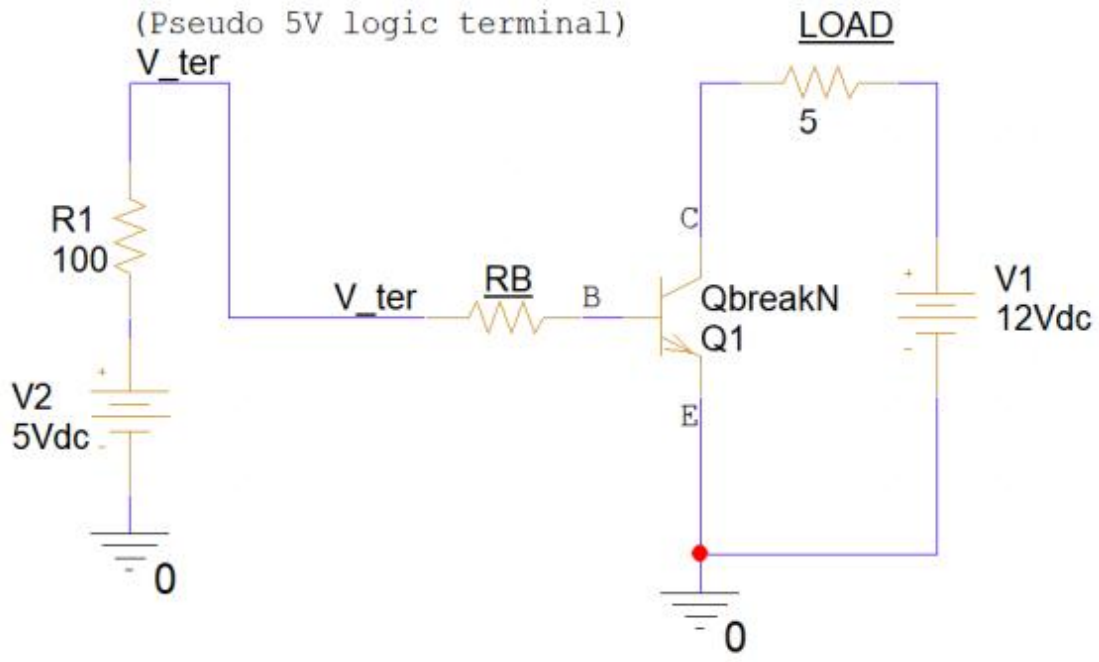


Figure 1.6: Select a resistor available in the market for R_B

3.4.1 Theory calculations

Notes: Explanations, formulas, and equations are expected rather than only results.

According to the limits of the LOAD and the transistor, we have:

$300mA\ (min) < I_C < 400mA$ (max)

According to the given information, we have:

$$I_{B(min)} = \frac{I_{C(min)}}{\beta} = \frac{300}{100} = 3\ mA$$

$$I_{B(max)} = \frac{I_{C(max)}}{\beta} = \frac{400}{100} = 4\ mA$$

So $3\ mA\ (min) < I_B < 4\ mA$ (max)

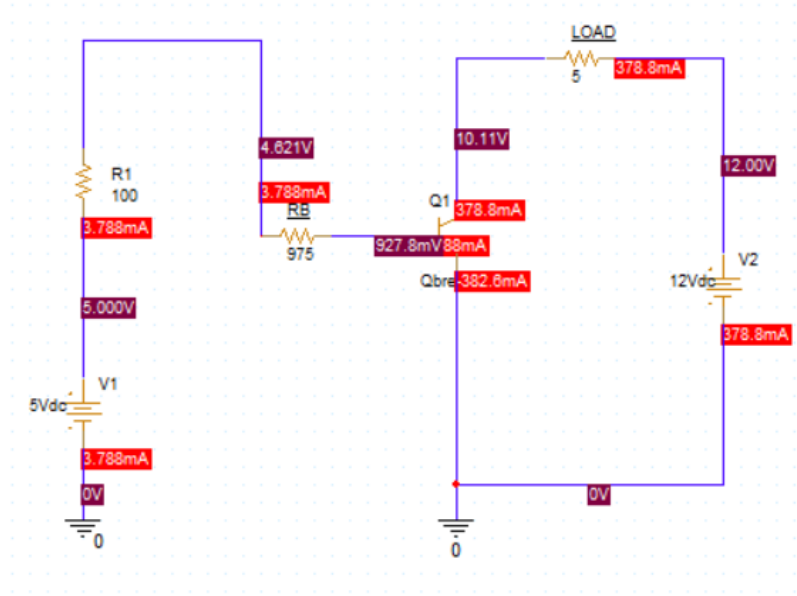
With $I_B(min) = 3\ mA$, we have: $R_B(max) = \frac{5-0,7}{3.10^{-3}} - 100 = 1333,(3)\Omega$

With $I_B(max) = 4\ mA$, we have: $R_B(min) = \frac{5-0,7}{4.10^{-3}} - 100 = 975\Omega$

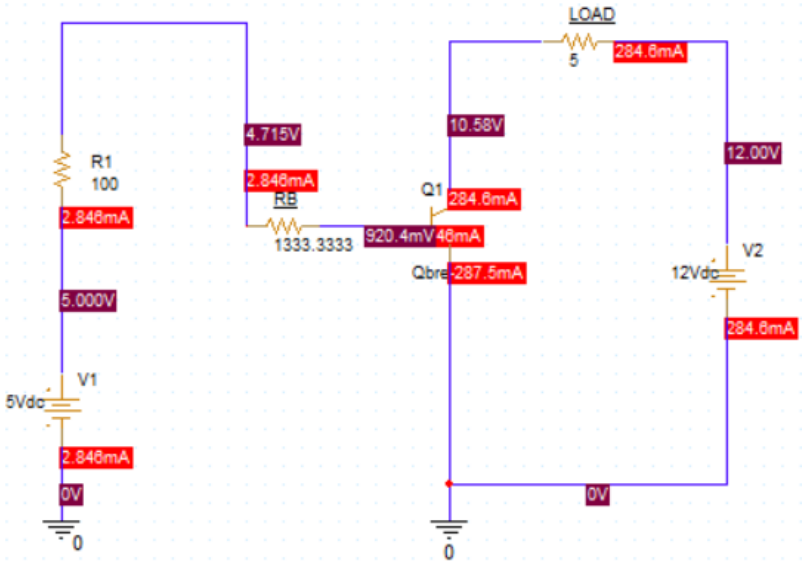
So:

$$975\ \Omega\ (min) < R_B < 1333,(3)\ mA\ (\text{max})$$
$$\Rightarrow\ R_B\ selected: 1100\Omega$$

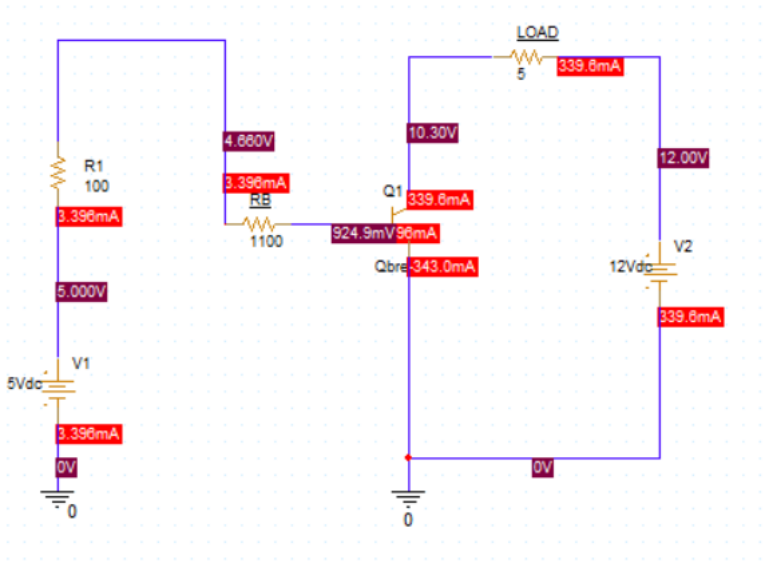
3.4.2 Simulation



Case $R_B(min)=975\Omega$



Case $R_B(max)=1333.3333\Omega$



Case R_B(selected)=1100Ω

3.4.3 Compare

		Theory			PSpice		
	R_B	V_{BE}	I_B	I_C	V_{BE}	I_B	I_C
$R_B(min)$	975Ω	0,7V	4mA	400mA	0,9278V	3,788mA	378,8mA
$R_B(max)$	1333, 3333Ω	0,7V	3mA	300mA	0,9204V	2.846mA	284,6mA
$R_B(selected)$	1100Ω	0,7V	3,58mA	358mA	0,9249V	3.396mA	339,6mA

3.5 Simple bias configuration

The circuit given in Figure 1.7 is known as a simple kind of NPN bias configuration. First, students simulate the circuit with two values of RC, respectively 10 Ohms and 1k Ohms. Then, give your statement on the change of the current I_E and explain the phenomena.

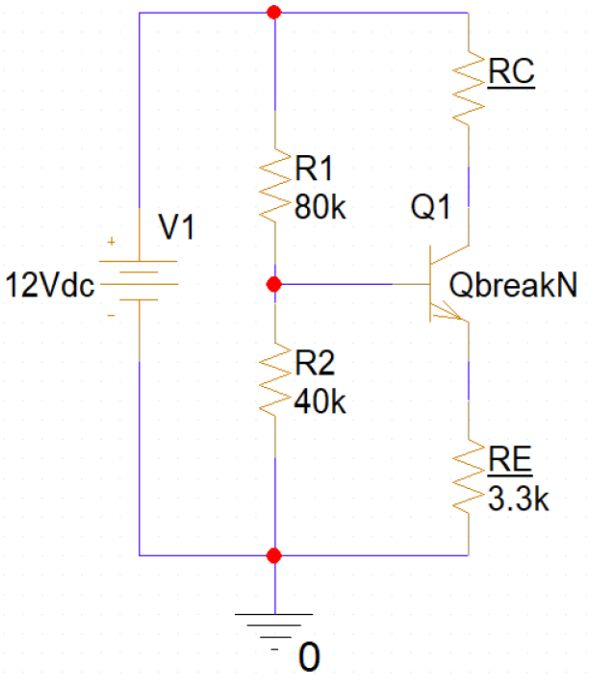
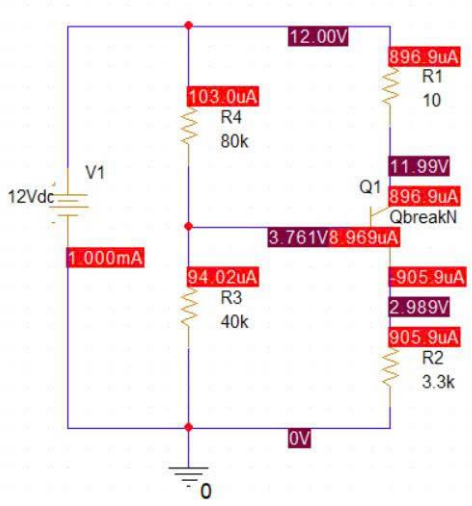


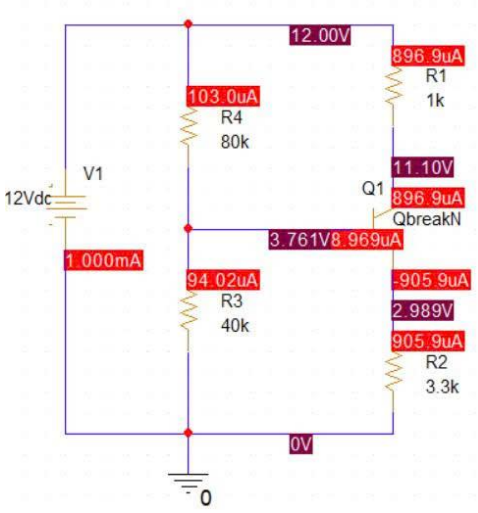
Figure 1.7: Simple bias configuration

3.5.1 Simulation

- With R_c=10Ω



- With R_c=1000Ω



3.5.2 Circuit analysis

Conduct some theoretical calculation to explain for the phenomena you have observed from the simulation.

The preceding simulation results indicate that the current flowing through the electronic circuit remains constant, notwithstanding the variation in the RC resistance value. This consistency will be accounted for in the subsequent theoretical calculation:

KVL in the bias divider loop ($R_1 – R_2 – V_{CC}$):

- V_1 source
- Voltage drops: 50k($i_1 - i_2$) across R_1 and 40k($i_2 - i_3$) across R_2

$$\Longrightarrow -12 + 50k(i_1 - i_2) + 40k(i_2 - i_3) = 0$$

KVL in emitter loop ($R_E – V_{BE} – R_2$):

- Voltage drops: 3,3k i_3 on R_E and 40k($i_2 - i_3$) on R_2
- 0,7V across base–emitter junction

Simplifies to:

$$-40ki_2 + 43{,}3ki_3 = -0{,}7$$

Transistor current relation:

$$i_E = i_C + i_B = 1{,}01i_C (\text{for } \beta = 100)$$

So:

$$i_3 = 1{,}01i_2$$

Since R_C does not appear in these KVL equations, the currents i_1, i_2, i_3 stay the same when R_C changes. Only V_C and V_{CE} change.

3.6 PNP Circuit

Figure 1.8 shows a very typical PNP transistor circuit. Calculate I_B , I_E , and I_C then simulate the circuit to double-check your calculation. Assume the current gain β = 100.

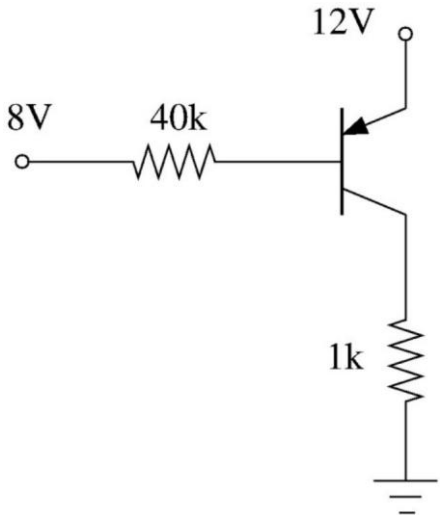


Figure 1.8: A PNP Circuit

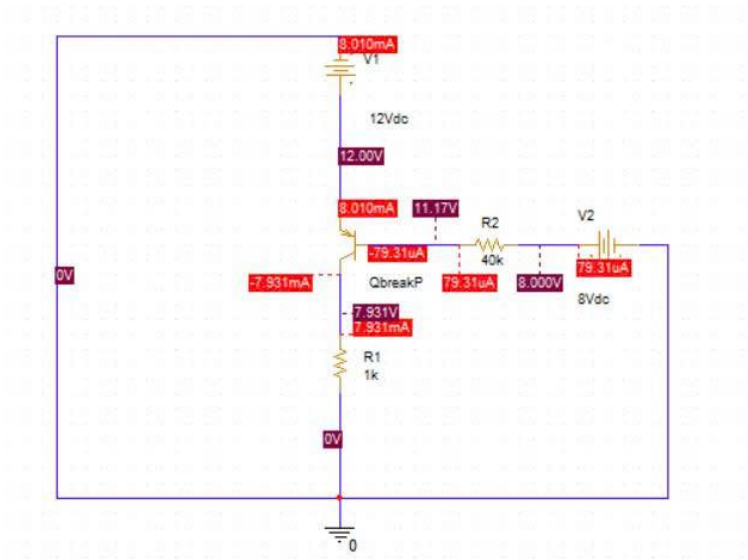
3.6.1 Theoretical calculation

$$V_{EB} = -V_{BE} = -0{,}7V$$
$$V_E = V_B + 0.7$$
$$\Rightarrow 12 = V_B + 0{,}7 \Rightarrow V_B = 11{,}3$$
$$\Rightarrow V_{BE} = V_B - V_E = -0{,}7\ (V)$$
$$I_B = \frac{8 - 11{,}3}{40000} = -8{,}25.10^{-5}\ (A)$$

Negative sign shows that the current I_B runs from base to the 8V source.

$$\Rightarrow I_B = 82{,}5\ \mu A$$
$$\Rightarrow I_C = \beta_{DC} \cdot I_B = 82{,}5.10^{-6}.100 = 8{,}25\ mA$$
$$I_E = I_B + I_C = 8{,}25.10^{-3} + 82{,}5.10^{-6} = 8{,}3325.10^{-3}\ A$$

3.6.2 Simulation



3.6.3 Comparison

	Theory	Simulation
I_B	82,5 μA	79,31 μA
I_C	8,25 mA	8,01 mA
I_E	8,3325mA	7,931 mA

3.7 Circuit with NPN and PNP bipolar junction transistors

Give the circuit in Figure 1.9. Calculate the Voltage at all nodes and the current in all branches. Assume the current gain of both transistors is the same at $\beta = 100$. Then per- form a simulation and compare the result with the theoretical calculation.

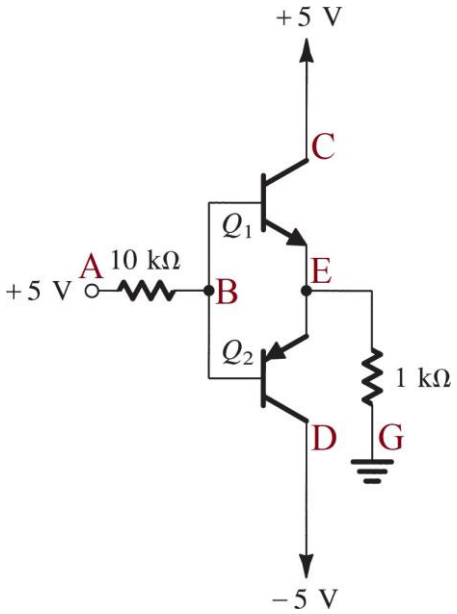


Figure 1.9: Circuit with NPN and PNP bipolar junction transistors

3.7.1 Theoretical calculation

We have:

• Base node B is driven from +5V through 10kΩ, that tends to pull V_B high (near +5V) unless a large base current flows.

• For Q_1 (NPN) to conduct, we need $V_B - V_E \approx V_{BE} \approx 0.7V$. That is easily achievable since V_B is near +5V.
• For Q_2 (PNP) to conduct, we require its emitter (which is node E) to be ≈ 0.7V more positive than its base B, which is impossible here because the supply only goes to +5V.
So Q_1 (NPN) will be ON and Q_2 (PNP) will be OFF in quiescent steady state.
Let

$$I_B = \text{Base current into Q1}$$

$$I_C \approx \beta I_B$$

$$I_E \approx (\beta + 1) I_B$$

Voltage at base (voltage divider / resistor drop from +5V):

$$V_B = 5V - I_B(10k\Omega)(1)$$

Emitter–base relation for the conducting NPN:

$$V_E = V_B - V_{BE} \text{ with } V_{BE} \approx 0{,}7V(2)$$

Emitter current flows through the 1kΩ to ground:

$$I_E = \frac{V_E}{1k\Omega}(3)$$

Current relation:

$$I_E = (\beta + 1) I_B(4)$$

Combine (1), (2), (3), and (4), we have:

$$\frac{5 - 10000 I_B - 0{,}7}{1000} = (\beta + 1) I_B$$

We got

$$I_B = \frac{4{,}3}{111000} \approx 3{,}8739.10^{-5} A = 38{,}74\,\mu A$$

Base voltage:

$$V_B = 5 - 10000 I_B \approx 4{,}613V$$

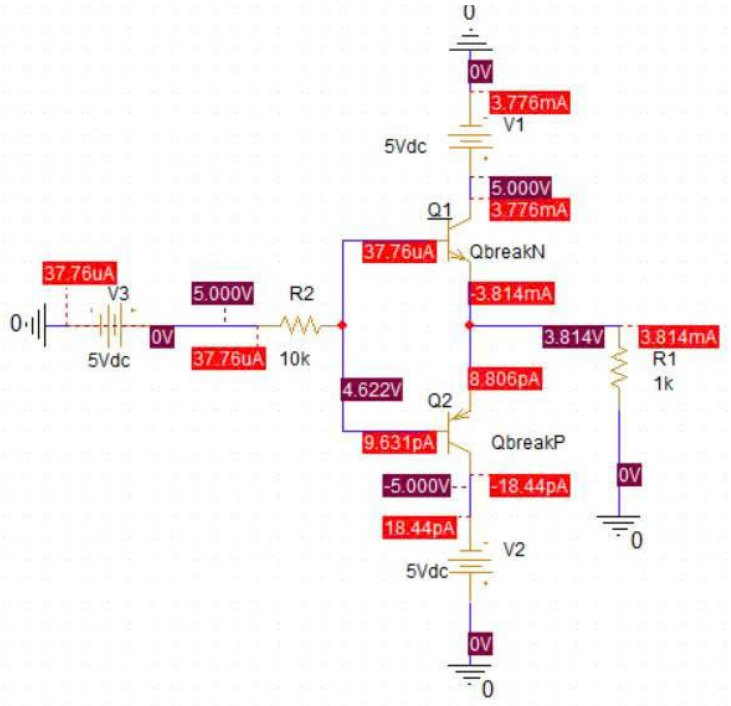
Emitter voltage:

$$V_E = V_B - 0{,}7V \approx 4{,}613 - 0{,}7 = 3{,}913V$$

Emitter current (through 1kΩ to ground):

$$I_E = \frac{V_E}{1000} \approx \frac{3{,}913}{1000} = 3{,}913\,mA$$

3.7.2 Simulation



3.7.3 Comparison

	I_B	I_C	I_{EG}	V_E	V_B
Theory	38,74µA	3,874µA	3,913mA	3,913V	4,613V
Simulation	37,76µA	3,776µA	3,814mA	3,814V	4,622V

3.8 NPN Circuit with E resistance

In Figure 1.10, calculate all the values of I_B , I_C , I_E , V_E , and V_C . Assume the voltage drop V_{BE} = 0.7V and the current gain coefficient of the transistor is β = 100. Then, perform a simulation to double-check your theoretical calculations.

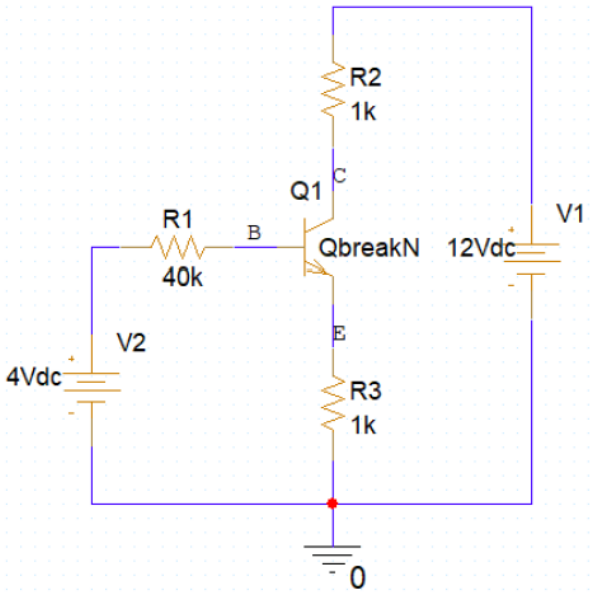


Figure 1.10: NPN Circuit with E resistance

3.8.1 Theoretical calculation

Notes: Explanations, formulas, and equations are expected rather than only results.

According to the KVL, we have the following equation:

$$-4 + I_B R_B + V_{BE} + I_E R_E = 0$$

And we also got $I_E = I_B + I_C = I_B + 100I_B = 101I_B$

$$\Leftrightarrow\ -4 + I_B R_B + V_{BE} + 101 I_B R_E = 0 \Leftrightarrow I_B = \frac{4 - V_{BE}}{R_B + 101 R_E} = \frac{4 - 0{,}7}{40.10^3 + 101.10^3} (1)$$

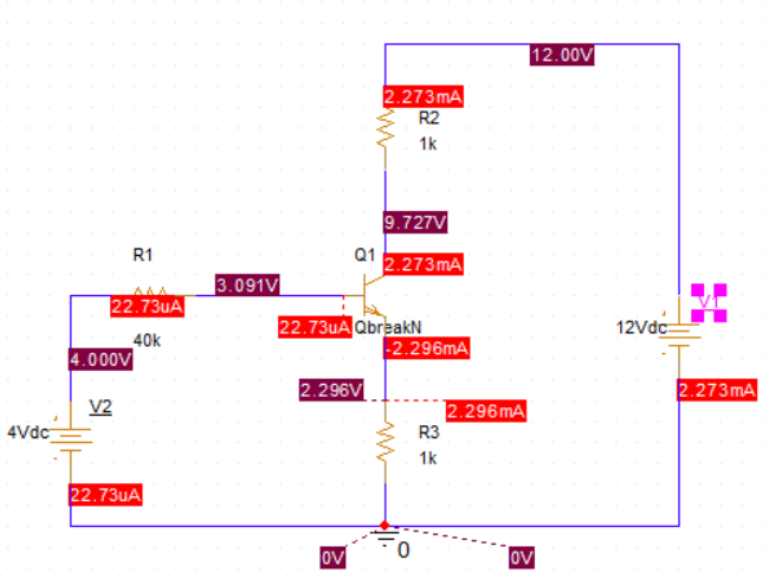
Solve (1), we have $I_B = 2{,}34\mu A$

$$I_C = I_B . \beta = 2{,}34mA$$

$$I_E = 101 . I_B = 2{,}36mA$$

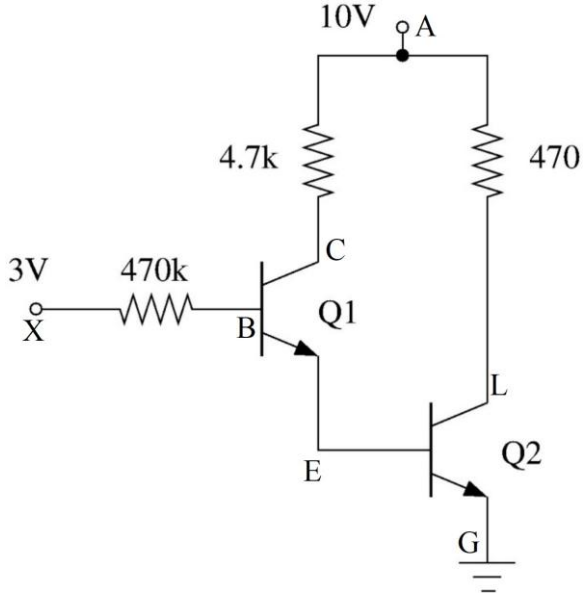
$$V_C = V_{CC} - I_C . R_C = 12 - 2{,}34 . 10^{-3} . 10^3 = 9{,}66V$$

3.8.2 Simulation



3.9 Darlington circuit

The circuit given in Figure 1.11 is known as a darlington circuit. Calculate I_{BE} , I_{AC} , I_{AL}, and the overall current gain $\frac{I_{AL}}{I_{BE}}$. After that, simulate the circuit to double-check your theoretical calculations. Assume both transistors have the same current gain coefficient β = 100.



3.9.1 Theoretical calculation

Because there are 2 BJT connected series, we write KVL from 3V source through Q_1

and Q_2 to ground

$$V_{source} - I_{B1}R_B - V_{BE1} - V_{BE2} = 0$$
$$3 - I_{B1} \cdot 470000 - 2 \cdot 0{,}7 = 0$$
$$\Rightarrow I_{B1} = 3{,}404 \cdot 10^{-6}\, A$$
$$I_{AC} = I_{C1} = \beta I_{B1} = 100 \cdot 3{,}404 \cdot 10^{-6} = 340{,}4 \cdot 10^{-6}\, A$$
$$I_{B2} = I_{BE} = I_{B1} + I_{C1} = I_{B1} + 101 I_{B1} = 101 I_{B1} = 343{,}8 \cdot 10^{-6}\, A$$
$$I_{AL} = \beta I_{B2} = 100 \cdot I_{B2} = 34{,}38 \cdot 10^{-3}\, A$$

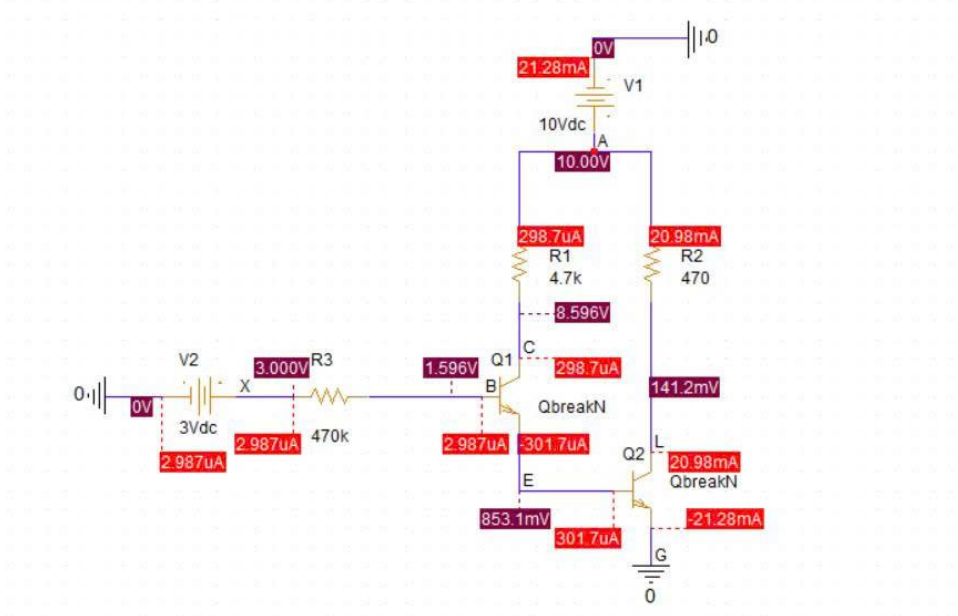
But we have:

$$V_L = V_{CC} - I_{AL}R_L = 10 - 34{,}38 \cdot 10^{-3} \cdot 470 = -6{,}16\, V$$

→ Physically impossible
So Q_2 has to be saturated.
Based on the data sheet of PC817, we have $V_{CE(sat)} = 0{,}2\, V$

$$I_{AL} = \frac{V_{CC} - V_{CE(sat)}}{R_L} = \frac{10 - 0{,}2}{470} = 20{,}85 \cdot 10^{-3}\, A$$
$$\frac{I_{AL}}{I_{BE}} = \frac{20{,}85 \cdot 10^{-3}}{343{,}8 \cdot 10^{-6}} = 60{,}64$$

3.9.2 Simulation



3.10 Common base

Figure 1.12 shows a bias techniques named common base bias. Calculate the values of I_E , I_B , I_C , and V_{CE} . Then simulate the circuit to double-check your theoretical calculations. Assume the current gain coefficient β = 100.

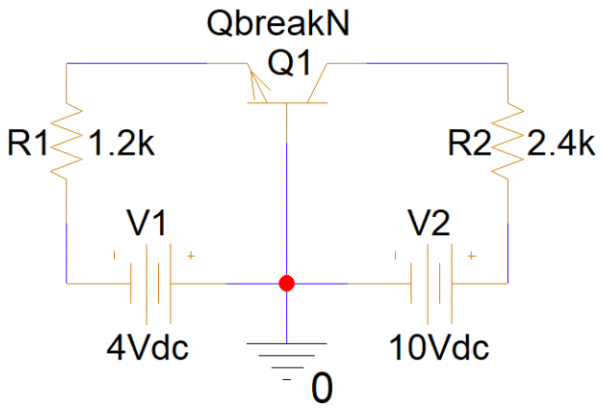


Figure 1.12: Common base

3.10.1 Theoretical calculation

Emitter voltage (common-base relation):
In forward-active operation the base–emitter drop is:

$$V_B - V_E \approx V_{BE} \approx 0{,}7V$$

Since $V_B = 0$:

$$V_E = V_B - V_{BE} = 0 - 0{,}7 = -0{,}7V$$

Emitter current I_E:
Current through R_1 sets the emitter current (current from the emitter node toward the left supply). Using the node voltages:

$$I_E = \frac{V_E - V_1}{R_1} = \frac{(-0{,}7) - (-4)}{1200} = 2{,}75\ \text{mA}$$

Collector current I_C and base current I_B:
Use $\alpha \approx \frac{\beta}{\beta+1} = \frac{100}{101}$

$$I_C = \alpha I_E = \frac{100}{101}.2{,}75\ \text{mA} = 2{,}7228\ \text{mA}$$

Base current:

$$I_B = I_E - I_C = 2{,}75\ \text{mA} - 2{,}7228\ \text{mA} = 0{,}0272\ \text{mA} = 27{,}2\ \mu\text{A}$$

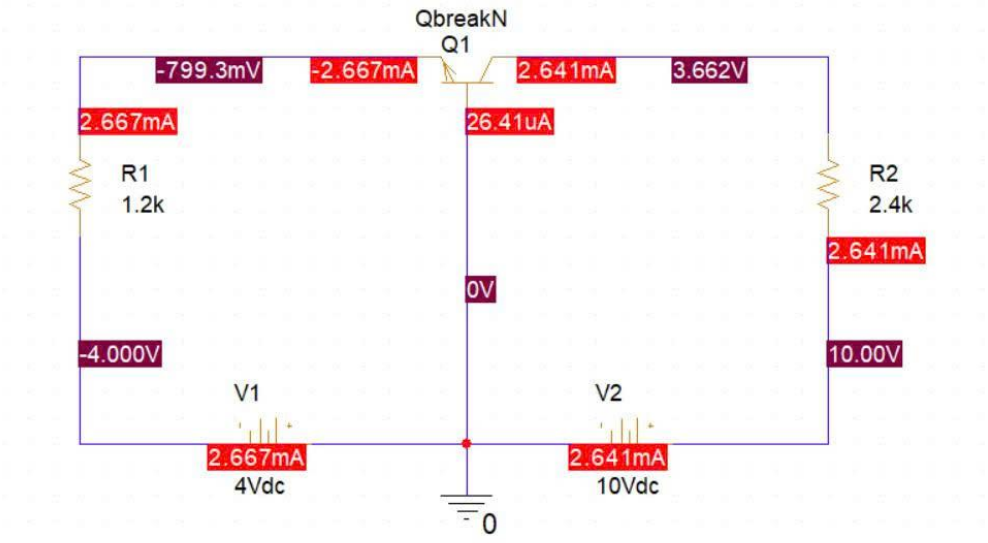
Collector voltage V_C and V_{CE}:
Collector node set by V_2 and drop across R_2:

$$V_C = V_2 - I_C R_2 = 10 - 2{,}7228.10^{-3}.2400 \approx 3{,}4653\ \text{V}$$

Then,

$$V_{CE} = V_C - V_E = 3{,}4653 - (-0{,}7) \approx 4{,}1653\ \text{V}$$

3.10.2 Simulation



3.11 Current mirror

The circuit shown in Figure 1.13 is known as a current mirror circuit. First, students do some theoretical calculations to get an understanding of it. After that, perform a simula- tion to double-check its principles and your analysis. Assume that the two transistors Q1 and Q2, are the same type and the current gain $\beta = 100$.

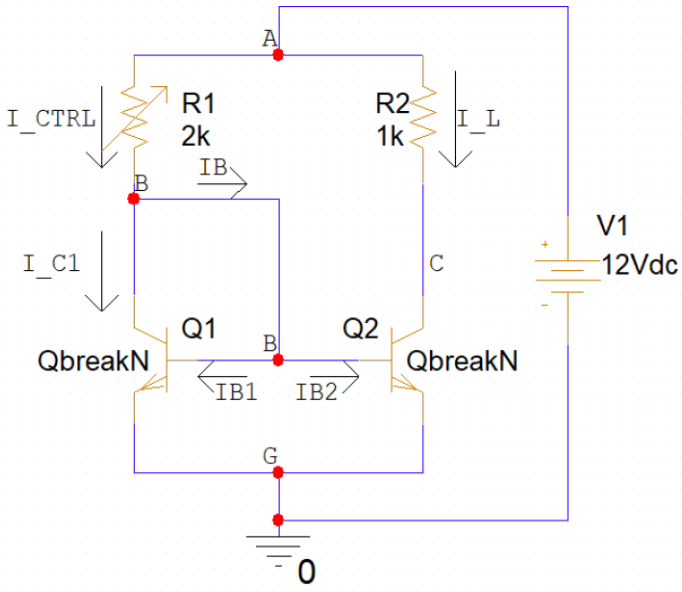


Figure 1.13: Current mirror circuit example

3.11.1 Theoretical calculation

Reference current through R_1:

The voltage across R_1 is $V_{CC} - V_B$. For the diode-connected transistor Q_1, the base voltage:

$$V_B \approx V_{BE} \approx 0{,}7\ V$$

$$I_{R1} = \frac{V_{CC} - V_B}{R_1} = \frac{12 - 0{,}7}{2000} = \frac{11{,}3}{2000} = 5{,}65\ \text{mA}$$

(That is, the total current coming down through R_1 into the base collector node).

KCL at the base/collector node (node B):

Current from R1 splits into I_{C1}(collector of Q_1)
and the base currents of both transistors:

$$I_{R1} = I_{C1} + I_{B1} + I_{B2}$$

Use $I_{C1} = \beta I_{B1}$ and $I_{C2} = \beta I_{B2}$.
If transistors are matched and both operate in active region, $I_{C1} = I_{C2} = I_C$. Then:
$I_{B1} = \frac{I_C}{\beta}$ and $I_{B2} = \frac{I_C}{\beta}$

So:

$$I_{R1} = I_C + \frac{I_C}{\beta} + \frac{I_C}{\beta} = I_C(1 + \frac{2}{\beta})$$

Thus:

$$\mathrm{I_C} = \frac{\mathrm{I_{R1}}}{1 + \frac{2}{\beta}} = \frac{\beta}{\beta + 2}\mathrm{I_{R1}} = \frac{100}{102}.5{,}65\ \mathrm{mA} \approx 5{,}54\ \mathrm{mA}$$

Base currents

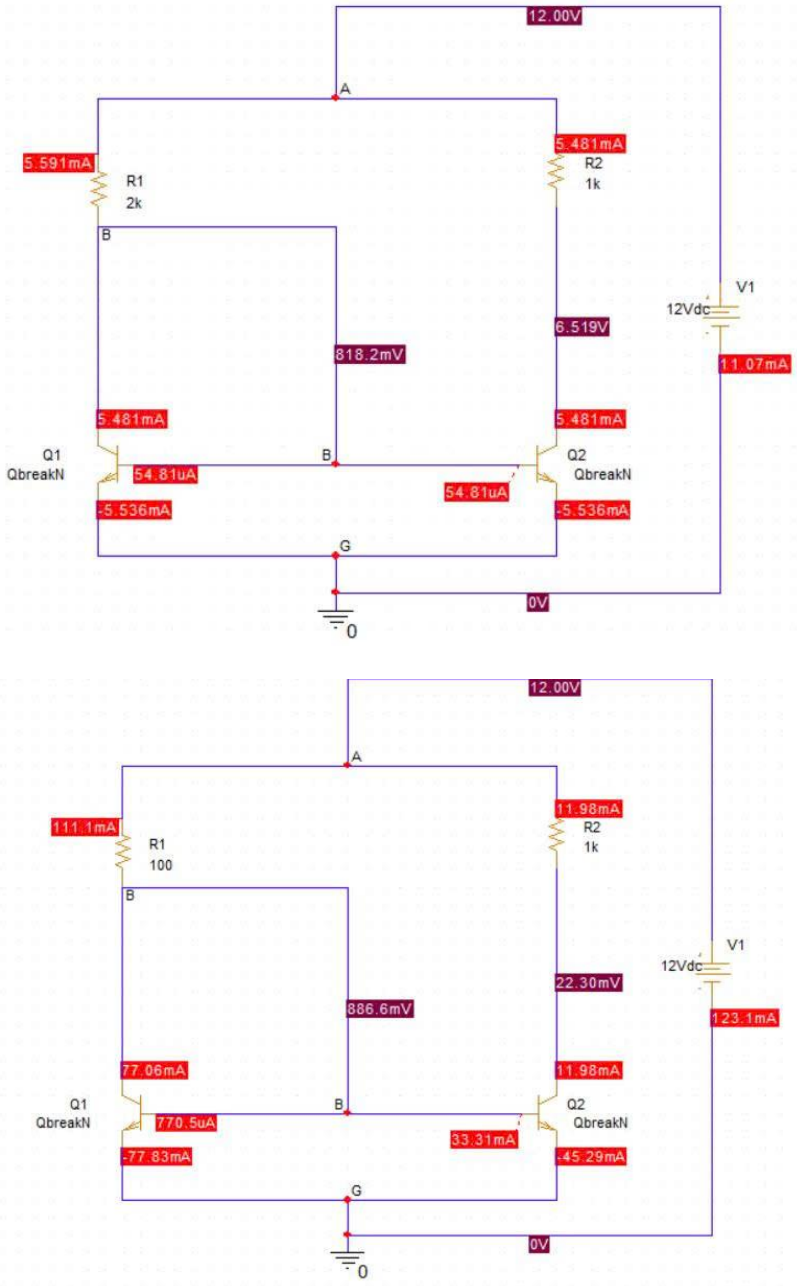
$$I_{B1} = I_{B2} = \frac{I_C}{\beta} = \frac{5{,}54\ \mathrm{mA}}{100} = 55{,}4\ \mu\mathrm{A}$$

Output/Load current I_L:
The mirrored output (through Q_2) is: $I_L = I_{C2} \approx 5{,}54\ \mathrm{mA}$
The circuit is called a current mirror.
The two transistors Q_1 and Q_2 have their bases tied together. Q_1 is diode-connected (its base and collector are tied), so the current through R_1 forces a base-emitter voltage V_{BE}. That same $V_{BE}$is applied to Q_2. If Q_2 has enough voltage headroom (sufficient V_{CE}), it will draw the same collector current as Q_1.
The case: $R_1 = 100\ \Omega$. We have, when calculated similarly:

$$I_{R1} \approx 113\ \mathrm{mA}$$
$$I_{C1} \approx 110{,}8\ \mathrm{mA}$$
$$I_{B1} = I_{B2} = 1{,}108\ \mathrm{mA}$$
$$I_L \approx 110{,}8\ \mathrm{mA}$$

– Phenomenon:
When $R_1 = 100\ \Omega$, the reference side (Q_1) tries to create a very large current (over $100\ mA$).
But the load resistor $R_2 = 1\ k\Omega$can only allow about $11\ mA$ from the 12 V supply.
Because of this, Q_2cannot produce the same current as Q_1, so Q_2goes into saturation, and the current mirror fails to mirror the reference current.
– Explanation:
A current mirror only works when the output transistor (Q_2) has enough voltage across it.
With $R_1 = 100\ \Omega$, the circuit tries to demand too much current—more than the load can supply—so Q_2saturates, and the output current is then stuck at only $11\ mA$, not the large reference current.
Therefore, the mirror can no longer copy the current.

3.11.2 Simulation



3.12 BJT's logic gate application

Figure 1.14 describes a straightforward NOT gate theoretical implementation using an NPN bipolar junction transistor. In the circuit, the NPN junction transistor operates in the saturation mode.

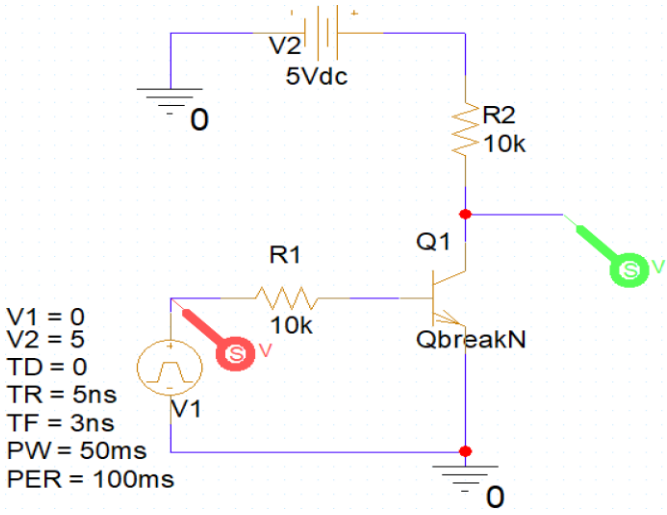
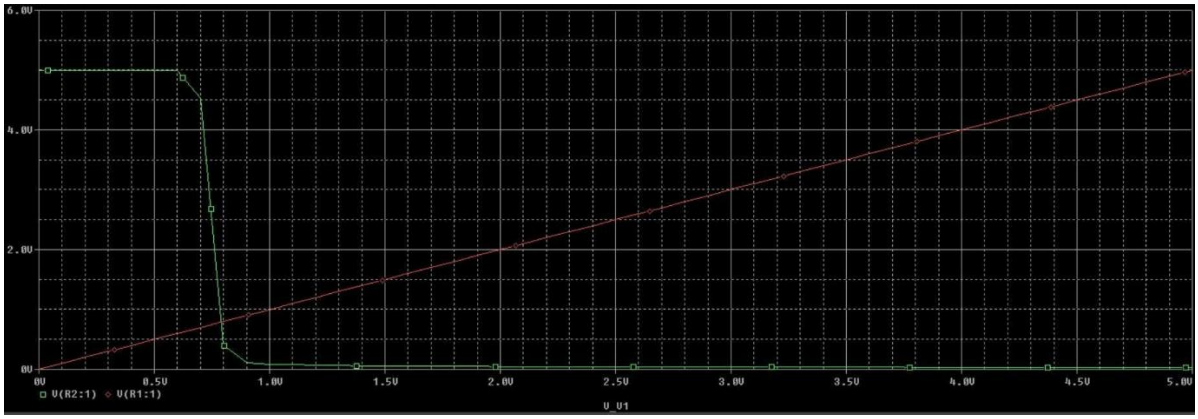


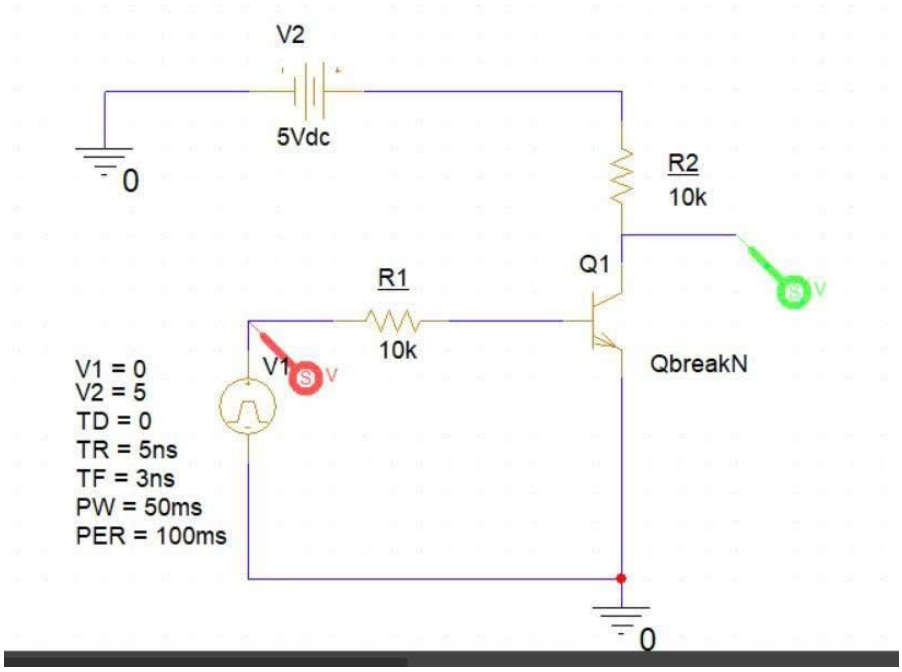
Figure 1.14: NPN theoretical NOT gate

V1 = 0 When the source is off, the voltage would be 0V.
V2 = 5 When the source is on, the voltage would be 5V.
TD = 0 Delay time. This exercise assumes that there is no delay. TR = 5ns The rise time of the pulse (from off to on stage).
TF = 3ns The fall time of the pulse (from on to off stage).
PW = 50ms Pulse width: The time in which the source keeps on. PER = 100ms The period of the signal.
Tips:

To get the Voltage Pulse Source component in the PSpice for TI, go to ***Place -> Pspice Compoment... -> Source -> Voltage Sources -> Pulse.***

3.12.1 Simulation





3.13 Opto

The element OK_1 in Figure 1.18 is an optocoupler, which includes a light-emitting diode (LED) and a photodiode. The photodiode's conductivity depends on the intensity of the light emitted by the LED, and of course, depends on the current intensity through the LED. When the voltage across the LED is lower than its barrier potential, the Opto is cut- off. When there is current through the LED, the Opto is in the transfer mode. Like the current gain β of a BJT, the Opto also has the current transfer ratio (CTR). Assume the LED has its own barrier potential V_F = 1.7V, and the Opto has the CTR = 2. Calculate the voltage V_{OUT} when the switch is closed. Finally, give your idea about what we may use an Opto for, and how to use it?

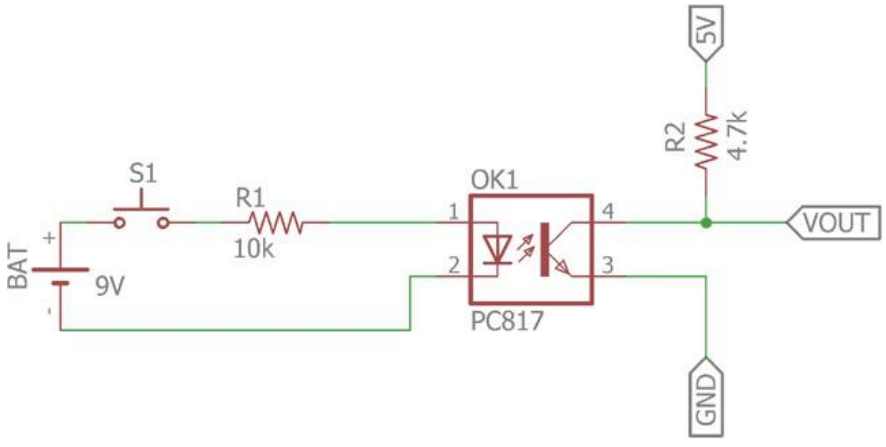


Figure 1.18: Voltage isolation with opto

Solution

$$I_F = I_{R1} = \frac{V_{Bat} - V_F}{R_1} = \frac{9 - 1{,}7}{10000} = 0{,}73 \text{ mA}$$
$$I_{R2} = I_C = I_F \times CTR = 2.0{,}73.10^{-3} = 1{,}46 \text{ mA}$$

So we have the output voltage:

$$V_{out} = 5 - I_{R2} \cdot R_2 = 5 - (1{,}46.10^{-3}.4700) = -1{,}86 \text{ V}$$

Because the output voltage is negative → **Physically impossible**
→ The circuit is in **saturation mode**
Based on the datasheet of **PC817**, we have:

$$V_{CE(sat)} = 0.2 \text{ V}$$
$$\Rightarrow V_{out} = V_{CE(sat)} = 0.2 \text{ V}$$

Applications of Optocouplers:
An optocoupler (or optical isolator) is a component that transfers signals through light to separate two circuits. It usually includes an LED and a phototransistor inside one package.
Electrical isolation: Protects low-voltage control circuits from high-voltage or noisy power circuits.
Safe signal transfer: Sends signals without direct electrical connection.
Noise reduction: Prevents ground loops and reduces electrical interference.
Safety protection: Ensures user and equipment safety in high-voltage systems.