Register	address	
SBND R0	0x0	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 **4 3 2 1 0**
	0 (r/w)	global reset (TODO)
	1 (r/w)	register reset (TODO)
	2 (r/w)	udp reset (TODO)
	3 (r/w)	FEMB clock encoder (TODO)
	4 (r/w)	HSD reset (TODO)
SBND R1	0x1	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 **3 2 1 0**
	3..0 (r/w)	FEMB clock encoder sw commands 4 downto 1 (TODO)
SBND R2	0x2	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 **7 6 5 4 3 2 1 0**
	0 (r/w)	WIB LED 0 and FEMB clock encoder disable command 1
	7..1 (r/w)	WIB LEDs (TODO)
SBND R3	0x3	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Register	address	
SBND R4	0x4	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 **3 2 1 0**
	0 (r/w)	FEMB clock select (TODO)
	1 (r/w)	FEMB command select and enable clock output on lemo 1 input (TODO)
	3..2 (r/w)	FEMB internal clock select??? (TODO)
SBND R5	0x5	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 **16** 15 14 13 12 11 10 9 8 **7 6 5 4 3 2 1 0**
	7..0 (r/w)	power measure select (TODO)
	16 (r/w)	power measure start (TODO)
SBND R6	0x6	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r)	power measurements (TODO)
SBND R7	0x7	**31** 30 29 28 27 26 25 24 23 22 21 20 **19 18 17 16** 15 14 13 12 **11 10 9 8** 7 6 5 4 **3 2 1 0**
	31 (r/w)	UDP readout disabled (TODO)
	19..16 (r/w)	UDP monitoring Board select (TODO)
	11..8 (r/w)	UDP monitoring Chip select (TODO)
	3..0 (r/w)	UDP monitoring channel select (TODO)
SBND R8	0x8	31 30 29 28 27 26 25 24 23 22 21 20 **19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0**
	0 (r/w)	Board 0 3.6V en (TODO)
	1 (r/w)	Board 0 2.8V en (TODO)
	2 (r/w)	Board 0 2.5V en (TODO)
	3 (r/w)	Board 0 1.5V en (TODO)
	4 (r/w)	Board 1 3.6V en (TODO)
	5 (r/w)	Board 1 2.8V en (TODO)
	6 (r/w)	Board 1 2.5V en (TODO)
	7 (r/w)	Board 1 1.5V en (TODO)
	8 (r/w)	Board 2 3.6V en (TODO)
	9 (r/w)	Board 2 2.8V en (TODO)
	10 (r/w)	Board 2 2.5V en (TODO)
	11 (r/w)	Board 2 1.5V en (TODO)
	12 (r/w)	Board 3 3.6V en (TODO)
	13 (r/w)	Board 3 2.8V en (TODO)
	14 (r/w)	Board 3 2.5V en (TODO)
	15 (r/w)	Board 3 1.5V en (TODO)
	16 (r/w)	Board 0 Bias en (TODO)
	17 (r/w)	Board 1 Bias en (TODO)
	18 (r/w)	Board 2 Bias en (TODO)
	19 (r/w)	Board 3 Bias en (TODO)

Register	address	
SBND R9	0x9	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 **0**
	0 (r/w)	P-Pod enable (TODO)
SBND R10	0xa	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 **1** **0**
	0 (r/w)	I2C wr strobe (TODO) (ok to make an action)
	1 (r/w)	I2c rd strobe (TODO) (ok to make an action)
SBND R11	0xb	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 **3** **2** **1** **0**
	3..0 (r/w)	i2c byte count (TODO)
SBND R12	0xc	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 **7** **6** **5** **4** **3** **2** **1** **0**
	7..0 (r/w)	i2c address (TODO)
SBND R13	0xd	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 **7** **6** **5** **4** **3** **2** **1** **0**
	7..0 (r/w)	i2c write data (TODO)

Register	address	
SBND R14	0xe	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r)	i2c read data (TODO)
SBND R15	0xf	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
SBND R16	0x10	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
SBND R17	0x11	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (r/w)	GXB analog reset (TODO)
	1 (r/w)	GXB digital reset (TODO)
SBND R18	0x12	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	3..0 (r/w)	link stat sel ? (TODO)
	8 (r/w)	TS latch ? (TODO)
	15 (r/w)	ERR cnt reset ? (TODO)
SBND R19	0x13	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Register	address	
SBND R20	0x14	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (r/w)	tx packet not enable (TODO)
	1 (r/w)	tx packet fifo
	2 (r/w)	tx analog reset
	3 (r/w)	tx digital reset
	4 (r/w)	tx pll powerdown enable?
SBND R21	0x15	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r/w)	comma sequence (TODO)
	17..16 (r/w)	comm sequence k-char bits
SBND R22	0x16	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
SBND R23	0x17	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
SBND R24	0x18	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Register	address																														
SBND R25	0x19	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBND R26	0x1a	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBND R27	0x1b	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBND R28	0x1c	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBND R29	0x1d	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Register	address	
SBND R30	0x1e	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
SBND R31	0x1f	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
WIB STATUS	0x100	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (a)	global reset
	1 (a)	control register reset
	2 (a)	UDP reset
	3 (a)	DAQ-path reset
	4 (r)	sys locked
	5 (r)	FEMB locked
	6 (r)	EB locked
	8 (r/w)	DUNE clk sel
	9 (r)	DUNE clk locked
	27..24 (r)	DAQ Link count
	31..28 (r)	FEMB count
WIB FW VERSION	0x101	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	7..0 (r)	rev (1-99) Manually updated
	15..8 (r)	day (1-31) Manually updated
	23..16 (r)	month (1-12) Manually updated
	31..24 (r)	year (20XX) Manually updated
WIB SYNTH DATE	0x102	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	7..0 (r)	day (1-31) automatically updated
	15..8 (r)	month (1-12) automatically updated
	23..16 (r)	year (00-99) automatically updated
	31..24 (r)	century (20) automatically updated

Register	address	
WIB SYNTH TIME	0x103	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	7..0 (r)	second (00-59) automatically updated
	15..8 (r)	minute (00-59) automatically updated
	23..16 (r)	hour (00-23) automatically updated
WIB ID	0x104	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	3..0 (r)	Slot number
	7..4 (r)	Crate number
	8 (r/w)	Use fake slot/crate
	19..16 (r/w)	Fake slot number
	23..20 (r/w)	Fake crate number
	27..24 (r/w)	Real slot number
	31..28 (r/w)	Real crate number
UDP CTRL	0x110	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (r/w)	enable readback
UDP TIMEOUT	0x111	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/w)	udp timeout
UDP DEST IP	0x112	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r)	destination IP
UDP DEST MAC LO	0x113	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r)	destination MAC[31..0]

Register	address	
UDP DEST MAC HI	0x114	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r)	destination MAC[47..32]
UDP DEST PORT	0x115	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r)	destination port
LFLASH CTRL	0x120	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (a)	run
	1 (r/w)	r/w
	2 (r)	done
	3 (r)	error
	4 (a)	reset
	31..16 (r/w)	address
LFLASH WRITE	0x121	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/w)	data
LFLASH READ	0x122	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r)	data

Register	address	
TS CTRL	0x130	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (a)	start
	1 (r)	busy
TS DATA	0x131	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r)	temp data
DTS CTRL	0x200	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	1 (r/w)	PDTS enable
	2 (r/w)	PDTS resetter enabled
	3 (r/w)	PDTS resetter counter reset
	4 (r/w)	PDTS data clk reset
	5 (r)	PDTS data clock locked
	8 (r/w)	tx ouput enable
	9 (r/w)	tx output rx data
	10 (r)	clk DUNE in reset
	11 (r)	clk DUNE in locked
	13..12 (r/w)	PDTS timing group
	19..16 (r)	PDTS state
DTS RESET COUNT	0x201	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	23..0 (r)	reset count
DTS EVENT COUNT	0x202	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r)	event count

Register	address	
DTS TIME LSB	0x203	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r)	time stamp 31..0
DTS TIME MSB	0x204	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r)	time stamp 63..32
DTS CONVERT CONTROL	0x205	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (r/w)	converts enabled
	1 (r)	out of sync
	2 (r/w)	local timestamp
	3 (r/w)	enable fake DTS
	4 (r/w)	halt
	5 (a)	start sync
	11..8 (r)	state
DTS CONVERT SYNC PERIOD	0x206	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/w)	convert period in 50Mhz clock ticks
DTS CONVERT LAST SYNC LSB	0x207	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r)	last good convert time 31..0

Register	address	
DTS CONVERT LAST SYNC MSB	0x208	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r)	last good convert time 63..32
DTS CONVERT MISSED SYNCS	0x209	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/w)	count of missed syncs
DTS CONVERT BLAME	0x20a	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r)	blame
PDTS RESETTER COUNT	0x20b	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r)	count of resetter resets
PDTS WORDS	0x20c	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	8..0 (r)	current 8b word from PDTS
	25..16 (r)	current 10b word from PDTS
DTS CDS Control	0x210	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (r/w)	input select (FP/BP)
	2 (r)	LOL
	3 (r)	LOS

Register	address	
DTS CDS I2C Control	0x212	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (a)	run
	1 (r/w)	r/w
	2 (r)	busy
	3 (r)	available
	4 (a)	reset
	11..8 (r/w)	byte count
	23..16 (r/w)	address
DTS CDS I2C WR DATA	0x213	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/w)	write data
DTS CDS I2C RD DATA	0x214	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r)	read data
DTS SI5344 Control	0x220	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (r/w)	enable
	1 (r/w)	reset
	2 (r)	LOL
	3 (r)	LOS
	4 (r)	interrupt
	9..8 (r/w)	input select
DTS SI5344 I2C Control	0x222	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (a)	run
	1 (r/w)	r/w
	2 (r)	busy
	3 (r)	available
	4 (a)	reset
	11..8 (r/w)	byte count
	23..16 (r/w)	address

Register	address	
DTS SI5344 I2C WR DATA	0x223	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/w)	write data
DTS SI5344 I2C RD DATA	0x224	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r)	read data
DTS SI5344 RST REQ	0x225	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	reset requests
DTS SI5344 RST PERF	0x226	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	resets performed

Register	address	
DTS SYNC CMD CONTROL	0x235	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r/w)	counter reset
DTS SYNC CMD COUNT 0	0x240	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/w)	count
DTS SYNC CMD COUNT 1	0x241	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/w)	count
DTS SYNC CMD COUNT 2	0x242	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/w)	count
DTS SYNC CMD COUNT 3	0x243	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/w)	count

Register	address	
DTS SYNC CMD COUNT 4	0x244	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/w)	count
DTS SYNC CMD COUNT 5	0x245	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/w)	count
DTS SYNC CMD COUNT 6	0x246	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/w)	count
DTS SYNC CMD COUNT 7	0x247	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/w)	count
DTS SYNC CMD COUNT 8	0x248	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/w)	count

Register	address	
DTS SYNC CMD COUNT 9	0x249	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/w)	count
DTS SYNC CMD COUNT 10	0x24a	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/w)	count
DTS SYNC CMD COUNT 11	0x24b	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/w)	count
DTS SYNC CMD COUNT 12	0x24c	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/w)	count
DTS SYNC CMD COUNT 13	0x24d	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/w)	count

Register	address	
DTS SYNC CMD COUNT 14	0x24e	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/w)	count
DTS SYNC CMD COUNT 15	0x24f	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/w)	count
DQM CTRL	0x800	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (r/w)	enable DQM packets
	7..4 (r/w)	DQM type (Modes: 0x0:Jack, 0x1:testing)
DQM CD SS	0x801	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (r/w)	stream number
	1 (r/w)	CD number
	3..2 (r/w)	FEMB number
	4 (r/w)	sub stream number (for jack mode)
FEMB POWER CONTROL	0x400	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (r/w)	FEMB 1 EN 3.6 V
	1 (r/w)	FEMB 1 EN 2.8 V
	2 (r/w)	FEMB 1 EN 2.5 V
	3 (r/w)	FEMB 1 EN 1.5 V
	4 (r/w)	FEMB 1 EN Bias V
	12..8 (r/w)	FEMB 2 Power Enables
	20..16 (r/w)	FEMB 3 Power Enables
	28..24 (r/w)	FEMB 4 Power Enables
	31 (r/w)	Master bias enable

Register	address	
FEMB POWER MON CONTROL	0x401	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (r/w)	reset
FEMB BIAS MON	0x402	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r)	Bias Vcc
	31..16 (r)	bias temp
FEMB FE MON	0x403	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r)	FE Vcc
	31..16 (r)	FE temp
FEMB 1 MON 0	0x410	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r)	Bias Vcc
	31..16 (r)	bias temp
FEMB 1 MON 1	0x411	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r)	Voltage
	31..16 (r)	Current
FEMB 1 MON 2	0x412	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r)	Voltage
	31..16 (r)	Current

Register	address	
FEMB 1 MON 3	0x413	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r)	Voltage
	31..16 (r)	Current
FEMB 1 MON 4	0x414	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r)	Voltage
	31..16 (r)	Current
FEMB 1 MON 5	0x415	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r)	Voltage
	31..16 (r)	Current
FEMB 1 MON 6	0x416	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r)	Voltage
	31..16 (r)	Current
FEMB 2 MON 0	0x420	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r)	Bias Vcc
	31..16 (r)	bias temp

Register	address																														
FEMB 2 MON 1	0x421	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	15..0 (r)	Voltage																															
	31..16 (r)	Current																															
FEMB 2 MON 2	0x422	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	15..0 (r)	Voltage																															
	31..16 (r)	Current																															
FEMB 2 MON 3	0x423	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	15..0 (r)	Voltage																															
	31..16 (r)	Current																															
FEMB 2 MON 4	0x424	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	15..0 (r)	Voltage																															
	31..16 (r)	Current																															
FEMB 2 MON 5	0x425	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	15..0 (r)	Voltage																															
	31..16 (r)	Current																															

Register	address	
FEMB 2 MON 6	0x426	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r)	Voltage
	31..16 (r)	Current
FEMB 3 MON 0	0x430	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r)	Bias Vcc
	31..16 (r)	bias temp
FEMB 3 MON 1	0x431	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r)	Voltage
	31..16 (r)	Current
FEMB 3 MON 2	0x432	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r)	Voltage
	31..16 (r)	Current
FEMB 3 MON 3	0x433	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r)	Voltage
	31..16 (r)	Current

Register	address	
FEMB 3 MON 4	0x434	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r)	Voltage
	31..16 (r)	Current
FEMB 3 MON 5	0x435	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r)	Voltage
	31..16 (r)	Current
FEMB 3 MON 6	0x436	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r)	Voltage
	31..16 (r)	Current
FEMB 4 MON 0	0x440	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r)	Bias Vcc
	31..16 (r)	bias temp
FEMB 4 MON 1	0x441	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r)	Voltage
	31..16 (r)	Current
FEMB 4 MON 2	0x442	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r)	Voltage
	31..16 (r)	Current

Register	address	
FEMB 4 MON 3	0x443	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r)	Voltage
	31..16 (r)	Current
FEMB 4 MON 4	0x444	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r)	Voltage
	31..16 (r)	Current
FEMB 4 MON 5	0x445	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r)	Voltage
	31..16 (r)	Current
FEMB 4 MON 6	0x446	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r)	Voltage
	31..16 (r)	Current
WIB MON 0	0x450	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r)	Bias Vcc
	31..16 (r)	bias temp

Register	address	
WIB MON 1	0x451	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r)	Voltage
	31..16 (r)	Current
WIB MON 2	0x452	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r)	Voltage
	31..16 (r)	Current
WIB MON 3	0x453	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r)	Voltage
	31..16 (r)	Current
WIB MON 4	0x454	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r)	Voltage
	31..16 (r)	Current
FEMB CNC	0x500	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (r/w)	CnC Clock Select (0 DTS,1 local)
	1 (r/w)	CnC Command Select
	2 (r/w)	Enable converts
	3 (r)	convert going down to FEMB
	4 (r/w)	DTS 100Mhz reset
	5 (r)	DTS 100Mhz locked
	8 (a)	stop femb data
	9 (a)	start femb data

Register	address	
FEMB SPY CONTROL	0x900	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	3..0 (r/w)	stream id
	4 (r/w)	ext en
	5 (r/w)	word en
	8 (r)	fifo empty
	20..12 (r/w)	word trig value
	31..30 (r)	spy state
FEMB SPY ARM	0x901	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (a)	arm spy buffer
	1 (a)	software trigger
FEMB SPY readout	0x902	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	8..0 (r/a)	spy data
FEMB 1 CONTROL	0x1000	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (r/w)	reset
	1 (r/w)	reconfigure reset
	7..4 (r/w)	enable processing link 4..1
FEMB 1 TRIGGER	0x1001	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	7..0 (r/w)	convert delay CD1.1
	15..8 (r/w)	convert delay CD1.2
	23..16 (r/w)	convert delay CD2.1
	31..24 (r/w)	convert delay CD2.2

Register	address	
FEMB 1 FAKE CD	0x1010	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (r/w)	fake COLDATA ASIC 1 sample data type 0/1 (samples/bytes)
	1 (r/w)	fake COLDATA ASIC 2 sample data type 0/1 (samples/bytes)
	2 (r/w)	fake COLDATA ASIC 1 data type 1 =¿ (CD packet is SOF+counter)
	3 (r/w)	fake COLDATA ASIC 2 data type 1 =¿ (CD packet is SOF+counter)
	7..4 (r/w)	RX data source (0 transceiver, 1 local fake data)
	11..8 (r/w)	TX data stream (0 idle, 1 fake COLDATA)
FEMB 1 FAKE CD 1 1 PACKETS	0x1011	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r)	fake COLDATA ASIC 1 stream 1 packets
FEMB 1 FAKE CD 1 2 PACKETS	0x1012	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r)	fake COLDATA ASIC 1 stream 2 packets
FEMB 1 FAKE CD 2 1 PACKETS	0x1013	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r)	fake COLDATA ASIC 1 stream 1 packets
FEMB 1 FAKE CD 2 2 PACKETS	0x1014	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r)	fake COLDATA ASIC 1 stream 2 packets
FEMB 1 FAKE CD RESERVED WORD	0x1015	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	15..0 (r/w)	reserved word CD 1
	31..16 (r/w)	reserved word CD 2

Register	address	
FEMB 1 FAKE CD 1 HEADER WORD	0x1016	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/w)	header words CD1
FEMB 1 FAKE CD 2 HEADER WORD	0x1017	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/w)	header words CD2
FEMB 1 FAKE CD ERR INJ	0x1020	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (a)	inject set errors on next event
FEMB 1 FAKE CD 1 ERR INJ	0x1021	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (r/w)	stream 1 bad checksum
	1 (r/w)	stream 1 bad SOF char
	2 (r/w)	stream 1 large frame
	3 (r/w)	stream 1 small frame
	4 (r/w)	stream 1 k-char in data
	15..8 (r/w)	stream 1 CD error word
	16 (r/w)	stream 2 bad checksum
	17 (r/w)	stream 2 bad SOF char
	18 (r/w)	stream 2 large frame
	19 (r/w)	stream 2 small frame
	20 (r/w)	stream 2 k-char in data
	31..24 (r/w)	stream 2 CD error word
FEMB 1 FAKE CD 2 ERR INJ	0x1022	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (r/w)	stream 3 bad checksu3
	1 (r/w)	stream 3 bad SOF cha4
	2 (r/w)	stream 3 large frame
	3 (r/w)	stream 3 small frame
	4 (r/w)	stream 3 k-char in data
	15..8 (r/w)	stream 3 CD error word
	16 (r/w)	stream 4 bad checksum
	17 (r/w)	stream 4 bad SOF char
	18 (r/w)	stream 4 large frame
	19 (r/w)	stream 4 small frame
	20 (r/w)	stream 4 k-char in data
	31..24 (r/w)	stream 4 CD error word

Register	address	
FEMB 1 STR 1 STATUS	0x1100	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (r)	LOS
	1 (r)	rx calibration busy
	4 (r/w)	rx analog reset
	5 (r/w)	rx digital reset
	6 (r)	rx is locked to reference
	7 (r)	rx is locked to data
	16 (r)	rx error detected
	17 (r)	rx disparity error
	18 (r)	rx runnign disparity
	20 (r)	rx pattern detect
	21 (r)	rx sync status
	22 (r/w)	reset rx error counter
	23 (r/w)	reset rx disp error counter
FEMB 1 STR 1 PACKET COUNT	0x1101	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r)	packet count
FEMB 1 STR 1 ERR CNT RESETS	0x1150	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (a)	reset all counters for this stream
	1 (a)	reset convert in wait count
	2 (a)	reset bad sof count
	3 (a)	reset unexpetect eof count
	4 (a)	reset missing eof count
	5 (a)	reset kchar in data count
	6 (a)	reset bad checksum count
	7 (a)	reset buffer full count
	8 (a)	reset timestamp incr count
	9 (a)	reset bad write count
	10 (a)	reset bad ro start count
FEMB 1 STR 1 ERR CNT CONVERT IN WAIT	0x1151	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of converts between a convert and waiting for data(action reset)
FEMB 1 STR 1 ERR CNT BAD SOF	0x1152	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of bad start of frame characters (action reset)

Register	address	
FEMB 1 STR 1 ERR CNT UNEXPECTED EOF	0x1153	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of early idle characters (action reset)
FEMB 1 STR 1 ERR CNT MISSING EOF	0x1154	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count missing end of frame idle (action reset)
FEMB 1 STR 1 ERR CNT KCHAR IN DATA	0x1155	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count k-chars in data (action reset)
FEMB 1 STR 1 ERR CNT BAD CHSUM	0x1156	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of bad checksums (action reset)
FEMB 1 STR 1 ERR CNT BUFFER FULL	0x1157	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of events lost due to the buffer being full (action reset)

Register	address	
FEMB 1 STR 1 ERR CNT RX ERROR	0x1158	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of symbol errors on the rx
FEMB 1 STR 1 ERR CNT RX DISP ERROR	0x1159	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of disp errors on the rx
FEMB 1 STR 1 ERR CNT T INCR	0x115a	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of timestamp increment errors
FEMB 1 STR 1 ERR CNT BAD WRITE	0x115b	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of bad write counts into CD to EB fifo
FEMB 1 STR 1 ERR CNT BAD RO START	0x115c	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of CD to EB fifo readouts that don't start with a SOF character
FEMB 1 STR 2 STATUS	0x1200	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (r)	rx ready
	1 (r)	tx ready (fake)
	2 (r)	pll locked
	4 (r)	rx is locked to reference
	5 (r)	rx is locked to data
	8 (r)	pll powerdown ???
	9 (r)	reconfigure busy
	10 (r)	rx calibration busy
	11 (r)	tx calibration busy
	12 (r)	rx analog reset
	13 (r)	rx digital reset
	14 (r)	tx analog reset
	15 (r)	tx digital reset
	16 (r)	rx error detected
	17 (r)	rx disparity error
	18 (r)	rx runnign disparity
	20 (r)	rx pattern detect
	21 (r)	rx sync status
	22 (r/w)	reset rx error counter
	23 (r/w)	reset rx disp error counter

Register	address	
FEMB 1 STR 2 PACKET COUNT	0x1201	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r)	packet count
FEMB 1 STR 2 ERR CNT RESETS	0x1250	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (a)	reset all counters for this stream
	1 (a)	reset convert in wait count
	2 (a)	reset bad sof count
	3 (a)	reset unexpetect eof count
	4 (a)	reset missing eof count
	5 (a)	reset kchar in data count
	6 (a)	reset bad checksum count
	7 (a)	reset buffer full count
	8 (a)	reset timestamp incr count
	9 (a)	reset bad write count
	10 (a)	reset bad ro start count
FEMB 1 STR 2 ERR CNT CONVERT IN WAIT	0x1251	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of converts between a convert and waiting for data(action reset)
FEMB 1 STR 2 ERR CNT BAD SOF	0x1252	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of bad start of frame characters (action reset)
FEMB 1 STR 2 ERR CNT UNEXPECTED EOF	0x1253	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of early idle characters (action reset)

Register	address	
FEMB 1 STR 2 ERR CNT MISSING EOF	0x1254	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count missing end of frame idle (action reset)
FEMB 1 STR 2 ERR CNT KCHAR IN DATA	0x1255	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count k-chars in data (action reset)
FEMB 1 STR 2 ERR CNT BAD CHSUM	0x1256	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of bad checksums (action reset4
FEMB 1 STR 2 ERR CNT BUFFER FULL	0x1257	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of events lost due to the buffer being full (action reset)
FEMB 1 STR 2 ERR CNT RX ERROR	0x1258	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of symbol errors on the rx

Register	address	
FEMB 1 STR 2 ERR CNT RX DISP ERROR	0x1259	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of disp errors on the rx
FEMB 1 STR 2 ERR CNT T INCR	0x125a	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of timestamp increment errors
FEMB 1 STR 2 ERR CNT BAD WRITE	0x125b	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of bad write counts into CD to EB fifo
FEMB 1 STR 2 ERR CNT BAD RO START	0x125c	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of CD to EB fifo readouts that don't start with a SOF character
FEMB 1 STR 3 STATUS	0x1300	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (r)	rx ready
	1 (r)	tx ready (fake)
	2 (r)	pll locked
	4 (r)	rx is locked to reference
	5 (r)	rx is locked to data
	8 (r)	pll powerdown ???
	9 (r)	reconfigure busy
	10 (r)	rx calibration busy
	11 (r)	tx calibration busy
	12 (r)	rx analog reset
	13 (r)	rx digital reset
	14 (r)	tx analog reset
	15 (r)	tx digital reset
	16 (r)	rx error detected
	17 (r)	rx disparity error
	18 (r)	rx runnign disparity
	20 (r)	rx pattern detect
	21 (r)	rx sync status
	22 (r/w)	reset rx error counter
	23 (r/w)	reset rx disp error counter

Register	address	
FEMB 1 STR 3 PACKET COUNT	0x1301	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r)	packet count
FEMB 1 STR 3 ERR CNT RESETS	0x1350	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (a)	reset all counters for this stream
	1 (a)	reset convert in wait count
	2 (a)	reset bad sof count
	3 (a)	reset unexpetect eof count
	4 (a)	reset missing eof count
	5 (a)	reset kchar in data count
	6 (a)	reset bad checksum count
	7 (a)	reset buffer full count
	8 (a)	reset timestamp incr count
	9 (a)	reset bad write count
	10 (a)	reset bad ro start count
FEMB 1 STR 3 ERR CNT CONVERT IN WAIT	0x1351	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of converts between a convert and waiting for data(action reset)
FEMB 1 STR 3 ERR CNT BAD SOF	0x1352	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of bad start of frame characters (action reset)
FEMB 1 STR 3 ERR CNT UNEXPECTED EOF	0x1353	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of early idle characters (action reset)
FEMB 1 STR 3 ERR CNT MISSING EOF	0x1354	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count missing end of frame idle (action reset)

Register	address	
FEMB 1 STR 3 ERR CNT KCHAR IN DATA	0x1355	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count k-chars in data (action reset)
FEMB 1 STR 3 ERR CNT BAD CHSUM	0x1356	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of bad checksums (action reset)
FEMB 1 STR 3 ERR CNT BUFFER FULL	0x1357	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of events lost due to the buffer being full (action reset)
FEMB 1 STR 3 ERR CNT RX ERROR	0x1358	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of symbol errors on the rx
FEMB 1 STR 3 ERR CNT RX DISP ERROR	0x1359	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of disp errors on the rx

Register	address	
FEMB 1 STR 3 ERR CNT T INCR	0x135a	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of timestamp increment errors
FEMB 1 STR 3 ERR CNT BAD WRITE	0x135b	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of bad write counts into CD to EB fifo
FEMB 1 STR 3 ERR CNT BAD RO START	0x135c	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of CD to EB fifo readouts that don't start with a SOF character
FEMB 1 STR 4 STATUS	0x1400	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (r)	rx ready
	1 (r)	tx ready (fake)
	2 (r)	pll locked
	4 (r)	rx is locked to reference
	5 (r)	rx is locked to data
	8 (r)	pll powerdown ???
	9 (r)	reconfigure busy
	10 (r)	rx calibration busy
	11 (r)	tx calibration busy
	12 (r)	rx analog reset
	13 (r)	rx digital reset
	14 (r)	tx analog reset
	15 (r)	tx digital reset
	16 (r)	rx error detected
	17 (r)	rx disparity error
	18 (r)	rx runnign disparity
	20 (r)	rx pattern detect
	21 (r)	rx sync status
	22 (r/w)	reset rx error counter
	23 (r/w)	reset rx disp error counter
FEMB 1 STR 4 PACKET COUNT	0x1401	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r)	packet count

Register	address	
FEMB 1 STR 4 ERR CNT RESETS	0x1450	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (a)	reset all counters for this stream
	1 (a)	reset convert in wait count
	2 (a)	reset bad sof count
	3 (a)	reset unexpetect eof count
	4 (a)	reset missing eof count
	5 (a)	reset kchar in data count
	6 (a)	reset bad checksum count
	7 (a)	reset buffer full count
	8 (a)	reset timestamp incr count
	9 (a)	reset bad write count
	10 (a)	reset bad ro start count
FEMB 1 STR 4 ERR CNT CONVERT IN WAIT	0x1451	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of converts between a convert and waiting for data(action reset)
FEMB 1 STR 4 ERR CNT BAD SOF	0x1452	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of bad start of frame characters (action reset)
FEMB 1 STR 4 ERR CNT UNEXPECTED EOF	0x1453	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of early idle characters (action reset)
FEMB 1 STR 4 ERR CNT MISSING EOF	0x1454	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count missing end of frame idle (action reset)

Register	address	
FEMB 1 STR 4 ERR CNT KCHAR IN DATA	0x1455	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count k-chars in data (action reset)
FEMB 1 STR 4 ERR CNT BAD CHSUM	0x1456	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of bad checksums (action reset)
FEMB 1 STR 4 ERR CNT BUFFER FULL	0x1457	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of events lost due to the buffer being full (action reset)
FEMB 1 STR 4 ERR CNT RX ERROR	0x1458	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of symbol errors on the rx
FEMB 1 STR 4 ERR CNT RX DISP ERROR	0x1459	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of disp errors on the rx
FEMB 1 STR 4 ERR CNT T INCR	0x145a	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of timestamp increment errors

Register	address	
FEMB 1 STR 4 ERR CNT BAD WRITE	0x145b	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of bad write counts into CD to EB fifo
FEMB 1 STR 4 ERR CNT BAD RO START	0x145c	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	Count of CD to EB fifo readouts that don't start with a SOF character
DAQ CONTROL	0x5000	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (r/w)	reset
	1 (r/w)	reconfigure reset
DAQ QSFP CONTROL	0x5001	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (r/w)	reset
	1 (r/w)	low power mode
	4 (r)	present
	5 (r)	interrupt
DAQ QSFP I2C Control	0x5002	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (a)	run
	1 (r/w)	r/w
	2 (r)	busy
	3 (r)	available
	11..8 (r/w)	byte count
	23..16 (r/w)	address

Register	address	
DAQ QSFP I2C WR DATA	0x5003	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/w)	write data
DAQ QSFP I2C RD DATA	0x5004	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r)	read data
DAQ SI5342 Control	0x5010	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (r/w)	enable
	1 (r/w)	reset
	2 (r)	LOL
	3 (r)	LOS XAXB
	4 (r)	interrupt
	7..5 (r)	LOS
	9..8 (r/w)	input select
DAQ SI5342 I2C Control	0x5011	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (a)	run
	1 (r/w)	r/w
	2 (r)	busy
	3 (r)	available
	4 (a)	reset
	11..8 (r/w)	byte count
	23..16 (r/w)	address
DAQ SI5342 I2C WR DATA	0x5012	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/w)	write data

Register	address	
DAQ SI5342 I2C RD DATA	0x5013	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r)	read data
DAQ RX	0x5014	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (r/w)	analog reset
	1 (r/w)	digital reset
	2 (r)	locked to ref
	3 (r)	locked to data
	4 (r)	cal busy
DAQ LINK 1 CONTROL	0x5100	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (r/w)	daq-linke-enabled
	1 (r/w)	cd debug mode (0 off, 1 on)
	9..8 (r)	fiber number
	19..16 (r)	FEMB mask
	31..24 (r/w)	CD Stream enable
DAQ LINK 1 STREAM STATUS	0x5101	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (r/w)	tx reset
	1 (r/w)	tx pll powerdown
	2 (r/w)	tx analog reset
	3 (r/w)	tx digital reset
	4 (r)	tx pll locked
DAQ LINK 1 EVENT COUNT	0x5102	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	event counter (reset)

Register	address	
DAQ LINK 1 DEBUG	0x5103	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (r/w)	debug mode enable
	1 (r/w)	debug send bad crcs
	31..16 (r/w)	bad crc mask and comp.
DAQ LINK 1 MISMATCH COUNT	0x5104	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	mismatch count (reset)
DAQ LINK 1 SPY BUFFER CONTROL	0x5110	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (a)	spy buffer start
	1 (r/w)	wait for trigger mode
	2 (r)	spy buffer empty
	3 (r)	spy buffer capturing data
DAQ LINK 1 SPY BUFFER READOUT DATA	0x5111	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	data characters
DAQ LINK 1 SPY BUFFER READOUT KDATA	0x5112	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	3..0 (r)	k-data bits
DAQ LINK 1 RX STREAM STATUS	0x5151	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (r)	rx ready
	1 (r)	rx analog reset
	2 (r)	rx digital reset
	3 (r)	rx cal busy
	4 (r)	rx is locked to ref
	5 (r)	rx is locked to data
	19..16 (r)	error detected
	23..20 (r)	running disparity
	27..24 (r)	pattern detect
	31..28 (r)	sync status

Register	address	
DAQ LINK 1 RX EVENT COUNT	0x5152	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	event counter (reset)
DAQ LINK 1 GEARBOX CTRL	0x5160	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (a)	reset all
	1 (a)	reset underflow counter
	16 (r/w)	enable counter
DAQ LINK 1 GEARBOX UNDERFLOW	0x5161	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31..0 (r/a)	counter (wr-reset)
FLASH CTRL	0xf000	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	0 (a)	run command
	2..1 (a)	command (11 erase, 01 read, 00 write,10 status)
	8 (r)	invalid write
	9 (r)	invalid erase
	16 (r)	busy
	30 (r)	reconfig busy
	31 (r/w)	reconfig
FLASH ADDRESS	0xf001	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	23..0 (r/w)	flash address

Register	address	
FLASH PAGE BYTE COUNT	0xf002	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 **7 6 5 4 3 2 1 0**
	7..0 (r/w)	byte count
FLASH STATUS	0xf003	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 **7 6 5 4 3 2 1 0**
	7..0 (r)	flash status
FLASH PAGE DATA START	0xf080	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31 ..0	(r/w) data to write to queue for flash write
FLASH PAGE DATA END	0xf0ff	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	31 ..0	(r/w) data to write to queue for flash write

Register	address																														
REG TEST 0	0xfff0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	31..0 (r/w)	test																															
REG TEST 1	0xfff1	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	31..0 (r/w)	test																															
REG TEST 2	0xfff2	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	31..0 (r/w)	test																															
REG TEST 3	0xfff3	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	31..0 (r/w)	test																															
REG TEST 4	0xfff4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	31..0 (r/w)	test																															

Register	address																														
REG TEST 5	0xfff5	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	31..0 (r/w)	test																															
REG TEST 6	0xfff6	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	31..0 (r/w)	test																															
REG TEST 7	0xfff7	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	31..0 (r/w)	test																															
REG LOCKED	0xfffc	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	6..0 (r)	clock domain locked																															
REG RD COUNT	0xfffd	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	31..0 (r/w)	register reads																															

Register	address																															
REG WR COUNT	0xfffe	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	31..0 (r/w)	register write																														