ID	Name	Description	Rationale	Design Validation	Verification Method
LRO-001	ADC Sampling rate	ADC sampling rate shall be at least 100 MegaSamples/s (10 ns time stamp)	Since we have long LAr pulses reasonable sampling frequency is 100-200 MS/s	Design	Design
LRO-002	ADC Synchronization	Synchronization of ADC modules shall be < 1 ns	It is important to match signals from different ADC modules to provide fine time resolution and for Charge-Light data merging	Design	2 x 2, Full Scale Demonstrator
LRO-003	ArCLight Light threshold	ArcLight Module shall be triggered when there is greater than > 20 photoelectrons	Signal to noise ratio allocated by system	Module testing	2 x 2, Full Scale Demonstrator
LRO-006	LCM Light threshold	LCM Module shall be triggered by > 10 photoelectrons	Signal to noise ratio allocated by system	Design	2 x 2, Full Scale Demonstrator
LRO-007	Time Stamp	Time stamp resolution shall be < 10 ns	Provides absolute time stamp when running ADC	Eng Analysis	2 x 2, Full Scale Demonstrator
LRO-008	Pileups time resolution	LRO shall be able to resolve 2 signals separated by > 200ns	This specification, in combination with LRO-12, should provide the required efficiency and accuracy in charge-light signal matching.	2 x 2 & ScSims	2 x 2 & ScSims
LRO-009	Time resolution of the LRO	The time resolution of the photon detection system to resolve neutrino interaction time shall be < 10ns	This specification, in combination with LRO-12, should provide the required efficiency and accuracy in charge-light signal matching.	Sc Sims, Full Scale Demonstrator	Full Scale Demonstrator