Name	Description	Rationale	Design Validation	Verification Method
ADC Sampling rate	ADC sampling rate shall be at least 100 MegaSamples/s (10 ns time stamp)	Since we have long LAr pulses reasonable sampling frequency is 100-200 MS/s	Design	Design
ADC Synchronizat ion	Synchronization of ADC modules shall be < 1 ns	It is important to match signals from different ADC modules to provide fine time resolution and for Charge-Light data merging	Design	2 x 2, Full Scale Demonstra- tor
ArCLight Light threshold	ArcLight Module shall be triggered when there is greater than > 20 photoelectrons	Signal to noise ratio allocated by system	Module testing	2 x 2, Full Scale Demonstra- tor
LCM Light threshold	LCM Module shall be triggered by > 10 photoelectrons	Signal to noise ratio allocated by system	Design	2 x 2, Full Scale Demonstra- tor
Time Stamp	Time stamp resolution shall be < 10 ns	Provides absolute time stamp when running ADC	Eng Analysis	2 x 2, Full Scale Demonstra- tor
Pileups time resolution	LRO shall be able to resolve 2 signals separated by > 200ns	This specification, in combination with LRO-12, should provide the required efficiency and accuracy in charge-light signal matching.	2 x 2 & ScSims	2 x 2 & ScSims
Time resolution of the LRO	The time resolution of the photon detection system to resolve neutrino interaction time shall be < 10ns	This specification, in combination with LRO-12, should provide the required efficiency and accuracy in charge-light signal matching.	Sc Sims, Full Scale Demonstra- tor	Full Scale Demonstra- tor
	ADC Sampling rate ADC Synchronizat ion ArCLight Light threshold LCM Light threshold Time Stamp Pileups time resolution Time resolution of	ADC Sampling rate shall be at least 100 MegaSamples/s (10 ns time stamp) ADC Synchronizat Synchronization of ADC modules shall be < 1 ns ion ArCLight Light threshold Photoelectrons LCM Module shall be triggered by > 10 photoelectrons LCM Stamp Stamp resolution shall be < 10 ns Pileups time resolution of the photon detection system to resolve neutrino interaction time	ADC Sampling rate shall be at least 100 MegaSamples/s (10 ns time stamp) ADC Synchronization of ADC modules shall be < 1 ns ArcLight Light Light Light Light Light Light threshold LCM Light threshold LCM Light threshold LCM Stamp LCM Light Light threshold LCM Light threshold LCM Light LCM Module shall be triggered when there is greater than > 20 photoelectrons Signal to noise ratio allocated by system Frovides absolute time stamp when running ADC This specification, in combination with LRO-12, should provide the required efficiency and accuracy in charge-light signal matching. This specification, in combination with LRO-12, should provide the required efficiency and accuracy in charge-light signal matching. This specification, in combination with LRO-12, should provide the required efficiency and accuracy in charge-light signal hall be < 10ns This specification, in combination with LRO-12, should provide the required efficiency and accuracy in charge-light signal	ADC Sampling rate shall be at least 100 MegaSamples/s (10 ns time stamp) ADC Synchronization of ADC modules shall be < 1 ns in Module shall be triggered when there is greater than > 20 photoelectrons LCM Light threshold LCM Module shall be < 10 ns Time Stamp LRO shall be able to resolve 2 signals separated by > 200ns Time Stamp Time time resolution of the photon detection resolution of the Poloton detection shall be < 10 ns ArcLight triggered when there is greater than > 20 photoelectrons Time Stamp Time stamp resolution shall be triggered by > 10 photoelectrons The time resolution of the photon detection resolution of the photon detection resolution of the LRO Time Stamp The time resolution of the photon detection resolution in combination with LRO-12, should provide the required system to resolve efficiency and accuracy in combination with LRO-12, should provide the required system to resolve efficiency and accuracy in combination with LRO-12, should provide the required shoul