ADC ASIC5

Status

5/3/2013 : Functionality check done at room temperature. Functionality check done at cold temperature. More in detail on cold temperature tests will follow.

Introduction

This 16-channel analog to digital converter ASIC (ADC ASIC) is designed to digitize with a resolution of 10-12 bits the charge signals from the Liquid Argon Time projection chamber at a rate up to 2 MS/s and multiplex 8:1 or 16:1 and serialize the data to a LVDS IO for readout through FPGA.

- **Analog to Digital Converters (ADC)** : 16
  - Input buffer with offset compensation
  - 12-bit ADC
  - Bias generator
  - Pattern generator: Selectable internal or external clock source.
  - Input Signal Range: 1.4 V (0.2~1.6V)
  - Input impedance > 10 MΩ
  - Input Capacitance ~ 1pF + 1pF (package capacitance)
- **First in First out (FIFO)**
  - 32 bit wide (Storage of 32 samples)
  - 192 bit long (16 channels * 12 bits)
  - FIFO Full indicator flag
  - FIFO empty indicator flag
- **Power**
  - ADC : ~ 3.6 mW/ch
  - Input buffer: ~ 1.28mW/ch
  - FIFO: ~ 1mW
  - Other Circuitry: ~ 0.8 mW + 66 µW
- **Layout size** 4.3 × 6.0 mm²
- **Die cut size** 4.5 × 6.1 mm²
- **Pad count, size, pitch** 80, 78.04 × 78.04 µm², 192 µm (top/bottom) and 279 µm (sides)
- **Technology** : CMOS 0.18µm – 1.8V, 1-poly, 6-metal, MiM cap, sil blk resistors

Description

- The ASIC is composed of 2 parts, the ADC and the FIFO.
  - The 16 ADCs have input buffers which convert voltage to current. The input buffer first samples the input signal (with a range of 0.2 V to 1.6 V), then provides a current output after compensating for offset voltage error. This current output is then supplied to the ADC which converts the input to digital in two phases. The MSB 6 bits are first determined followed by the LSB 6 bits. After the conversion the thermometer code is converted to binary and latched. The output of ADC 16 can be monitored externally.
  - The data from the 16 ADCs is transferred parallelly to the FIFO block (192 bits wide by 32 deep). Data is written to the FIFO on the rising edge of the internal write clock when bit F1 = 0. For test purposes the FIFO write clock is on pin IdxMp/n when bit F1 = 1.
  - After three write cycles the empty flag goes low.
  - On the rising edge of SYNC, a block of data is latched from the FIFO into the output shift register in one clock cycle (two falling edges of CLK). On subsequent falling edges of CLK, data is shifted out of the output shift register MSB first on pins O16p/n and O8p/n. On the falling edge of SYNC the read address is incremented.
  - A block of data is comprised of 200 bits. After 100 clock cycles, the upper 100 bits are shifted out on pin O16p/n and the lower 100 bits on pin O8p/n. The four MSBs of each block is the header 1010.
- The ADC along with the input buffers are biased internally using a bias generator and a bangap voltage reference. The bangap voltage (VBGR) can be monitored and/or controlled externally.

- Multiple options are available to provide the ASIC signals for conversion. These options can be accessed by programming the appropriate bits in the shift register. Description of these options is given below Table 1.
- A power down (PD) feature is used to put the ADC into sleep mode so that very low power is consumed when the ADC is idle.
- A global reset signal can be generated in the ASIC to reset all latches in the ADC and the FIFO. Table 2 illustrates the generation of a global reset signal. When the CLK signal is high, if the Chip Select (CS) signal goes low, the global reset low is generated. The table also indicates that the different combinations of CS, SDI and CK_STRB are used for different purposes. When the chip select is high it acts as a clock feeding the shift registers.
- The ADC has a set of DC current sinks which absorb constant offset current from the sample and hold. The amount of current absorbed is controlled by switches which are in turn controlled by 4 signals. The amount of offset current can be varied from 0 to 256 μA in 16 steps of 16 μA each.
- Each ADC has a set of 8 registers which contain bits that control signals in the ADC. These are PD and 3 bits of the decoder that control the offset current. More details of the register map are given in Table 1. In addition to the channel register there is a set of 8 global registers. These bits control the clock generator, the enable for the offset and the output enable signal for the ADC 16 output pads.
- The operation of the shift registers is as follows.
    - Data is shifted into the load shift register on the rising edge of CK while CS is high.
    - The MSB is shifted into position D0 on the first rising edge of CK.
    - The LSB is shifted into position D0 on the 8th rising edge of CK.
    - The MSB is shifted out of SDO on the 9th rising edge of CK.
    - The LSB is shifted out of SDO on the 16th rising edge of CK.
    - NOTE: The default value of each register is 00.

Table 1. Channel and Global Register Map

	S0	S1	S2	S3	S4	S5	S6	S7	S8
Channel	D0	D1	D2	D3	PCSR	PDSR	SLP	TSTIN	NA
Global	RES	F1	CLK0	CLK1	FRQC	EN_GR	RES	F2	RES

D0-D3: Decoded into 16 signals decides the amount of offset current to be drawn from the sample and hold.
PCSR: '1' = PD can be controlled externally. '0'= PD is controlled by PDSR
PDSR: If PCSR is 0, '1'=PD is set high. '0'=PD is set low.
SLP: '1'=ADC is in sleep mode. '0'=ADC is operating normally.
TSTIN: '1'=Test input is digitized '0'=FE Input is digitized
FRQC: Frequency of internal clock generator '1'=2 MHz '0'=1 MHz
EN_GR: '0'= Disables offset current absorption. '1'=Enables the offset current absorption.
The description of F2, F1, CLK0 and CLK1 and the are given in *Table 2.*

Table 2. Clock generation settings

1. Register Bits

F0 = No connect
F1 = 0, FIFO write clock is the ADC write clock. F1 =1, FIFO write clock is on pin IdxMp/n.
F2 = 0, FIFO clock generator = off. F2 = 1, FIFO clock generator = on.

2. Input Pins

CS	**SDI**	**CK_STRB**	**Function**	Comments
0	0	0	ADC Data	Default
0	0	1	FIFO Test	FIFO Test Pattern
0	1	x	Fifo Reset	**Priority**
1	Data	Falling Edge	Shift Data	Load Registers Serially
Falling Edge	x	0	Buffer Data	Buffer Serial Data
Falling Edge	x	1	Global Reset	**Highest Priority**

CLK1	**CLK0**	**Description**
0	0	ADC clocks from monostable
0	1	ADC external clocks
1	0	ADC clocks from digital generator of FIFO
1	1	ADC clocks from monostable

- *Figure 1* shows the order that the shift register is loaded from global to channel.

Figure 1 Shift Register Loading

- The ADC has an internal pattern generator which is based on monostables. If this feature is enabled it only needs a start of conversion signal to function. The FIFO has a digital generator which is based upon a 100 MHz clock. If the digital generator feature is enabled then, all clocks of the ADC and the FIFO can be generated by this block hence providing the ability to run both the blocks using a single signal.
- All digital inputs except the PD or power down signal are LVDS. Channels 8 and 16 of the FIFO are accessible externally.
-

- Figure 2 shows the functional block diagram of the ASIC and Figure 3 shows the timing diagram of the ADC. Figure 4 shows the FIFO timing diagram. The MSB clock of the ADC is shared with the FIFO as the write clock.

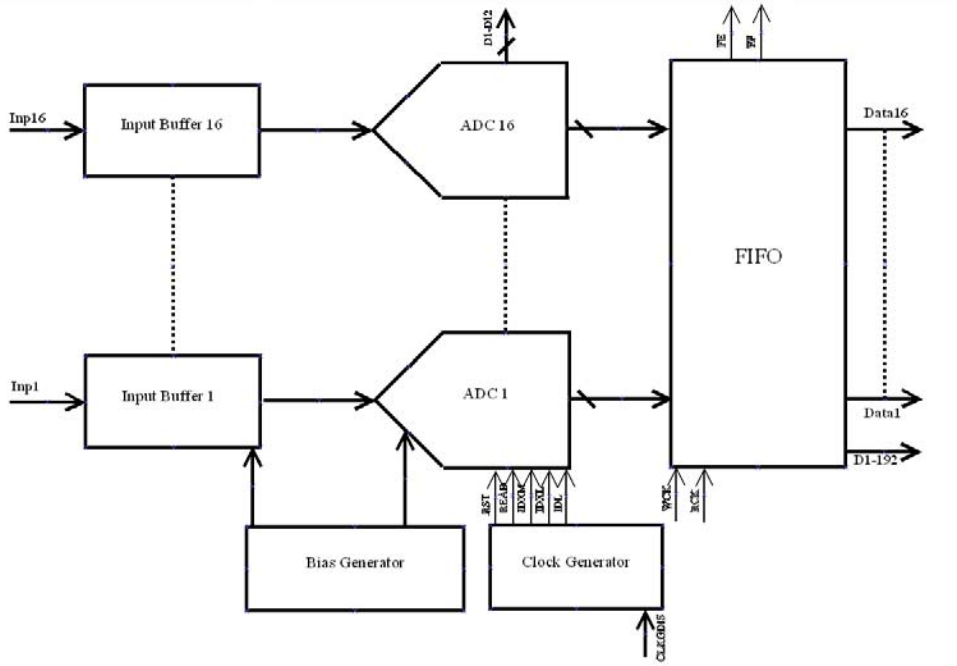


Figure 2. Functional Block Diagram

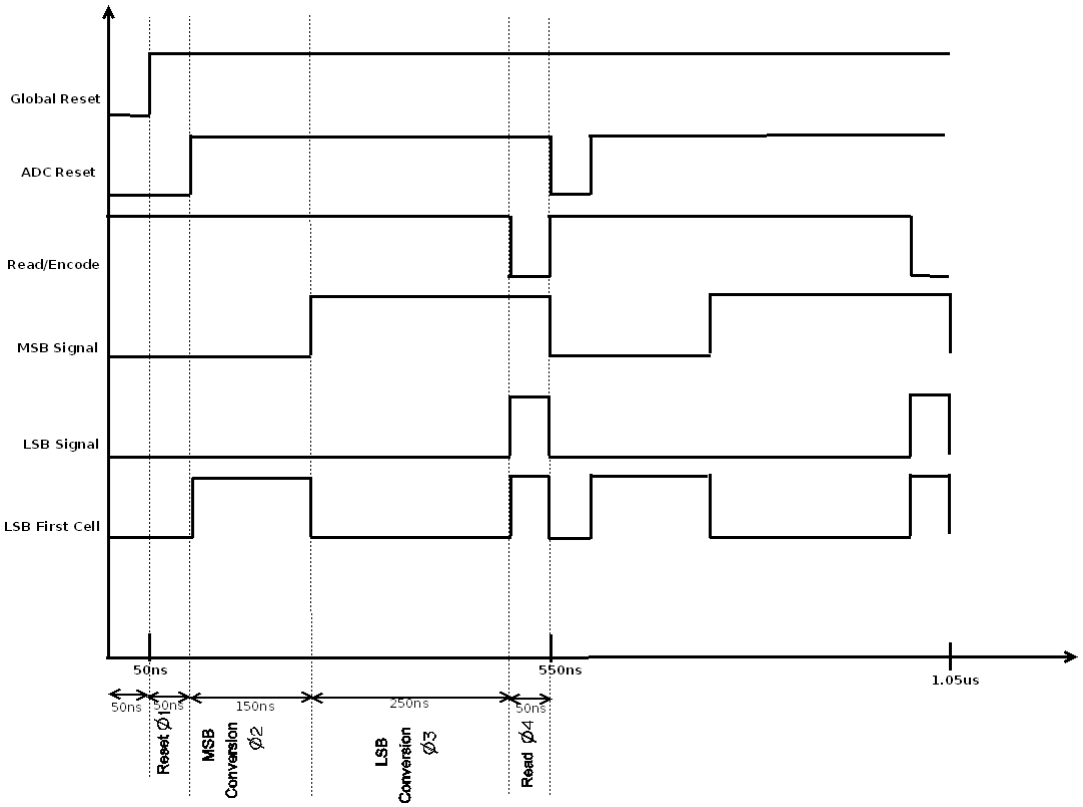


Figure 3. ADC Timing Diagram.

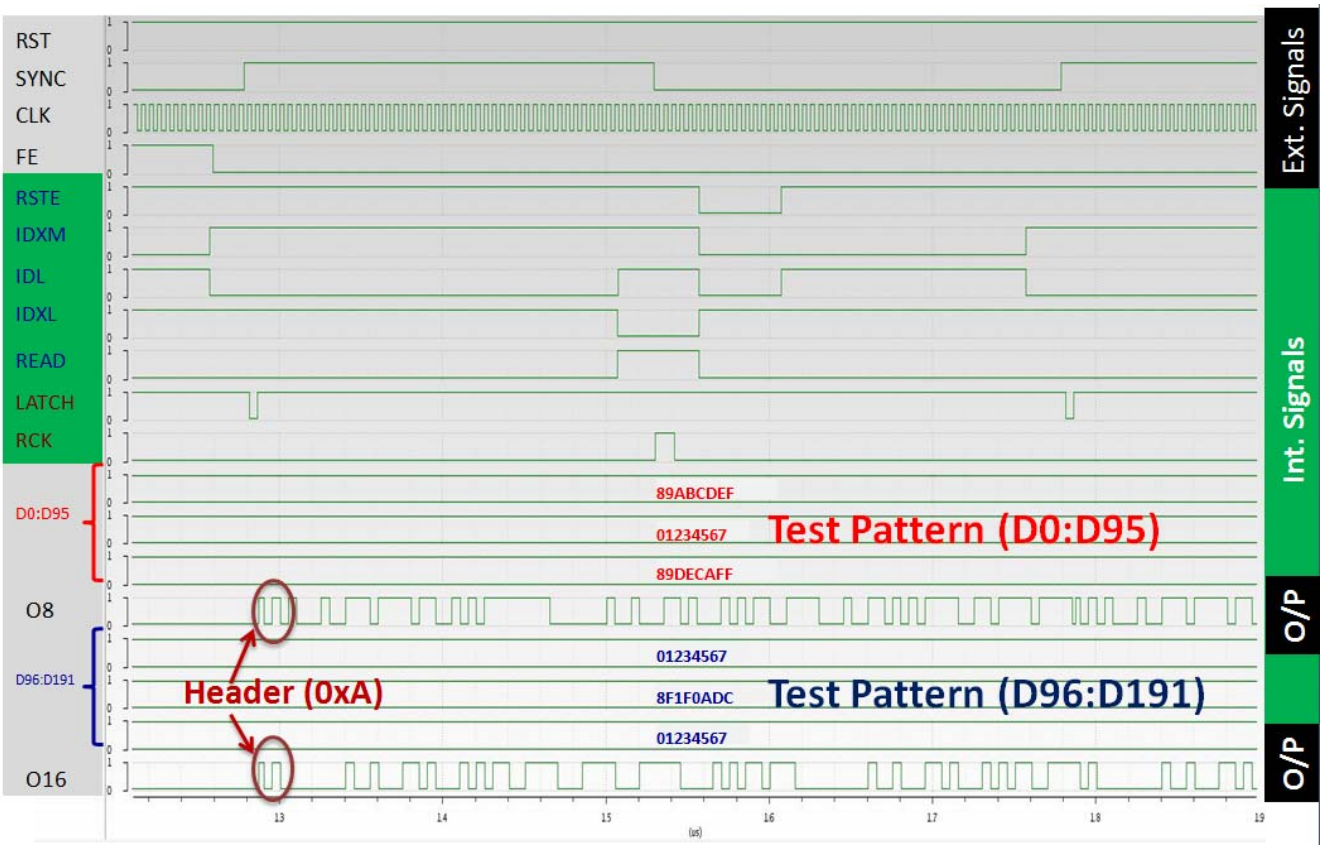


Figure 4. FIFO Timing Diagram

Pinout Information

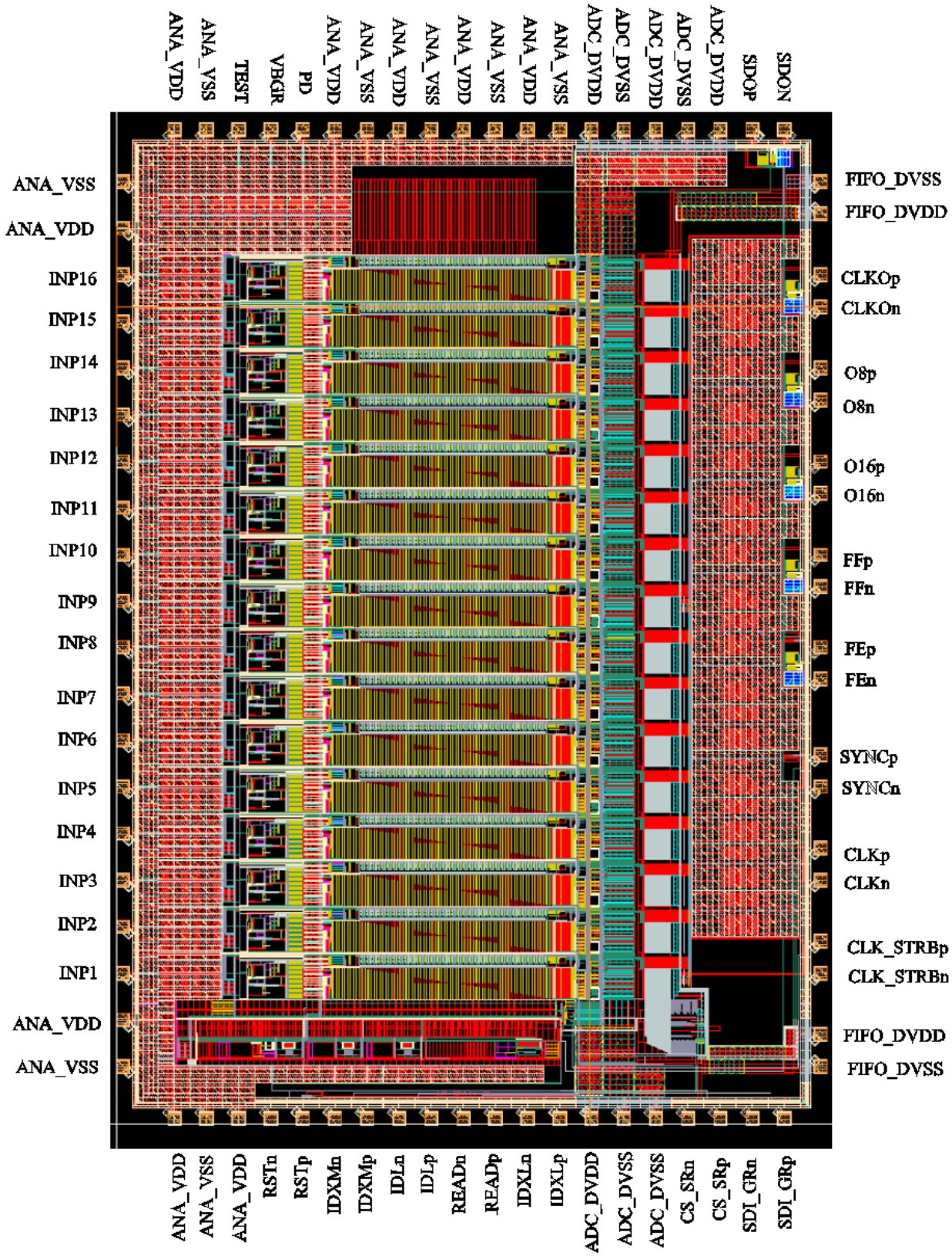


Figure 5. ASIC Pinout

Table 1. ASIC Pin List.

Num. Pins	Pin Num.	Signal Name	In/Out/Power	Reqd/Development	Description
4	1, 20, 22, 68, 70, 72, 74, 79	ANA_VSS	Power	Reqd	Analog ground: 0 V.
6	2, 19, 21, 23, 69, 71, 73, 75, 80	ANA_VDD	Power	Reqd	Analog supply for input buffers and analog section of ADCs: +1.8 V.
16	3~18	Inputs (16-1)		Reqd	Analog Inputs from channel to the input buffer (0.2 V -1.6 V). ESD protected.
1	24	RSTn	In	Development	LVDS n-input. Clock for reseting ADC cells. ESD protected.
1	25	RSTp	In	Development	LVDS p-input. Clock for reseting ADC cells. ESD protected.
1	26	IDXMn	In	Development	LVDS n-input. Clock for MSB conversion in ADC. ESD protected.
1	27	IDXMp	In	Development	LVDS p-input. Clock for MSB conversion in ADC. ESD protected.
1	28	IDLn	In	Development	LVDS n-input. Clock for LSB conversion in ADC. ESD protected.
1	29	IDLp	In	Development	LVDS p-input. Clock for LSB conversion in ADC. ESD protected.
1	30	READn	In	Development	LVDS n-input. Clock to encode thermometer code output of ADC to binary. ESD protected.
1	31	READp	In	Development	LVDS p-input. Clock to encode thermometer code output of ADC to binary. ESD protected.
1	32	IDXLn	In	Development	LVDS n-input. Clock for LSB cells in ADC. ESD protected.
1	33	IDXLp	In	Development	LVDS p-input. Clock for LSB cells in ADC. ESD protected.
2	34, 63, 65, 67	ADC_DVDD	Power	Reqd	Digital supply to ADC digital section: +1.8 V.
2	35, 36, 64, 66	ADC_DVSS	Power	Reqd	Digital ground for ADC digital section: 0 V.
1	37	CS_SRn	In	Reqd	LVDS n-input. On rising edge of CS, data is latched into the shift registers. ESD protected.
1	38	CS_SRp	In	Reqd	LVDS p-input. On rising edge of CS, data is latched into the shift registers. ESD protected.
1	39	SDI_GRn	In	Reqd	LVDS n-input. Serial data input. ESD protected.
1	40	SDI_GRp	In	Reqd	LVDS p-input. Serial data input. ESD protected.
2	41, 59	FIFO_DVSS	Power	Reqd	Digital ground for FIFO: 0 V.
2	42, 60	FIFO_DVDD	Power	Reqd	Digital Supply for FIFO: +1.8 V.
1	43	CLK_STRBn	In	Reqd	LVDS n-input. Dual purpose. Clock for shift registers and input trigger for internal monostable pattern generator. ESD protected.
1	44	CLK_STRBp	In	Reqd	LVDS p-input. Dual purpose. Clock for shift registers and input trigger for internal monostable pattern generator. ESD protected.
1	45	CLKn	In	Reqd	LVDS n-input. Dual purpose. Readout clock and clock to run ADC and FIFO with a single clock input. ESD protected.
1	46	CLKp	In	Reqd	LVDS p-input. Dual purpose. Readout clock and clock to run ADC and FIFO with a single clock input. ESD protected.
1	47	SYNCn	In	Development	LVDS n-input. FIFO Read Clock. ESD protected.
1	48	SYNCp	In	Development	LVDS p-input. FIFO Read Clock. ESD protected.

Num. Pins	Pin Num.	Signal Name	In/Out/Power	Reqd/Development	Description
1	49	FEn	Out	Reqd	LVDS n-output. FIFO empty indicator. ESD protected.
1	50	FEp	Out	Reqd	LVDS p-output. FIFO empty indicator. ESD protected.
1	51	FFn	Out	Development	LVDS n-output. FIFO full indicator. ESD protected.
1	52	FFp	Out	Development	LVDS p-output. FIFO full indicator. ESD protected.
1	53	O8n	Out	Reqd	LVDS n-output. Data output from FIFO channel 8. ESD protected.
1	54	O8p	Out	Reqd	LVDS p-output. Data output from FIFO channel 8. ESD protected.
1	55	O16n	Out	Reqd	LVDS n-output. Data output from FIFO channel 16. ESD protected.
1	56	O16p	Out	Reqd	LVDS p-output. Data output from FIFO channel 16. ESD protected.
1	57	CLKOn	Out		LVDS n-output. Regeenerated output of CLK. ESD protected.
1	58	CLKOp	Out		LVDS p-output. Regeenerated output of CLK. ESD protected.
1	61	SDOn	Out	Debug	LVDS n-output. Serial data output. ESD protected.
1	62	SDOp	Out	Debug	LVDS p-output. Serial data output. ESD protected.
1	76	PD	In	Optional	CMOS level. Power down mode pin for ADC. ESD protected.
1	77	VBGR		Debug	Bandgap reference monitor. ~1.18V at room temp.
1	78	TEST	In	Debug	Test Input for ADC
80		**Total Pin**			

Note:

Reqd: Indicates a required input or output

Optional: Indicates that the input or output is not necessary but is an added feature

Debug/Development: Indicate that the input or output is only for testing during development.

Packaging Information

Bonding Diagram

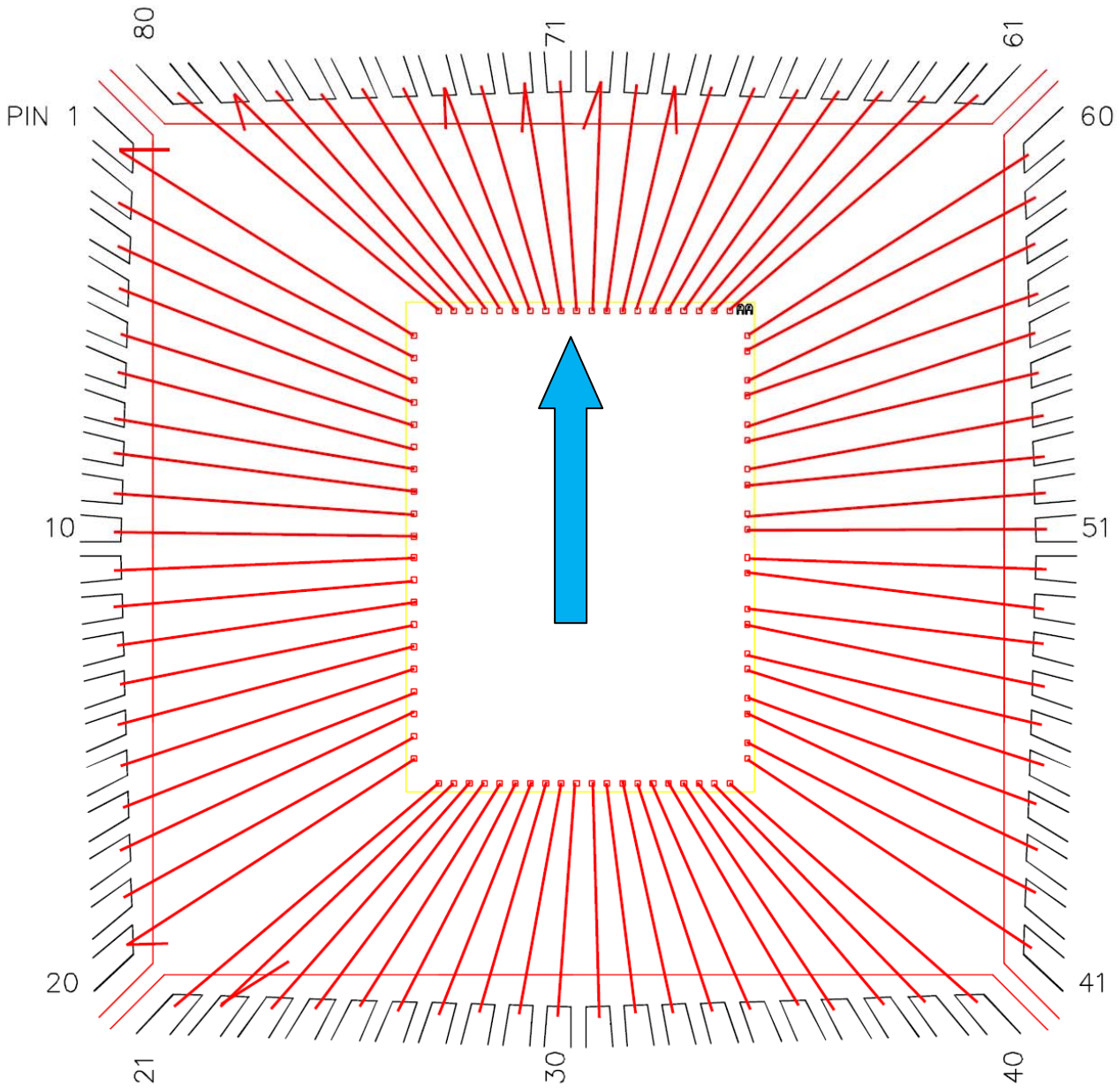
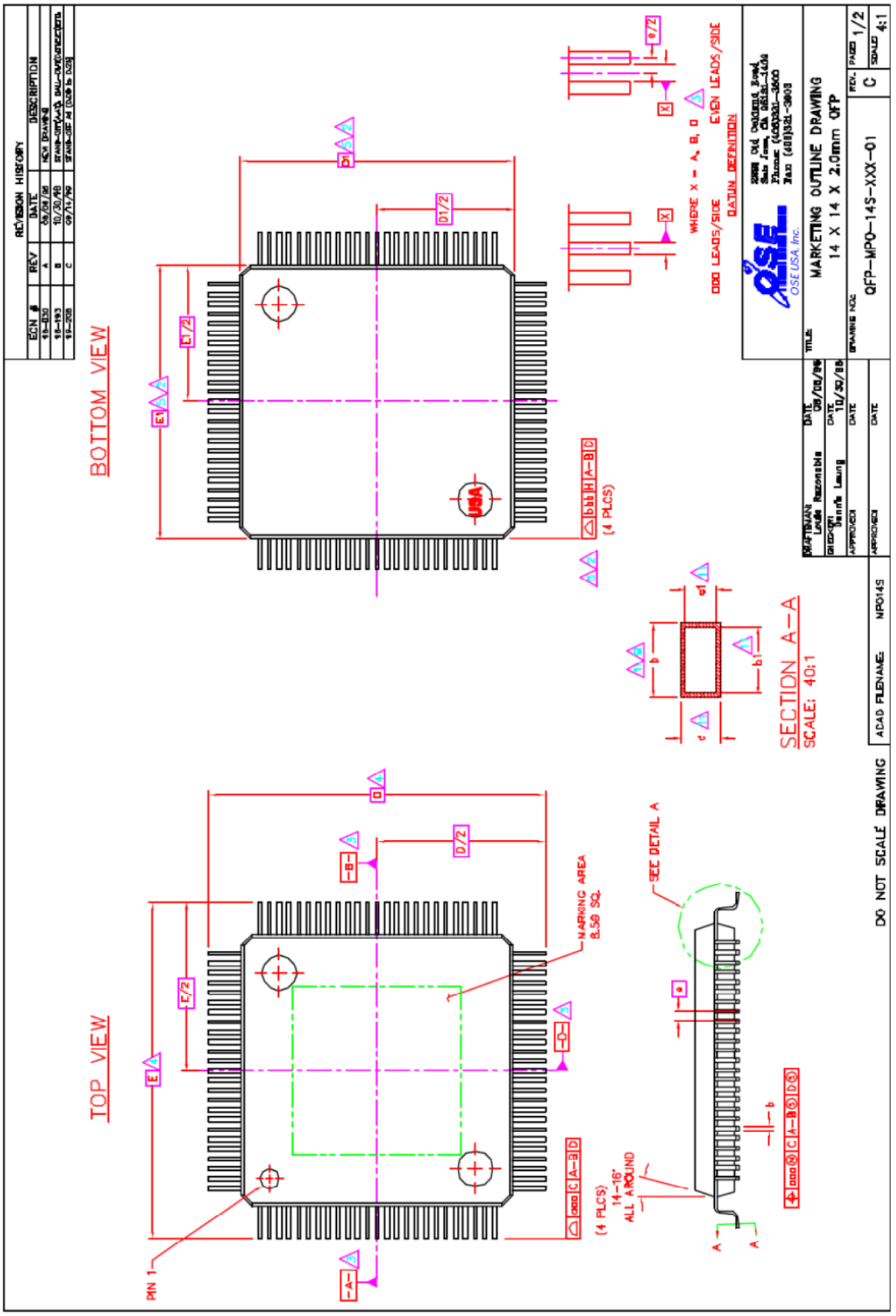


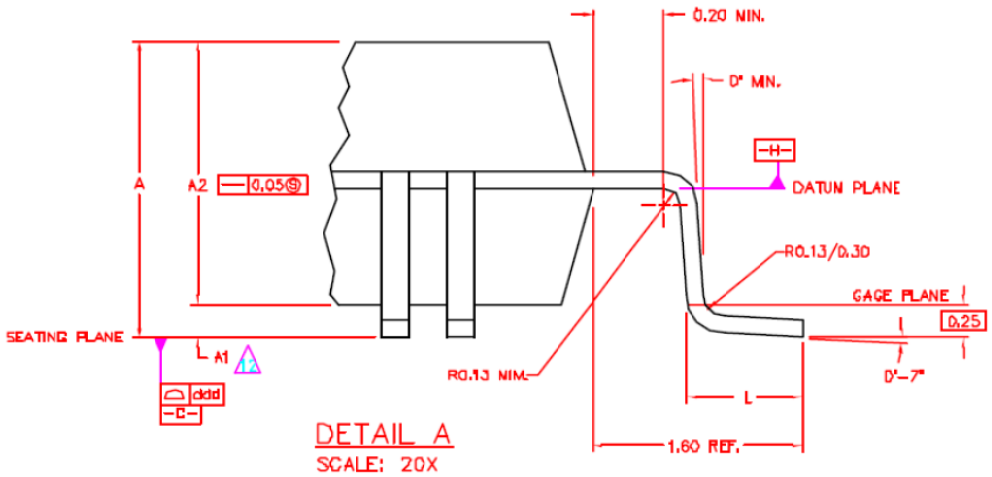
Figure 6. Bonding Diagram

Package Name: LQFP80A
Package Cavity Size: 10.5 x 10.5 mm2
Downbond-to-substrate-package-pin-numbers: 1, 20, 22, 79
Min. bond pad size X: 78.04 um
Min. bond pad size Y: 78.04 um
Min. pad pitch: 192 um
Min. pad spacing: 113.96 um


REVISION HISTORY
ECN #
REV
DATE
DESCRIPTION
MARKETING OUTLINE DRAWING
14 X 14 X 2.0mm QFP
QFP-WPO-14S-XXX-01
TOP VIEW
BOTTOM VIEW
SECTION A-A
SCALE: 40:1
SEE DETAIL A
MARKING AREA
8.50 SQ.
PIN 1
DO NOT SCALE DRAWING

BROOKHAVEN NATIONAL LABORATORY
Instrumentation Division

REVISION HISTORY			
ECN #	REV	DATE	DESCRIPTION
16-030	A	06/06/96	NEW DRAWING
98-193	B	10/30/98	STAND-OFF(A1), CAVITY/SLUG SIZE ETC.
98-206	C	09/14/99	STAND-OFF A1 (0.80 to 0.95)



DETAIL A
SCALE: 20X

SYMBOL	LEAD COUNT: FOOT PRINT 80: 3.2 FP			NOTE
	MIN.	NOM.	MAX.	
A	----	----	2.45	
A1	0.00	----	0.25	
A2	1.95	2.00	2.10	
D	17.20 BSC			
D1	14.00 BSC			
E	17.20 BSC			
E1	14.00 BSC			
L	0.73	0.88	1.03	
e	0.65 BSC			
b	0.22	----	0.38	
b1	0.22	0.30	0.33	
c	0.11	----	0.20	
c1	0.11	----	0.16	
	Tolerance of form and position			
aaa	0.20			
bbb	0.20			
ccc	0.13			
ddd	0.10			

SYMBOL	LEAD COUNT: FOOT PRINT 100: 3.2 FP			NOTE
	MIN.	NOM.	MAX.	
A	----	----	2.45	
A1	0.00	----	0.25	
A2	1.95	2.00	2.10	
D	17.20 BSC			
D1	14.00 BSC			
E	17.20 BSC			
E1	14.00 BSC			
L	0.73	0.88	1.03	
e	0.50 BSC			
b	0.17	0.22	0.27	
b1	0.17	0.20	0.23	
c	0.11	----	0.20	
c1	0.11	----	0.16	
	Tolerance of form and position			
aaa	0.20			
bbb	0.20			
ccc	0.08			
ddd	0.08			

NOTES:

1. ALL DIMENSIONS ARE IN MM. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982.
2. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE BODY SIZE BY AS MUCH AS 0.20.
3. DATUMS A-B AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
4. TO BE DETERMINED AT SEATING PLANE -C-.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
6. SURFACE FINISH OF THE PACKAGE IS #24-27 CHARMILLE (1.6-2.3$\mu m R_a$). PIN 1 AND EJECTOR PIN MAY BE LESS THAN 0.1 $\mu m R_a$.
7. DAMBAR REMOVAL: PROTRUSION DOES NOT EXCEED 0.08. INTRUSION DOES NOT EXCEED 0.03.
8. BURR: BURR DOES NOT EXCEED 0.08 IN ANY DIRECTION.
9. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUN b DIMENSION BY MORE THAN 0.08. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 FOR 0.40 AND 0.50 PITCH PACKAGE.
10. CORNER RADIUS OF PLASTIC BODY DOES NOT EXCEED 0.20.
11. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25 FROM THE LEAD TIP.
12. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
13. FINISH OF LEADS IS TIN/LEAD PLATED.
14. ALL SPECIFICATIONS AND DIMENSIONS ARE SUBJECTED TO IPAC'S MANUFACTURING PROCESS FLOW AND MATERIALS.
15. THE PACKAGES DESCRIBED IN THIS DRAWING CONFORM TO JEDEC NO-108C AND MS-022B. WHERE DESCREPANCIES BETWEEN THE JEDEC AND IPAC DOCUMENTS EXIST, THIS DRAWING WILL TAKE THE PRECEDENCE.

OSE USA, Inc.
2221 Old Oakland Road
San Jose, CA 95131-1402
Phone: (408)321-8600
Fax: (408)321-8601

DRAFTSMAN: Leslie Recendiz	DATE: 06/06/96	TITLE: MARKETING OUTLINE DRAWING 14 X 14 X 2.0mm QFP
CHECKED: Dennis Leung	DATE: 10/30/98	
APPROVED	DATE	DRAWING NO: QFP-MPO-145-XXX-01
APPROVED	DATE	REV: C
		PAGE: 2/2
		SCALE: NONE

DO NOT SCALE DRAWING

ACAD FILENAME: MP0145