

LARASIC6 (IC139)

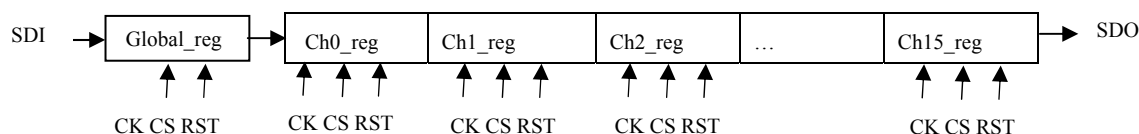
v4 - 8/4/16 - corrected pinout

- **Front-End Channels : 16**
 - charge amplifier, 5th order shaping amplifier, output buffer
 - charge preamplifier polarity: selectable negative (for non-collecting mode) or both (for collecting mode)
 - charge amplifier coupling: AC or DC
 - adaptive reset (up to 1 nA)
 - integrated test capacitor: ≈ 200 fF
 - shaping amplifier peaking time: selectable 0.5, 1, 2, or 3 μ s
 - shaper output, temperature and bandgap reference monitors
 - channel gain: selectable 4.7, 7.8, 14, or 25 mV/fC
 - baseline: selectable 200 mV (for non-collecting mode), or 900 mV (for collecting mode)
 - max signal: 1.4 V peak to peak (0.2~1.6V)
 - temperature sensor: 0.8728 V @ 25°C + 2.868 mV / °C
- **Power**
 - channels: ~ 10 mW/ch with buffer, ~ 6 mW/ch without buffer
 - input MOSFET: ~ 3.9 mW
 - charge amp: ~ 0.8 mW
 - shaper: ~ 1 mW
 - output buffers: ~ 4 mW
 - common circuitry: ~ 4 mW
- **Layout size** 6.0×5.7 mm²
- **Die cut size** 6.1×5.9 mm²
- **Pad count, size, pitch** $80, 78.04 \times 78.04$ μ m², 192 μ m (sides) and 292.32 μ m (top/bottom)
- **Technology :** CMOS 0.18 μ m – 1.8V, 1-poly, 6-metal, MiM cap, sil blk resistors
- **Updates to this version**
 - smart reset
 - increased unbuffered drive capability
 - decreased pull-up or pull-down currents in digital inputs
 - increased protection of digital and test inputs

Description

- The ASIC is composed of 16 front-end channels, each implementing a low noise charge amplifiers with fully compensated continuous reset and test capacitor (200fF), a fifth order shaping amplifier with complex conjugate poles, and an output buffer driving maximum signal of 1.4 V_{pp} (i.e. 0.2 V to 1.6 V). Common to all channels are the internal bias generators, the global configuration inputs and the global shift register.
- The ASIC has four global configuration inputs: Clock (CK), Chip Select (CS), Reset (RST), and Serial Data Input (SDI); and one global configuration output: Serial Data Output (SDO). See the Serial Data Map below. *A Reset is also generated with a CS pulse if CK is kept high. The duration of the reset is from falling-edge of CS to falling-edge of CK.*

Serial Data Map



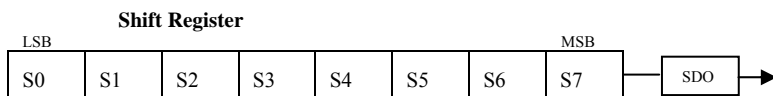
- The ASIC has one global shift register and sixteen channel shift registers (each 8 bits long). At the falling edge of each CK, the configuration data is serially shifted into the shift registers. At the falling edge of CS, the data is latched from the shift registers to the configuration pins. The output of each shift register is serially available through its SDO pin. See the Register Map below for more details.

- The first three bits of the global register are un-used. Bit STB sets Channel 0 to monitor either the analog channel signal, or the temperature/bandgap reference (dedicated by bit STB1). Bit SLK sets the leakage current of each channel to either 100 pA or 500 pA. Bit SLKH increases the leakage current by a factor 10.
- Each channel register has 8 bits: STS, SNC, SG0, SG1, ST0, ST1, SDC, and SDF.
 - STS enables the 200 fF test capacitor individually for each channel. The analog test pulse can be applied through pin TEST. The pin can be terminated (50 Ohm) when not connected to a pulse generator.
 - SNC selects the baseline to either 200 mV (for unipolar pulse in collecting mode) or 900 mV (for bipolar pulse in non-collecting mode).
 - The channel gain can be independently adjusted to 4.7, 7.8, 14 or 25 mV/fC, through two dedicated bits (SG0 and SG1).
 - The peaking time of each channel can be set independently to 0.5, 1, 2 or 3 μ s through two dedicated bits (ST0 and ST1).
 - SDC sets the output coupling to either AC or DC.
 - SDF sets the output buffer to either selected or bypassed (also powered down).

Register Map



Figure 3 An 8-bit shift register.



Data is shifted into the load shift register on the rising edge of CK while CS is high.

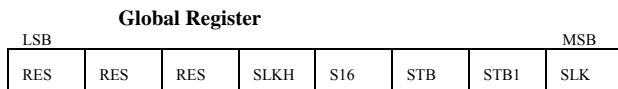
The MSB is shifted into position D0 on the first rising edge of CK.

The LSB is shifted into position D0 on the 8th rising edge of CK.

The MSB is shifted out of SDO on the 9th rising edge of CK.

The LSB is shifted out of SDO on the 16th rising edge of CK.

NOTE: The default value of each register is 00.



RES - Reserved.

SLKH - Leakage current increase x10, 0 = disabled, 1 = enabled

STB - 0 = Monitor analog channel signal. 1 = Monitor temperature or bandgap reference.

STB1 - 0 = Monitor temperature. 1 = Monitor bandgap reference.

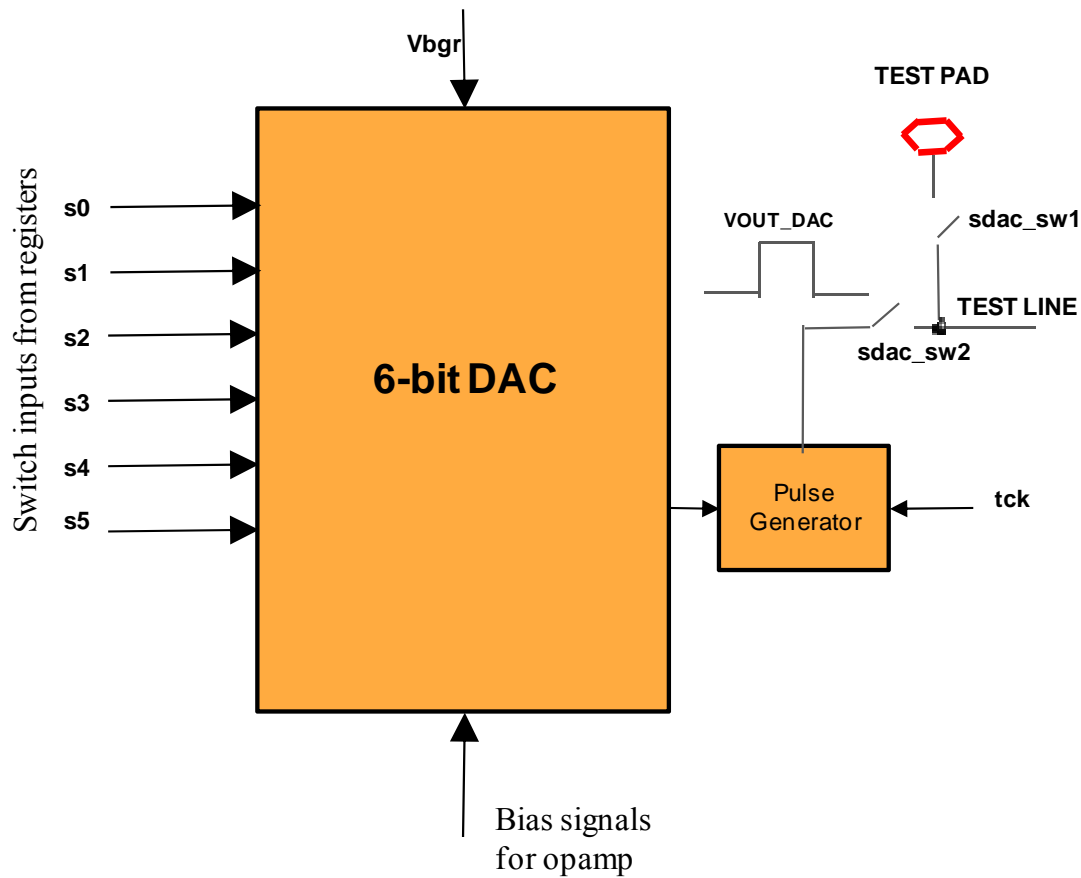
SLK - Leakage current control. 0 = 500 pA. 1 = 100 pA.

S16 - Enable high filter in ch16, 0 = disabled, 1 = enabled

Channel Register							
LSB				MSB			
STS	SNC	SG0	SG1	ST0	ST1	SDC	SDF

STS - Test capacitance. 0 = disabled. 1 = enabled.
 SNC - Baseline selection. 0 = 900 mV (for non-collecting mode). 1 = 200 mV (for collecting mode).
 SG (0,1) - Gain selection. 00 = 4.7 mV/fC, 10 = 7.8 mV/fC, 01 = 14 mV/fC, 11 = 25 mV/fC.
 ST (0,1) - Peak time selection. 00 = 1.0 us, 10 = 0.5 us, 01 = 3 us, 11 = 2 us.
 SDC - Output coupling. 0 = dc coupling. 1 = ac coupling.
 SBF - Output buffer bypass. 0 = output buffer powered down and bypassed. 1 = output buffer selected.

On Chip DAC and Pulse Generator



The ASIC contains a 6-bit Current Scaling DAC and a pulse generator for test and calibration of the Front-End channels:

- Output Voltage Range: 0 to 1.18V
- Resolution: 18.75mV
- Power: 1mW
- Temperature Range: 27°C to -200°C
- Settling time: < 130ns
- Linearity: $\pm 0.12\%$

Global register 2 is added before the first one to provide the inputs for the DAC.

Global Register 2:

LSB					MSB		
sdac0	sdac1	sdac2	sdac3	sdac4	sdac5	sdacsw1	sdacsw2

sdac0-sdac5 : 6-bit input to the DAC where sdac0 is the LSB and sdac5 is the MSB

sdacsw1 : 0 = test input to the channels is disconnected from the external test pin. 1 = test input to the channels is connected to the external test pin.

sdacsw2: 0 = test input to the channels is disconnected from the DAC output. 1 = test input to the channels is connected to the DAC output.

The output of the DAC is fed to a pulse generator that is controlled by CK clock input to generate the output voltage pulse.

- The ASIC makes the analog amplitudes available at pins O0~O15. Output buffers are available for the analog outputs (enabled with SDF). Each buffer dissipates approximately 5 mW. When the buffers are enabled, the ASIC can drive 400 pF || 250 Ω (effective load of cable and intermediate amplifier). When the buffers are disabled, the ASIC can drive up to 20 pF (see Table I for the simulated gain and peaktime versus load capacitance—gain less than desired value due to the passive compensation network of the output buffer, which is not bypassed).

Table 1. Simulated Gain and Peaktime vs. Load Capacitance.
(at 27°C, gain at 4.7 mV/fC, peaktime at 0.5 us, output buffer disabled)

C_load (pF)	Gain (mV/fC)	Δ Gain (%)	Peaktime (ns)	Δ Peaktime (%)
0.001	4.15	0	586	0
0.5	4.13	-0.4	587	0.3
1	4.12	-0.8	587	0.3
2	4.08	-1.6	587	0.3
3	4.00	-3.7	587	0.3
5	3.99	-3.9	589	0.6
10	3.83	-7.6	591	1.0
15	3.69	-11.0	594	1.4
20	3.56	-14.2	596	1.8

- The ASIC has single test devices (NMOS, PMOS, and resistor), listed in Table 2.

Table 2. ASIC Test Structures.

Device	Signal (ASIC Pin No.)	Description
4.08 nm thin oxide PMOS		
	VDDT (32)	Bulk connection of all PMOS test devices.
	GP (29)	Gate connection of all PMOS test devices.
PMOS2V W/L = 2/0.18, M = 5	DPCH018 (30), SPCH018 (31)	Drain and source connection of 1.8V nominal VT PMOS transistor.
PMOS2V W/L = 2/0.36, M = 5	DPCH036 (33), SPCH036 (34)	Drain and source connection of 1.8V nominal VT PMOS transistor.
PMOS2V W/L = 2/0.72, M = 5	DPCH072 (35), SPCH072 (36)	Drain and source connection of 1.8V nominal VT PMOS transistor.

Device	Signal (ASIC Pin No.)	Description
4.08 nm thin oxide NMOS		
	GN (71)	Gate connection of all NMOS test devices, except DNCH018A.
NMOS2V W/L = 2/0.18, M = 5	GNA (74), DNCH018A (73), SNCH018A (72)	Gate, drain and source connection of 1.8V nominal VT NMOS transistor.
NMOS2V W/L = 2/0.18, M = 5	DNCH018 (70), SNCH018 (69)	Drain and source connection of 1.8V nominal VT NMOS transistor.
NMOS2V W/L = 2/0.27, M = 5	DNCH027 (68), SNCH027 (67)	Drain and source connection of 1.8V nominal VT NMOS transistor.
NMOS2V W/L = 2/0.36, M = 5	DNCH036 (66), SNCH036 (65)	Drain and source connection of 1.8V nominal VT NMOS transistor.
NMOS2V W/L = 2/0.72, M = 5	DNCH072 (64), SNCH072 (63)	Drain and source connection of 1.8V nominal VT NMOS transistor.
Resistors		
rppolyrpo R=5K	RES(75)	P+ Poly resistor without silicide
rppolyrpo R=5K	RES2(28)	P+ Poly resistor without silicide

Pinout Information

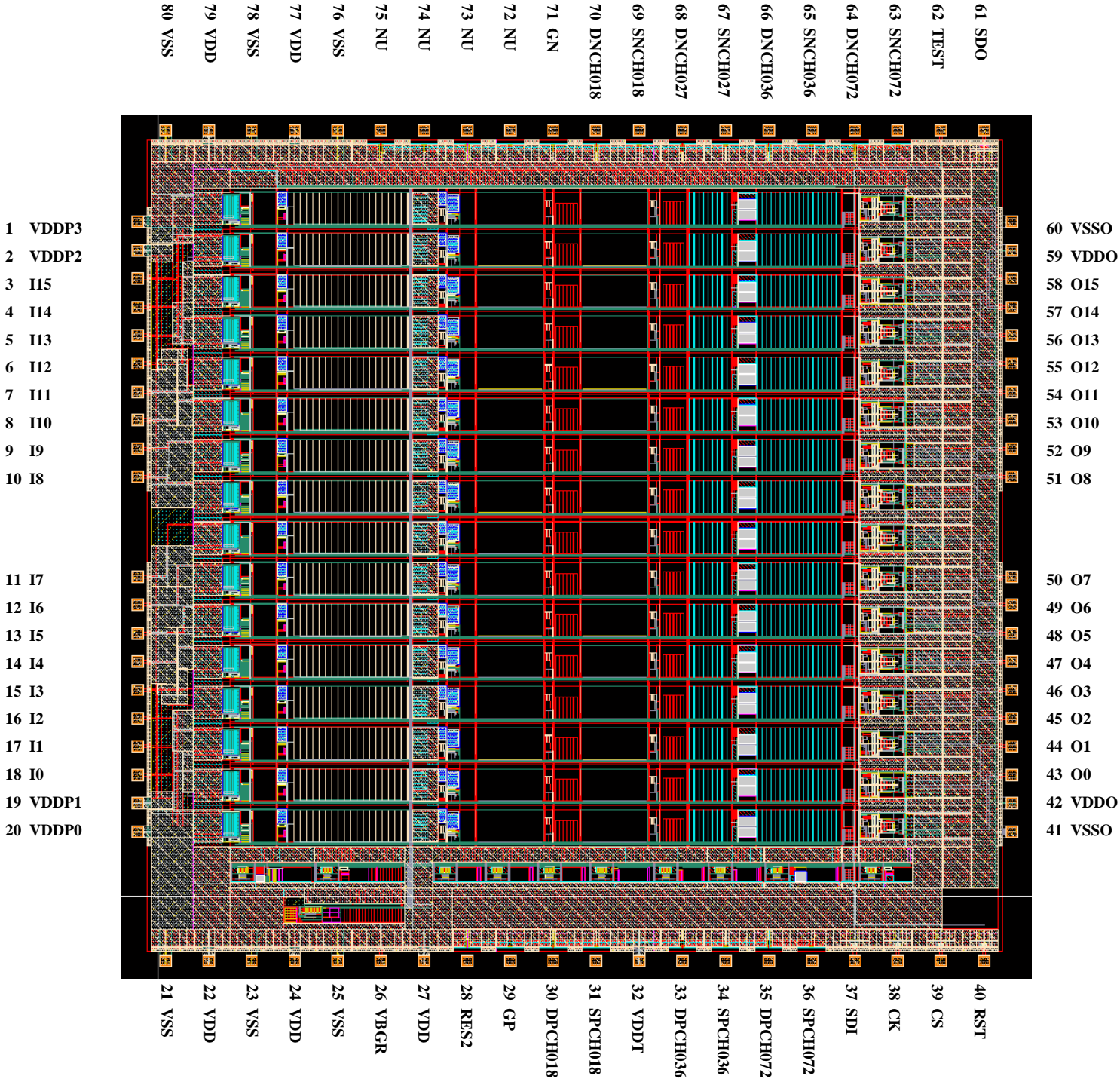
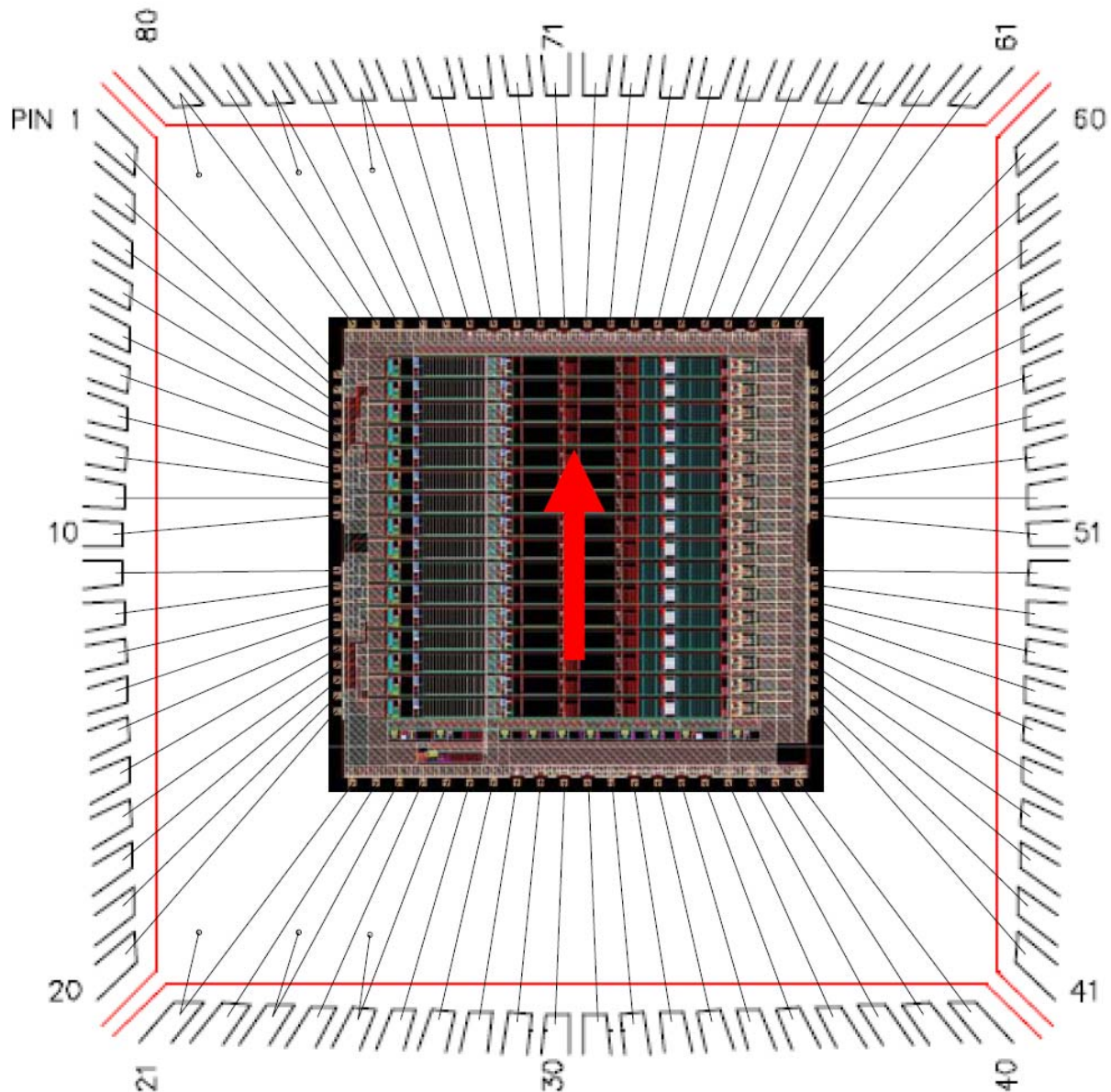


Table 1. ASIC Pin List.

Num. Pins	Pin Num.	Signal Name	In/Out	Description
4	1, 2, 19, 20	VDDP (3, 2, 1, 0)		Analog supply for the 1 st stage of the charge amplifiers: +1.8V. VDDP0 (ch0~ch3), VDDP1 (ch 4~ch7), VDDP2 (ch8~ch11), VDDP3 (ch12~ch15).
6	21, 23, 25, 76, 78, 80	VSS		Analog ground: 0 V.
5	22, 24, 27, 77, 79	VDD		Analog supply: +1.8 V.
2	41, 60	VSSO		Analog ground for output buffer: 0 V.
2	42, 59	VDDO		Analog supply for output buffer: +1.8 V.
16	3~18	Charge Inputs I (15~0)	In	DC or AC coupled charge input from detector. ESD protected (mild).
16	43~58	Channel Output (0~15)	Out	Channel analog output. ESD protected
1	26	VBGR		Bandgap reference monitor. ~1.18V at room temp.
1	28, -	RES2	In/Out	5 kOhm resistor connected to VSS
1	27	VDDT		Bulk connections of PMOS test devices: +1.8 V.
2	29, 71, -	GP, GN, -	In/Out	Gate connections of test devices. GP (all PMOS), GNA (NMOS 018A), GN (all the rest NMOS).
3	30, 33, 35	DPCH (018, 036, 072)	In/Out	Drain connections of PMOS test devices: length = 0.18, 0.36, 0.72 um.
3	31, 34, 36	SPCH (018, 036, 072)	In/Out	Source connections of PMOS test devices: length = 0.18, 0.36, 0.72 um.
4	-, 70, 68, 66, 64	DNCH (-, 018, 027, 036, 072)	In/Out	Drain connections of NMOS test devices: length = 0.18, 0.27, 0.36, 0.72 um.
4	-, 69, 67, 65, 63	SNCH (-, 018, 027, 036, 072)	In/Out	Source connections of NMOS test devices: length = 0.18, 0.27, 0.36, 0.72 um.
1	37	SDI	In	CMOS level. Digital serial data input. ESD protected.
1	38	CK	In	CMOS level. Clock for shift registers. ESD protected.
1	39	CS	In	CMOS level. On falling edge of CS, data is latched into the shift registers. ESD protected.
1	40	RST	In	CMOS level. Global active low reset. ESD protected.
1	61	SDO	Out	CMOS level. Output of shift register. Tristated with CS. ESD protected.
1	62	TEST	In	Test pulse input. ESD protected.
4	72-75	-	-	New test structures (Gabriele Giacomini) - keep grounded
80		Total Pin		

Packaging Information

Bonding Diagram



Package Name: LQFP80A
Package Cavity Size: 10.5 x 10.5 mm²
Downbond-to-substrate-package-pin-numbers: 21, 23, 25, 76, 78, 80
Min. bond pad size X: 78.04 um
Min. bond pad size Y: 78.04 um
Min. pad pitch: 192 um
Min. pad spacing: 113.96 um

