LARASIC4 (IC125)

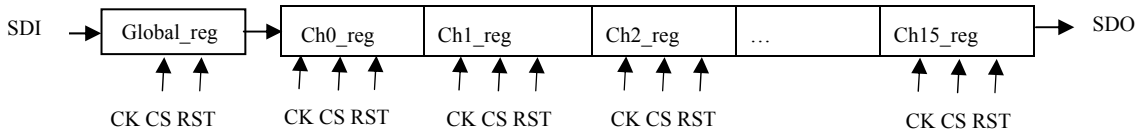
- **Front-End Channels** : 16
  - charge amplifier, 5th order shaping amplifier, output buffer
  - charge preamplifier polarity: selctable negative (for non-collecting mode) or both (for collecting mode)
  - charge amplifier coupling: AC or DC
    --adaptive reset (up to 1 nA)
  - integrated test capacitor: ≈ 200 fF
  - shaping amplifier peaking time: selectable 0.5, 1, 2, or 3 us
  - shaper output, temperature and bandgap reference monitors
  - channel gain: selectable 4.7, 7.8, 14, or 25 mV/fC
  - baseline: selectable 200 mV (for non-collecting mode), or 900 mV (for collecting mode)
  - max signal: 1.4 V peak to peak (0.2~1.6V)
  - temperature sensor: 0.8728 V @ 25°C + 2.868 mV / °C
- **Power**
  - channels: ~ 10 mW/ch with buffer, ~ 6mW/ch without buffer
    - input MOSFET: ~ 3.9 mW
    - charge amp: ~ 0.8 mW
    - shaper: ~ 1 mW
    - output buffers: ~ 4 mW
  - common circuitry: ~ 4 mW
- **Layout size** 6.0 × 5.7 mm²
- **Die cut size** 6.1 × 5.9 mm²
- **Pad count, size, pitch** 80, 78.04 × 78.04 µm², 192 µm (sides) and 292.32 µm (top/bottom)
- **Technology** : CMOS 0.18µm – 1.8V, 1-poly, 6-metal, MiM cap, sil blk resistors

Description

- The ASIC is composed of 16 front-end channels, each implementing a low noise charge amplifiers with fully compensated continuous reset and test capacitor (200fF), a fifth order shaping amplifier with complex conjugate poles, and an output buffer driving maximum signal of 1.4 V_{pp} (i.e. 0.2 V to 1.6 V). Common to all channels are the internal bias generators, the global configuration inputs and the global shift register.

- The ASIC has four global configuration inputs: Clock (CK), Chip Select (CS), Reset (RST), and Serial Data Input (SDI); and one global configuration output: Serial Data Output (SDO). See the Serial Data Map below.

Serial Data Map



- The ASIC has one global shift register and sixteen channel shift registers (each 8 bits long). At the falling edge of each CK, the configuration data is serially shifted into the shift registers. At the falling edge of CS, the data is latched from the shift registers to the configuration pins. The output of each shift register is serially available through its SDO pin. See the Register Map below for more details.
  - The first five bits of the global register are un-used. Bit STB sets Channel 0 to monitor either the analog channel signal, or the temperature/bandgap reference (dedicated by bit STB1). Bit SLK sets the leakage current of each channel to either 100 pA or 300 pA.
  - Each channel register has 8 bits: STS, SNC, SG0, SG1, ST0, ST1, SDC, and SDF.
    - STS enables the 200 fF test capacitor individually for each channel. The analog test pulse can be applied through pin TEST. The pin can be terminated (50 Ohm) when not connected to a pulse generator.

- SNC selects the baseline to either 200 mV (for unipolar pulse in collecting mode) or 900 mV (for bipolar pulse in non-collecting mode).
- The channel gain can be independently adjusted to 4.7, 7.8, 14 or 25 mV/fC, through two dedicated bits (SG0 and SG1).
- The peaking time of each channel can be set independently to 0.5, 1, 2 or 3 µs through two dedicated bits (ST0 and ST1).
- SDC sets the output coupling to either AC or DC.
- SDF sets the output buffer to either selected or bypassed (also powered down).

Register Map

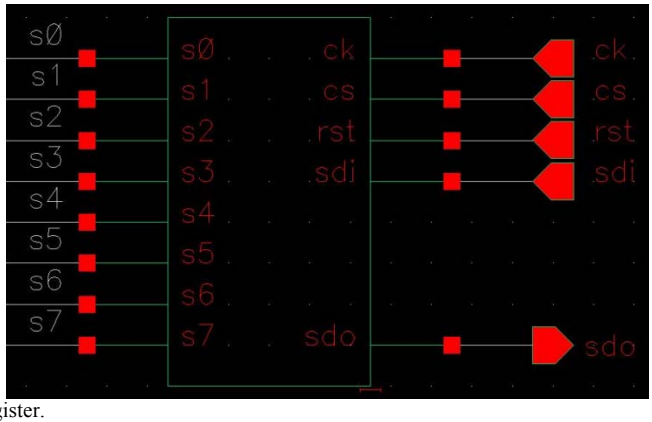


Figure 3 An 8-bit shift register.

Shift Register

LSB							MSB	
S0	S1	S2	S3	S4	S5	S6	S7	SDO

Data is shifted into the load shift register on the rising edge of CK while CS is high.
The MSB is shifted into position D0 on the first rising edge of CK.
The LSB is shifted into position D0 on the 8th rising edge of CK.
The MSB is shifted out of SDO on the 9th rising edge of CK.
The LSB is shifted out of SDO on the 16th rising edge of CK.

NOTE: The default value of each register is 00.

Global Register

LSB							MSB
RES	RES	RES	RES	S16	STB	STB1	SLK

RES - Reserved.
STB - 0 = Monitor analog channel signal. 1 = Monitor temperature or bandgap reference.
STB1 - 0 = Monitor temperature. 1 = Monitor bandgap reference.
SLK - Leakage current control. 0 = 500 pA. 1 = 100 pA.
S16 - Enable high filter in ch16, 0 = disabled, 1 = enabled

Channel Register

LSB							MSB
STS	SNC	SG0	SG1	ST0	ST1	SDC	SDF

STS - Test capacitance. 0 = disabled. 1 = enabled.
SNC - Baseline selection. 0 = 900 mV (for non-collecting mode). 1 = 200 mV (for collecting mode).
SG (0,1) - Gain selection. 00 = 4.7 mV/fC, 10 = 7.8 mV/fC, 01 = 14 mV/fC, 11 = 25 mV/fC.
ST (0,1) - Peak time selection. 00 = 1.0 us, 10 = 0.5 us, 01 = 3 us, 11 = 2 us.

SDC - Output coupling. 0 = dc coupling. 1 = ac coupling.
SBF - Output buffer bypass. 0 = output buffer selected. 1= output buffer powered down and bypassed.

- The ASIC makes the analog amplitudes available at pins O0~O15. Output buffers are available for the analog outputs (enabled with SDF). Each buffer dissipates approximately 5 mW. When the buffers are enabled, the ASIC can drive 400 pF || 250 Ω (effetive load of cable and intermiate amplifer). When the buffers are disabled, the ASIC can drive up to 20 pF (see Tatble I for the simulated gain and peaktime versus load capacitance—gain less than disired value due to the passive compensation network of the output buffer, which is not bypassed).

Table 1. Simulated Gain and Peaktime vs. Load Capacitance.
(at 27°C, gain at 4.7 mV/fC, peaktime at 0.5 us, output buffer disabled)

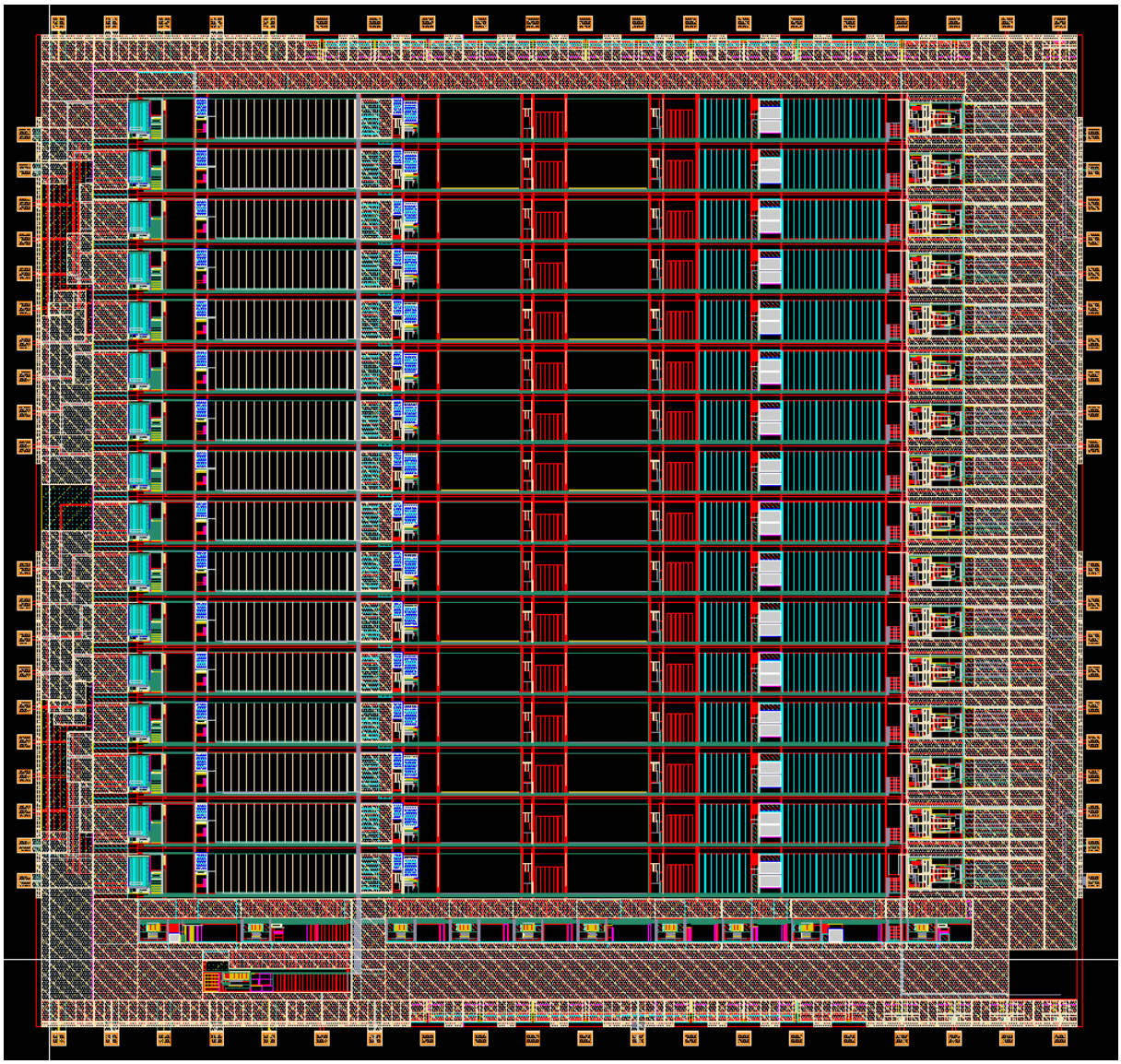
C_load (pF)	Gain (mV/fC)	ΔGain (%)	Peaktime (ns)	ΔPeaktime (%)
0.001	4.15	0	586	0
0.5	4.13	-0.4	587	0.3
1	4.12	-0.8	587	0.3
2	4.08	-1.6	587	0.3
3	4.00	-3.7	587	0.3
5	3.99	-3.9	589	0.6
10	3.83	-7.6	591	1.0
15	3.69	-11.0	594	1.4
20	3.56	-14.2	596	1.8

- The ASIC has single test devices (NMOS, PMOS, and resistor), listed in Table 2.

Table 2. ASIC Test Structures.

Device	Signal (ASIC Pin No.)	Description
4.08 nm thin oxide PMOS		
	VDDT (32)	Bulk connection of all PMOS test devices.
	GP (29)	Gate connection of all PMOS test devices.
PMOS2V W/L = 2/0.18, M = 5	DPCH018 (30), SPCH018 (31)	Drain and source connection of 1.8V nominal VT PMOS transistor.
PMOS2V W/L = 2/0.36, M = 5	DPCH036 (33), SPCH036 (34)	Drain and source connection of 1.8V nominal VT PMOS transistor.
PMOS2V W/L = 2/0.72, M = 5	DPCH072 (35), SPCH072 (36)	Drain and source connection of 1.8V nominal VT PMOS transistor.
4.08 nm thin oxide NMOS		
	GN (71)	Gate connection of all NMOS test devices, except DNCH018A.
NMOS2V W/L = 2/0.18, M = 5	GNA (74), DNCH018A (73), SNCH018A (72)	Gate, drain and source connection of 1.8V nominal VT NMOS transistor.
NMOS2V W/L = 2/0.18, M = 5	DNCH018 (70), SNCH018 (69)	Drain and source connection of 1.8V nominal VT NMOS transistor.
NMOS2V W/L = 2/0.27, M = 5	DNCH027 (68), SNCH027 (67)	Drain and source connection of 1.8V nominal VT NMOS transistor.
NMOS2V W/L = 2/0.36, M = 5	DNCH036 (66), SNCH036 (65)	Drain and source connection of 1.8V nominal VT NMOS transistor.
NMOS2V W/L = 2/0.72, M = 5	DNCH072 (64), SNCH072 (63)	Drain and source connection of 1.8V nominal VT NMOS transistor.
Resistors		
rppolyrpo R=5K	RES(75)	P+ Poly resistor without silicide
rppolyrpo R=5K	RES2(28)	P+ Poly resistor without silicide

Pinout Information



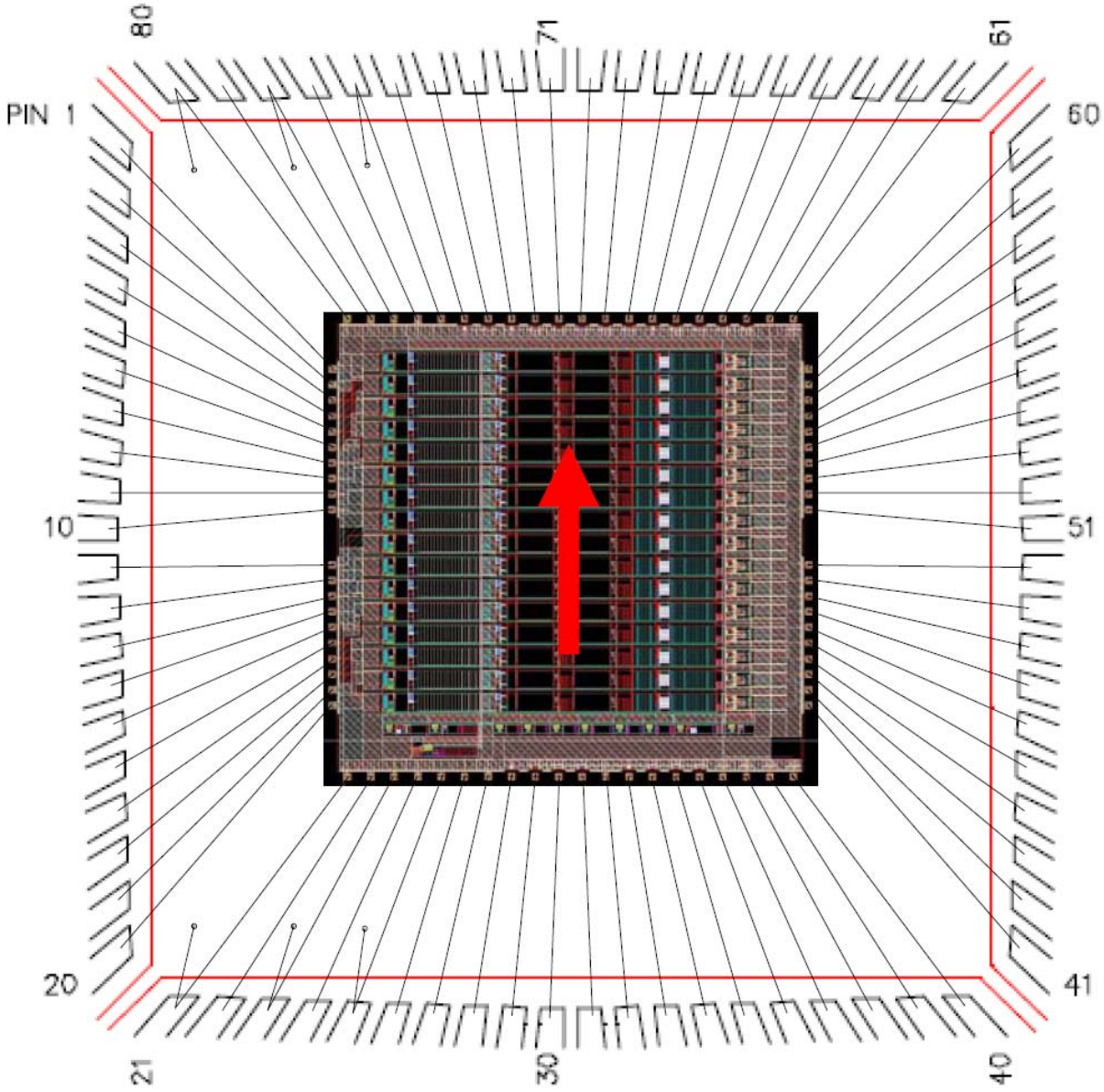
BROOKHAVEN NATIONAL LABORATORY
Instrumentation Division

Table 1. ASIC Pin List.

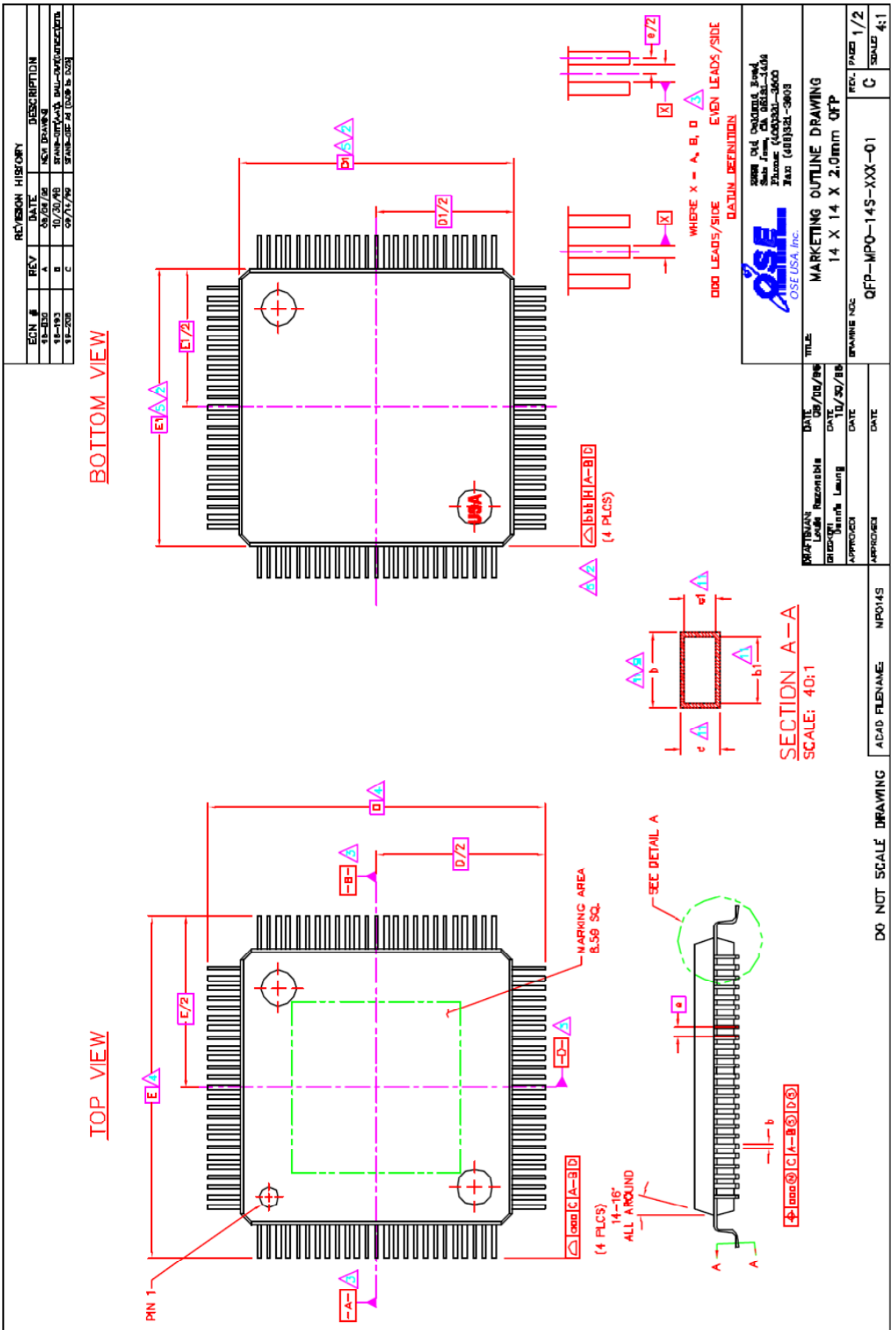
Num. Pins	Pin Num.	Signal Name	In/Out	Description
4	1, 2, 19, 20	VDDP (3, 2, 1, 0)		Analog supply for the 1st stage of the charge amplifiers: +1.8V. VDDP0 (ch0~ch3), VDDP1 (ch 4~ch7), VDDP2 (ch8~ch11), VDDP3 (ch12~ch15).
6	21, 23, 25, 76, 78, 80	VSS		Analog ground: 0 V.
5	22, 24, 27, 77, 79	VDD		Analog supply: +1.8 V.
2	41, 60	VSSO		Analog ground for output buffer: 0 V.
2	42, 59	VDDO		Analog supply for output buffer: +1.8 V.
16	3~18	Charge Inputs I (15~0)	In	DC or AC coupled charge input from detector. ESD protected (mild).
16	43~58	Channel Output (0~15)	Out	Channel analog output. ESD protected
1	26	VBGR		Bandgap reference monitor. ~1.18V at room temp.
2	28, 75	RES2, RES	In/Out	5 kOhm resister connected to VSS
1	27	VDDT		Bulk connections of PMOS test devices: +1.8 V.
4	29, 71, 74	GP, GN, GNA	In/Out	Gate connections of test devices. GP (all PMOS), GNA (NMOS 018A), GN (all the rest NMOS).
3	30, 33, 35	DPCH (018, 036, 072)	In/Out	Drain connections of PMOS test devices: length = 0.18, 0.36, 0.72 um.
3	31, 34, 36	SPCH (018, 036, 072)	In/Out	Source connections of PMOS test devices: length = 0.18, 0.36, 0.72 um.
5	73, 70, 68, 66, 64	DNCH (018A, 018, 027, 036, 072)	In/Out	Drain connections of NMOS test devices: length = 0.18, 0.27, 0.36, 0.72 um.
5	72, 69, 67, 65, 63	SNCH (018A, 018, 027, 036, 072)	In/Out	Source connections of NMOS test devices: length = 0.18, 0.27, 0.36, 0.72 um.
1	37	SDI	In	CMOS level. Digital serial data input. ESD protected.
1	38	CK	In	CMOS level. Clock for shift registers. ESD protected.
1	39	CS	In	CMOS level. On falling edge of CS, data is latched into the shift registers. ESD protected.
1	40	RST	In	CMOS level. Gobal active low reset. ESD protected.
1	61	SDO	Out	CMOS level. Output of shift register. Tristated with CS. ESD protected.
1	62	TEST	In	Test pulse input. ESD protected.
80		**Total Pin**		

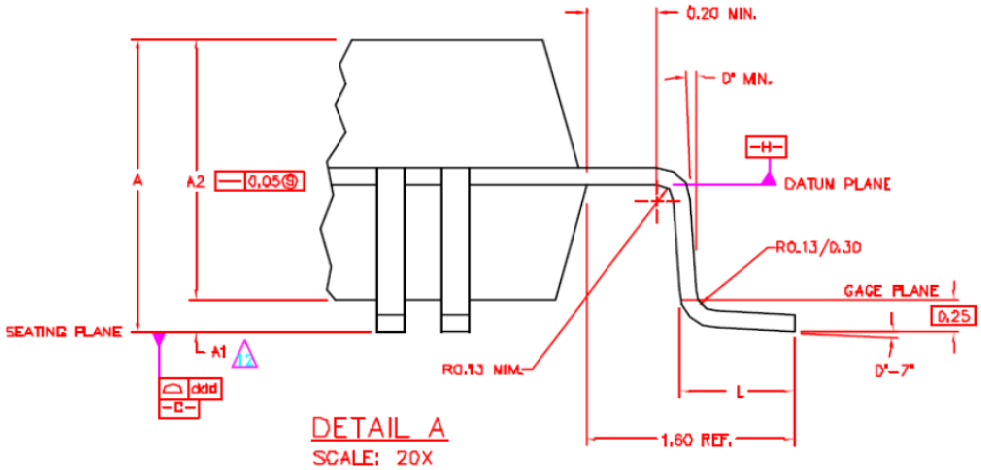
Packaging Information

Bonding Diagram



Package Name: LQFP80A
Package Cavity Size: 10.5 x 10.5 mm2
Downbond-to-substrate-package-pin-numbers: 21, 23, 25, 76, 78, 80
Min. bond pad size X: 78.04 um
Min. bond pad size Y: 78.04 um
Min. pad pitch: 192 um
Min. pad spacing: 113.96 um


REVISION HISTORY
ECN # REV DATE DESCRIPTION
98-159 A 09/24/98 NEW DRAWING
98-193 B 10/30/98 SEATING PLANE, BALL-DIMENSIONS
98-208 C 09/14/99 SEATING PLANE (0.08 to 0.25)
BOTTOM VIEW
TOP VIEW
SECTION A-A
SCALE: 40:1
SEE DETAIL A
MARKING AREA
8.59 SQ.
PIN 1
(4 PLCS)
14-16° ALL AROUND
(4 PLCS)
DO NOT SCALE DRAWING
OSE USA, Inc.
MARKETING OUTLINE DRAWING
14 X 14 X 2.0mm QFP
QFP-WPO-14S-XXX-01
NPO14S
1/2
4:1



DETAIL A
SCALE: 20X

SYMBOL	LEAD COUNT: FOOT PRINT 88; 3.2 FP			NOTE
	MIN.	NOM.	MAX.	
A	---	---	2.45	
A1	0.00	---	0.25	
A2	1.95	2.00	2.10	
D	17.20 BSC			
D1	14.00 BSC			
E	17.20 BSC			
E1	14.00 BSC			
L	0.73	0.88	1.03	
e	0.65 BSC			
b	0.22	---	0.38	
b1	0.22	0.30	0.33	
c	0.11	---	0.20	
c1	0.11	---	0.16	
	Tolerance of form and position			
aaa	0.20			
bbb	0.20			
ccc	0.13			
ddd	0.10			

SYMBOL	LEAD COUNT: FOOT PRINT 100; 3.2 FP			NOTE
	MIN.	NOM.	MAX.	
A	---	---	2.45	
A1	0.00	---	0.25	
A2	1.95	2.00	2.10	
D	17.20 BSC			
D1	14.00 BSC			
E	17.20 BSC			
E1	14.00 BSC			
L	0.73	0.88	1.03	
e	0.50 BSC			
b	0.17	0.22	0.27	
b1	0.17	0.20	0.23	
c	0.11	---	0.20	
c1	0.11	---	0.16	
	Tolerance of form and position			
aaa	0.20			
bbb	0.20			
ccc	0.08			
ddd	0.08			

REVISION HISTORY

ECN #	REV	DATE	DESCRIPTION
96-030	A	06/06/96	NEW DRAWING
98-193	B	10/30/98	STAND-OFF A1 CALL-OUT ADDED
99-206	C	02/14/99	STAND-OFF A1 (0.10 to 0.25)

NOTES:

1. ALL DIMENSIONS ARE IN MM. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982.
2. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE BODY SIZE BY AS MUCH AS 0.20.
3. DATUMS A-B AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
4. TO BE DETERMINED AT SEATING PLANE -C-.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
6. SURFACE FINISH OF THE PACKAGE IS #24-27 CHARMILLE (1.6-2.3 $\mu m R_a$). PIN 1 AND EJECTOR PIN MAY BE LESS THAN 0.1 $\mu m R_a$.
7. DAMBAR REMOVAL: PROTRUSION DOES NOT EXCEED 0.08. INTRUSION DOES NOT EXCEED 0.03.
8. BURR: BURR DOES NOT EXCEED 0.08 IN ANY DIRECTION.
9. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 FOR 0.40 AND 0.50 PITCH PACKAGE.
10. CORNER RADIUS OF PLASTIC BODY DOES NOT EXCEED 0.20.
11. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25 FROM THE LEAD TIP.
12. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
13. FINISH OF LEADS IS TIN/LEAD PLATED.
14. ALL SPECIFICATIONS AND DIMENSIONS ARE SUBJECTED TO IPAC'S MANUFACTURING PROCESS FLOW AND MATERIALS.
15. THE PACKAGES DESCRIBED IN THIS DRAWING CONFORM TO JEDEC MO-108C AND MS-022B. WHERE DESCREPANCIES BETWEEN THE JEDEC AND IPAC DOCUMENTS EXIST, THIS DRAWING WILL TAKE THE PRECEDENCE.

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DRAFTSMAN: Louie Rezendes DATE: 06/06/96
CHECKER: Dennis Leung DATE: 10/30/98
APPROVED: DATE:
APPROVED: DATE:

TITLE: MARKETING OUTLINE DRAWING
14 X 14 X 2.0mm QFP

DRAWING NO: QFP-MPO-145-XXX-01
REV: C
PAGE: 2/2
SCALE: NONE

DO NOT SCALE DRAWING
ACAD FILENAME: MPO145