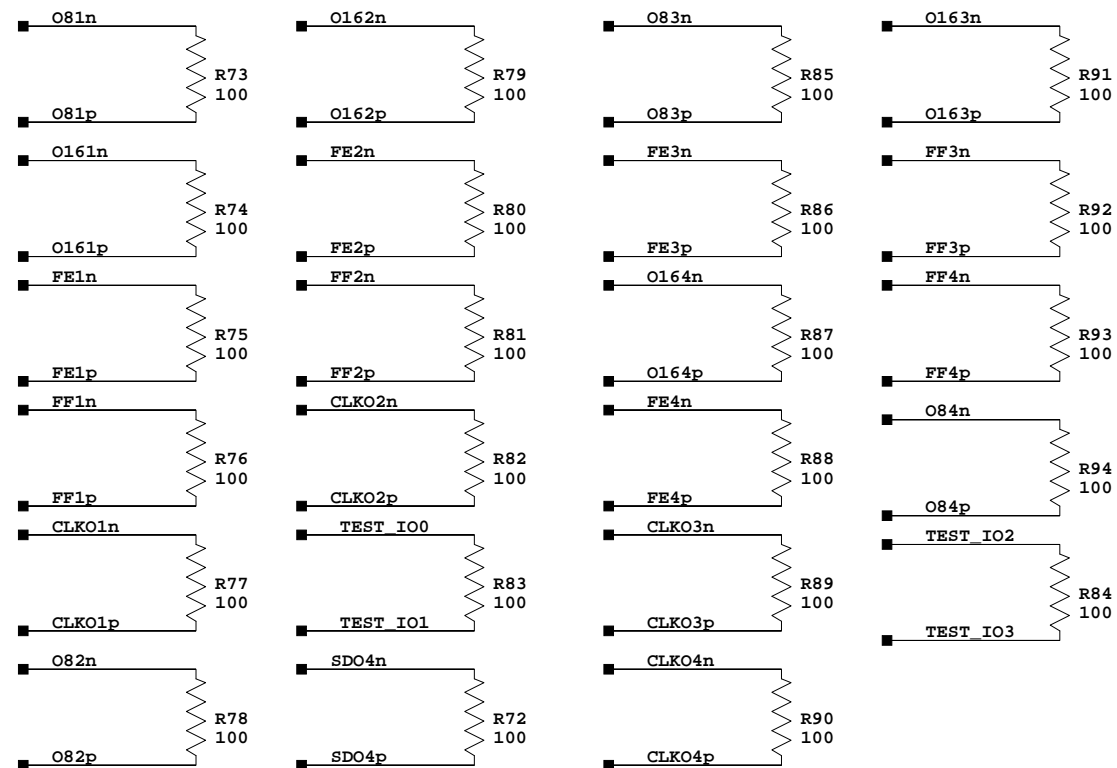


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081n		ADC_FD_0_N[0]	ADC_FD_2_N[0]	083n	
081p	AF5	ADC_FD_0_P[0]	ADC_FD_2_P[0]	083p	
0161n	AF4	ADC_FD_0_N[1]	ADC_FD_2_N[1]	0163n	
0161p	AE6	ADC_FD_0_P[1]	ADC_FD_2_P[1]	0163p	
FE1n	AE5	ADC_FE_N[0]	ADC_FE_N[2]	FE3n	
FE1p	AF8	ADC_FE_P[0]	ADC_FE_P[2]	FE3p	
FF1n	AF7	ADC_FF_N[0]	ADC_FF_N[2]	FF3n	
FF1p	AF10	ADC_FF_P[0]	ADC_FF_P[2]	FF3p	
CLK1n	AE10	ADC_CLK_N[0]	ADC_CLK_N[2]	CLK3n	
CLK1p	AC24	ADC_CLK_P[0]	ADC_CLK_P[2]	CLK3p	
CS_SR1n	AC23	ADC_CS_N[0]	ADC_CS_N[2]	CS_SR3n	
CS_SR1p	AC26	ADC_CS_P[0]	ADC_CS_P[2]	CS_SR3p	
SYNC1n	AC25	ADC_SYNC_N[0]	ADC_SYNC_N[2]	SYNC3n	
SYNC1p	AB24	ADC_SYNC_P[0]	ADC_SYNC_P[2]	SYNC3p	
CLK01n	AB23	MISC_I_L_N[0]	MISC_I_L_N[2]	CLK03n	
CLK01p	AF6	MISC_I_L_P[0]	MISC_I_L_P[2]	CLK03p	
	AE7				
082n		ADC_FD_1_N[0]	ADC_FD_3_N[0]	084n	
082p	AF16	ADC_FD_1_P[0]	ADC_FD_3_P[0]	084p	
0162n	AF15	ADC_FD_1_N[1]	ADC_FD_3_N[1]	0164n	
0162p	AE15	ADC_FD_1_P[1]	ADC_FD_3_P[1]	0164p	
FE2n	AE14	ADC_FE_N[1]	ADC_FE_N[3]	FE4n	
FE2p	AF17	ADC_FE_P[1]	ADC_FE_P[3]	FE4p	
FF2n	AE17	ADC_FF_N[1]	ADC_FF_N[3]	FF4n	
FF2p	AF19	ADC_FF_P[1]	ADC_FF_P[3]	FF4p	
CLK2n	AE19	ADC_CLK_N[1]	ADC_CLK_N[3]	CLK4n	
CLK2p	W25	ADC_CLK_P[1]	ADC_CLK_P[3]	CLK4p	
CS_SR2n	W24	ADC_CS_N[1]	ADC_CS_N[3]	CS_SR4n	
CS_SR2p	AA24	ADC_CS_P[1]	ADC_CS_P[3]	CS_SR4p	
SYNC2n	AA23	ADC_SYNC_N[1]	ADC_SYNC_N[3]	SYNC4n	
SYNC2p	V24	ADC_SYNC_P[1]	ADC_SYNC_P[3]	SYNC4p	
CLK02n	V23	MISC_I_L_N[1]	MISC_I_L_N[3]	CLK04n	
CLK02p	AE21	MISC_I_L_P[1]	MISC_I_L_P[3]	CLK04p	
	AD20				
CLK_STRBn		ADC_STRB_L_N	FE_RST_L	RST_FE	
CLK_STRBp	AD26	ADC_STRB_L_P	FE_CS_L	CS_FE	
	AD25		FE_CK_L	CK_FE	
SDI_GR1n		ADC_SDI_L_N	FE_SDI_L	SDI_L_FE_IN	
SDI_GR1p	AE26	ADC_SDI_L_P	FE_SDO_L	SDO_L	
	AE25				
SDO4n		ADC_SDO_L_N	TEST_I00	TEST_I00	
SDO4p	AF25	ADC_SDO_L_P	TEST_I01	TEST_I01	
	AF24		TEST_I02	TEST_I02	
			TEST_I03	TEST_I03	

## LVDS TERMINATION

### PLACE UNDER FPGA

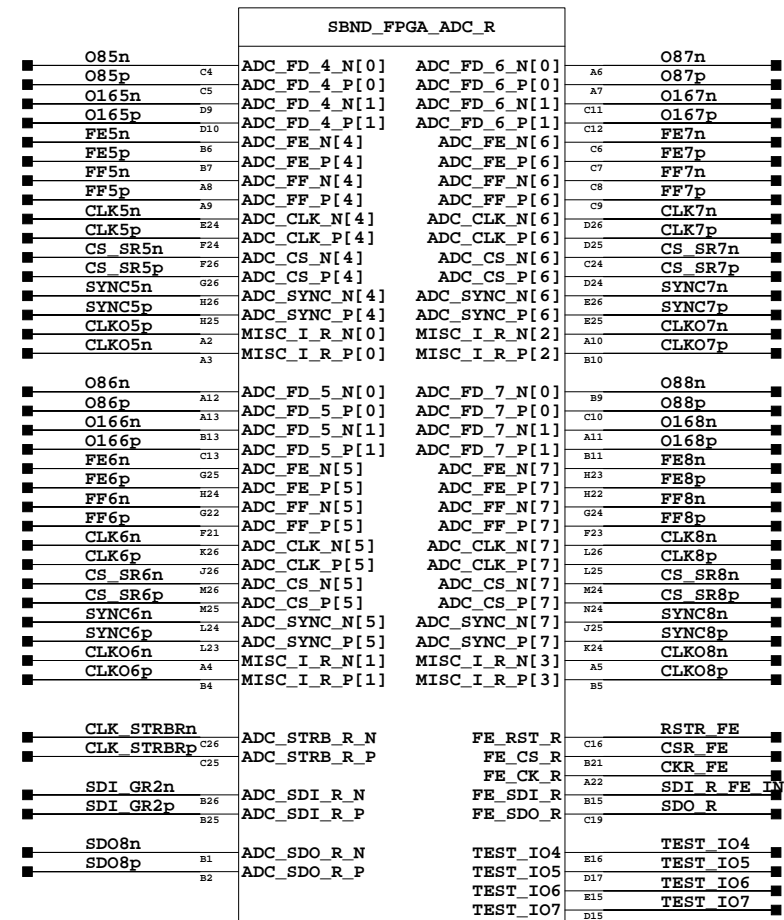
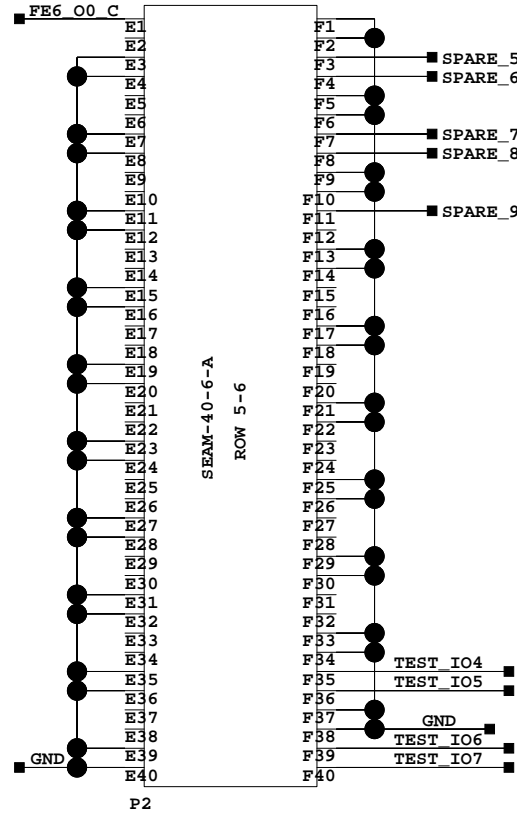
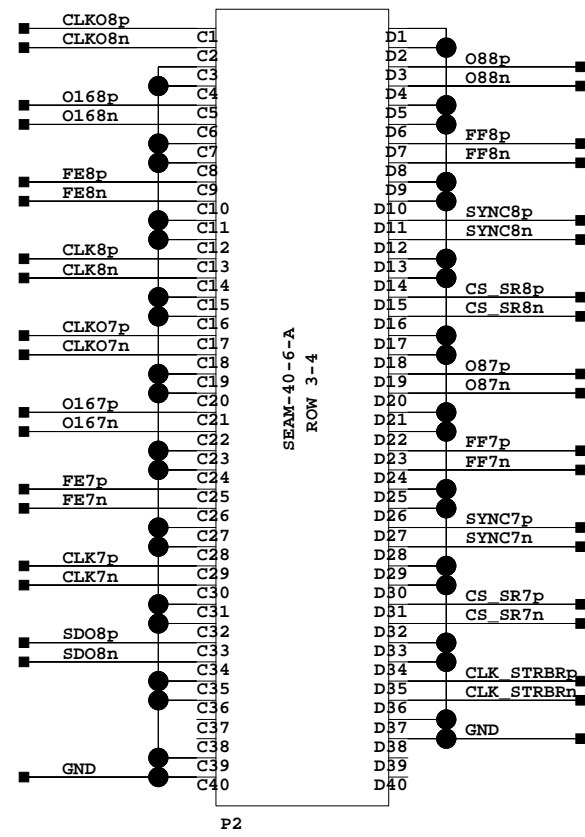
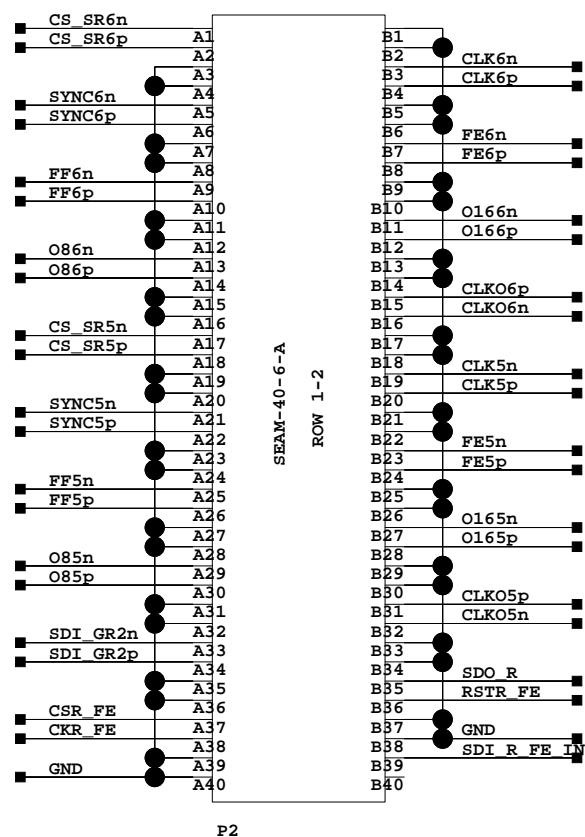


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SBND\_ADC\_IO\_L

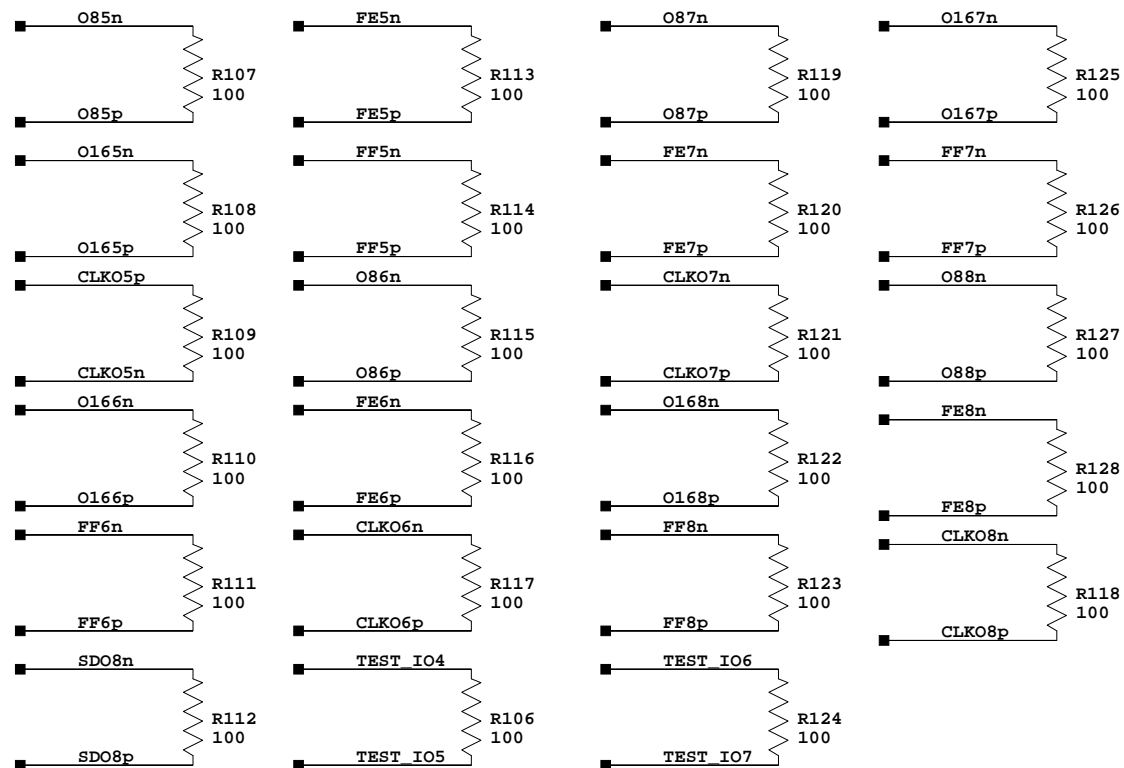
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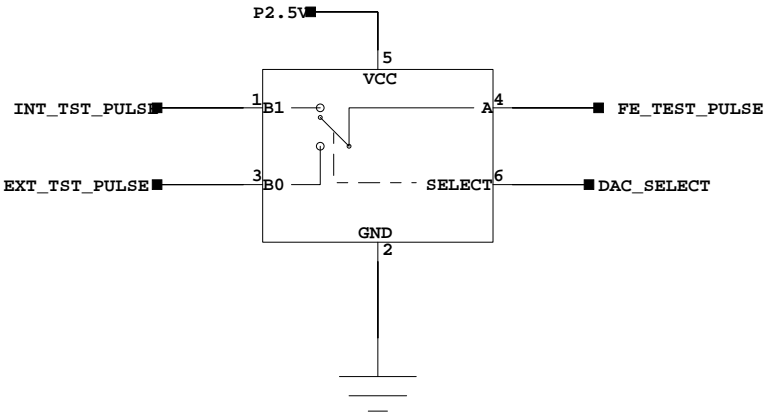
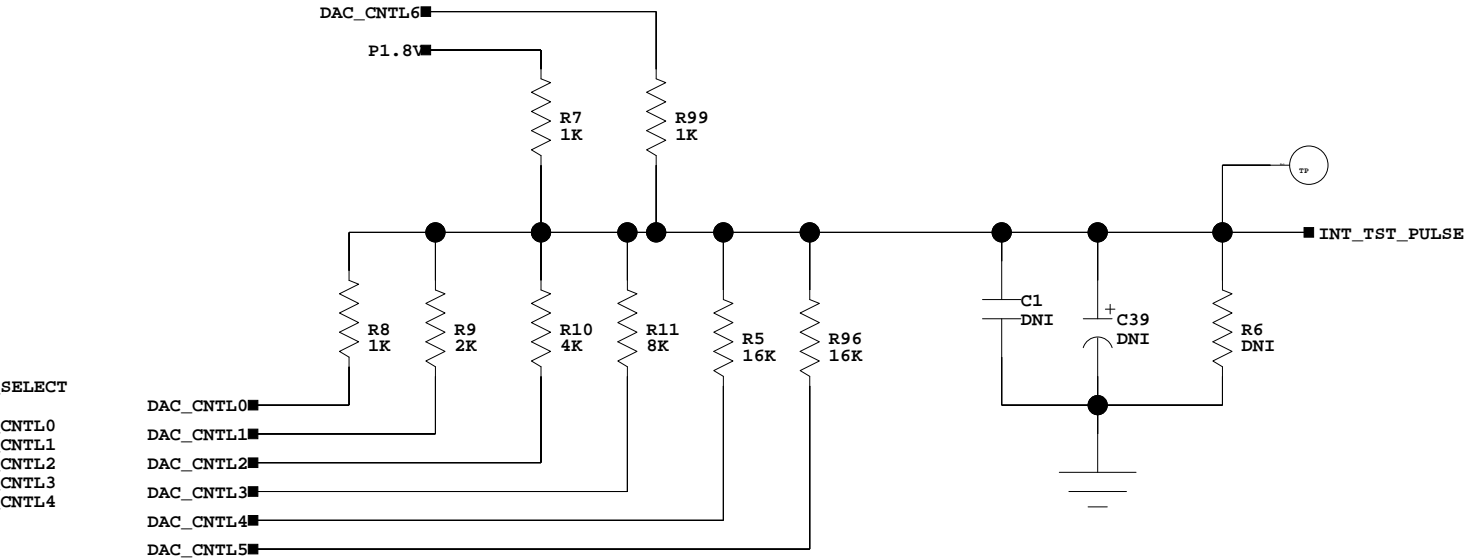
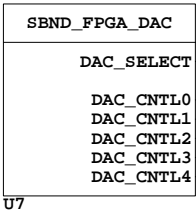
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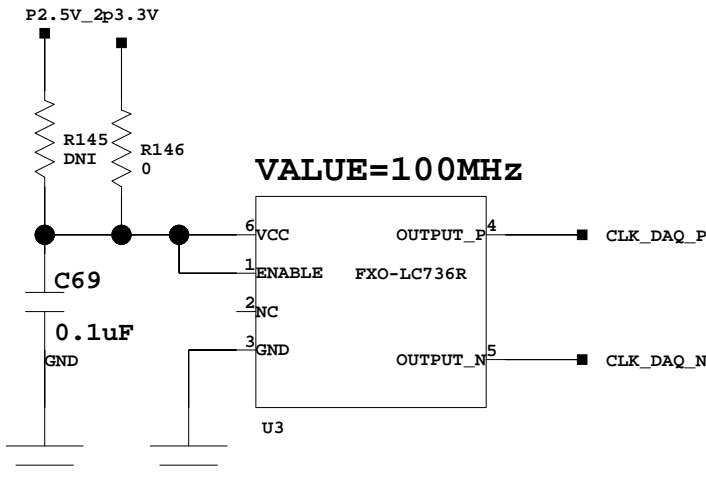
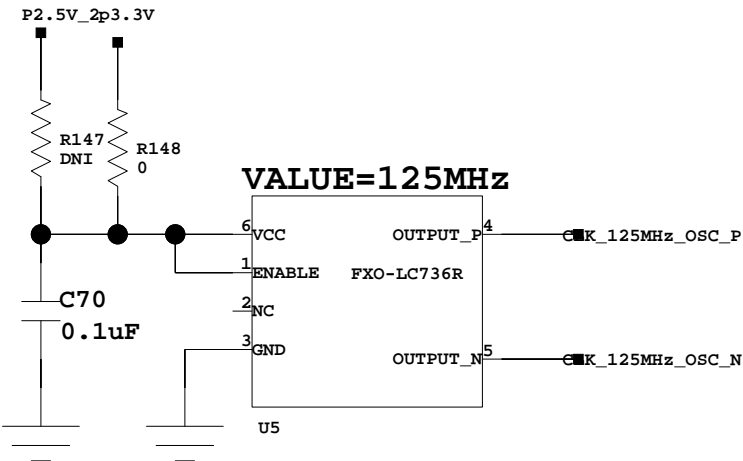
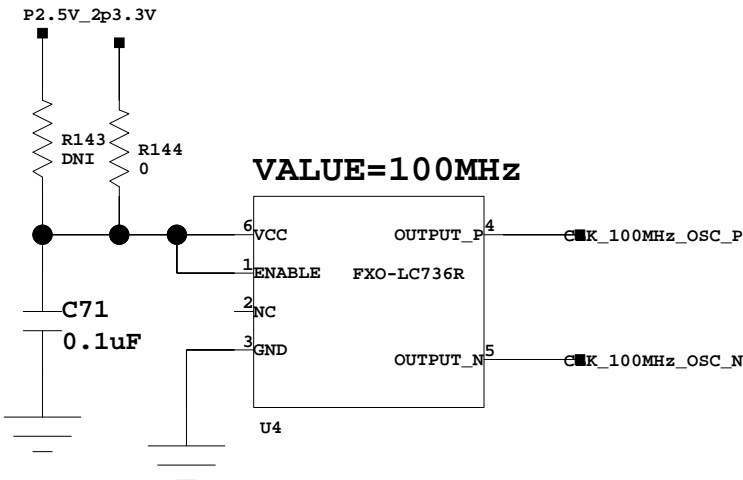


# LVDS TERMINATION

## PLACE UNDER FPGA

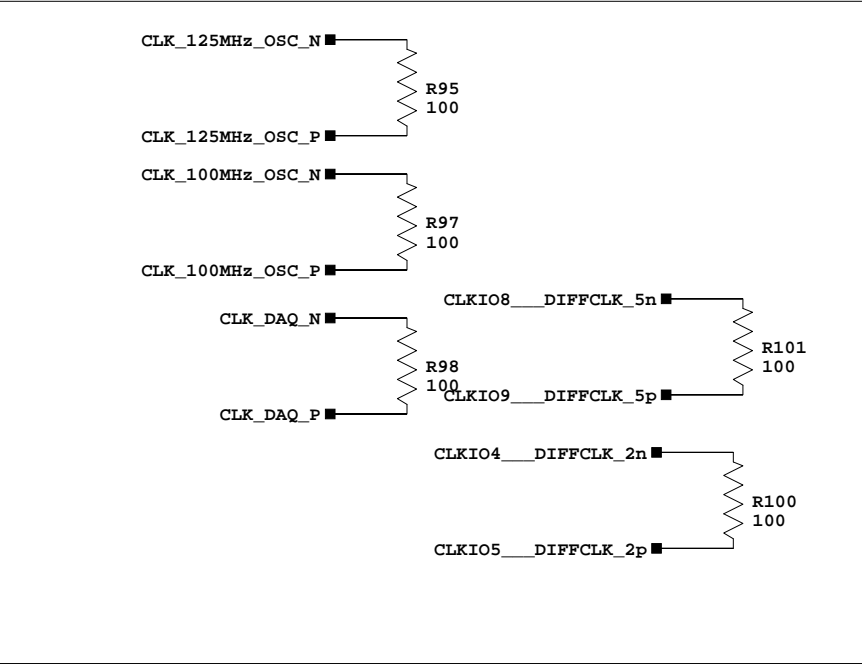






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SBND_CLK_T_N U9	CLK_125MHz_OSC_N
SBND_CLK_T_P T9	CLK_125MHz_OSC_P
CLK_125MHz_OSC_N K9	CLK_125M_spare_N
CLK_125MHz_OSC_P L9	CLK_125M_spare_P
CLK_100MHz_OSC_N T15	CLK_100MHz_OSC_N
CLK_100MHz_OSC_P T14	CLK_100MHz_OSC_P
CLK_DAQ_N N26	CLK_DAQ_N
CLK_DAQ_P N25	CLK_DAQ_P
CLK_DAQ_N L14	CLK_EXT_N
CLK_DAQ_P L15	CLK_EXT_P
CLK_100MHz_OSC_N K10	REFCLK4n
CLK_100MHz_OSC_P L10	REFCLK4p
I2C_SCL_DIF U10	REFCLK1n
I2C_SCL_DIF T10	REFCLK1p
CLKIO4__DIFFCLK_2n P26	CLKIO4__DIFFCLK_2n
CLKIO5__DIFFCLK_2p R26	CLKIO5__DIFFCLK_2p
CLKIO8__DIFFCLK_5n A14	CLKIO8__DIFFCLK_5n
CLKIO9__DIFFCLK_5p B14	CLKIO9__DIFFCLK_5p

U7



UNDER FPGA



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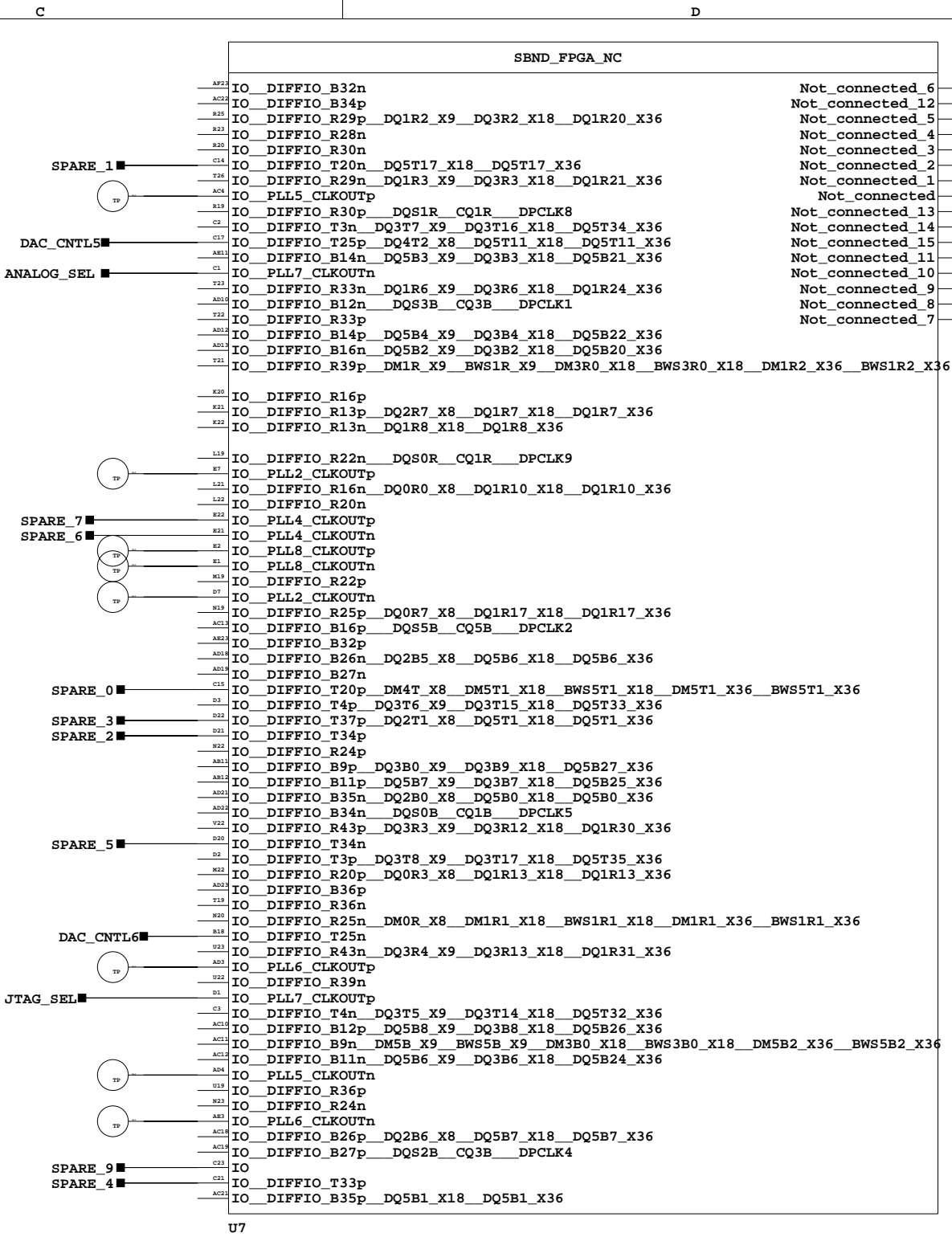
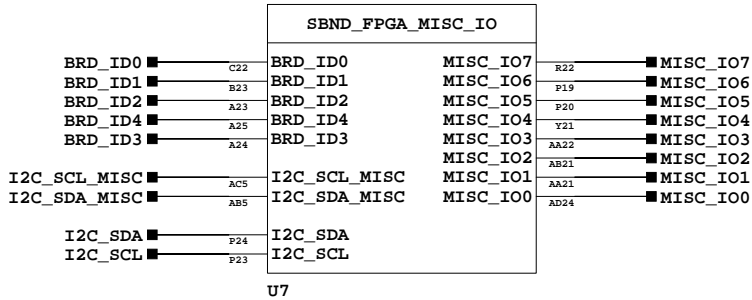
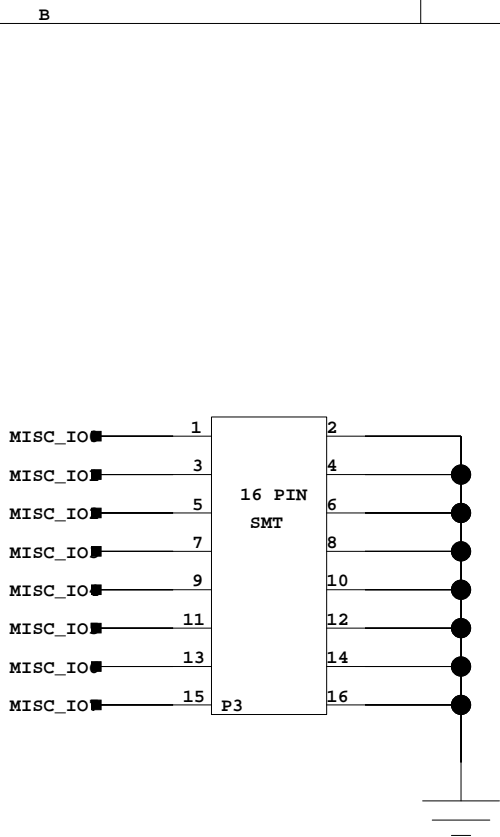
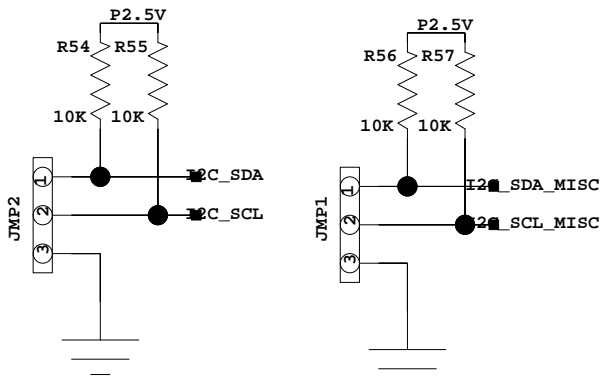
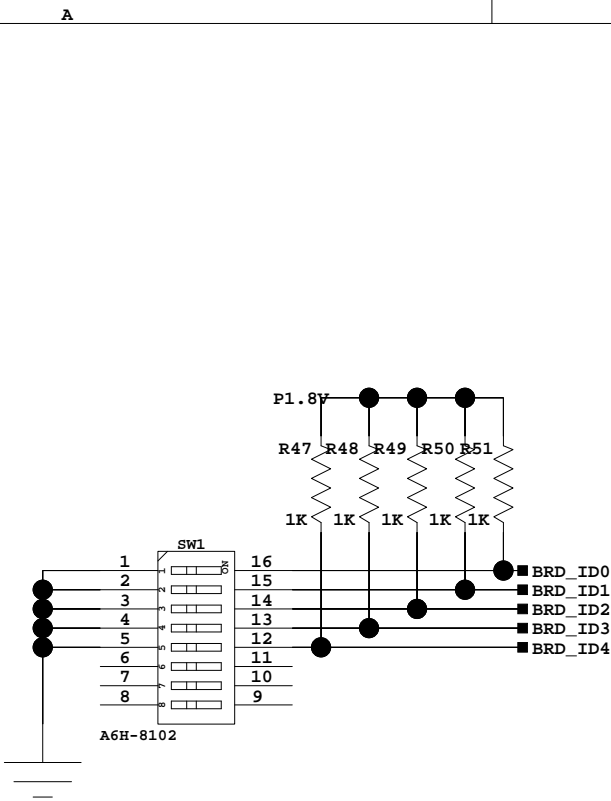
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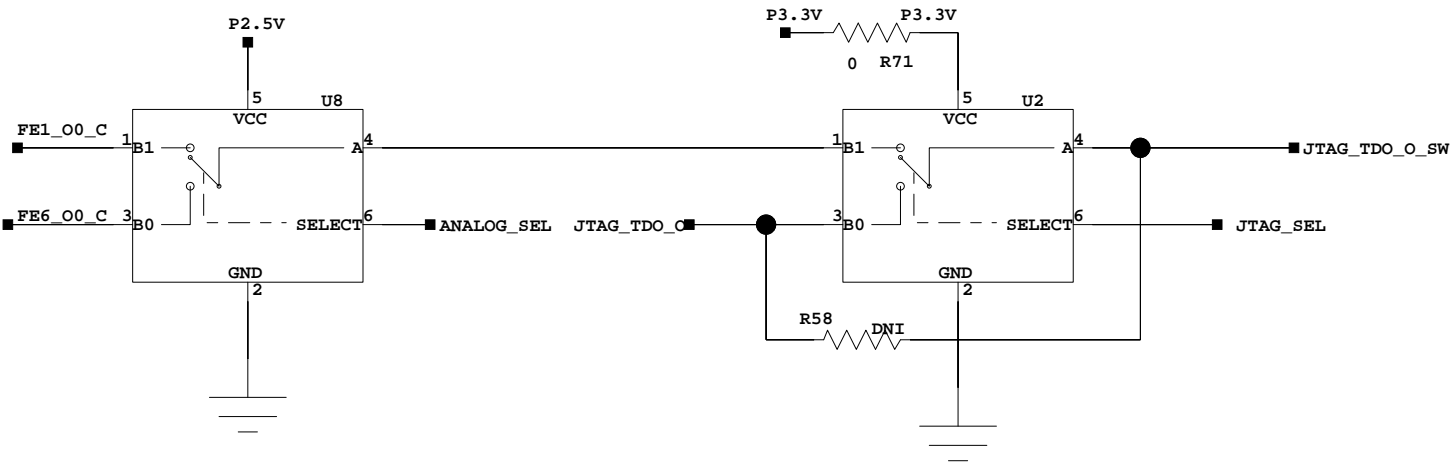
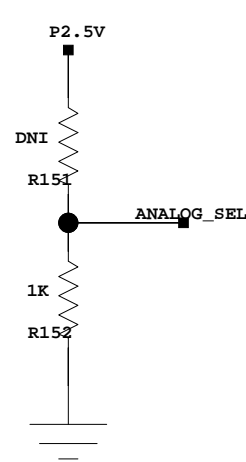
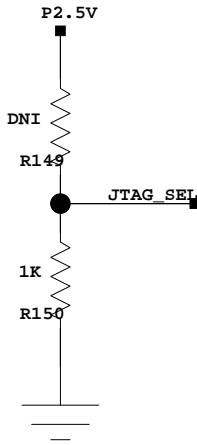
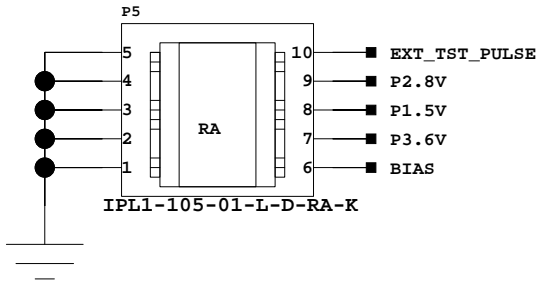
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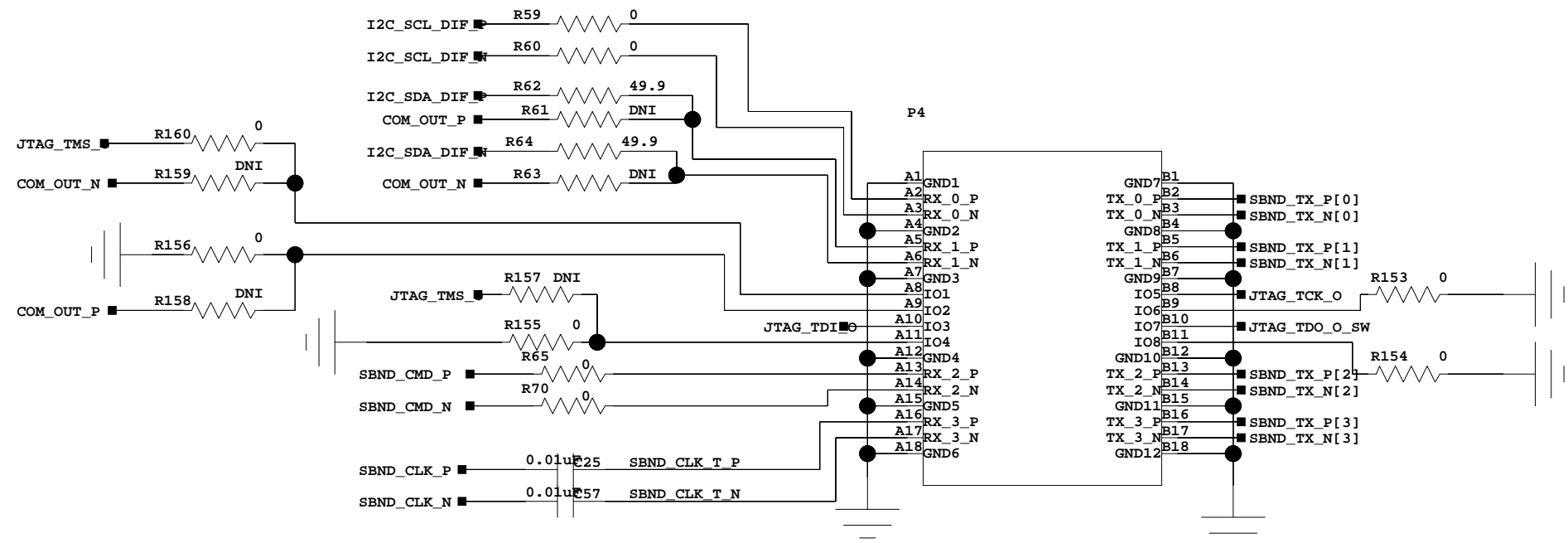
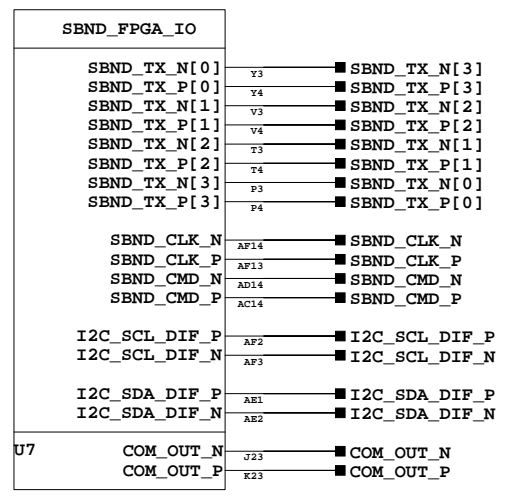
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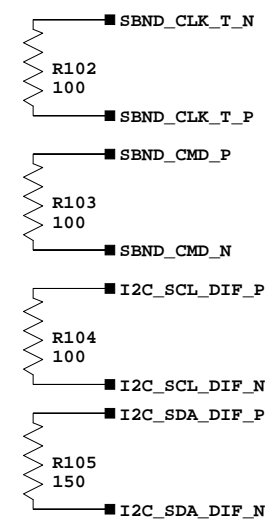
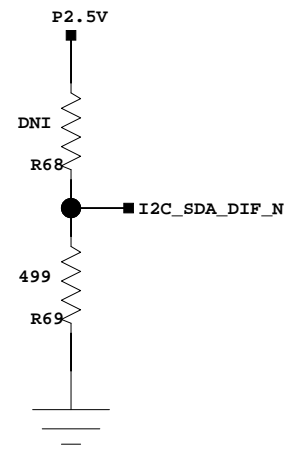
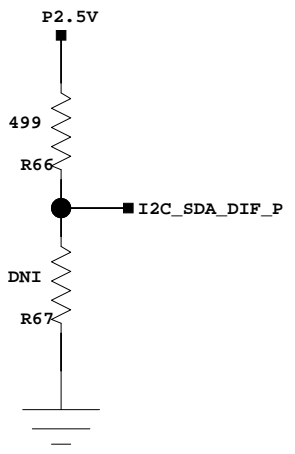
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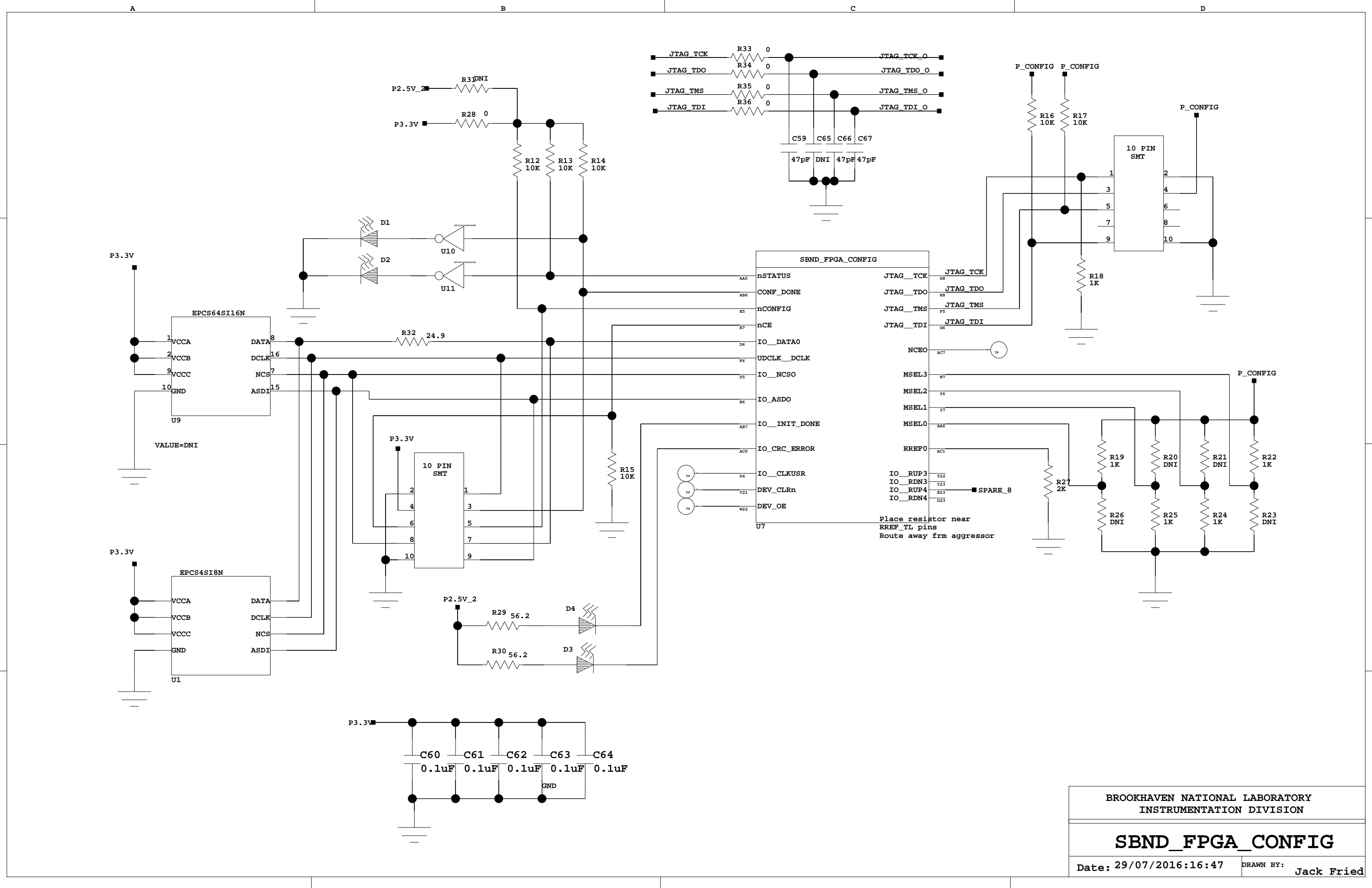
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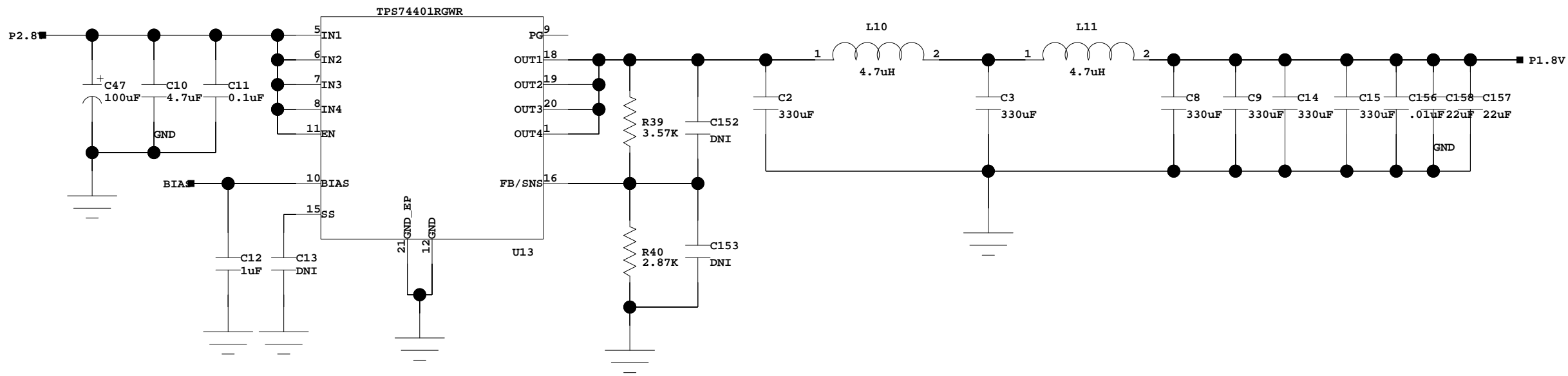
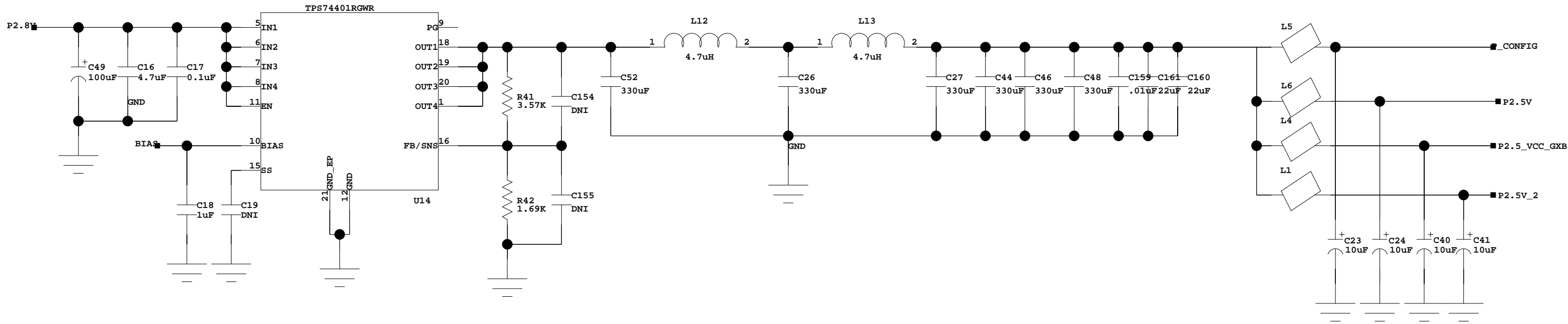
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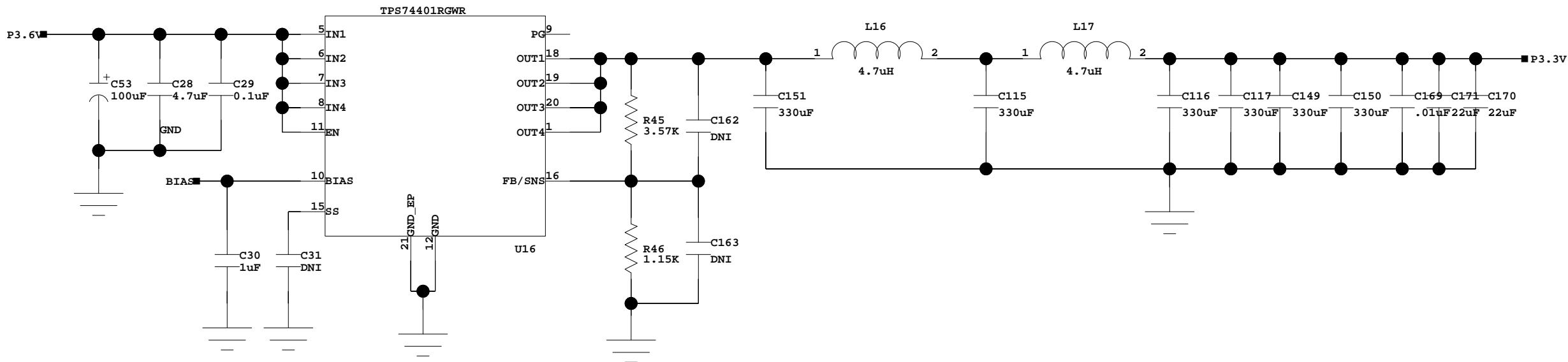
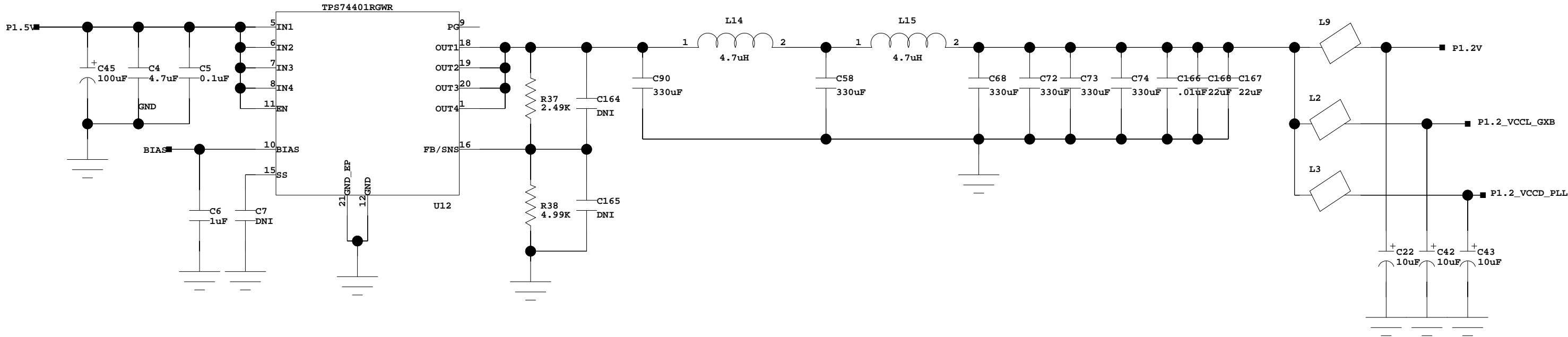


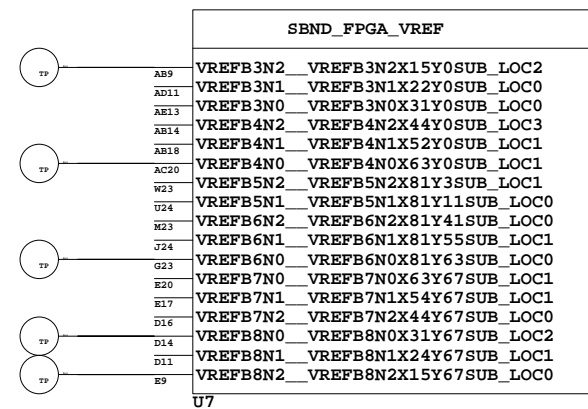
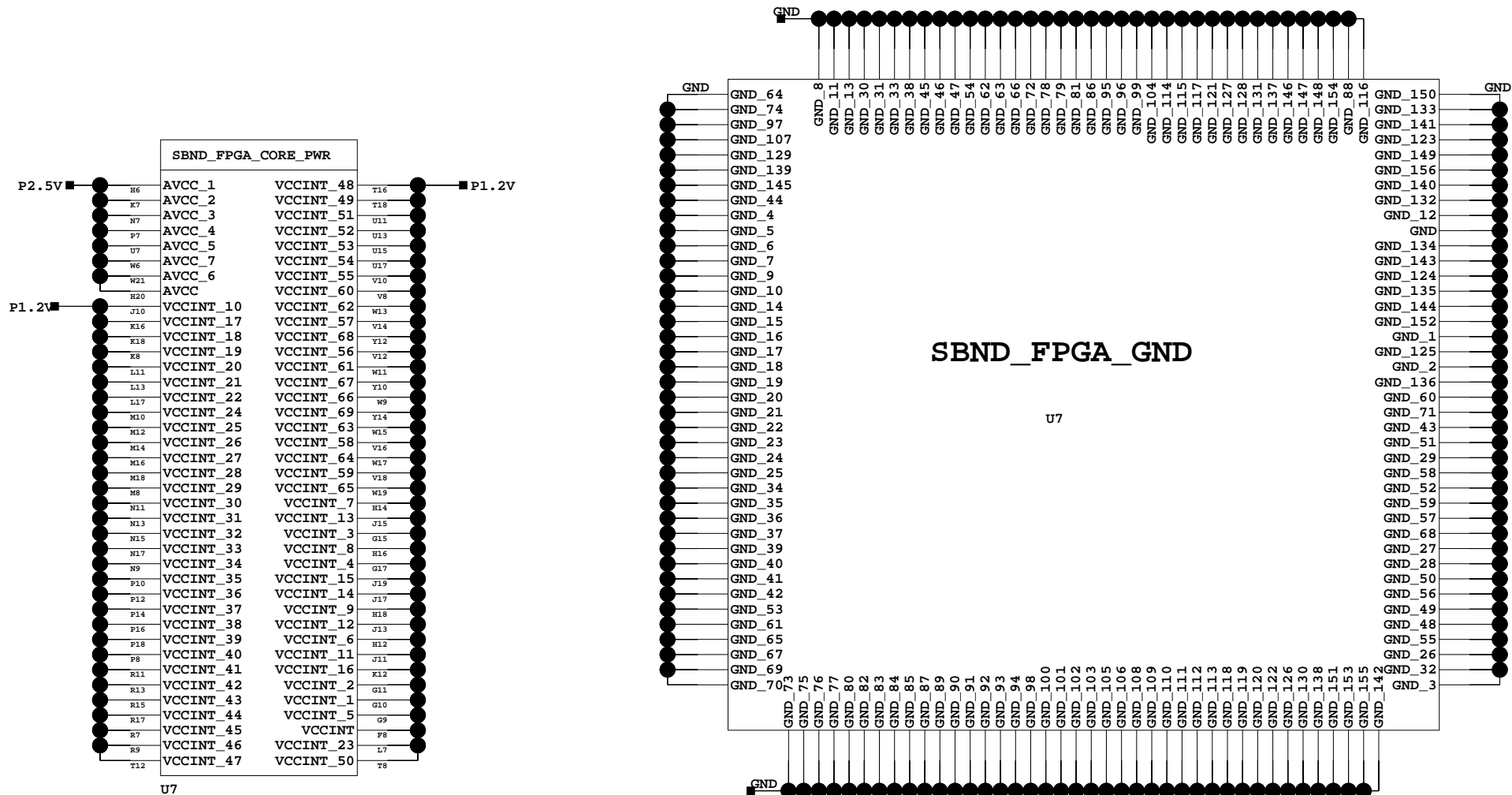
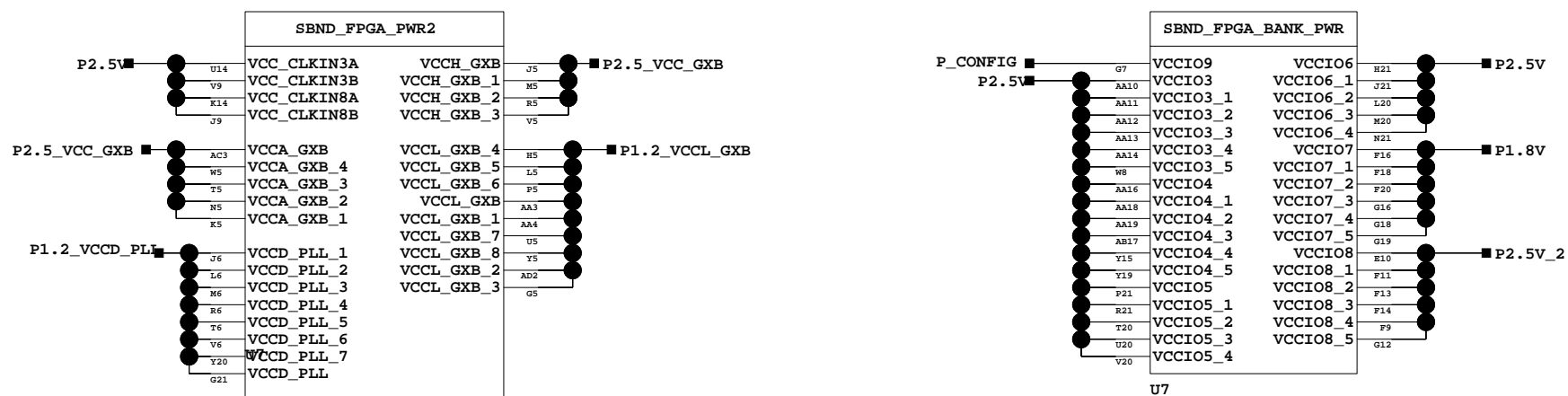
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## SBND\_PWR\_1

Date: 29/07/2016:16:48

DRAWN BY:  
Jack Fried





## SBND\_FPGA\_PWR

