ADC ASIC7 – Rev 1.3

Revision Notes

Pin CLK_STRB was renamed to SCK. Pin 43 (FIFO_DVDD) in Table 4 was updated to match the ASIC pinout in Figure 10.

Status

7/11/2016 : The ASIC is in fabrication.

Introduction

A 16-channel analog to digital converter ASIC (ADC ASIC) was developed to digitize signals from the front-end of a Liquid Argon Time Projection Chamber with a resolution of 10-12 bits. The ADC converts at rates up to 2MS/s and the data can be multiplexed on two 8:1 serial LVDS outputs or one 16:1 serial LVDS output during readout by a data acquisition system.

- **Analog to Digital Converters (ADC)** : 16 channels
  - Input buffer with offset compensation
  - 12-bit ADC
  - Bias generator
  - Pattern generator: Selectable internal or external clock source.
  - Input Signal Range: 1.4 V (0.2~1.6V)
  - Input impedance > 10 MΩ
  - Input Capacitance ~ 1pF + 1pF (package capacitance)
- **First in First out (FIFO)**
  - 32 bits deep (Storage of 32 samples)
  - 192 bits wide (16 channels * 12 bits)
  - FIFO Full indicator flag
  - FIFO empty indicator flag
- **Power**
  - ADC : ~ 3.6 mW/ch
  - Input buffer: ~ 1.28mW/ch
  - FIFO: ~ 1mW
  - Other Circuitry: ~ 0.8 mW + 66 µW
- **Layout size** 4.6 × 6.0 mm²
- **Die cut size** 4.520 × 6.103 mm²
- **Pad count, size, pitch** 80, 78.04 × 78.04 µm², 192 µm (top/bottom) and 279 µm (sides)
- **Technology** : CMOS 0.18µm – 1.8V, 1-poly, 6-metal, MiM cap, sil blk resistors

ADC Block

- The ASIC is composed of 2 blocks, an ADC and a FIFO block.
  - Each of the 16 ADC channels has an input buffer which converts voltage to current. During the sampling phase, the input buffer samples the voltage (with a dynamic range of 0.2 V to 1.6 V) then provides a current output after compensating for offset voltage error. During the conversion, the ADC digitize the current from the buffer in two phases. In the first phase the 6 MSB bits are determined followed by the 6 LSB bits in the second phase. After the conversion, the thermometer code is converted to binary and latched in a buffer.
  - The data (192 bits) from the 16 ADC channels is transferred parallelly to the FIFO block (192 bits wide by 32 deep) on the rising edge of the internal write clock when bit F0 = 0. For test purposes the FIFO write clock is on pin IdxMp/n when bit F0 = 1.
  - At power-on or after a reset, data can be read from the ASIC starting at the third conversion cycle.
  - On the rising edge of ADC_CONV, a block of data (192 bits) is latched from the FIFO into the serial output buffer in one clock cycle (two rising edges of the 200MHz CLK). On subsequent falling edges of CLK, data is shifted out of the output shift register MSB first (MSBF) on pins D0p/n and D1p/n. On the falling edge of ADC_CONV the read address is incremented.
  - In the serial buffer the data length is increased to 200 bits. That is, two 4-bit metadata headers (1010) are added to the serial data string at bit positions 96-99 and 196-199. During readout, data is shifted out

MSBF and after 100 CLK cycles, the upper 100 bits are shifted out on pin D1p/n and the lower 100 bits on pin D0p/n. The four MSBs of each block is the header 1010.

- The ADC along with the input buffers are biased internally using a bias generator and a bangap voltage reference. The bangap voltage can be monitored and/or controlled externally on pin VBGR.
- Each ADC channel is configured locally by an 8 bit channel register. In addition, there is a 16 bit global register which sets the global configurations. Details on each bit can be found in Table 2 in the ASIC Configuration section.
- Multiple options are available to provide the ASIC signals for conversion. These options can be accessed by programming the appropriate bits in the shift register as listed in Table 2. The ADC has an internal pattern generator which is based on monostables. If this feature is enabled (CLK1:CLK0 = 00 or 11), it only needs a start of conversion signal to function. The FIFO has a digital generator which is based upon a 200 MHz clock. If the digital generator feature is enabled (CLK1:CLK0 = 10), then all clocks for the ADC and the FIFO can be generated by this block hence, providing the ability to run both blocks using a single external CLK. For test purposes, the conversion signals can be accessed from external pins when (CLK1:CLK0 =01).
- A power down (PD) feature is used to put the ADC into sleep mode so that very low power is consumed when the ADC is idle.
- The ADC has a set of DC current sinks which absorb constant offset current from the sample and hold. The amount of current absorbed is controlled by switches which are in turn controlled by 4 signals. The amount of offset current can be varied from 0 to 256 µA in 16 steps of 16 µA each.
- All digital inputs are LVDS except PD, CS,SDI, and SDO which are CMOS 1.8V.
- Figure 1 shows the functional block diagram of the ASIC and Figure 2 shows the timing diagram of the ADC.

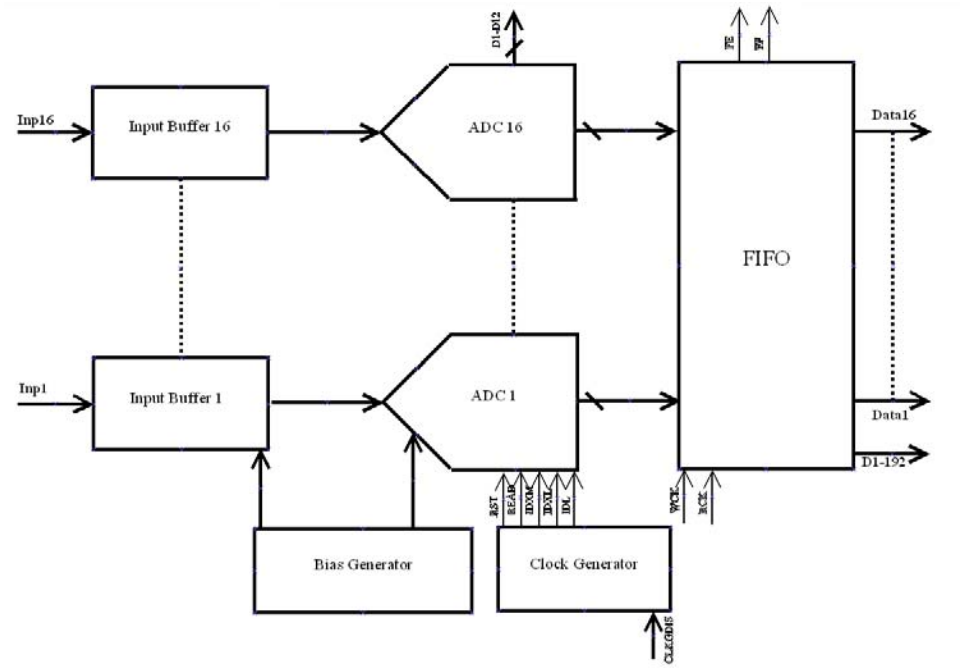


Figure 1 Functional Block Diagram

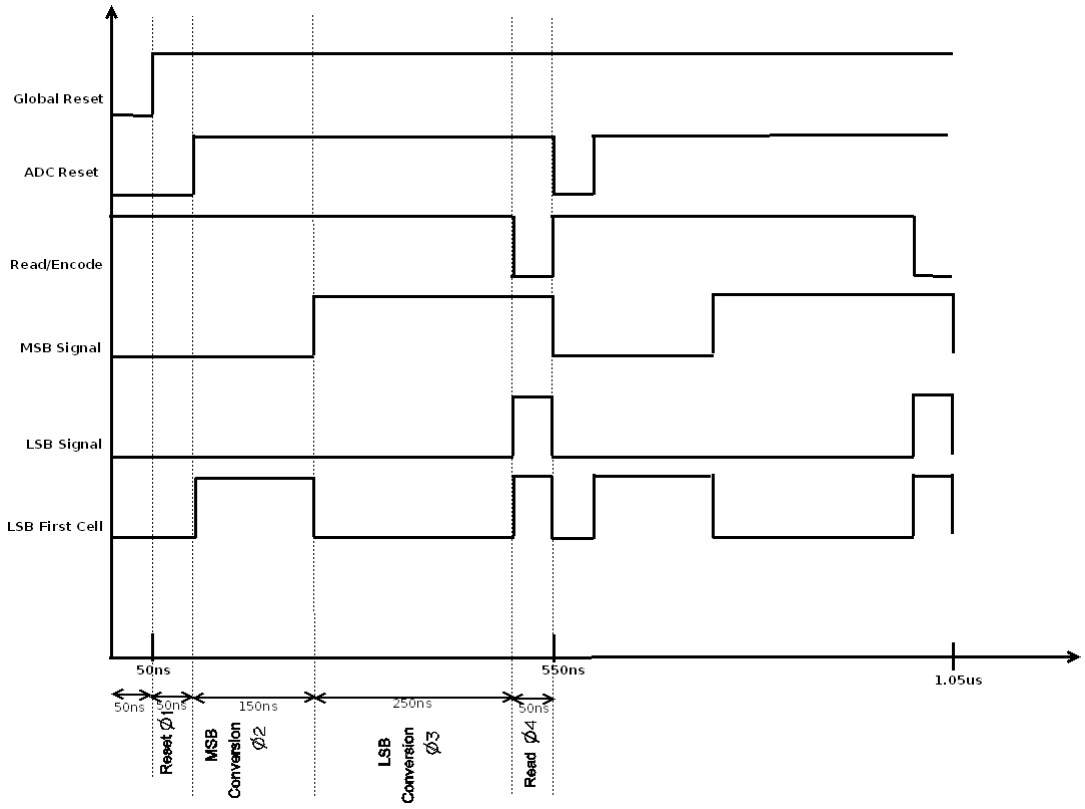


Figure 2 ADC Timing Diagram

FIFO Block

The FIFO block is comprised of a memory module and a controller. The memory module is 192 bits wide by 32 bits deep. A block diagram of the ADC controller is shown in Figure 3. The controller interface consists of LVDS inputs CLKp/n (200 MHz clock), ADC_CONVp/n (2 MHz ADC convert), and CMOS 1.8V inputs SCK and CS (chip select). The LVDS outputs are Clkop/n (regenerated 200 MHz clock), D0p/n (lower 100 data bits), D1p/n (upper 100 data bits),and ADC_BUSYp/n (which goes high 1.5ns after the first CLK rising edge during the ADC conversion cycle). A description of these I/Os can be found in the ASIC pin list (Table 4). The controller generates soft and global reset signals, SPI configuration signals, and convert/readout signals for the ASIC.

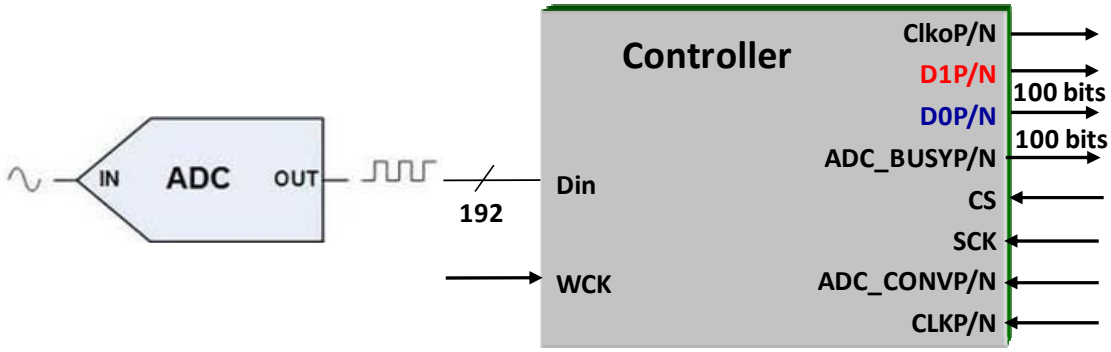


Figure 3 Block diagram of the ADC and the controller

ASIC Reset

The controller generates global and soft resets for the SPI registers and the control logic. The generation of an active low soft reset or a global reset is illustrated in Figure 4. When CS is high, a soft reset is generated which resets the control logic only. When SCK is high, a falling edge on CS generates a global reset which resets the control logic, the SPI and configuration buffer, ADC latches, and the serial output buffer. The controller default status at power up or after a reset (soft or global) is ADC data conversion and readout.

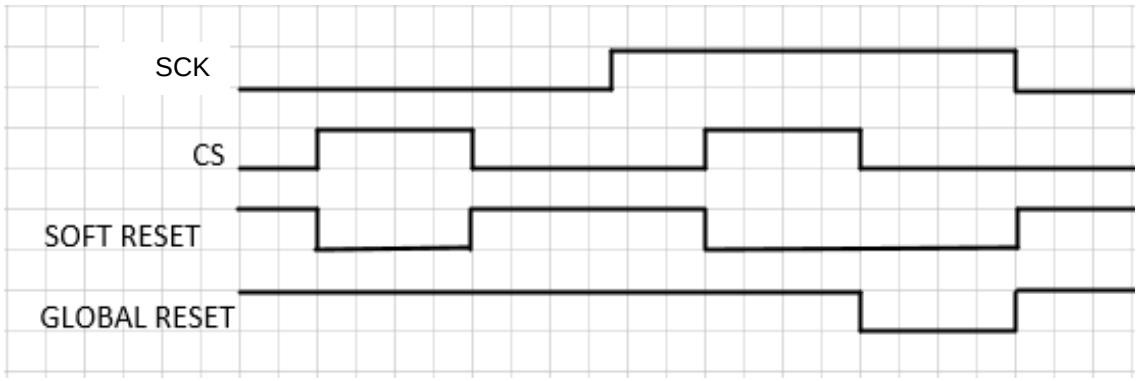


Figure 4 Generation of active low soft and global reset

Summary of global and soft reset procedure

- Soft reset: whenever CS = 1
- Global reset: SCK = 1 and falling edge of CS
- Normal operation: CS = 0 and SCK = 0

ASIC Configuration

A simplified timing diagram is shown in Figure 5 where 3-bits (101) are written to the SPI. When CS is high, the controller puts the ASIC in configuration mode. While CS is high, data is shifted most significant bit first (MSBF) into the SPI registers on CMOS pin SDI on the falling edge of CMOS pin SCK. The falling edge of CS latches the SPI register content into the configuration BUFFER. A second write to the SPI register put the previous write data on pin SDO.

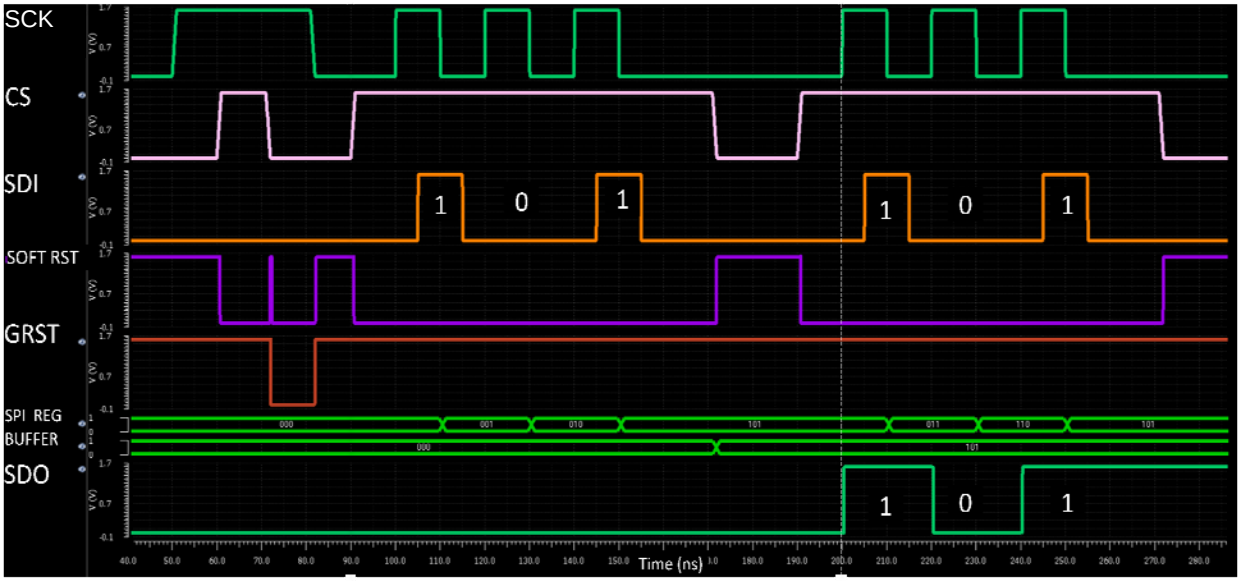


Figure 5 Timing diagram of a 3-bit SPI. Writing and reading the SPI with 101

Summary of configuration procedure

- Send a rising edge on pin CS
- Shift data on pin SDI into SPI register MSBF on the falling edge of pin SCK
- After shifting in the entire string, a falling edge on CS copy the SPI register into the configuration BUFFER
- A second write to the SPI register put the previous write data on pin SDO with a half clock shift
- The ASIC has total of 144 SPI bits (16 channels x 8 bits + 16 global bits)

Figure 6 is an illustration of the order of the SPI configuration bits. The SPI register has a total of 144 bits with bit0 (CLK0) in the global register as the LSB and bit143 (TSTIN) in channel 16 as the MSB. The order of the channel register bits and global register bits is listed in Table 1 and a register map is presented in Table 2.

Figure 6 Shift Register Loading. The global register and the channel registers are concatenated to form the SPI register.

Table 1. Channel and Global Register Map

	S0	S1	S2	S3	S4	S5	S6	S7
Channel	D0	D1	D2	D3	PCSR	PDSR	SLP	TSTIN
Global	F4	F5	sLSB	RES4	RES3	RES2	RES1	RES0
Global	CLK0	CLK1	FRQC	EN_GR	F0	F1	F2	F3

Table 2 ASIC configuration register map. The channel numbers (ch) are from 1 to 16

Channel Register Bit Name	**Bit Position**	**Default Value**	**Description**
TSTIN	16+7+(ch - 1)*8	0	1 = Test input is digitized, 0 = FE Input is digitized.
SLP	16+6+(ch - 1)*8	0	1=ADC is in sleep mode, 0=ADC is operating normally.
PDSR	16+5+(ch - 1)*8	0	If PCSR is 0, 1=PD is set high. 0=PD is set low.
PCSR	16+4+(ch - 1)*8	0	1 = PD can be controlled externally. 0= PD is controlled by PDSR
D3:D0	16+3:0+(ch -1)*8	0	Decoded into 16 signals decides the amount of offset current to be drawn from the sample and hold. 00 = 32 LSB step = 32 LSB. Each LSB is 500 nA.
Global Register Bit Name	**Bit Position**	**Default Value**	**Description**
RES4:0	15:11	0	These bits are reserved
sLSB	10	0	LSB current steering mode control. 0 = full, 1 = partial
F5	9	0	F5=0, ADC data is selected and pipelined. F5=1, test data is selected and pipelined. **See Figure 7.**
F4	8	0	F4=0, bit F5 controls the pipeline. F4=1, CMOS pins CS and SCK controls the pipeline. **See Table 3 for V*.** CS= 0 & SCK = 0, ADC data is selected and pipelined. CS= 0 & SCK =1, test data is selected and pipelined. **See Figure 7.**
F3	7	0	F3=0, IDL falling edge is delayed of 5-10ns after IDXM rising edge. F3=1, delay of 1 clock cycle on LVDS pin CLK
F2	6	0	F2=0, the signal generator is on. F2=1, the signal generator is off.
F1	5	0	F1=0, a rising edge on LVDS pin ADC_CONV starts the sampling and readout. F1 = 1, the readout is compatible to V* version
F0	4		F0 = 0, the ADC write clock is generated internally. F0=1, the ADC write clock is on LVDS pin IDXM
EN_GR	3	0	0= Disables offset current absorption. 1=Enables the offset current absorption.
FRQC	2	0	Frequency of internal clock generator 1=2 MHz 0=1 MHz
CLK1:CLK0	1:0	0	00 or 11 = ADC clocks from monostable, 01 = ADC external clocks, 10 = ADC clocks from digital generator of FIFO
Total	**144 Bits**		**128 channel bits and 16 global bits**

ASIC Readout

Pins CS, SCK, and SDI are kept low during readout. A rising edge on Pin ADC_CONV starts an ADC conversion cycle and latches previous conversion data from the FIFO into the serial output data buffer. The subsequent falling edge of ADC_CONV increments the FIFO read pointer. Output pin ADC_BUSY goes from low to high at the beginning of the conversion cycle then goes low after 485 ns. **The period of ADC_CONV must be greater than or equal to 500 ns.** The rising and falling edges on ADC_CONV will be accepted only if the ADC is idle. If the ADC is busy, both the rising and falling edges on ADC_CONV will be ignored. The ADC conversion cycle is configured by six global bits (F5:F0) as summarized in Table 2.

Figures 8 and 9 are timing diagram illustrations of the ADC conversion and readout for 500 ns period and 50% duty cycle on ADC_CONV. If the ADC is not busy a rising edge on ADC_CONV initiates (a) the ADC conversion cycle and (b) the readout cycle simultaneously.

a) ADC Conversion Cycle
ADC_CONV starts the ADC conversion cycle by asynchronously enabling the counter that generates the internal signals. That is, the counter only starts incrementing on the first rising edge of the 200MHz clock after the rising edge of ADC_CONV. ADC_BUSY goes high 1.5 ns after the first rising edge of the 200MHz clock. During the 485 ns window while the ADC is busy (AdcBusy = 1) any other rising and falling edge pairs on ADC_CONV will be ignored. The counter resets after 97 clock cycles (485ns) bringing ADC_BUSY low with it.

b) ADC Readout Cycle
In addition to the conversion, a rising edge on ADC_CONV initiates the readout cycle. After the rising edge on ADC_CONV, it takes one clock cycle (or the first two rising edges of the 200 MHz clock) to latch data from the DATA BUFFER into the SERIAL OUTPUT BUFFER. An example of the serial output buffer loaded with the test pattern is shown in Figure 7. Serial data is then shifted out MSBF on the subsequent falling edges of the 200 MHz clock on LVDS ports D1p/n and D0p/n. The lag time for data with respect to the falling edge of the 200 MHz clock is 1.6 ns. It should be noted that the MSB of the header on port D0 and D1 can become corrupt. Therefore, there are effectively 3 header bits available.

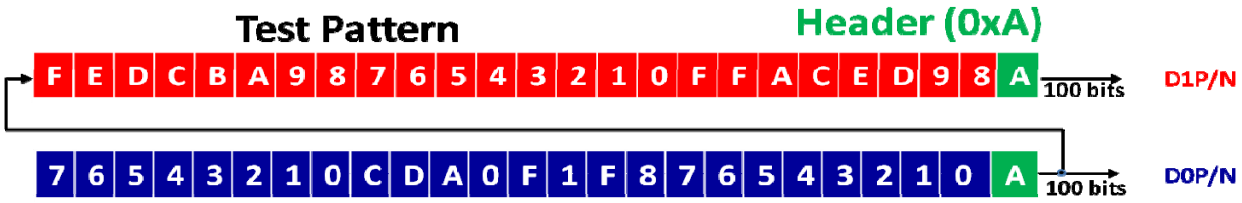


Figure 7 A frame of test pattern data plus nibble header (3 bits of nibble header are available 1010) leaded onto the serial output BUFFER

Summary of readout procedure

- Rising edge of ADC_CONV starts the conversion/readout cycle and latch data into the output serial BUFFER
- ADC_BUSY goes high 1.5 ns after the first rising edge of the 200MHz clock
- If the ADC is busy, all rising/falling edge pairs on ADC_CONV is ignored (not valid)
- Data latency of 3 valid rising edges on ADC_CONV
- The counter resets after 97 clock cycles (485 ns) to give the ASIC time to rearm
- Period of ADC_CONV ≥ 500 ns
- If the period of ADC_CONV < 500 ns, the header will be in the wrong location in the data stream
- Pulse width of ADC_CONV ≥ 50 ns
- If the pulse width of ADC_CONV is < 50ns, the data in the output data buffer will be overwritten with new data before readout of the sample is complete
- Data lag time with respect to the falling edge of the 200 MHz clock is 1.6 ns
- After the readout is complete the ASIC remains idle until another rising edge on ADC_CONV

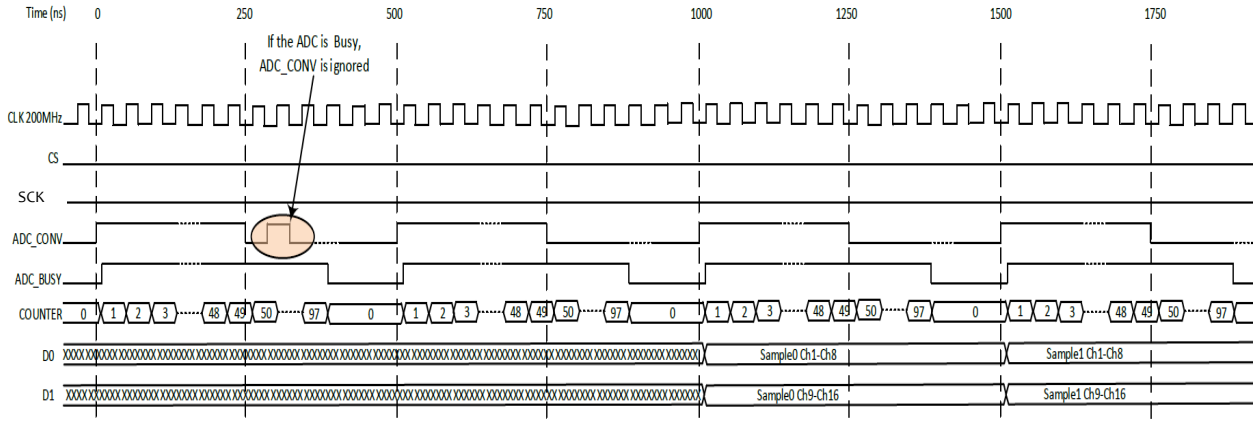


Figure 8 ADC conversion and readout

After a latency of three valid rising edges on ADC_CONV, the FIFO read pointer is incremented by the falling edge of the third ADC_CONV provided the corresponding rising edge was valid. A valid rising edge on ADC_CONV is defined as ADC_CONV going high when ADC_BUSY is low. That is, at startup or after a reset, any increment of the read pointer is disabled internally until after the third valid edge of ADC_CONV. Therefore, data can be read starting at the third valid convert/read cycles as shown in Figure 9.

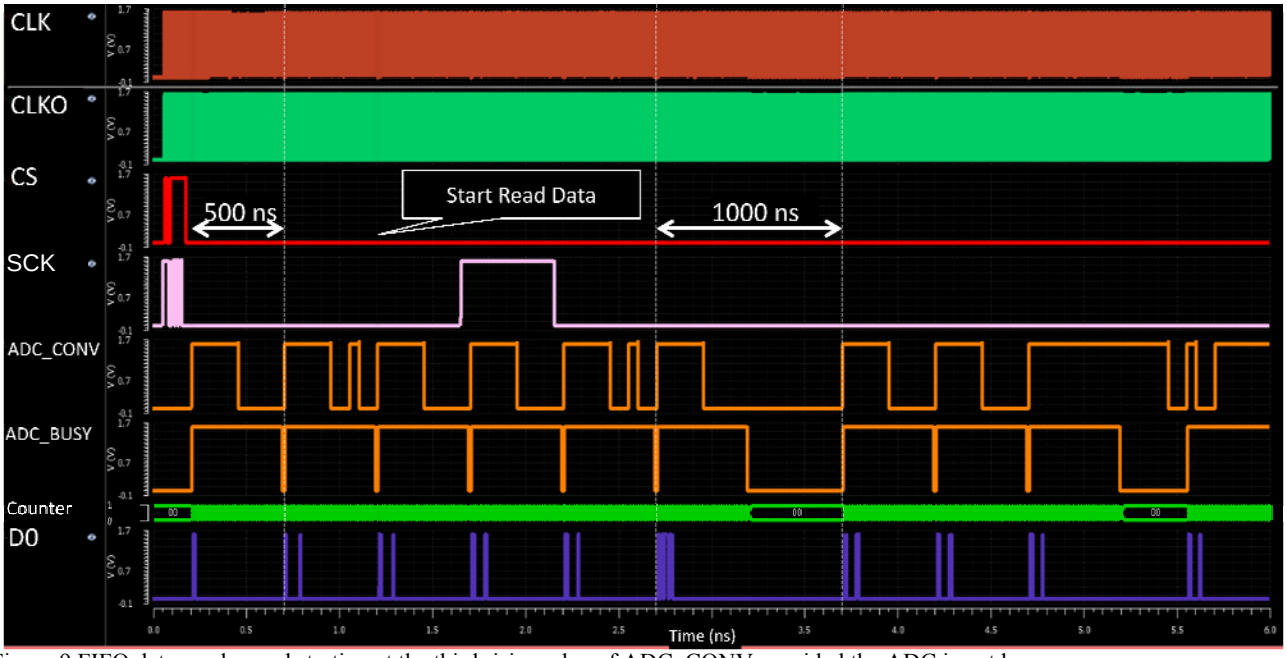


Figure 9 FIFO data can be read starting at the third rising edge of ADC_CONV provided the ADC is not busy

Backward compatibility to ADC V*

1. F0 = 0, FIFO write clock is generated internally. F0 = 1, FIFO write clock is on pin IdxME.

2. When F1 = 1 The controller defaults to the V* operation.

   - Clock generator starts on the rising edge of the clock. A Rising edge on ADC_CONV latches FIFO data into the output buffer. The counter rolls over after 100 clocks or 500 ns (an ADC cycle).
   - Fifo empty goes low after three ADC cycles. FIFO empty is multiplexed on pin FE/ADC_BUSY when F1 = 1.
   - FIFO read pointer is generated by a falling edge on ADC_CONV. FE is kept high for the first three write cycles after a reset. For the first three clock cycles, the same data will be read from the FIFO. While the FIFO is not empty, subsequent falling edge on ADC_CONV will increment the FIFO read pointer.

3. F2 = 0, internal clock generator is enabled. F2 = 1, controller is disabled.

Table 3 Input pin functionality

CS	**SDI**	**SCK**	**Function**	Comments
0	0	0	ADC Data	Default
0	0	1	FIFO Test	FIFO Test Pattern
1	x	x	Fifo soft Reset	Priority
1	Serial data in	Falling Edge	Shift SPI Data/ Fifo soft Reset	Load SPI Registers
Falling Edge	x	0	Buffer Data	Buffer SPI Serial Data
Falling Edge	x	1	Global Reset	Highest Priority

Pinout Information

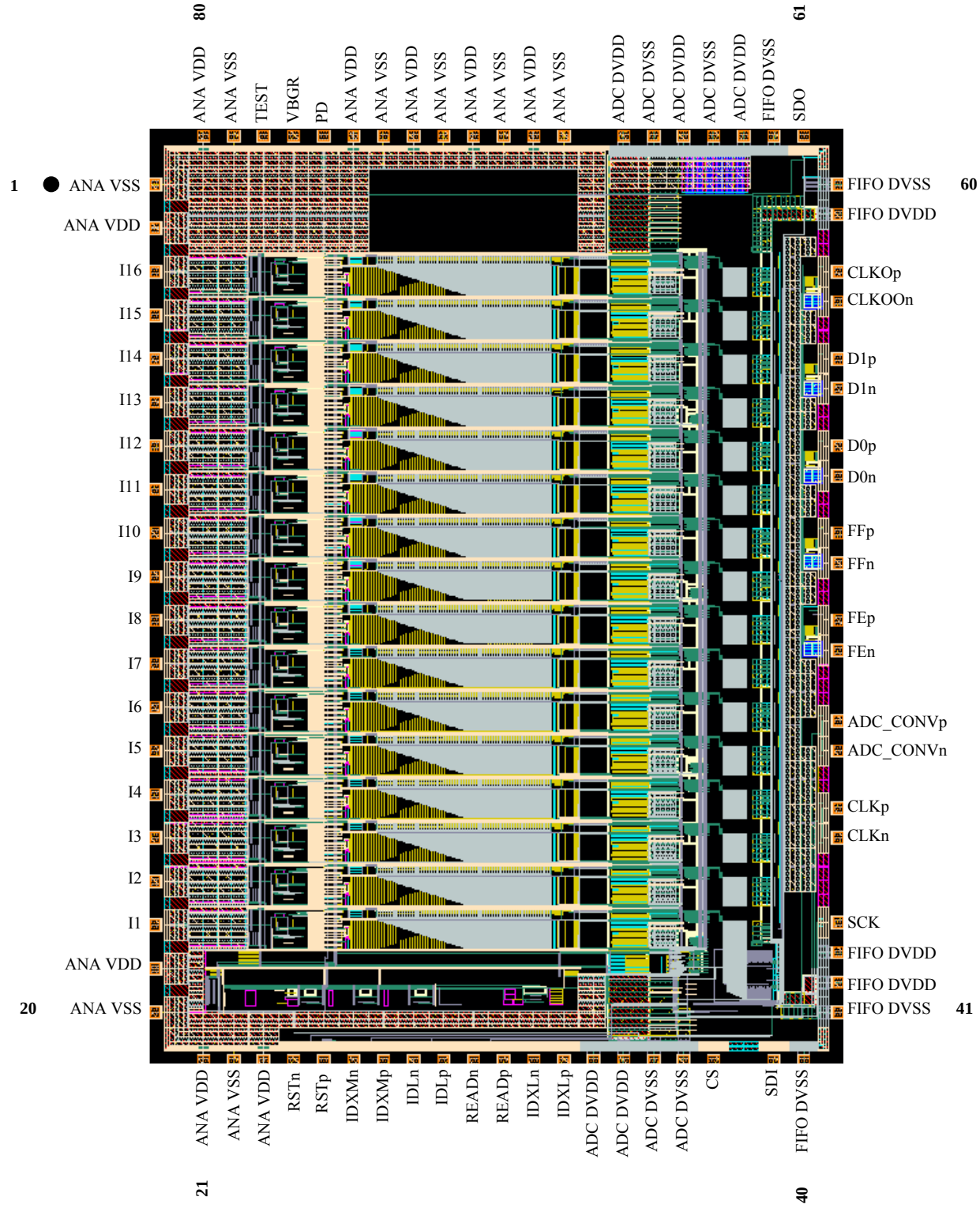


Figure 10 ASIC Pinout

Table 4. ASIC Pin List.

Num. Pins	Pin Num.	Signal Name	In/Out/Power	Reqd/Development	Description
8	1, 20, 22, 68, 70, 72, 74, 79	ANA_VSS	Power	Reqd	Analog ground: 0 V.
9	2, 19, 21, 23, 69, 71, 73, 75, 80	ANA_VDD	Power	Reqd	Analog supply for input buffers and analog section of ADCs: +1.8 V.
16	3~18	Inputs (16-1)		Reqd	Analog Inputs from channel to the input buffer (0.2 V -1.6 V). ESD protected.
1	24	RSTn	In	Development	LVDS n-input. Clock for reseting ADC cells. ESD protected.
1	25	RSTp	In	Development	LVDS p-input. Clock for reseting ADC cells. ESD protected.
1	26	IDXMn	In	Development	LVDS n-input. Clock for MSB conversion in ADC. ESD protected.
1	27	IDXMp	In	Development	LVDS p-input. Clock for MSB conversion in ADC. ESD protected.
1	28	IDLn	In	Development	LVDS n-input. Clock for LSB conversion in ADC. ESD protected.
1	29	IDLp	In	Development	LVDS p-input. Clock for LSB conversion in ADC. ESD protected.
1	30	READn	In	Development	LVDS n-input. Clock to encode thermometer code output of ADC to binary. ESD protected.
1	31	READp	In	Development	LVDS p-input. Clock to encode thermometer code output of ADC to binary. ESD protected.
1	32	IDXLn	In	Development	LVDS n-input. Clock for LSB cells in ADC. ESD protected.
1	33	IDXLp	In	Development	LVDS p-input. Clock for LSB cells in ADC. ESD protected.
5	34,35, 63, 65, 67	ADC_DVDD	Power	Reqd	Digital supply to ADC digital section: +1.8 V.
4	36, 37, 64, 66	ADC_DVSS	Power	Reqd	Digital ground for ADC digital section: 0 V.
1	38	CS	In	Reqd	CMOS chip select. ESD protected.
1	39	SDI	In	Reqd	CMOS serial data input. ESD protected.
4	40,41, 60,62	FIFO_DVSS	Power	Reqd	Digital ground for FIFO: 0 V.
2	42,43, 59	FIFO_DVDD	Power	Reqd	Digital Supply for FIFO: +1.8 V.
1	44	SCK	In	Reqd	CMOS dual purpose. Clock for shift registers and input trigger for internal monostable pattern generator. ESD protected.
1	45	CLKn	In	Reqd	LVDS n-input. Dual purpose. Readout clock and clock to run ADC and FIFO with a single clock input. ESD protected.
1	46	CLKp	In	Reqd	LVDS p-input. Dual purpose. Readout clock and clock to run ADC and FIFO with a single clock input. ESD protected.
1	47	ADC_CONVn	In	Reqd	LVDS n-input. FIFO Read Clock. ESD protected.
1	48	ADC_CONVp	In	Reqd	LVDS p-input. FIFO Read Clock. ESD protected.
1	49	FEn	Out	Reqd	LVDS n-output. FIFO empty indicator. ESD protected.
1	50	FEp	Out	Reqd	LVDS p-output. FIFO empty indicator. ESD protected.
1	51	FFn	Out	Development	LVDS n-output. FIFO full indicator. ESD protected.
1	52	FFp	Out	Development	LVDS p-output. FIFO full indicator. ESD protected.

Num. Pins	Pin Num.	Signal Name	In/Out/Power	Reqd/Development	Description
1	53	D0n	Out	Reqd	LVDS n-output. Data output from FIFO channel 8. ESD protected.
1	54	D0p	Out	Reqd	LVDS p-output. Data output from FIFO channel 8. ESD protected.
1	55	D1n	Out	Reqd	LVDS n-output. Data output from FIFO channel 16. ESD protected.
1	56	D1p	Out	Reqd	LVDS p-output. Data output from FIFO channel 16. ESD protected.
1	57	CLKOn	Out		LVDS n-output. Regeenerated output of CLK. ESD protected.
1	58	CLKOp	Out		LVDS p-output. Regeenerated output of CLK. ESD protected.
1	61	SDO	Out	Reqd	CMOS -output. Serial data output. ESD protected.
1	76	PD	In	Optional	CMOS level. Power down mode pin for ADC. ESD protected.
1	77	VBGR		Debug	Bandgap reference monitor. ~1.18V at room temp.
1	78	TEST	In	Debug	Test Input for ADC
80		**Total Pin**			

Note:

Reqd: Indicates a required input or output

Optional: Indicates that the input or output is not necessary but is an added feature

Debug/Development: Indicate that the input or output is only for testing during development.

Packaging Information

Bonding Diagram

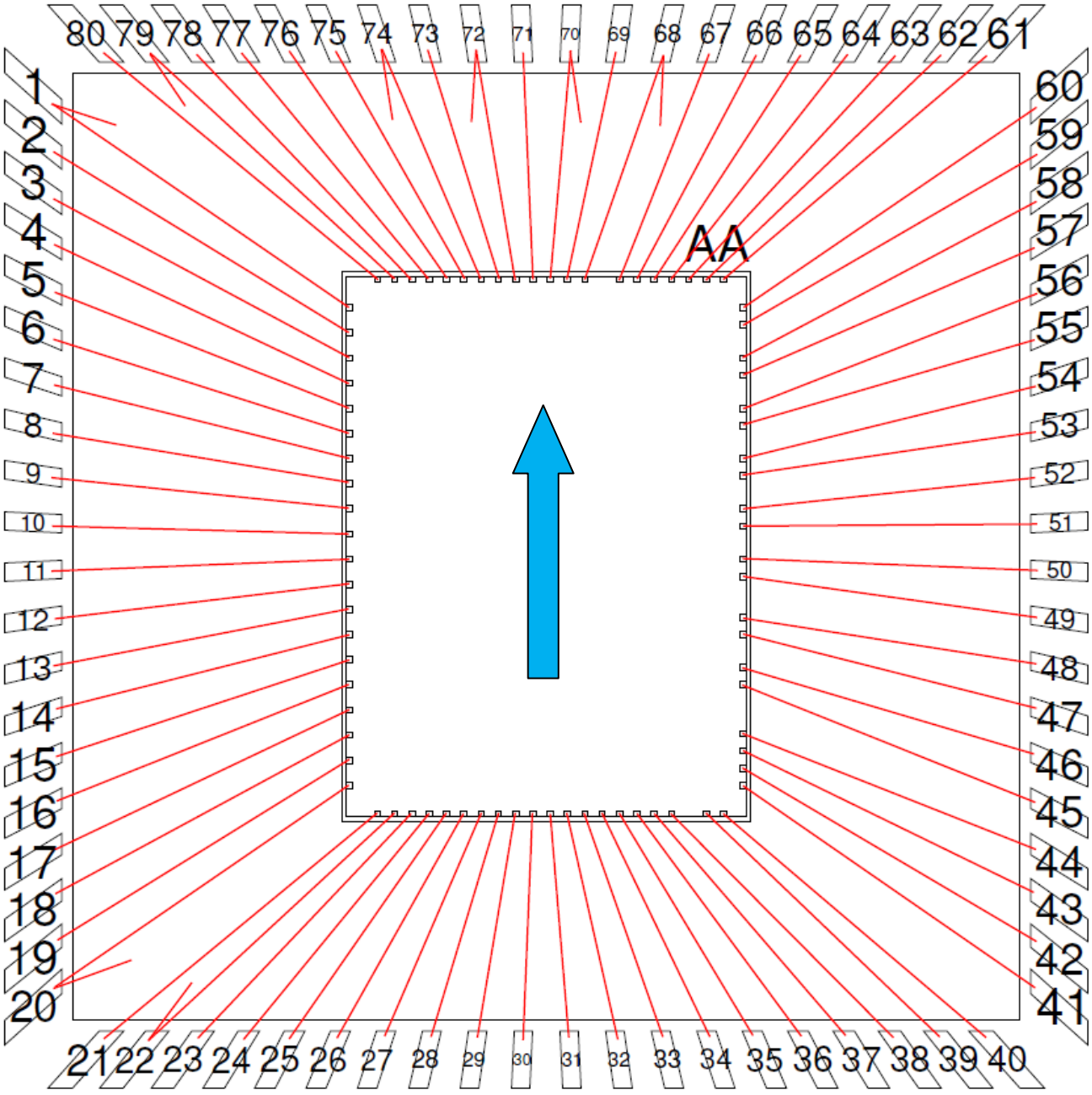
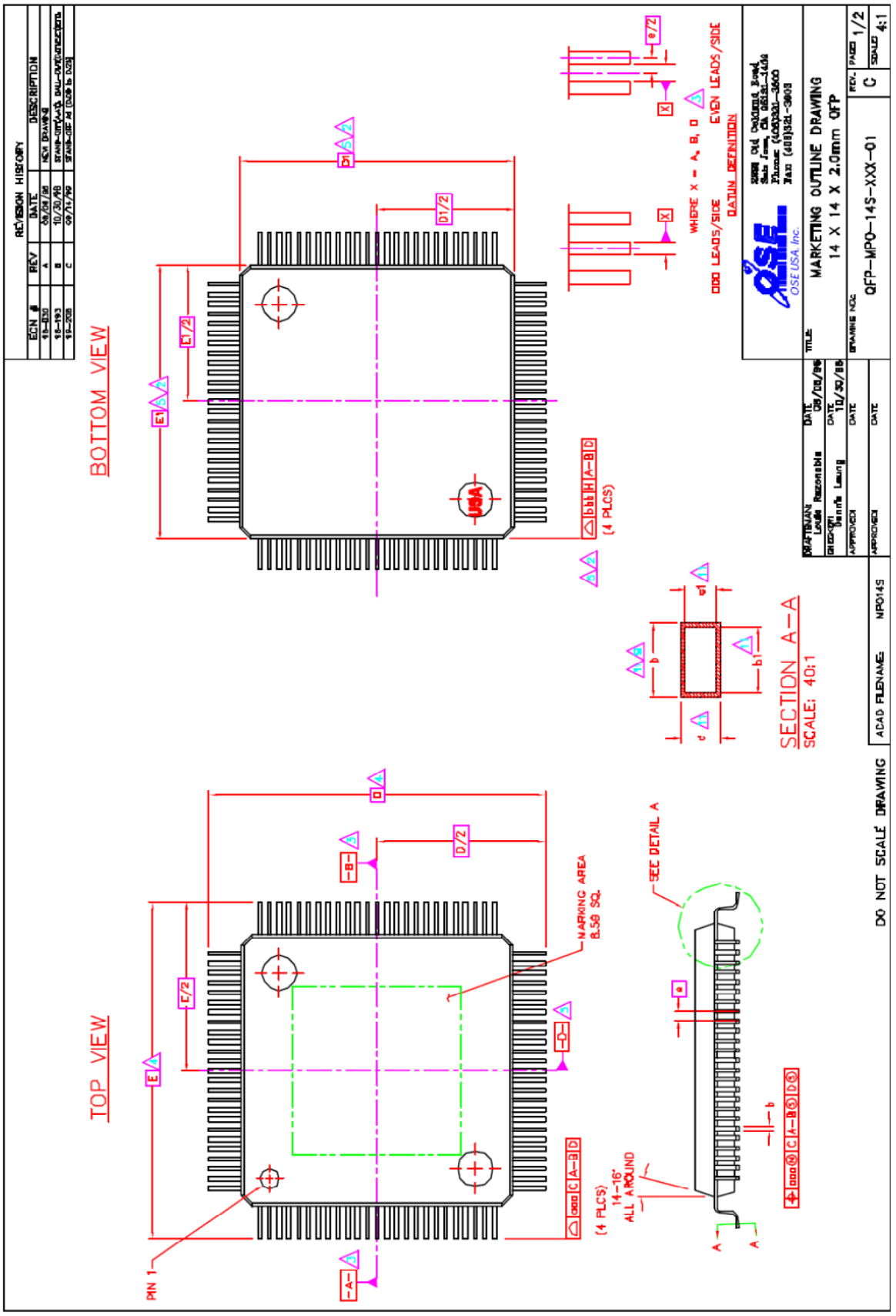
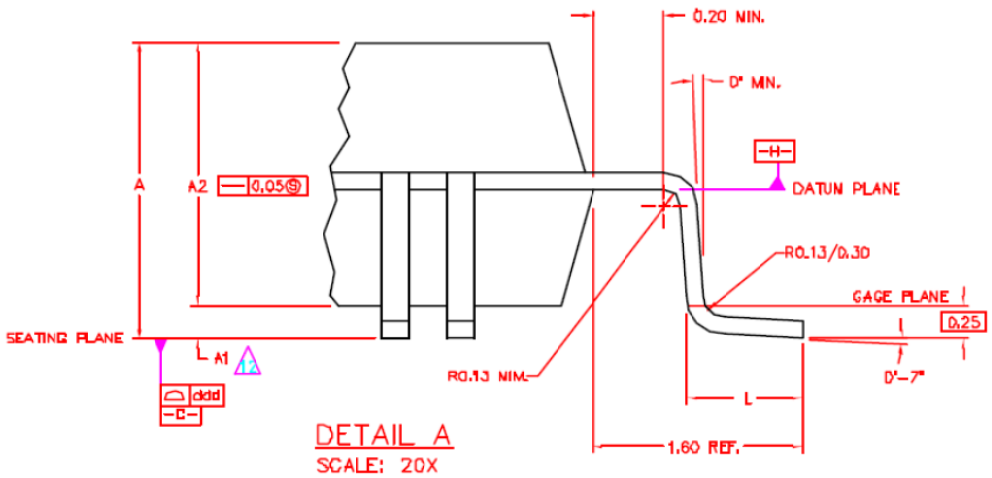


Figure 11. Bonding Diagram

Package Name: ISE_LQFP_14x14_80
Package Cavity Size: 10.5 x 10.5 mm2
Downbond-to-substrate-package-pin-numbers: 1, 20, 22, 68, 70, 72, 74, 76, 79
Min. bond pad size X: 68 um
Min. bond pad size Y: 64 um
Min. pad pitch: 192 um
Min. pad spacing: 113.96 um


REVISION HISTORY
ECN #
REV
DATE
DESCRIPTION
MARKETING OUTLINE DRAWING
14 X 14 X 2.0mm QFP
QFP-WPO-14S-XXX-01
BOTTOM VIEW
TOP VIEW
SECTION A-A
SCALE: 40:1
SEE DETAIL A
MARKING AREA
8.50 SQ.
PIN 1
DO NOT SCALE DRAWING

REVISION HISTORY			
ECN #	REV	DATE	DESCRIPTION
16-030	A	06/06/96	NEW DRAWING
98-193	B	10/30/98	STAND-OFF(A,A1), CAVITY(E1,E2)ETC.
98-206	C	09/14/99	STAND-OFF A1 (0.80 to 0.95)



DETAIL A
SCALE: 20X

NOTES:

1. ALL DIMENSIONS ARE IN MM. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982.
2. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE BODY SIZE BY AS MUCH AS 0.20.
3. DATUMS A-B AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
4. TO BE DETERMINED AT SEATING PLANE -C-.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
6. SURFACE FINISH OF THE PACKAGE IS #24-27 CHARMILLE (1.6-2.3$\mu m R_a$). PIN 1 AND EJECTOR PIN MAY BE LESS THAN 0.1$\mu m R_a$.
7. DAMBAR REMOVAL: PROTRUSION DOES NOT EXCEED 0.08. INTRUSION DOES NOT EXCEED 0.03.
8. BURR: BURR DOES NOT EXCEED 0.08 IN ANY DIRECTION.
9. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUN b DIMENSION BY MORE THAN 0.08. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 FOR 0.40 AND 0.50 PITCH PACKAGE.
10. CORNER RADIUS OF PLASTIC BODY DOES NOT EXCEED 0.20.
11. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25 FROM THE LEAD TIP.
12. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
13. FINISH OF LEADS IS TIN/LEAD PLATED.
14. ALL SPECIFICATIONS AND DIMENSIONS ARE SUBJECTED TO IPAC'S MANUFACTURING PROCESS FLOW AND MATERIALS.
15. THE PACKAGES DESCRIBED IN THIS DRAWING CONFORM TO JEDEC NO-108C AND MS-022B. WHERE DESCREPANCIES BETWEEN THE JEDEC AND IPAC DOCUMENTS EXIST, THIS DRAWING WILL TAKE THE PRECEDENCE.

SYMBOL	LEAD COUNT: FOOT PRINT 80: 3.2 FP			NOTE
	MIN.	NOM.	MAX.	
A	----	----	2.45	
A1	0.00	----	0.25	
A2	1.95	2.00	2.10	
D	17.20 BSC			
D1	14.00 BSC			
E	17.20 BSC			
E1	14.00 BSC			
L	0.73	0.88	1.03	
e	0.65 BSC			
b	0.22	----	0.38	
b1	0.22	0.30	0.33	
c	0.11	----	0.20	
c1	0.11	----	0.16	
	Tolerance of form and position			
aaa	0.20			
bbb	0.20			
ccc	0.13			
ddd	0.10			

SYMBOL	LEAD COUNT: FOOT PRINT 100: 3.2 FP			NOTE
	MIN.	NOM.	MAX.	
A	----	----	2.45	
A1	0.00	----	0.25	
A2	1.95	2.00	2.10	
D	17.20 BSC			
D1	14.00 BSC			
E	17.20 BSC			
E1	14.00 BSC			
L	0.73	0.88	1.03	
e	0.50 BSC			
b	0.17	0.22	0.27	
b1	0.17	0.20	0.23	
c	0.11	----	0.20	
c1	0.11	----	0.16	
	Tolerance of form and position			
aaa	0.20			
bbb	0.20			
ccc	0.08			
ddd	0.08			

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DO NOT SCALE DRAWING | ACAD FILENAME: MP0145

DRAFTSMAN: Laulie Rezendiz	DATE: 06/06/96	
CHECKED: Dennis Leong	DATE: 10/30/98	
APPROVED	DATE	
APPROVED	DATE	

TITLE: MARKETING OUTLINE DRAWING
14 X 14 X 2.0mm QFP

DRAWING NO: QFP-MPO-145-XXX-01 | REV: C | PAGE: 2/2 | SCALE: NONE