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The CRIM firmware is modified to implement sequencer control latch. This is firmware version 9 (v.9). By default (after power up) the CRIM's control latch is not enabled and the CRIM behavior is the same as in the previous v.8. The following additional features are implemented:

- Sequencer control bit in the SGATE register. See TL bit below:

## SGATE width register GW, 0xC020

| VME Data bits | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TC | X | X | X | X | TL | X | X | X | G6 | G5 | G4 | G3 | G20 | G1 | G0 |

Note: G0...G6 - gate width select bits in 150.6 ns steps in INT mode, X - Don't care
TL – sequencer latch control bit (1 – enable, 0 – disable latch control)
TC – sequencer control bit (1 – enable TCALB, 0 – disable TCALB)

- Sequencer control latch reset VME command. See below 0x0404 bit combination:

## Software CNRST register CR, 0xC080

| VME Data bits | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | SS | LR | CR | 0 | 0 | 0 | 0 | 0 | SS | LR | CR | 0 |

Note: Writing **0x0202** to this register generates counter reset pulse in EXT mode,
Writing **0x0404** to this register generates sequencer control latch reset pulse,
Writing **0x0808** to this register starts single sequence of CNRST, SGATE and TCALB in INT or MTM mode when no frequency is selected (F11…F0 are set to zero)

After the sequencer control latch is enabled (gatew(10) = 1), the CRIM will accept only one TCALB signal from the Minerva MTM. In order to accept another TCALB signal one need to issue a reset command (write 0x0404 to the Software CNRST register).