A 2-Bit-Per-Cycle SAR ADC prototype for application in Biohybrid Systems Interfacing

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***Abstract*—The exploration of bioelectric action potentials within fungal mycelium networks has created new possibilities for the development of biohybrid systems for sensing and communication. With recent studies suggesting possible neuromorphic processing through distinct patterns of electrical spikes, the demand to interface with such networks increases. However, reliable capturing and processing of such signals due to their low frequency, amplitude, and noise susceptibility presents a significant engineering challenge; this work demonstrates a prototype of a successive approximation register analogue to digital converter designed to facilitate accurate data acquisition of biological signals. The proposed design is capable of resolving 2 bits per conversion cycle by employing a four-fully-differential-comparator scheme and dynamic voltage scaling, achieving higher bit rates without sacrifices in terms of power consumption or resolution. Initial FPGA-in-the-loop simulations demonstrate the concept's functionality setting the foundation for developing advanced biohybrid interface systems, thus supporting novel applications in the emerging fields of neuromorphic computing and environmental sensing.**

***Index Terms*—SAR ADC, 2-bit-per-cycle ADC, FPGA Prototyping, FIL Simulation, Mixed-Signal Circuits, Neuromorphic Computing, Biohybrid Interfacing, Unconventional Computing, Advanced Sensing**

I. Introduction

Fungal-mycelial networks provide a promising case for exploring biohybrid systems, due to their inherent capabilities for sensing, environmental adaptation, and computation, utilising the generated electrical action potentials [1]. In contrast, to "all-or-nothing" action potentials mitigated from propagating within animal neural networks [2], their mycelial counterparts consist of slow and variable-amplitude stimuli ranging from 0.03 to $2.3mV$ with action durations up to several hours [3], [4]. Despite their weak strength, these action potentials are theorized to serve as a means of communication with other fungal colonies in immediate proximity [5]. Recent investigations have also revealed the ability of these signals to serve as an intermediary between the mycelium and environmental stimuli, either in the form of mechanical, chemical, or optical disturbances, by modulating embedded spike patterns, thus constituting a form of adaptive environmental sensing [6], [7]. Beyond mere sensing, mycelial networks demonstrate potential as unconventional computing platforms. As recently demonstrated [8], [9], these networks could perform simple Boolean operations, paving the way for neuromorphic and analogue computing applications. Several works in literature, using multidisciplinary approaches including numerical simulations, electrical equivalent models, and experimental verification [10]–[13] indicate that the basic operations of AND, OR, and NOT can be implemented by the mycelial network, thus constituting a complete Boolean algebraic set, presenting a unique opportunity for the exploration of biohybrid systems. However, the realization of practical applications requires the development of robust interface suites capable not only of mimicking the aforementioned environmental stimuli but also of accurately capturing the resulting action potentials. The latter poses a challenge, since these signals are often characterized by low frequency, low amplitude, and, by extension, significant noise susceptibility [14]–[16]. Conventional signal acquisition systems, such as those currently in use in neural applications, may not be able to respond to these demands. Hence, the development of a bespoke solution that bridges the gap between digital data acquisition technologies and biological substrates is deemed imperative. Perhaps the most critical link on this chain is the Analogue-to-Digital Converter (ADC). Among various architectures, the Successive Approximation Register (SAR) ADCs have gained popularity for a wide range of applications, since they offer a silver lining in balancing resolution, with sampling frequency and power consumption, while maintaining resilience to noise distortions [17], [18]. In essence, an ADC following this principle implements a binary search algorithm to compare, evaluate, and digitize input voltages, offering an ideal solution for low- to medium-speed applications, where the preservation of signal integrity and power efficiency are paramount [19]. Although SAR ADCs represent an active research topic, recent advances mainly focus on optimizing power consumption or noise resilience through novel comparator designs [20], at the expense of resolution or sampling frequency, therefore, making it difficult to adapt these designs for biohybrid interface applications. In this work, we present an early-stage prototype of a novel SAR ADC capable of resolving 2 bits per conversion step, designed as part of a broader strategy towards biohybrid system development. This prototype, comprising a four-fully-

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differential-comparator scheme, and dynamic voltage scaling, promises to achieve low latency, high sampling frequency and energy-efficient operation. Initial performance insights as gathered by logic synthesis and implementation, as well as FPGA-in-the-Loop simulations are discussed, highlighting the potential for eventual integration on nanoscale SoC architectures, establishing a critical foundation to develop biohybrid interfacing solutions, supporting future innovations in the fields of neuromorphic computing and environmental sensing.

II. Proposed SAR ADC Architecture

A. Comparator Scheme

Direct interface with analogue electrical stimuli is achieved using a four-comparator scheme (Fig. 1(a)). These comparators are used to evaluate the input voltage against dynamically adjustable voltages generated by the low- and high-side DACs. Depending on the design, these DACs are controlled either by serial interface, as in the proof-of-concept case analyzed in Section III, or by parallel interface, as in the case of application-specific DAC designs. The result is the generation of a 4-bit thermometer code, thus streamlining the binary search process towards faster and reliable conversions. In addition, the fully differential comparator design offers immunity to common-mode noise, further contributing to the preservation of signal integrity. The comparator outputs directly interface with the controller's thermometer-to-binary decoder (T2B), instantiated within the ADC's main logic block.

B. Thermometer to Binary Decoder

The T2B decoder is implemented as a combinational-logic block converting the comparator's results into a 2-bit binary code plus one carry-bit acting as an overflow-case flag. Adding to the system's overall reliability is the decoder's support of both synchronous and asynchronous reset elements, allowing for an efficient and rapid transition response and edge-case management, e.g., overflow-flag assertion. Moreover, the decoder logic is synthesized and implemented using logic-minimization techniques, ergo, optimizing the end-product's area footprint and by extension contributing in reaching the low-power consumption milestone, as demanded by the target application.

C. Main Logic

The operation of the ADC presented in this work is governed by a Moore Finite-State Machine (FSM), which manages the entire conversion process through six well-defined states, namely:

1) `IDLE` – The FSM remains in this state while waiting for a start conversion signal.
2) `UPDATE_DACs` – The FSM updates the DAC inputs according to the SAR register value.
3) `WAIT_SETTLING` – A delay is introduced to allow the DAC outputs to settle.
4) `COMPARE` – The comparator evaluates the input signal against the DAC output.
5) `DONE` – The conversion process is complete and the result is finalised.

The FSM orchestrates the timing sequences, manages the control signals to the DACs and updates the SAR register (i.e., the conversion result) based on the outputs from the comparators and the T2B decoder. The FSM is meticulously designed for minimal state transition latency and optimized for digital resource utilization. During the state of `UPDATE_DACs`, the SAR logic computes and dispatches the appropriate reference voltage to the Low- and High-Side DACs with minimal overhead. In the `COMPARE` state, input signal sampling and bit evaluation, updating the SAR and DAC registers, accordingly. The `DONE` state asserts a completion flag, enabling downstream digital components to effectively capture the converted digital value. A key feature of the FSM is the priority-based state transition mechanism, which ensures that critical operations, such as those in the `COMPARE` and `SET_BITS` states, are prioritized effectively, avoiding data hazards. Care has been taken to incorporate both synchronous and asynchronous resets, adding to the system's robustness, especially in mixed-signal environments. The design is complemented by the inclusion of a SampleAndHold (S&H) module, used for for analogue input stabilization, within the end application's timing constraints, effectively reducing jitter and enhancing accuracy. The overall design philosophy emphasizes low power consumption, achieved through clock gating and power-aware state management. These design choices not only make the ADC suitable for nanoscale and SoC integration but also align with the power efficiency requirements of neuromorphic and sensor interface applications. The RTL design has also been structures to facilitate a seamless transition from the FPGA-based prototyping stage to future ASIC implementations, preserving the critical performance metrics required for advanced electronic systems.

III. Co-simulation and Performance Metrics

A. Overview of Simulation Methodology

The validation of the proposed 2-bit per cycle SAR ADC was carried out using a combination of HDL Co-Simulation and FPGA-in-the-Loop (FIL) methodologies. These techniques were instrumental in verifying the performance of the design under realistic operating conditions and bridging the gap between simulation and hardware implementation. The HDL Co-Simulation setup involved interfacing the VHDL modules directly with MATLAB/Simulink. This allowed for cycle-accurate testing of critical components such as the comparator array, thermometer-to-binary decoder, and the main FSM itself. This setup allows for real-time monitoring of internal signals, facilitating precise timing analysis and the detection of any potential logic hazards. FIL performed further validation, using an Artix-7 35T FPGA Evaluation Kit. The SAR ADC design was synthesized and mapped onto the FPGA, allowing the Simulink model to drive real hardware through a low-latency JTAG interface. The FIL setup enabled the execution of Hardware-in-the-Loop (HIL) simulations, ensuring the fidelity of the design.

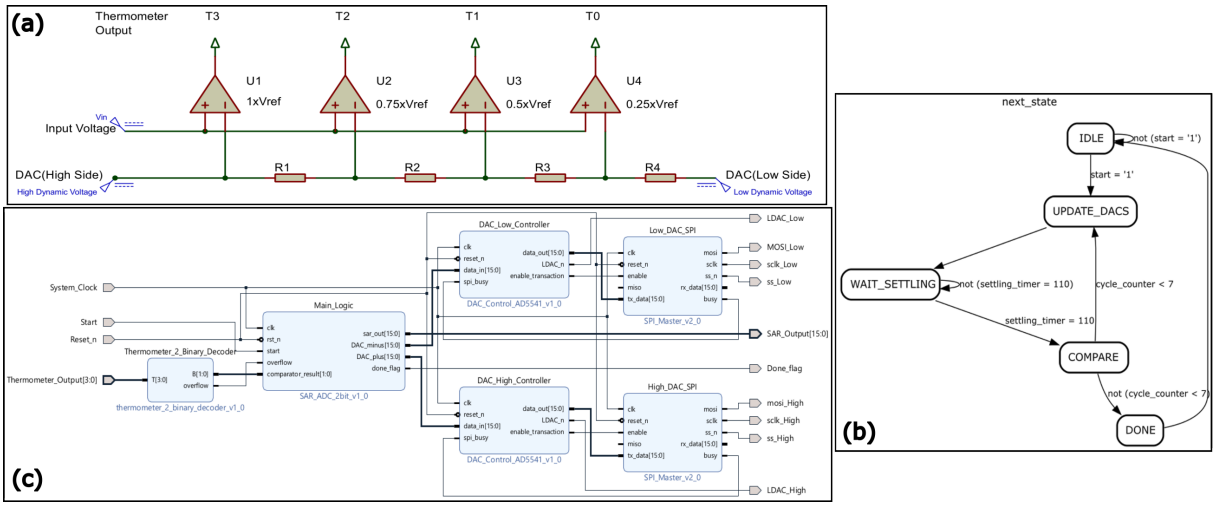

Fig. 1. Overview of the 2-bit-per-cycle SAR ADC prototype consisting of AD5541 DACs and OPA4353 OpAmps as comparators. (a) The four-fully-differential-comparator circuit responsible for converting the analogue input into a digital-ready thermometer code. (b) Main Finite-State-Machine governing the ADC operation. (c) Simplistic block diagram demonstration of the full SAR ADC.

B. Testbench and simulation Configuration

The primary goal of the simulations, at the current stage of development, was to verify the 2-bit-per-cycle resolution, the decoding combinational logic, and the state machine transitions within a controlled simulation environment. As such, static input voltages that represented critical operating points, including minimum and maximum input ranges, mid-scale transitions, and scenarios that could trigger the thermometer code overflow. An emphasis was placed on assessing the stability of the FSM, the DAC settling behaviour, and the consistency of the comparator output. During FIL testing, the ADC model was interfaced using the JTAG interface. This configuration allowed for real-time extraction of conversion cycles, ensuring accurate replication of the simulated model. The captured digital outputs were monitored to validate the accuracy of conversion and resilience to bit errors in different operational scenarios. As a result, a robust assessment of the proposed architecture was provided, ensuring that the ADC operates as intended in real-world conditions, with future work focusing on dynamic waveform reproduction when generated by memristive elements as part of a wider bioinspired computing system.

C. Comparison with Conventional SAR ADCs

The proposed 2-bit per cycle SAR ADC architecture demonstrates significant advantages over conventional 1-bit per cycle SAR ADCs in terms of conversion speed, power efficiency, and resource use. By resolving two bits per clock cycle, the proposed design achieves a 50% reduction in conversion time, allowing a 16-bit conversion to complete in only eight clock cycles, compared to the sixteen cycles required by conventional designs. This improvement in conversion speed directly translates into higher sampling rates, positioning the proposed ADC as a compelling solution for high-speed applications such as neuromorphic computing and real-time data acquisition. The resource utilization analysis

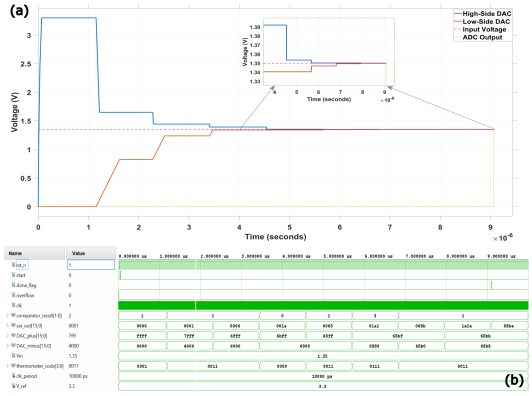

Fig. 2. FIL simulation using an AD5541 as low- and high-side DACs(a) Digitisation of the input value using dynamic voltage scaling, as simulate during using FIL methods. (b) Behavioural simulation of the proposed design demonstrating the conversion cycle.

reveals that the proposed design employs 64 Look-Up Tables (LUT) and 77 Flip-Flops (FF), translating to 0.3% and 0.19% of available FPGA resources, respectively. In contrast, conventional SAR ADC uses only 16 LUTs (0.08%) and 24 FFs (0.06%). Additionally, while both designs employ similar global clock buffer resources (1 BUFG, 3.13%), the proposed architecture requires more I/O pins (54 - 25.71%) compared to the conventional design (21 - 10%). Although the resource usage increases by 0.22% and 15.71% respective in terms of FFs and I/O pins respectively, the resulting resource allocation still remains a small fraction of the available total for the selected FPGA. Additionally, the proposed design offers increased power efficiency with a total on-chip power consumption of the 2-bit-per-cycle ADC is 0.121 W, i.e., nearly 95% lower than the conventional design's 2.348 W, ergo, deeming the increase of allocated resources modest, in relation to the architectural and performance gains. The reduction in power consumption is also con-

TABLE I
COMPARISON OF RESOURCE UTILIZATION AND POWER CONSUMPTION

Metric	Proposed 2-bit-per-cycle SAR ADC	Conventional 1-bit-per-cycle SAR ADC
LUT Utilization	64 (0.31%)	16 (0.08%)
FF Utilization	77 (0.19%)	24 (0.06%)
I/O Pins	54 (25.71%)	21 (10%)
Global Buffers (BUFG)	1 (3.13%)	1 (3.13%)
Total On-Chip Power (W)	**0.121**	**2.348**
Junction Temperature (°C)	25.6	36.2
Thermal Margin (°C)	74.4	63.8

tributing to improved thermal performance, with a junction temperature of 25.6°C for the proposed design compared to 36.2°C for the conventional ADC. The thermal margin is significantly increased to 74.4°C from 63.8°C, highlighting the suitability of the design for low-power and thermally constrained environments. Overall, the proposed 2-bit-per-cycle SAR ADC presents a balanced approach, achieving high conversion speed and power efficiency with only a modest increase in FPGA resource use. These characteristics make it a promising candidate for advanced systems that require rapid and efficient analogue-to-digital conversion, such as those found in neuromorphic computing and dynamic signal processing environments.

IV. ADDRESSING SIGNAL ACQUISITION CHALLENGES IN BIOHYBRID INTERFACES

Developing reliable biohybrid interfaces involves several challenges in terms of signal acquisition and processing. The first obstacle, perhaps the most important to overcome, is separating weak bioelectric action potentials from noise-generated artefacts. An ADC capable of maintaining an adequate sampling frequency without resolution trade-offs is more capable of distinguishing mycelium network action potentials from other environment generated signals, hence being less prone to cataloguing "false positives". Similarly, given their inherent variability in amplitude and slow temporal evolution, increasing the risk of the action potentials being submerged in background noise is a common trend, as explained by the Johnson noise theory (thermal noise) and constrained by the Nyquist sampling criterion [15], [21]. The task of acquiring said patterns is further complicated given their ability to evolve given the environmental condition fluctuations. It is therefore paramount to maintain, as much as possible, signal integrity during the digitisation process. The proposed design represents a promising solution to address these challenges. Common-mode noise rejection, due to its fully differential comparator design, enhances immunity to "false positive" artifact generation, thus ensuring signal integrity. Its capacity for dynamic voltage scaling also allows it to adapt to varying signal amplitudes, without sacrificing its resolution, a feature particularly useful for monitoring signals that may fluctuate in response to environmental condition shifts. Moreover, the ADC's low-latency performance translates in ease of cataloguing fast and slow signals with similar accuracy. Given the broad spectrum of electrical activity within the mycelial network, where signals can range from single-spiking depolarisations to prolonged bursts and fluctuations, incorporation of these features into the converter supports more accurate and reliable interfacing. In addition, the design's modular nature, optimized for minimal resource allocation, makes it easy to deploy in a variety of evaluation platforms, providing empirical evidence of its robustness in handling realistic, dynamic signals. Using the FIL methodology [see III], the ADC response to a diverse range of waveforms consisting of biological and non-biological noise-based components can be evaluated, ensuring that the ADC can successfully distinguish the former and, if not, allow for the development of better acquisition strategies.

V. CONCLUSIONS AND FUTURE WORK

The proposed 2-bit-per-cycle ADC design represents a vital step in realizing interface between digital computing systems and biological substrates. By comprising a four-fully-differential-comparator scheme and dynamic voltage scaling within its architecture, and thus exceptional resilience to noise, this ADC can address significant challenges bioelectric signal acquisition, like distinguishing biological signals from noise, maintaining signal integrity under dynamic conditions, and ensuring high-resolution sampling of low-amplitude action potential activity. Initial FIL validation has also indicated the prototype's potential for reliable signal acquisition, setting a solid foundation for deployment in biohybrid interface systems and neuromorphic applications. As a next step, a fully functional hardware implementation must be realized and tested for integration into complete biohybrid interfaces. This procedure includes adding support for real-time processing of dynamic waveforms, similar to those generated by biological systems. Additional experimentation must also be conducted to validate the ADC's performance to dynamically adjust stimuli. Hence, exposure to such cases inside the FIL environment is deemed a mandatory step for testing under these conditions, thus ensuring its reliability in practical applications. As the final goal is for this system to be incorporated into novel applications in the fields of unconventional, bioinspired computing, exploration of miniaturization options for eventual integration into nanoscale SoC architectures must also be conducted to enhance the design's overall versatility.

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