Variability Tolerance Analysis of Memristive Wave Cellular Automata

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***Abstract*—In the era of high-performance computing, the integration of Cellular Automata (CA) principles into low-power hardware is a challenging but intriguing endeavor. At the same time, memristors have gained attention due to their potential in in-memory neuromorphic computing. As such, the concept of Wave Cellular Automata (WCA) is presented a novel computing paradigm that leverages CA principles and memristive devices for in-memory computing. However, memristive devices are subject to variability effects, which can impact their performance and, in the case of WCAs, the generation of oscillations crucial for computation. This paper explores the variability tolerance analysis of WCA both in CBRAM device level, but also in its oscillatory behavior. The analysis reveals that WCA operation remains robust even in the presence of variability, with the impact on oscillation amplitude being minor. All in all, proper circuit design and element selection play a significant role in mitigating the effects of variability.**

***Index Terms*—Cellular Automata, Memristor, Oscillator, Variability Analysis, Wave Computing**

I. Introduction

Today's computing systems still seek ways to become faster and more reliable in order to comply with the high standards set by the state-of-the-art demanding computational applications. In 1948, John von Neumann introduced a novel discrete computational model grounded in elementary rules, specifically referred to as Cellular Automata (CA) [1]. To elaborate further, CA are structured within cells, typically organized in a grid-like topology. Each cell possesses a distinct state, which undergoes evolution through discrete time steps, guided by predetermined rules contingent upon the states of neighboring cells. Their most salient feature lies in the coexistence of memory and processing units within the same medium, akin to the intricate biological organ, the brain. For this reason, they offer inherent parallelism during computing tasks, and can effortlessly pave the way to be employed in modeling and brain-mimicking tasks for solving complex computing problems [2]–[5].

The integration of CAs into low-power hardware is a very interesting and challenging problem that can help the scientific community move towards to more efficient computing paradigms, as well as to more feasible manufacturing attempts bringing the favorable in-memory computing architectures in terms of both size and performance. In particular, promising candidates that can help to cope with this task are memristors. To elaborate more, a memristor is a passive circuit component that incorporates two-terminals and its operation is based in the Resistive Switching (RS) behaviour as an after-effect of placing supply voltage or current to its aforementioned terminals. It was first suggested by L. Chua in 1971 [6], and has received a great deal of attention recently [7], [8] because of its intriguing potential as a highly promising structural hardware component for in-memory neuromorphic computing and emulation of neurological functions [9]–[12]. Moreover, in the literature it has been successfully utilized for CA applications such as image processing, and modeling of brain diseases [13]–[15].

However, this novel nanoscale electronic component usually exhibits some varying effects that should be taken seriously into consideration, so to avoid defects in the corresponding circuit design [16]. One of the most efficient ways to check the reliability and the performance of these novel computing nanodevices is the study of the variability [17]. Managing variability is crucial for ensuring that memristive nanodevices [18], function reliably under various operating conditions, paving the way for technological advancements and more reliable in-memory computing components [19]. To further elaborate, variability encompasses deviations in manufacturing processes, material properties, environmental conditions, and even the inherent stochastic nature of memristive nanodevices and directly impacts the consistent performance of both relevant analog but also digital circuits, affecting their parameters such as speed, power consumption, and reliability. This includes creating more robust and efficient electronics, improving manufacturing yields, and ensuring consistent performance throughout the lifetime of the designed electronic systems. It should be pointed out that while literature usually focuses on devices' variability, it usually lacks of application specific impact, which typically use these devices in a more complex way, such as for producing oscillations.

This work is targeted in exploring the variability not only in memristive devices, but also to oscillatory circuits that mimic the brain behaviour and represent a fully analog CA cell, in order to examine their efficiency and robustness. In the following Section II, the circuit of the CA cell is introduced and its oscillating operation is analyzed. Furthermore, in Section III, the tentative variability of the memristive device is explored, so as to investigate the robustness of the core element of the proposed design. The impact of the variability to the oscillatory circuit is discussed in Section IV to ensure the

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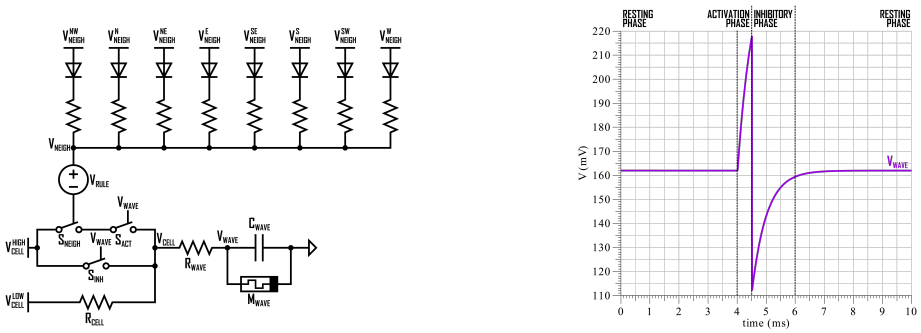


(a) (b)

Fig. 1. (a) Wave Cellular Automaton circuit. (b) WCA output oscillation and operational phases.

use of these structures in more complex systems for real-time efficient computing. Last but not least, Section V discusses the importance of variability impact towards more tolerant electronic circuits and concludes with the most important attributes of this work.

II. Wave Cellular Automata Concept

CAs as computational tool for physical processes are able of efficiently implementing computations in hardware, capitalizing on their intrinsic parallelism [20]. More specifically, the application of novel unconventional nanoelectronic devices of memristors has led to the successful development of various CA-based computing approaches, such as Memristive Cellular Automata (MemCA) [21], and Memristive Cellular Nonlinear Networks (M-CNN) [22]. Lately, the incorporation of a wave generation circuitry capable of illustrating wave propagation within a cellular-like architecture has been introduced as the Wave Cellular Automata (WCA) concept. The aforementioned wave generators can form an interconnected network that enables the propagation of electrical wave signals with the ability to spatially interact with one another, hence replicating the neighborhood and evolution concepts of CA.

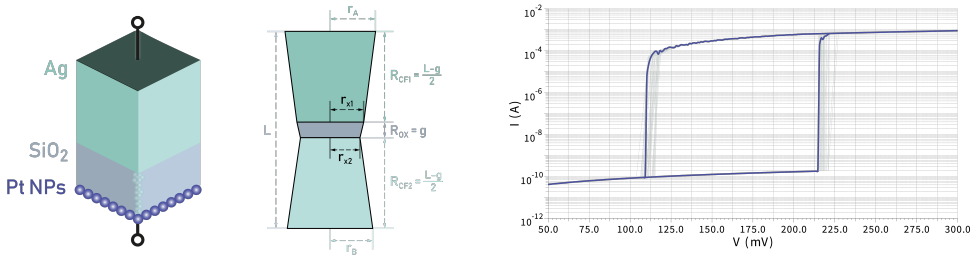
The WCA circuit, as depicted in Fig. 1(a), exhibits oscillations in the output voltage V_{WAVE} (Fig. 1(b)) between the SET and RESET voltage thresholds of the unipolar memristive CBRAM device M_{WAVE}. In order to produce these output oscillations, the cell is connected to its Moore neighborhood voltage outputs ($V_{NEIGH}^{N;E;S;W}$). To establish distinct rules for the WCA, a constant voltage supply, referred to as V_{RULE}, is implemented following the joint point of all neighbors V_{NEIGH}. By assigning distinct values to V_{RULE}, it becomes simpler to reach the S_{NEIGH} threshold with a reduced requirement for synchronous activation of neighboring nodes.

For the oscillation triggering, a constant DC voltage is applied. For the oscillations to persist over time, it is necessary to configure the R_{WAVE} and C_{WAVE} values in a manner that prevents the voltage divider V_{WAVE} from reaching an equilibrium point between the SET and RESET voltage thresholds. The voltage supplies V_{CELL}^{HIGH} and V_{CELL}^{LOW} are responsible for delivering this required power through the control circuit, which consists of two branches. One branch is responsible for keeping the cell in an idle condition, while the other branch governs the initiation of oscillation when the requirements set by the rule in place have been satisfied. All in all, the S_{NEIGH} switch is engaged at reaching the threshold set by the rule used, hence initiating the oscillation. To ensure the proper operation of the WCA and prevent sudden oscillation interruption, the S_{ACT} switch is incorporated in series with S_{NEIGH}, serving as a self-restraint switch. Moreover, for the smooth operation of the WCA, the S_{INH} switch is introduced to prevent sudden interruptions in the oscillation process and guarantees the successful inhibition of the WCA in order not to be affected by any rule on the computation time-step.

The operation of the WCA can be delineated into three distinct phases (Fig. 1(b)). The initial phase is characterized as the resting phase, during which the oscillating unit remains idle and awaits activation. The second phase is referred to as the activation phase, which occurs when the stimulus surpasses the threshold required for WCA activation, leading to the initiation of the oscillatory activity. Then, the inhibitory phase follows, during which the oscillation reaches its lowest voltage level and thereafter increases until it returns to its idle level once more. The activation of the oscillating unit is restricted to occur just during the resting phase, subsequent to the activation of the corresponding neighboring units in accordance with the established rule.

III. Device Variability Analysis

The utilization of memristors within WCA cells is important in the generation of oscillations, which are indispensable for establishing a predefined time-step. In this work, Conductive-Bridging RAM (CBRAM) modeled devices were employed due to their suitability for this application. To elaborate further, our oscillator requires a unipolar device to produce the necessary oscillations, while also taking into consideration physical parameters such as the temperature and the energy efficiency of the oscillating system. These devices base their operation in the electrochemical metallization principle, where a conductive metallic filament is formed during a SET operation, while the same filament undergoes a dissolution during a RESET operation in a solid dielectric material, referred as switching layer [23]. In order to achieve a realistic and seamless integration of these memristor devices within the simulated circuit, a compact memristor model as proposed by [24] has



(a) (b) (c)

Fig. 2. (a) Structure of the fabricated CBRAM device. (b) Model representation for the CBRAM device. (c) I-V curves of the device utilized in the simulations. In solid lines the average curve is depicted, while faint lines indicate each distinct cycle employed.

been employed. This model adeptly encapsulates the intricate dynamics of unipolar CBRAM devices, incorporating essential attributes such as drift, diffusion, and thermo-diffusion effects, which are indispensable for simulating the switching behavior of memristors. In this way, the model can accurately capture the resistive switching operations of the used CBRAM devices, i.e. the formation and breakage of the Conductive Bridge (CB) between the active and inert electrodes (Fig. 2(b)). Notably, this model has been fitted to fabricated CBRAM devices of $Ag/SiO_2/Pt$ NPs configuration (as seen in Fig. 2(a)) that exhibit unipolar characteristics.

Variability plays a pivotal role in the performance of electronic circuits and systems, a principle that extends to memristors as well [25]. The relentless trend towards the miniaturization of electronic components, while exacerbating the influence of variability on the performance and reliability of integrated circuits, has concurrently introduced additional, albeit less dominant, sources of random voltage and current fluctuations. These variations range from fluctuations in Random Telegraph Noise (RTN) currents to quantum-mechanical-induced effects, such as direct tunneling and hopping effects [26]. Moreover, they encompass the more typical variations originating from manufacturing processes, resulting in device inhomogeneity, and the influence of environmental conditions, such as humidity and pressure, which can induce substantial deviations from the anticipated behavior of both individual devices and complete systems [27]. Out of these various sources of variability, they can be distinguished to two fundamental types: device-to-device (DTD) variability and cycle-to-cycle (CTC) variability [28]. CTC and DTD variability poses a critical challenge in ensuring the robustness and reliability of electronic systems [29], particularly in data-sensitive applications, where even small deviations can lead to substantial errors and data degradation.

In the context of this study, we investigate the inherent variability in the behavior of the utilized CBRAM devices and its impact on the overall circuit performance. The I-V characteristic curves of the employed unipolar device during simulations are depicted in Fig. 2(c), where the solid line indicates the average I-V behavior over 200 periods and the faint lines indicate the respective behavior at each of these cycles. It becomes evident that the SET process is being triggered around $220mV$, while for the RESET process

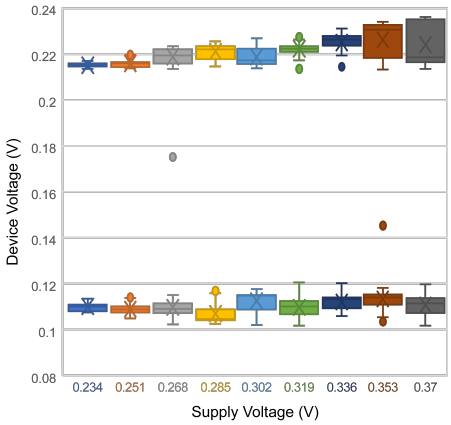


Fig. 3. Impact of variability in the range of lowest and highest voltage values under different V_{CELL}^{HIGH} supply voltages for the oscillating output (V_{WAVE}).

$\simeq 110mV$ are sufficient, with the device variability altering these values by $\pm 1.5\%$ and $\pm 2.6\%$, respectively. This result demonstrates the stochastic nature of the CB formation and dissolution processes due to the combination of drift, diffusion, and thermo-diffusion effects. As the memristor plays a vital role in WCA operation by producing the required oscillation, its variability impact on output oscillation requires to be properly investigated.

IV. Impact of Variability on Oscillations

Focusing on complex circuits and systems, the propagation of variability may generate cascading effects, amplifying the impact on the overall system performance. In IC design such undesirable fluctuations can lead to compromised functionality and reduced yield. It is vital to understand these changes in order to mitigate the adverse effects and manage the impact of variability [30], enabling the design of robust and reliable electronic systems that can tolerate and adapt to component fluctuations, ensuring consistent and predictable performance under varying operating conditions.

Regarding the WCA circuitry and in particular the oscillatory part, the simulated distributions of the lowest and highest voltage variations seen in the output oscillation voltage amplitude V_{WAVE} under different V_{CELL}^{HIGH} supply voltages are depicted in Fig. 3 for over 100 cycles. Thus, it becomes evident that the stochastic behavior of an oscillation is increasing by increasing the supply voltage to the oscillator unit. At the

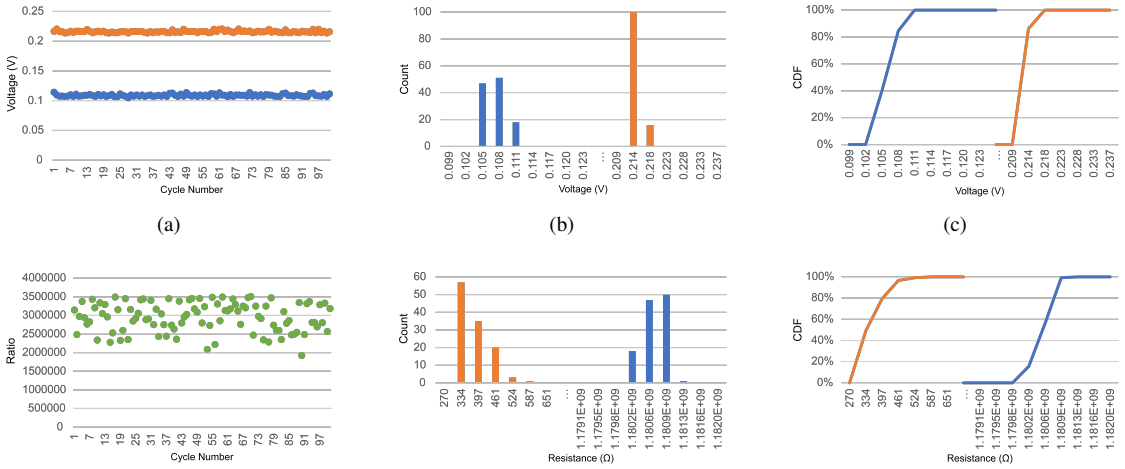


Fig. 4. (a) Evolution of the oscillation output V_{WAVE} at the lowest and the highest oscillation voltages as a function of the number of cycles. (b) Distributions and (c) cumulative distribution functions of the oscillation output V_{WAVE} at the lowest and the highest oscillation voltages. (d) SET and RESET resistances ratio as a function of the number of cycles. (e) Distributions and (f) cumulative distribution functions of the SET and RESET resistances. The aforementioned simulations have been performed for $V_{CELL}^{HIGH} = 0.251V$.

same time, there are cases (i.e. $0.268V$ and $0.353V$) that oscillation is falsely activated with catastrophic results for the computing outcome of the WCA. Considering the fact that oscillation synchronization is playing a vital role for the computing phase of the WCA, it is important to keep variations as low as possible avoiding false activations. As such, the case of $V_{CELL}^{HIGH} = 0.251V$ is considered for a more detailed analysis.

In Fig. 4, key measurements regarding the impact of device's variability on the oscillation are presented, derived from a wide range of simulations. Beginning with Fig. 4(a), the time evolution of the oscillating output highest and lowest points is illustrated, denoted as V_{WAVE}, across the entire span of simulation cycles. Subsequently, in Fig. 4(b), the histogram depicted represent the relationship between applied voltage amplitudes and the corresponding switching counts for both the SET and RESET operations that form a symmetric distribution. Fig. 4(c) showcases the cumulative distribution function (CDF) of the respective voltages with RESET voltages to showcase higher CTC variability effects. At this point, it is important to highlight that these oscillations points have presented a reduced variability effect to $\pm 0.8\%$ and $\pm 1.8\%$ for highest and lowest point accordingly. This can be attributed to the RC circuit in parallel with the CBRAM device that is able to minimize variability impact on oscillation through its time delaying and filtering phenomena.

Shifting our focus to Fig. 4(d), the High-Resistance State (HRS) to Low-Resistance State (LRS) switching ratio performance measured over successive cycles is presented showcasing a good state variability of the device to around 3×10^6 for most of the cases serving successfully the computing operations. In Fig. 4(e), the histogram display the resistance values obtained in both HRS and LRS states, along with the frequency of their occurrence. It is evident that resistances in LRS present a positively skewed distribution, while in HRS a negatively skewed one, showcasing the resistance limits in which the oscillation changes slope. Finally, Fig. 4(f) presents the CDF corresponding to the information previously described.

V. Discussion and Conclusions

The integration of variability-aware design methodologies can facilitate the optimization procedure of system-level performance metrics while accounting for the inherent variations in individual components. By incorporating statistical analysis, process variations can be effectively modeled and managed, enabling the development of robust circuit designs that are resilient to fluctuations in device parameters. Adopting a variability-aware design paradigm is crucial for addressing the challenges posed by component variability, enabling the development of next-generation electronic systems with enhanced performance, reliability, and efficiency.

Our findings presented above indicate minor effect of variability in the operation of WCA, which can be attributed to the proper design of the circuit which utilizes the RC effects in combination with unipolar CBRAM devices. In this work, the effects of CTC variability are modeled and investigated without affecting circuit proper operation, while DTD variability has not yet been addressed and is an ongoing work. It is important to highlight that increasing supplying voltage may speed up WCA operation, but also increases oscillation variability reaching to even catastrophic results in some cases, which leads to the conclusion that properly selected elements are vital for successful circuit operation. Further experimentation with the device structure can aid in further minimizing the CTC variability effects, while investigating parameters such as noise, sparsity and temperature phenomena along with longer time-scales as well as DTD variability can shed light in the appropriateness of the fabrication methods employed.

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