SEMINAR
MÄLARDALENS UNIVERSITET

ADRIAN HANSSON FIELD APPLICATION ENGINEER

Agenda

- EMC Design Tips

Times:

13:15 – 14:00

14:15 – 15:00

Würth Elektronik eiSos: part of a strong & reliable family-owned company

WÜRTH GROUP

- Over 85,600 employees*
- Sales of 19.95 billion €*
- Over 400 companies
- In more than 80 countries
- Family-owned company
- Rating by Standard & Poor's: A/stable

* according to the preliminary annual financial statement 2022

Prof. Dr. h. c. mult. Reinhold Würth
Chairman of the Supervisory Board of the Würth Group´s Family Trusts

The Würth Elektronik Group

1.33 bn €
Sales

15
Quality & Design Centers

8,200
Employees

23
Production plants

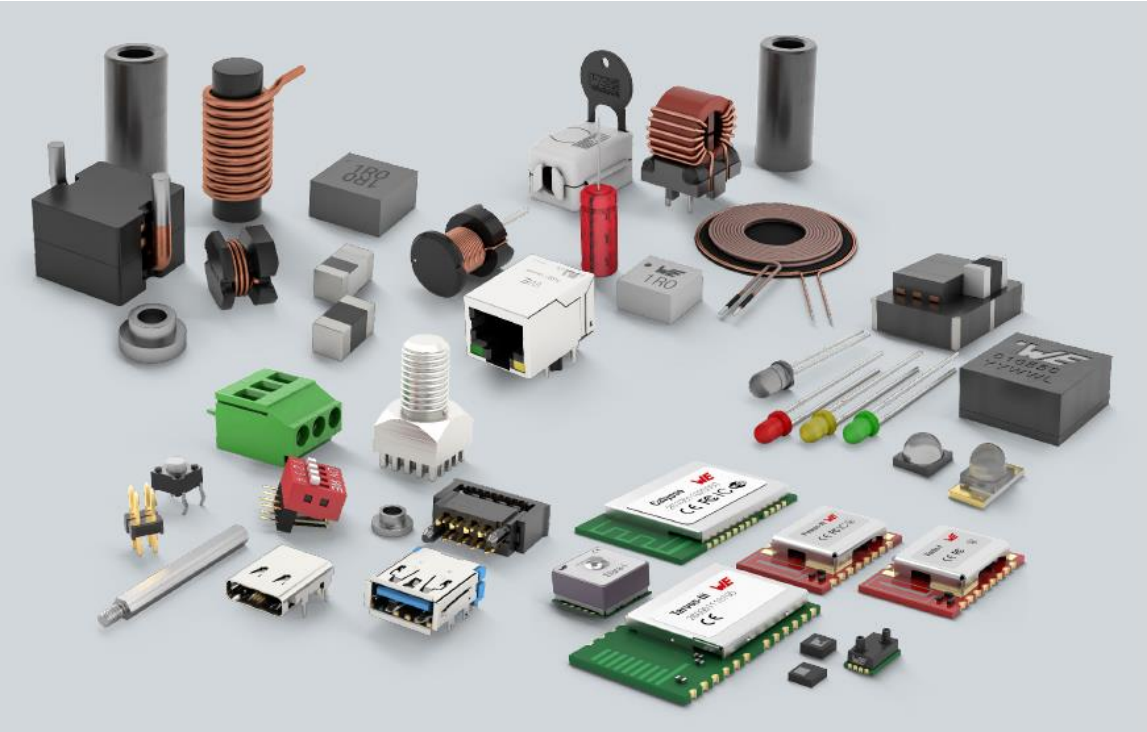
50
Countries

13
Warehouses

More Details

The Würth Elektronik Group

Würth Elektronik eiSos
Electronic & Electromechanical Components



Würth Elektronik CBT
Printed Circuit Boards

Würth Elektronik ICS
Intelligent Power- and
Control Systems

Less Details

EMC DESIGN TIPS

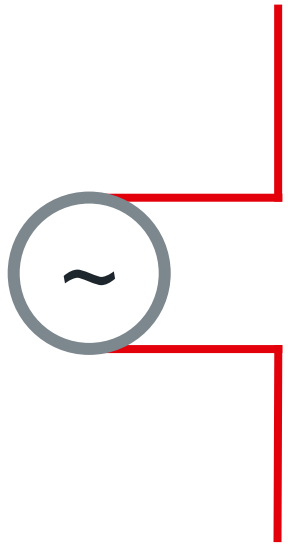
WÜRTH ELEKTRONIK MORE THAN YOU EXPECT

Agenda

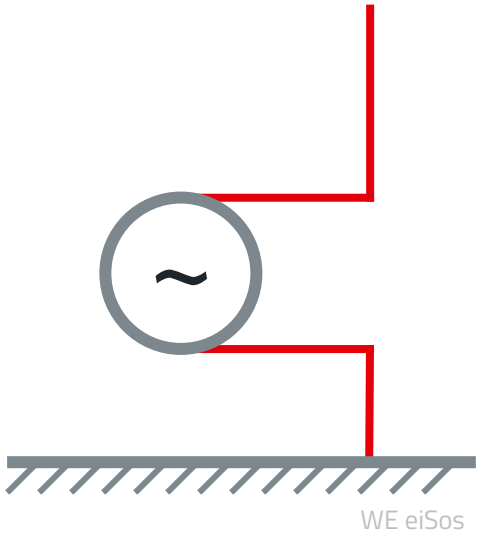
- Coupling paths
- Ground Concept
- Layer Stack
- Filter Capacitors & Via Arrangement
- Filter Placement
- Layout Considerations
  - Power Inductors
  - Overvoltage Protection
  - Crystals & Oscillators
- Shielding
  - For Casings
  - For Cables

COUPLING PATHS

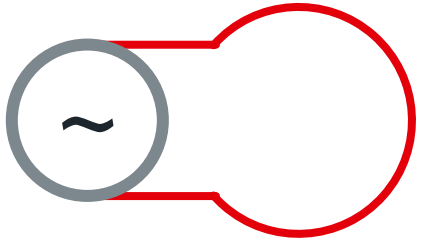
Everything is an Antenna



Electric Dipole Antenna



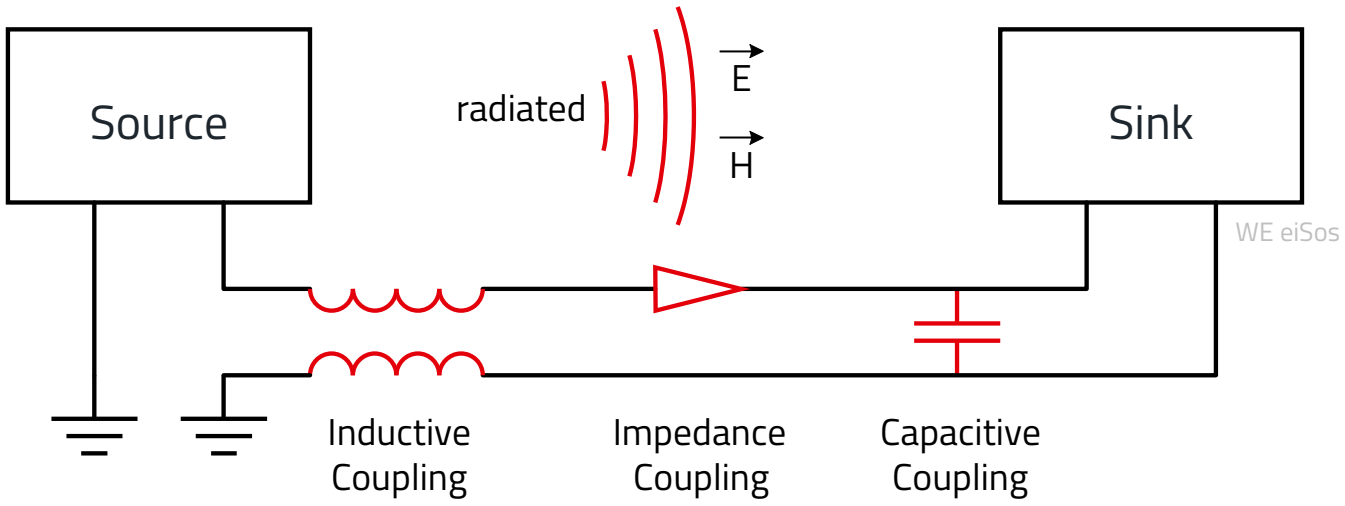
Electric Monopole Antenna



Magnetic Loop Antenna

Reducing EMI

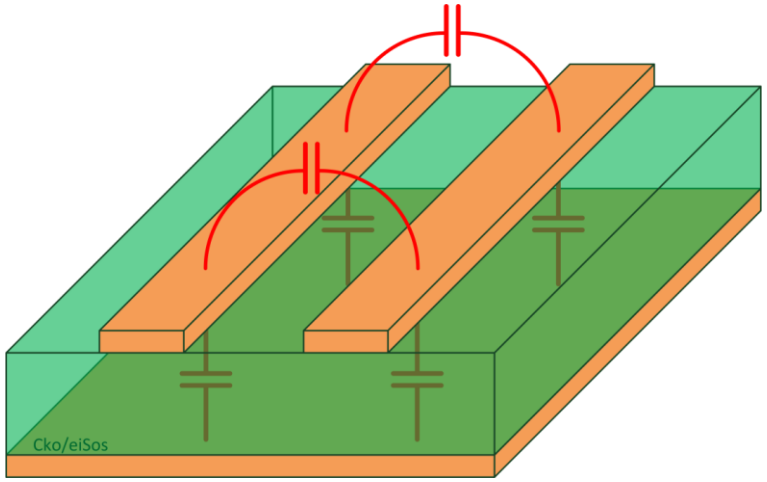
- Sufficient EMC can be achieved by suited measures at the noise source, coupling path or sink.
  - **Primary Measure** Reduce emission from noise source
  - **Secondary Measure** Break coupling paths
  - **Tertiary Measure** Increase immunity of the sink



Capacitive Coupling

Origins

- Originates from high dU/dt
- Parallel conductors form a parasitic capacitance
- Coupling capacitance is directly proportional to the length of the parallel trace run



Isolating Components	typ. Coupling Capacitance
Optocoupler	1 ~ 5pF
Solid State Relay	5 ~ 10pF
Electromechanical Relay	10 ~ 100pF
Transformers in SMPS	Up to 1000 pF

Capacitive Coupling

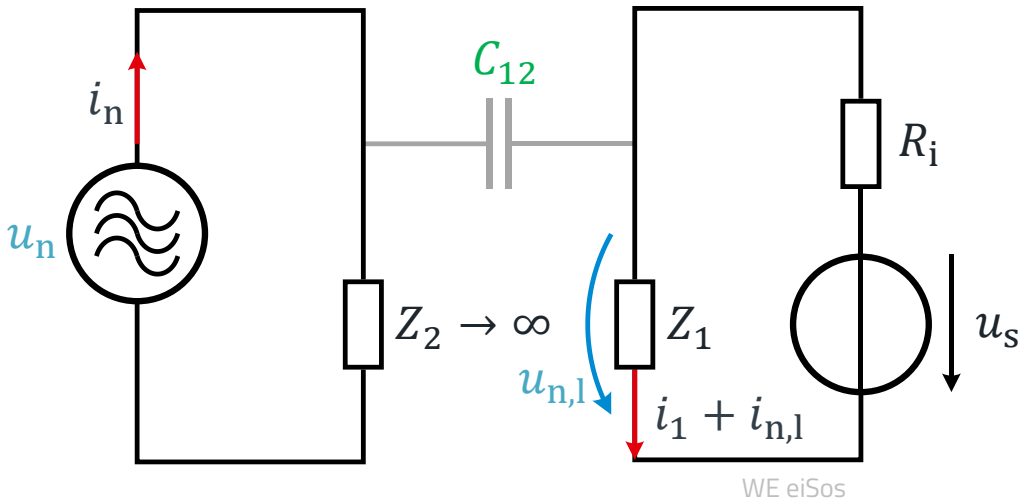
Effects

- Dominant, if structure dimensions are smaller than 10% wavelength of the exciting electric field (< λ/10).
  - Why λ/10? → Harmonics

- Voltage interference at the load:

$$u_{\mathrm{n,l}} = i_{\mathrm{n}} \cdot \frac{R_{\mathrm{i}} \cdot Z_1}{R_{\mathrm{i}} + Z_1} = C_{12} \cdot \frac{\mathrm{d}u_{\mathrm{n}}}{\mathrm{d}t} \cdot \frac{R_{\mathrm{i}} \cdot Z_1}{R_{\mathrm{i}} + Z_1}$$

$$C_{12} = \varepsilon * \frac{A}{d}$$



Capacitive Coupling

Measures to decrease coupling

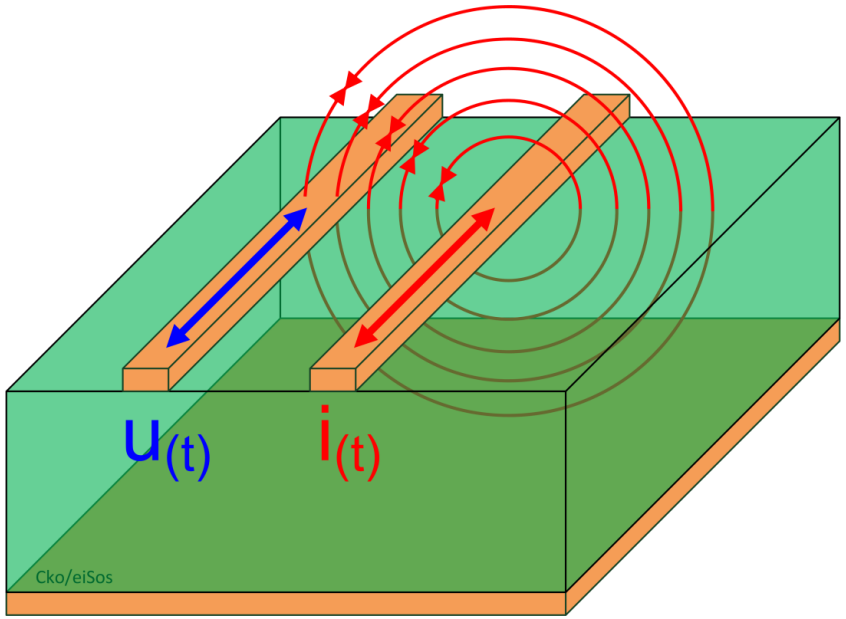
- **Primary Measure**
  - Decrease dI/dt by selecting a slower signal edges
  - A Low pass filter to take off the edges

- **Secondary Measure**
  - Shorten/avoid parallel trace runs
  - Small areas for switched polygons (e.g. DC/DC switch node)
  - Increase distance between affected paths
  - Electrical shielding (Cable, PCB, Housing)

Inductive Coupling

Origins

- Originates from high dI/dt
- Parallel traces form a parasitic transformer
- Mutual Inductance increases with shorter distance



Inductive Coupling

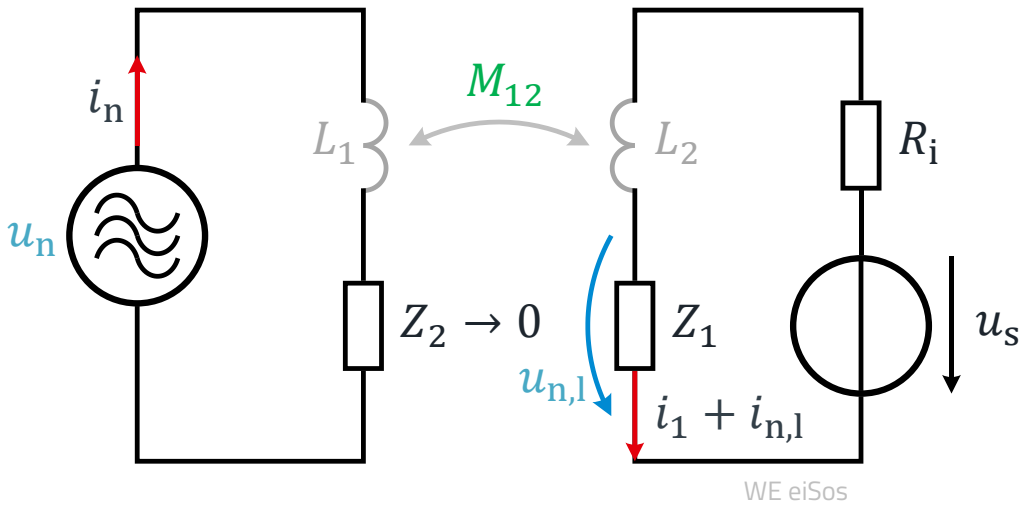
Effects

- Takes effect, if loops are larger than 25% the wavelength of the exciting magnetic field (< λ/4).

- Voltage interference at the load:

$$u_{\mathrm{n,l}} = M_{12} \cdot \frac{\mathrm{d}i_{\mathrm{n}}}{\mathrm{d}t} \cdot \frac{Z_1}{R_{\mathrm{i}} + Z_1}$$

$$M_{12} = \mu * N_1 N_2 * \frac{A}{l}$$



Inductive Coupling

Measures to decrease coupling

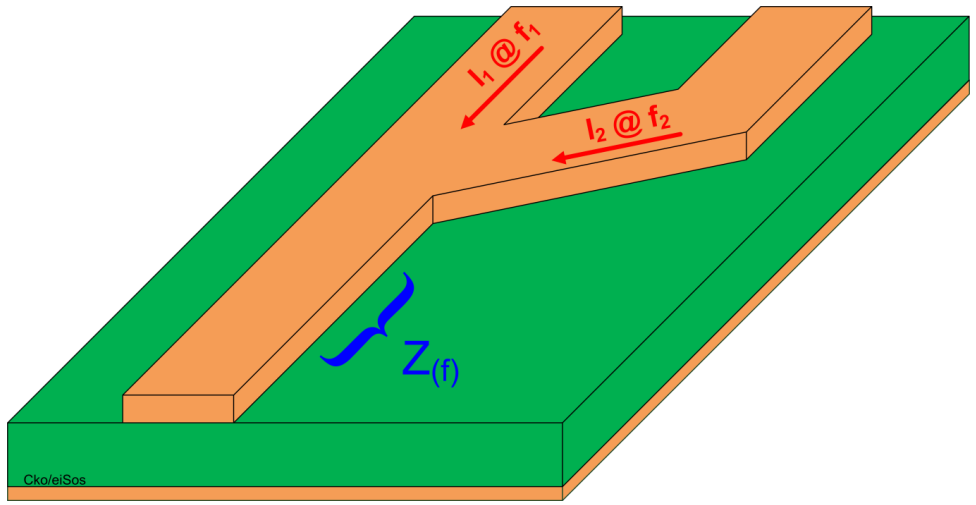
- **Primary Measure**
  - Decrease dI/dt by selecting a lower switching frequency and slower signal edges
  - A filter Inductor/Ferrite to take off the edges

- **Secondary Measure**
  - Decrease magnetic loop area
  - Increase distance between affected circuits
  - Orthogonal component placement
  - Magnetic shielding with ferrite materials (soft permeability, high μ_r)

Impedance Coupling

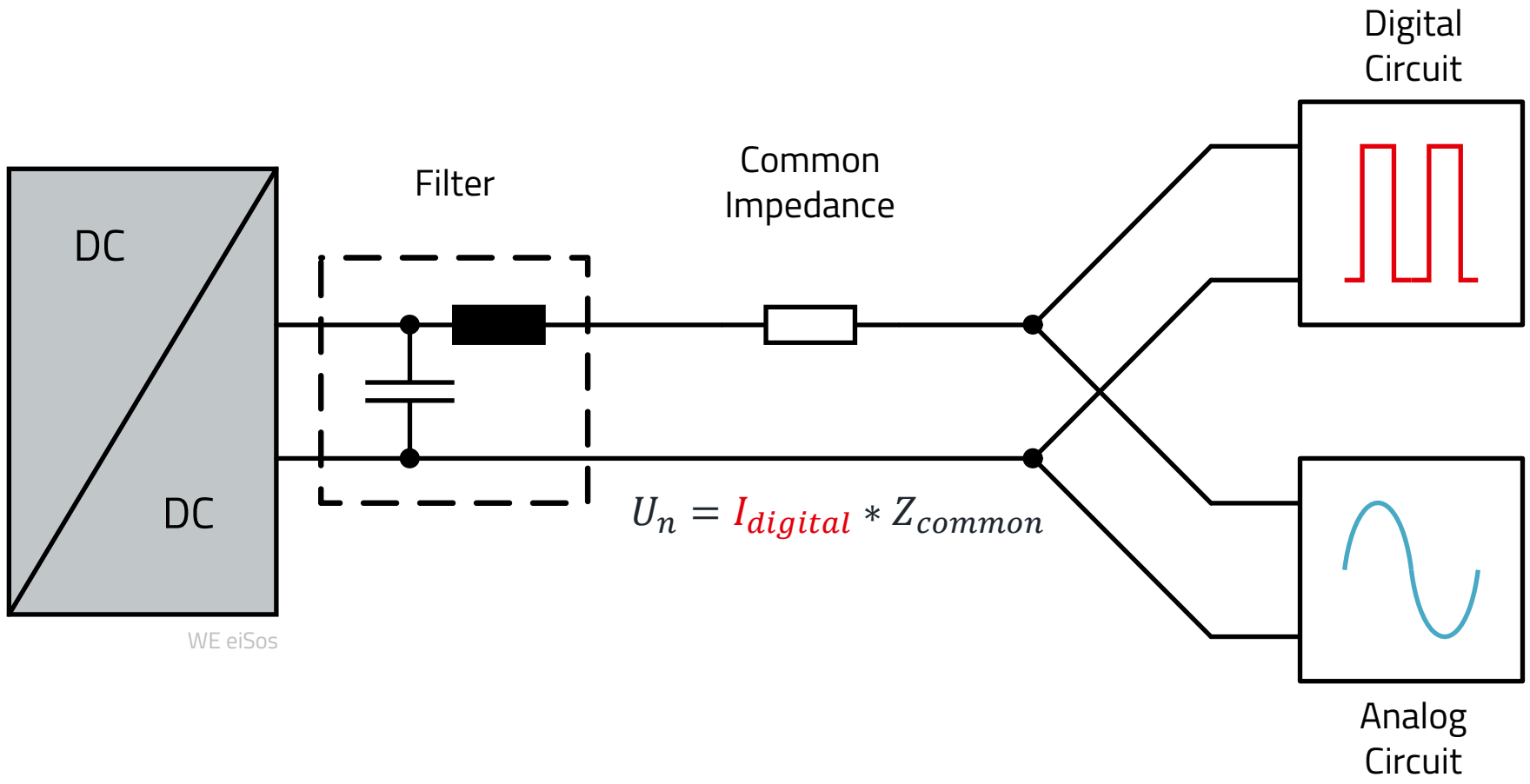
Origins

- Interference affects circuits with a mutual traces
- Circuits share an impedance and therefore the voltage across that impedance
- Main cause for high mutual impedances is self-inductance across copper traces



Impedance Coupling

A closer look



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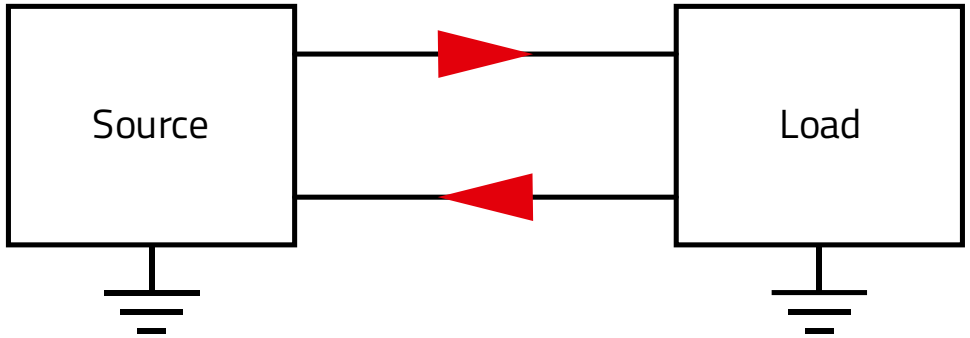
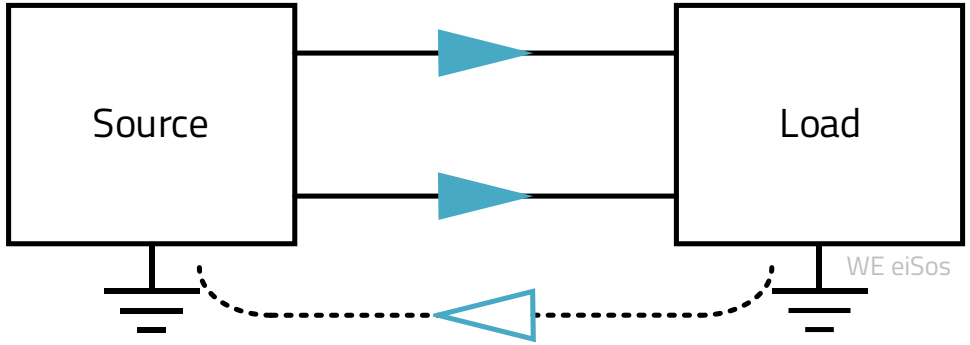
Noise Transmission Modes

Differential Mode



- Noise and useful signal use the same paths
- Earth is not affected

Common Mode

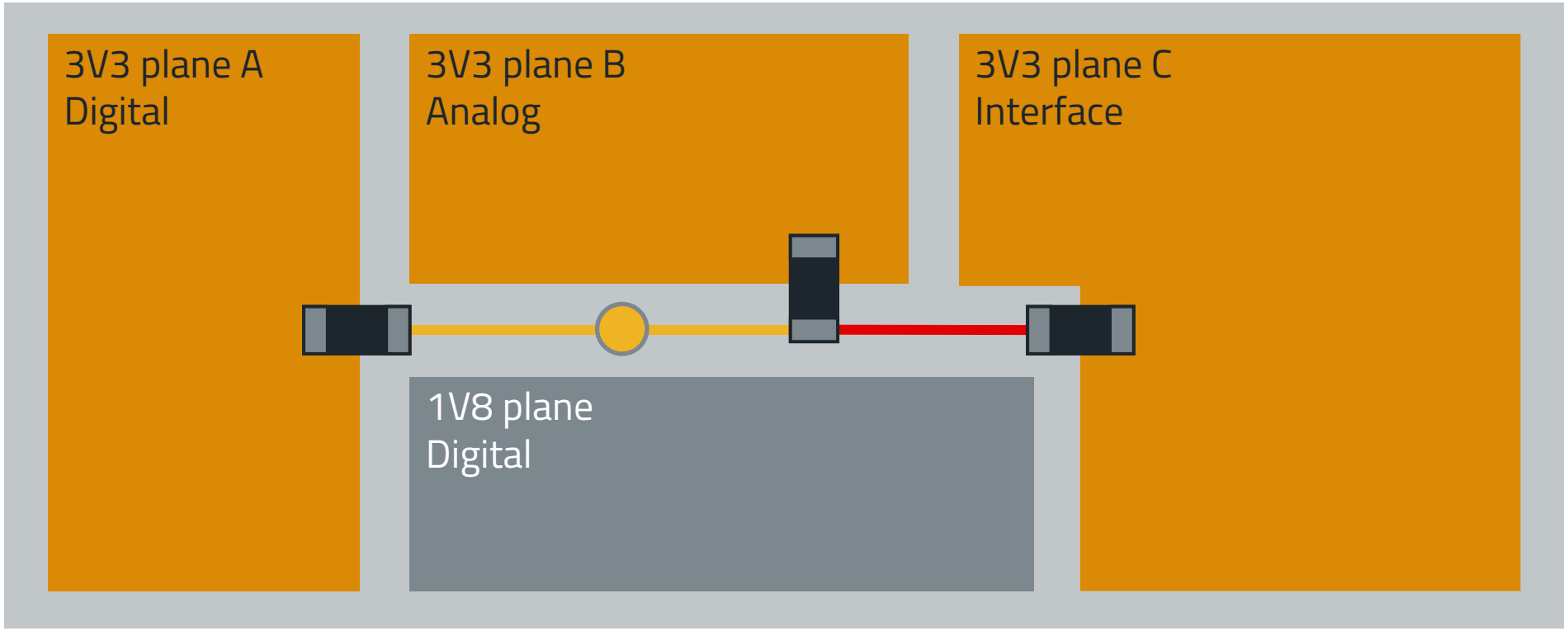


- Noise uses both lines in same direction
- Earth is used a return path

GROUND CONCEPT

Seperating functional blocks

Power Distribution



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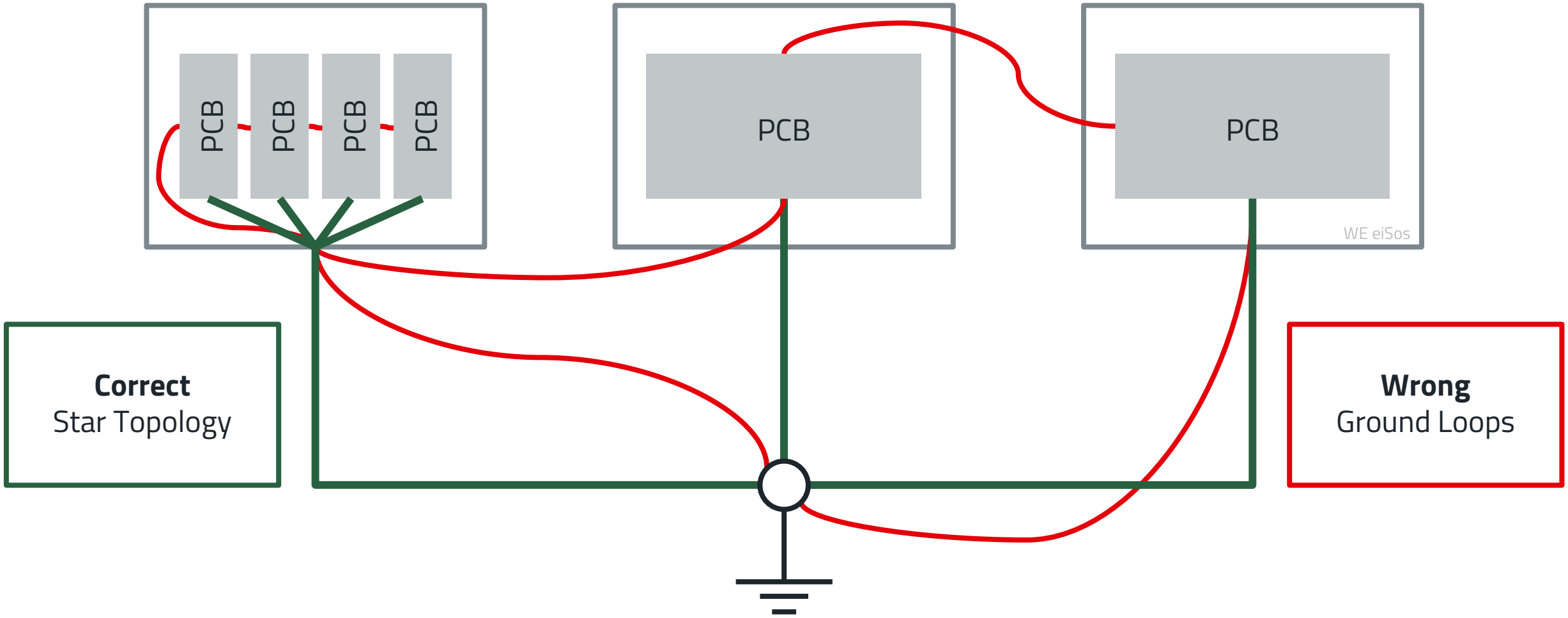
Splitting and Decoupling Vcc - Star Topology

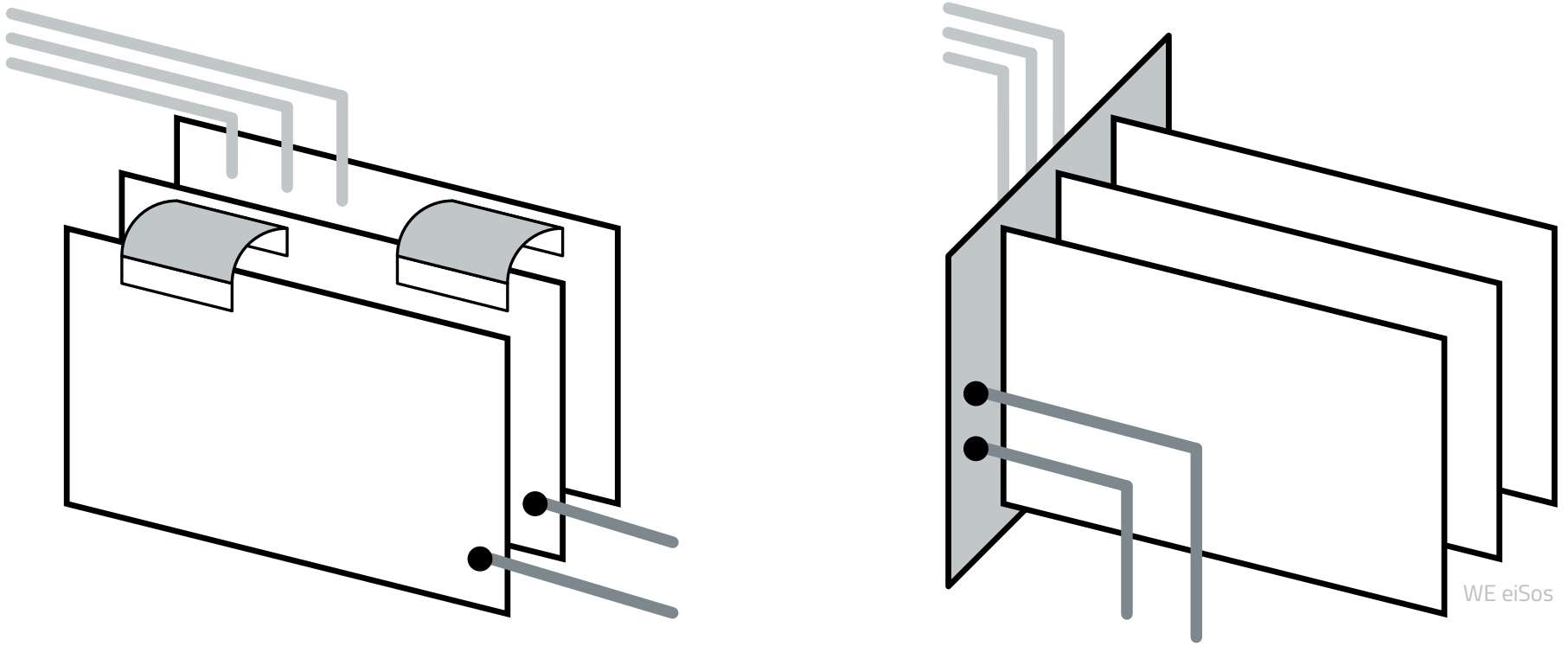
Ground Concept

Distribution across multiple PCBs



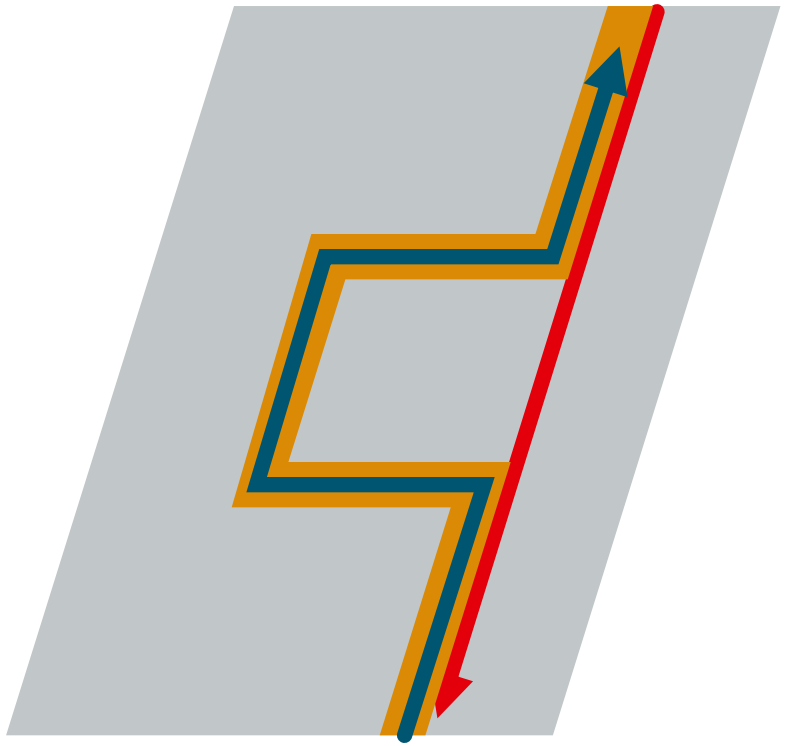
Ground Concept

Distribution across multiple PCBs

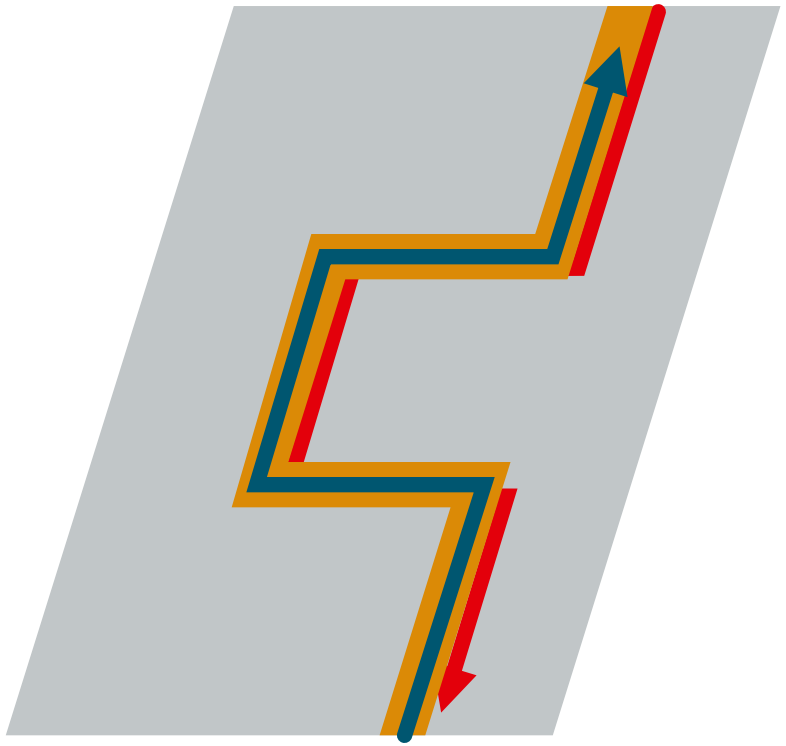


Changes in the Construction can make or break EMC

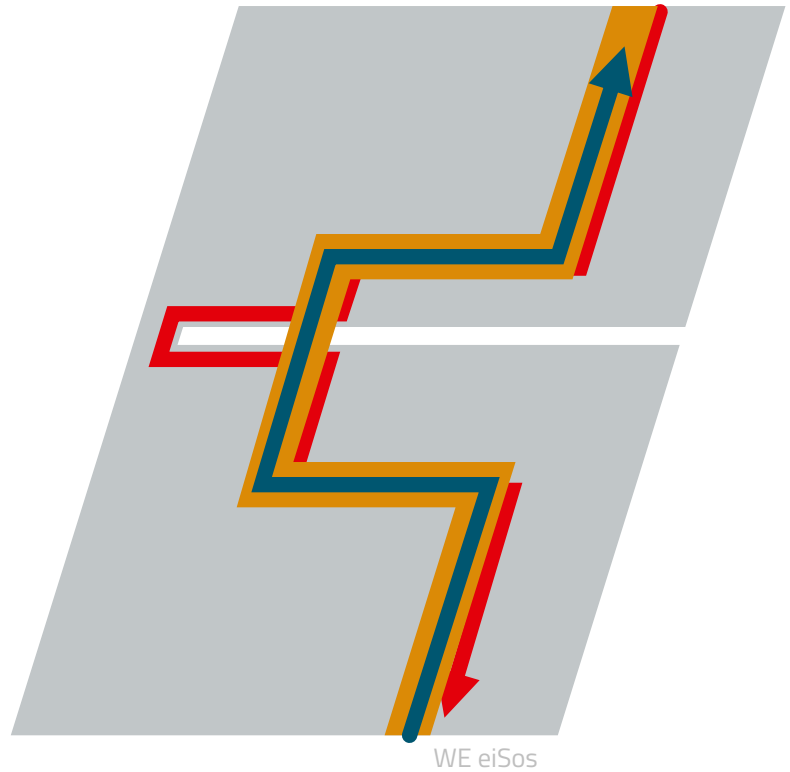
Path of least Impedance



DC Return Path



AC Return Path

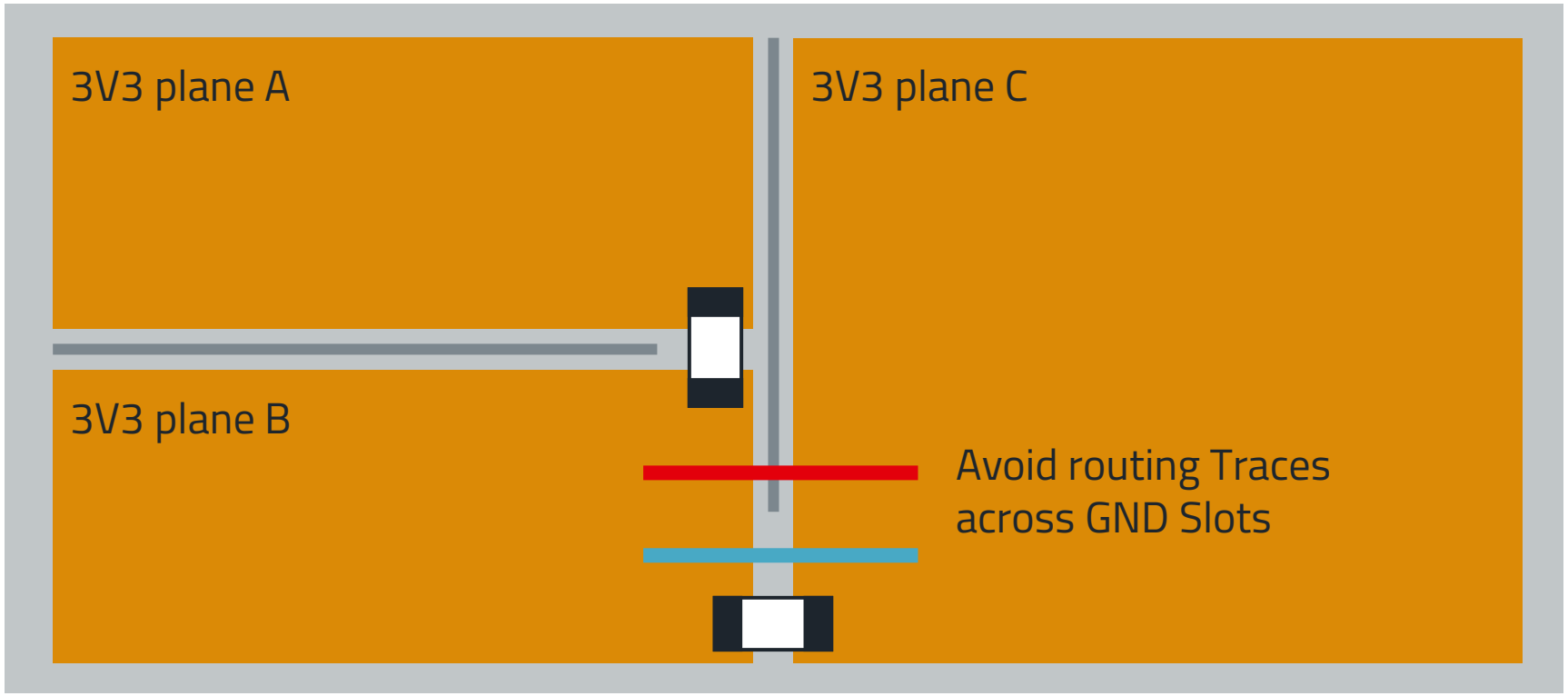


Slotted AC Return Path

Seperating functional blocks

Splitting GND?

Plane intact
@ PCB Edge



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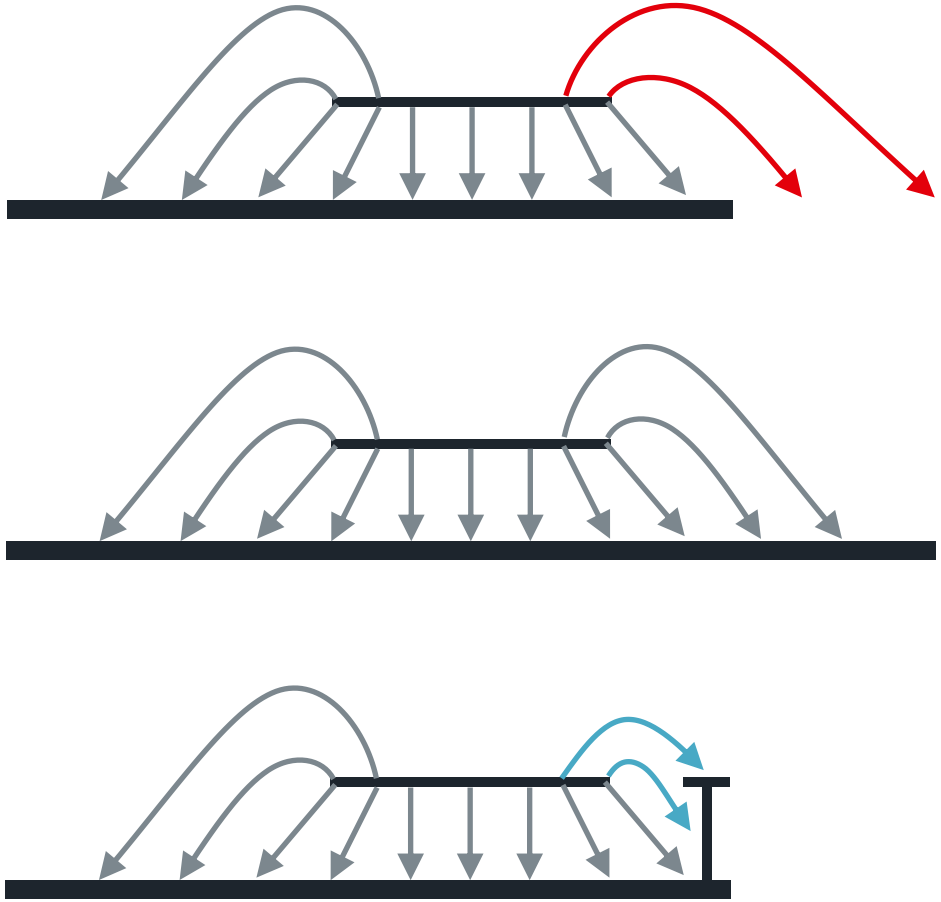
Slotting the GND Plane to form seperate reference points (AGND, DGNG, PGND)

Fringing at PCB Edges

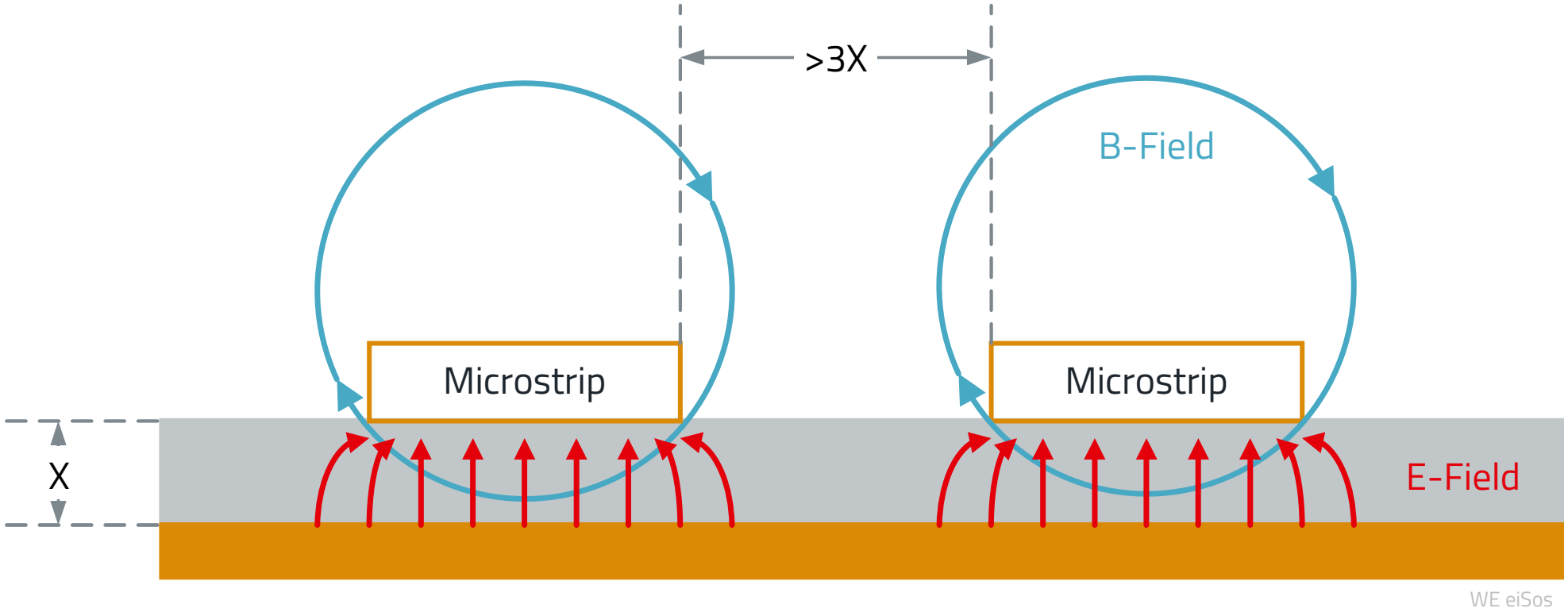
GND Guard Ring



Ca. 10mm between Vias

Minimizing Crosstalk

Distance between traces



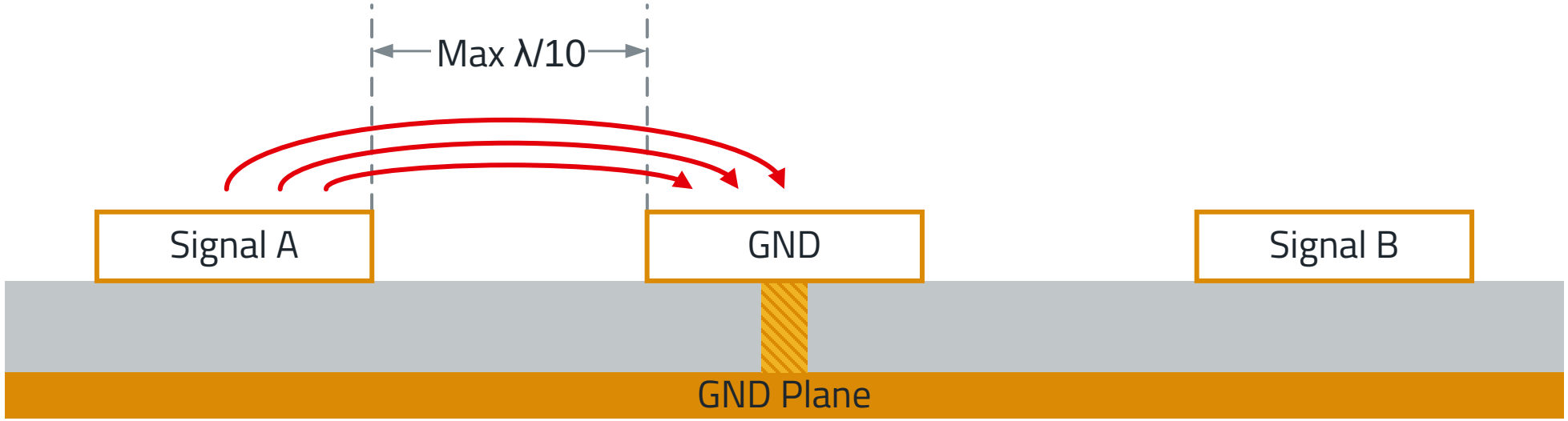
Crosstalk can be reduced to 1% by placing Strip Lines at 3 times the substrate thickness apart

Minimizing Crosstalk

GND Fence

- Inserting a copper area that is tightly bound to GND
  - Shielding the noise source

- Distance between Vias: Max. λ/10 of the highest noise frequency



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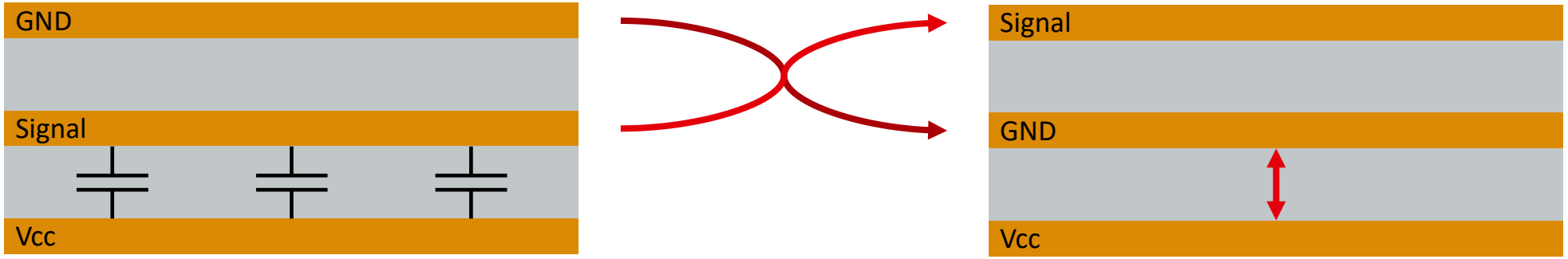
LAYER STACK

Layer Stack

Minimizing Crosstalk



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- Sandwiching the Signal Layer between GND and Vcc leads to capacitive coupling
  - Ripple, Transient Loads on Vcc can leak into Signal Layer
- GND as a shield between Signal and VCC
  - High Frequency Noise is directly diverted to Ground
  - low impedance GND Plane as reference point
- Capacitive Coupling depends on Substrate Thickness

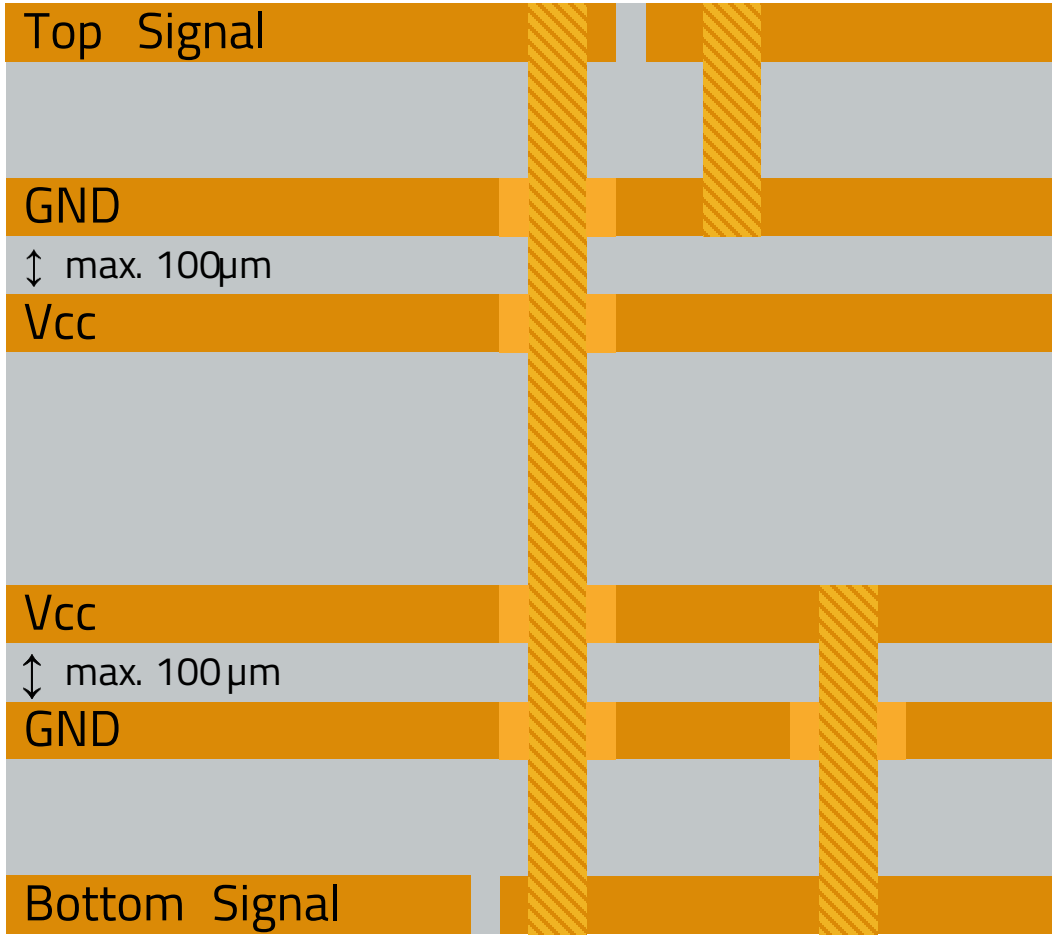
Layer Stack for double-sided PCBs

At least 6 Layers for ideal Spacing/ Routing

Layer Count is always a tradeoff

- Cost
- Routing Complexity

- Crosstalk between Signals
- Noise decoupling
- Signal Integrity
- Self Interference



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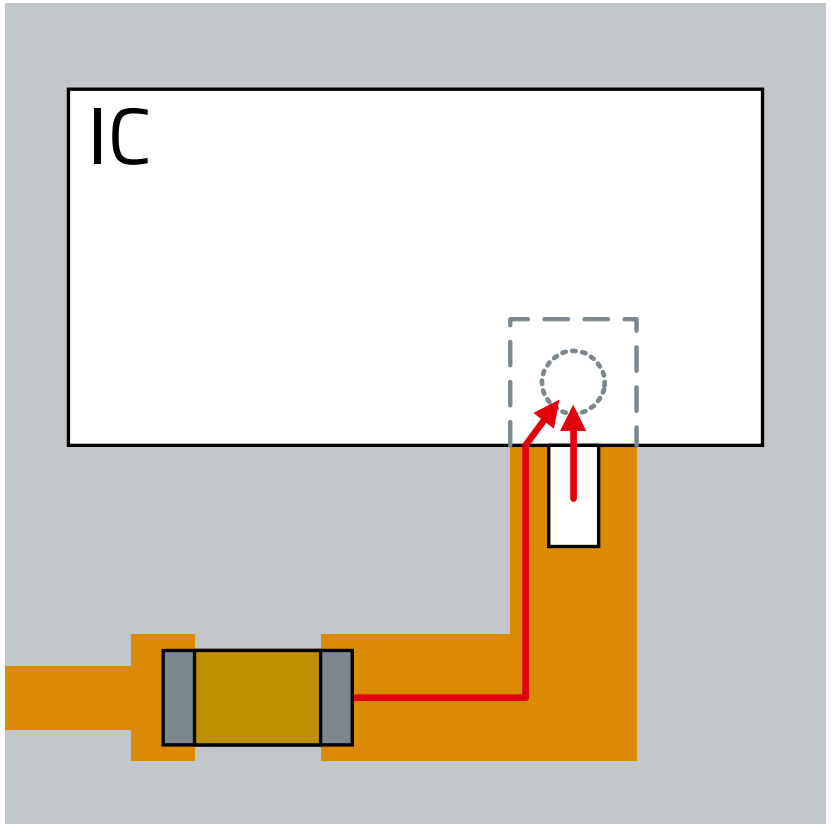
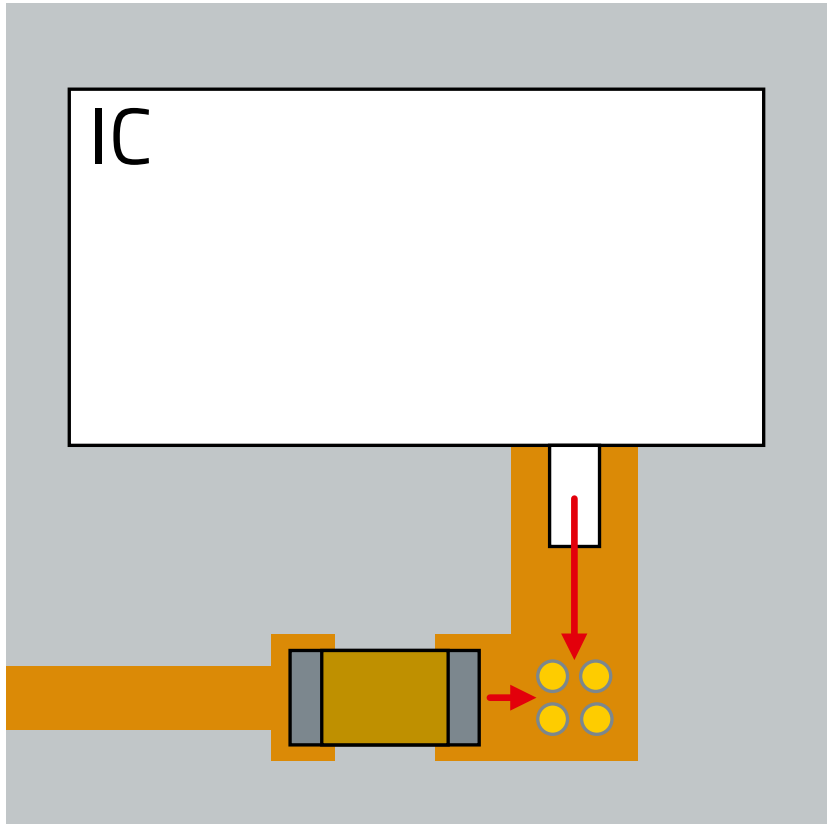
FILTER CAPACITORS & VIA ARRANGEMENT

Via Placement

Ground Connection @ IC Pins



bad



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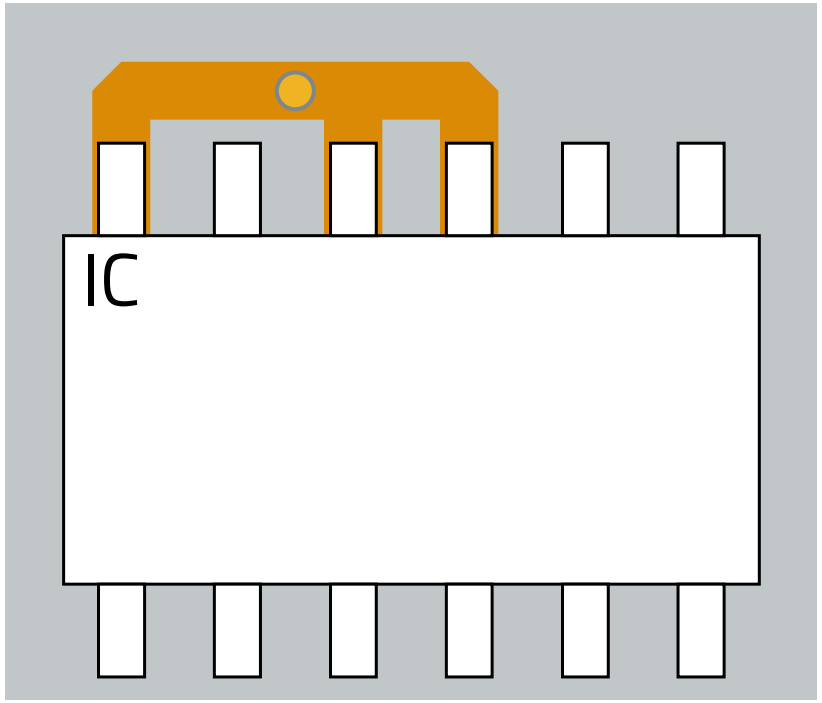
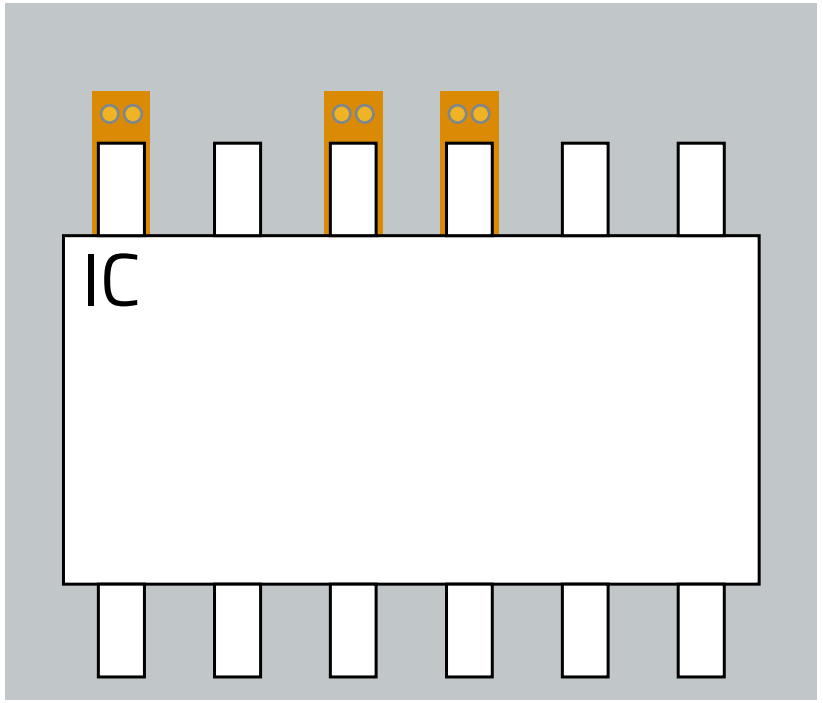
good

Via Placement

Ground Connection @ IC Pins



Bad



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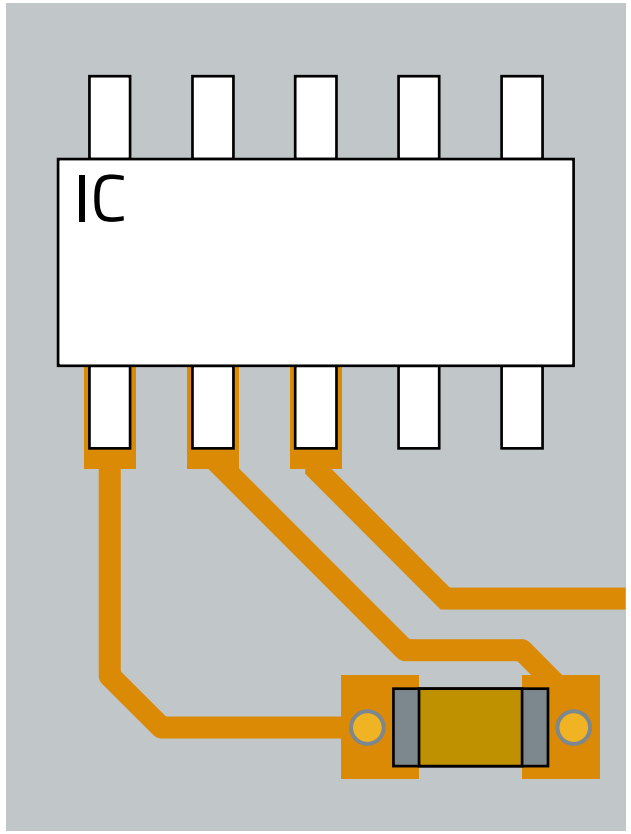
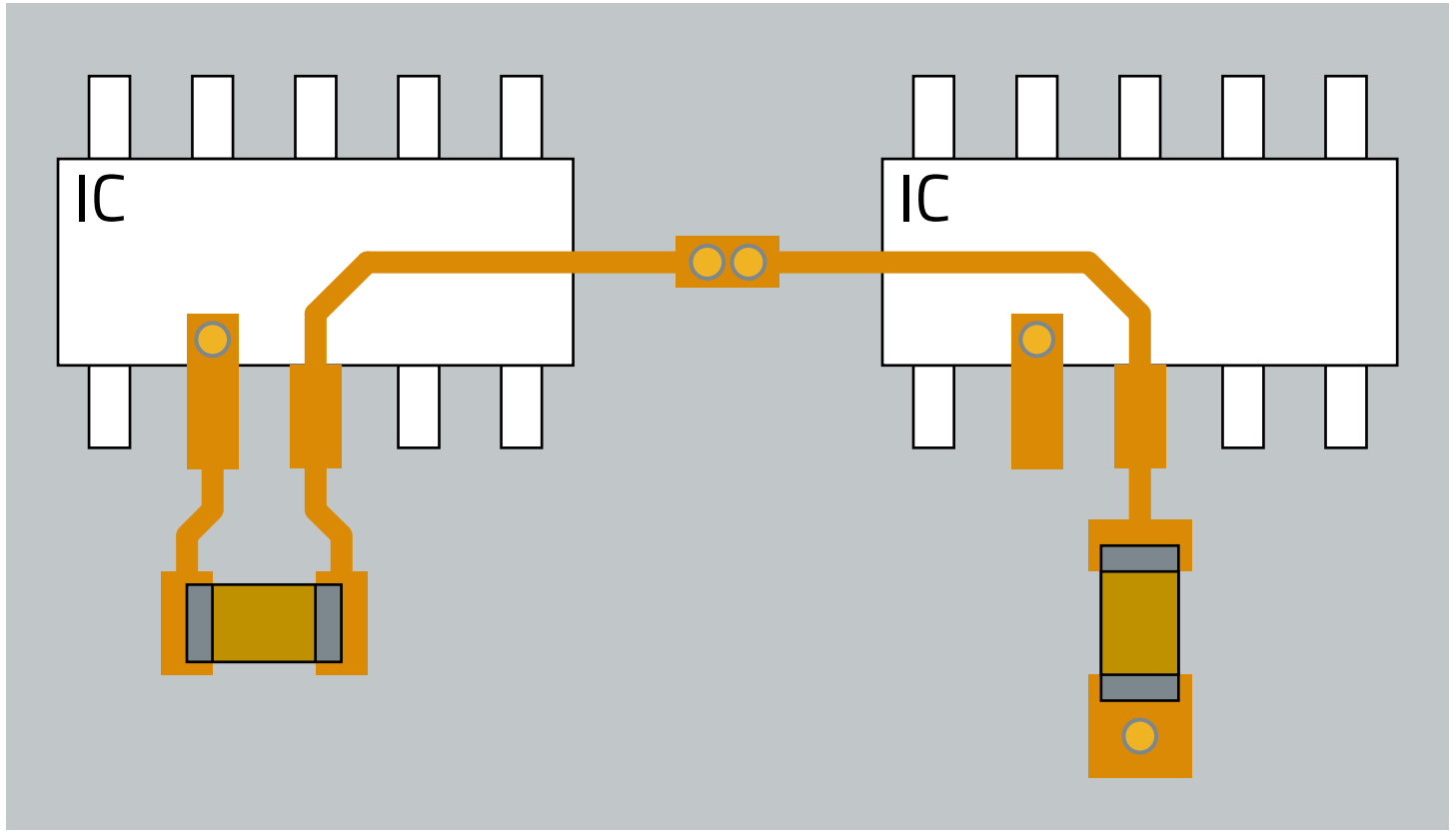
Better

Blocking Capacitors

Routing to Ground and Supply Pins



Bad
Large Loop area, Parallel Traces



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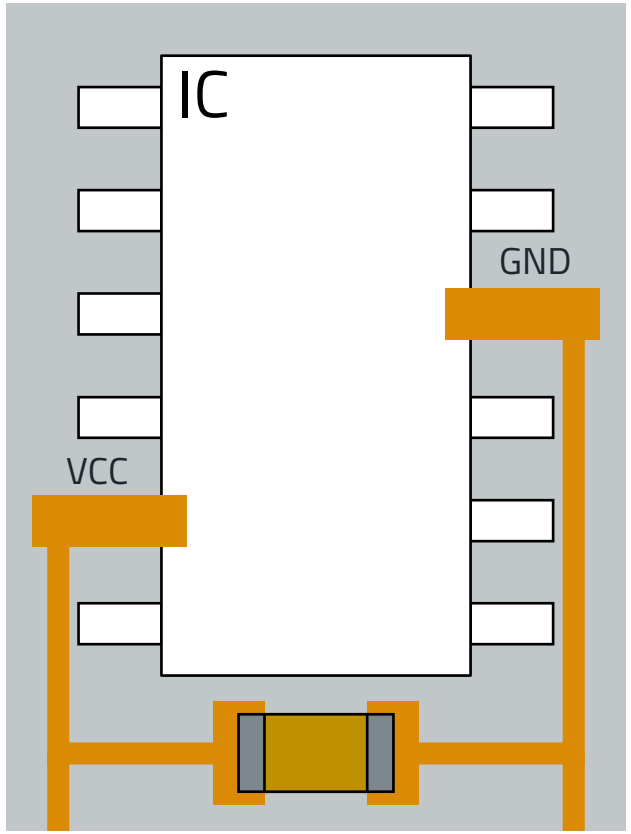
Bad
RF Current is drawn from Via instead of Cap

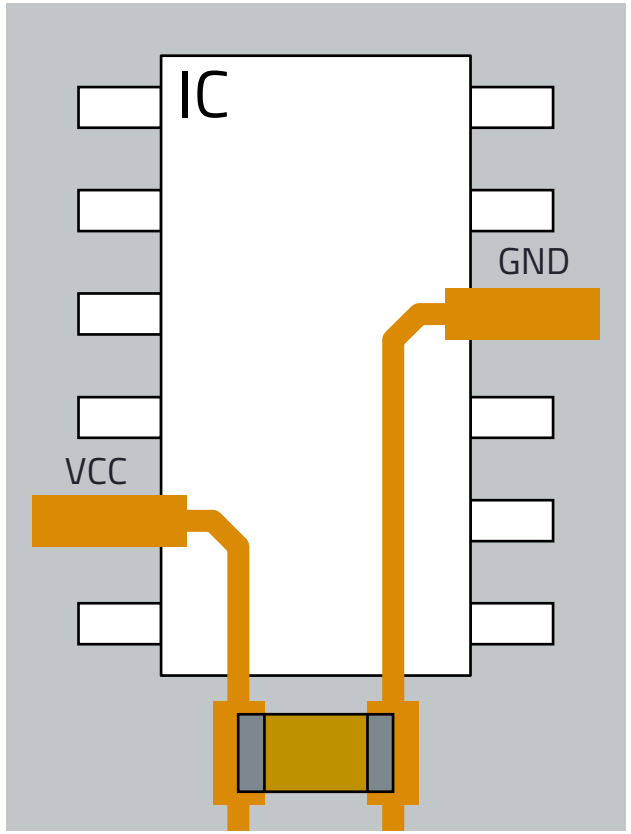
Also Bad
Shared Impedance on Vcc

Blocking Capacitors

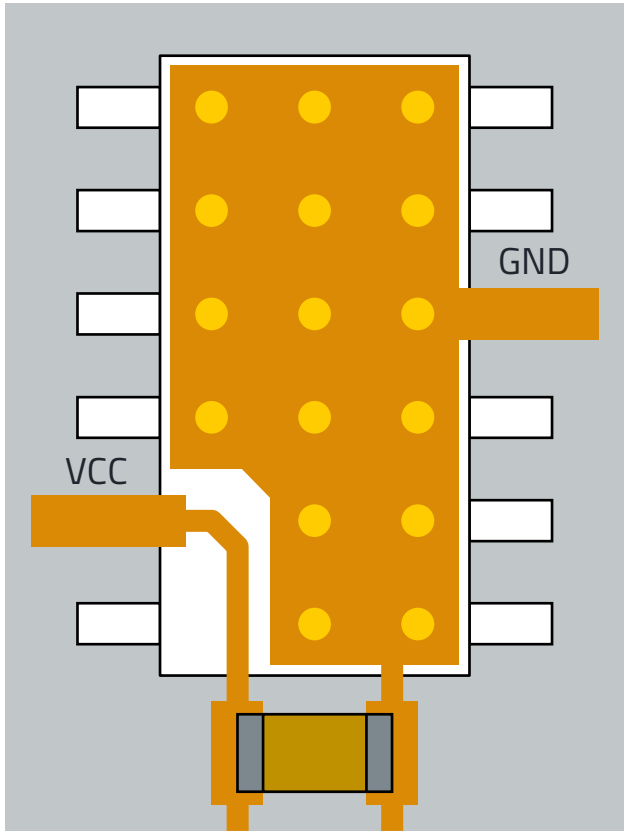
Routing to Ground and Supply Pins



Bad
Connecting the Cap using stubs



Good
Directing current along Capacitor pads



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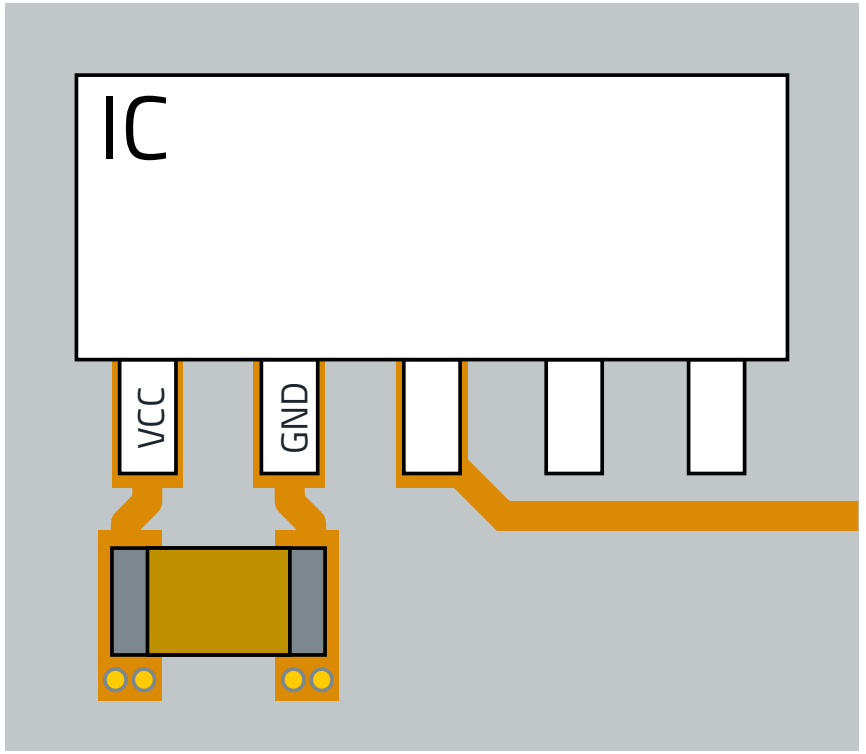
Better
GND Plane to account for loops inside the IC

Blocking Capacitors

Routing to Ground and Supply Pins

- RF Currents are fed from the Capacitor
  - Vcc/GND Plane only see low frequency currents
  - Keeps magentic loop for RF as small as possible
  - Distance of Cap to PIN ≤ 0,3mm
- Low impedance connection to the capacitor
  - Keep lines symmetrical (if possible)
- Parallel Vias reduce impedance to GND/Vcc planes



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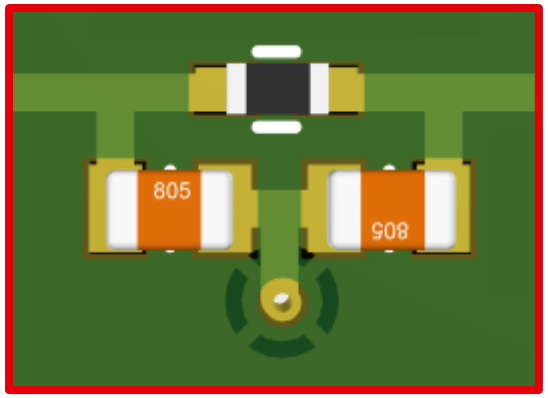
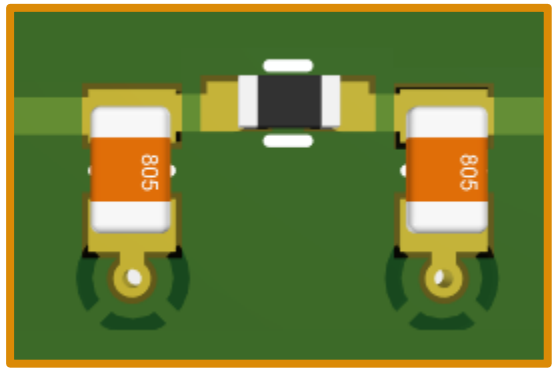
Filter Arrangement

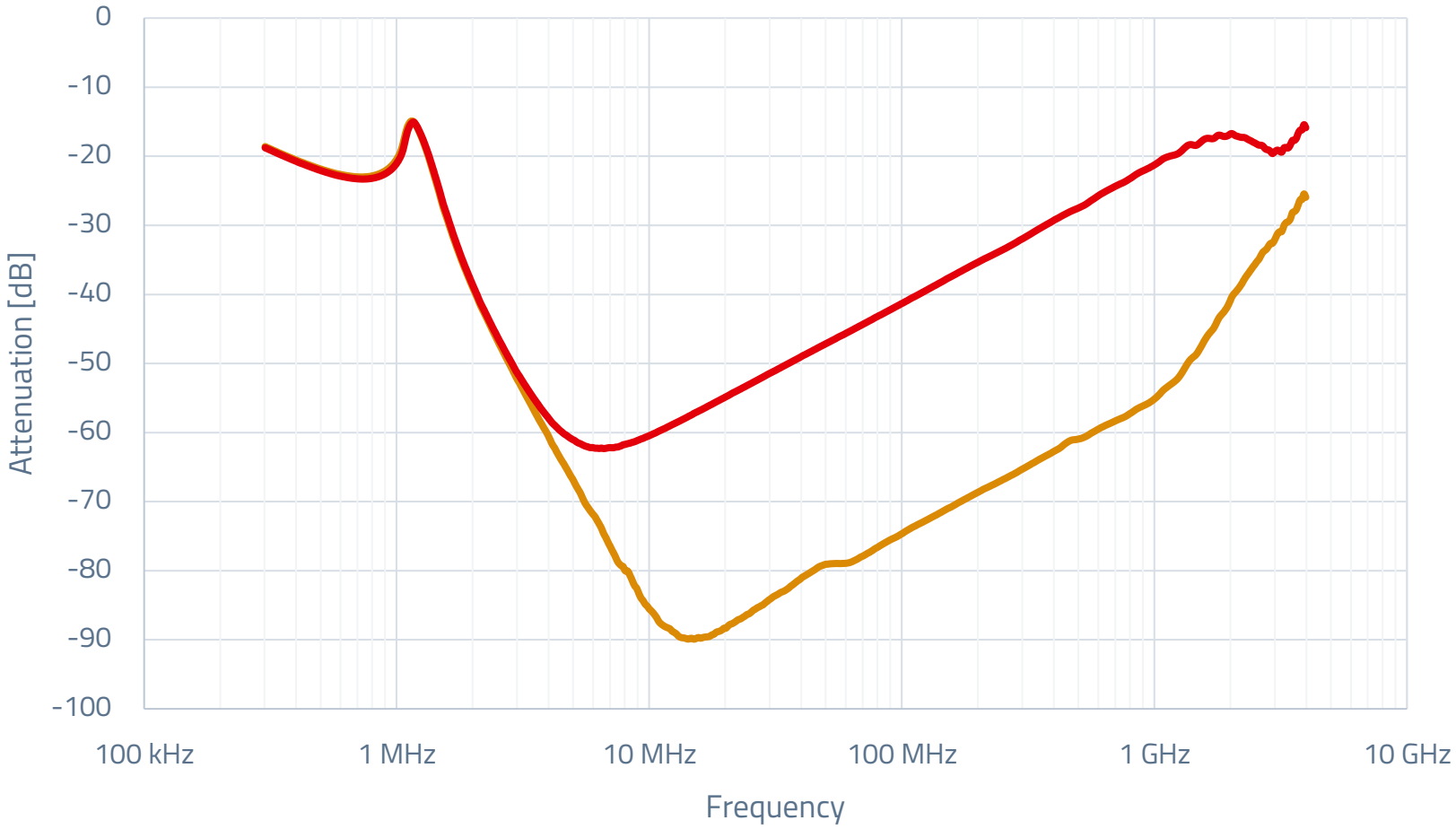
Layout: Influence on Insertion Loss



0805, Bad Layout

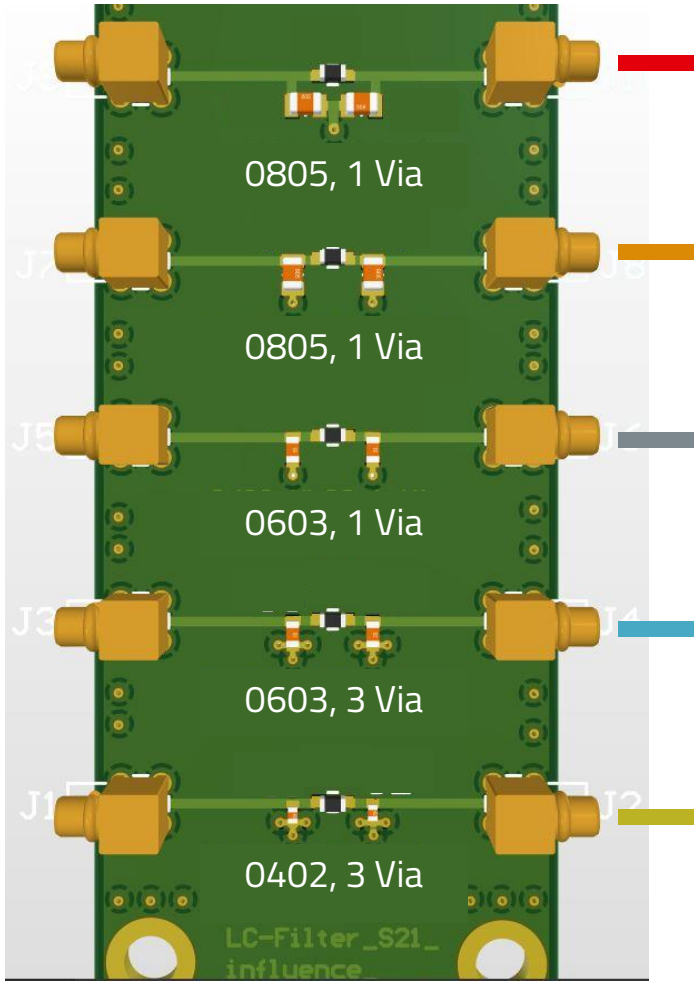


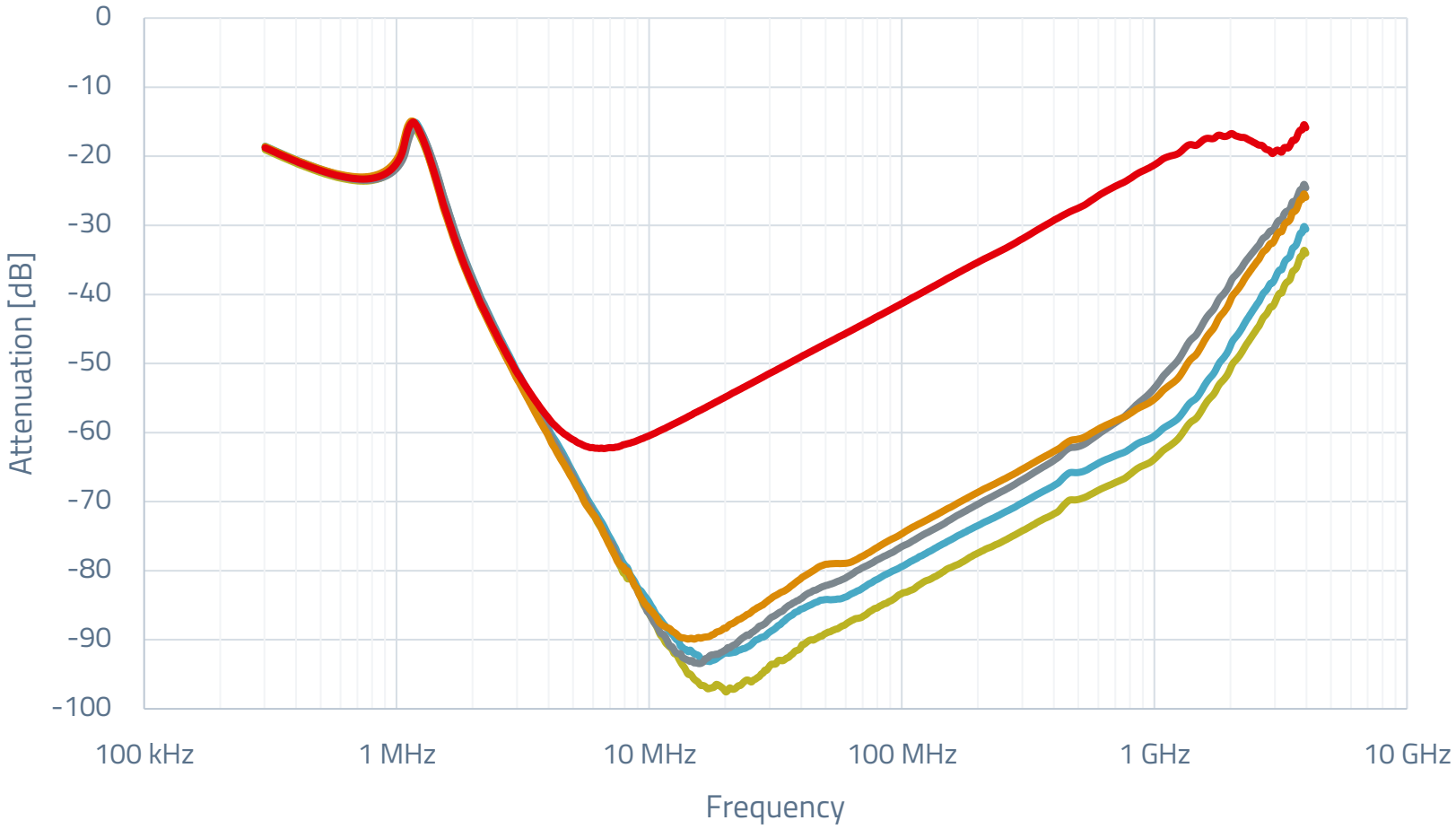
0805, Good Layout



Filter Arrangement

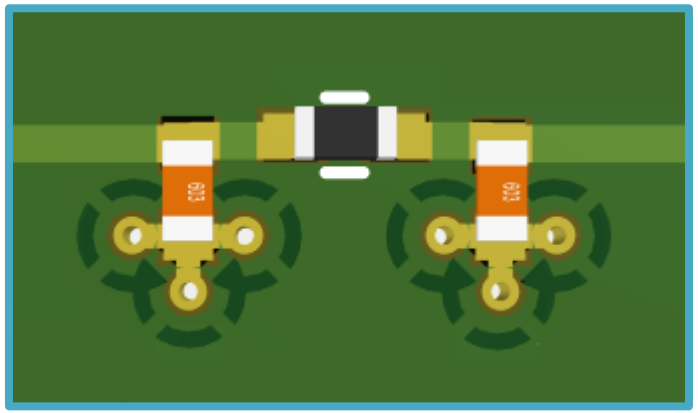
Size and Via Count: Influence on Insertion Loss



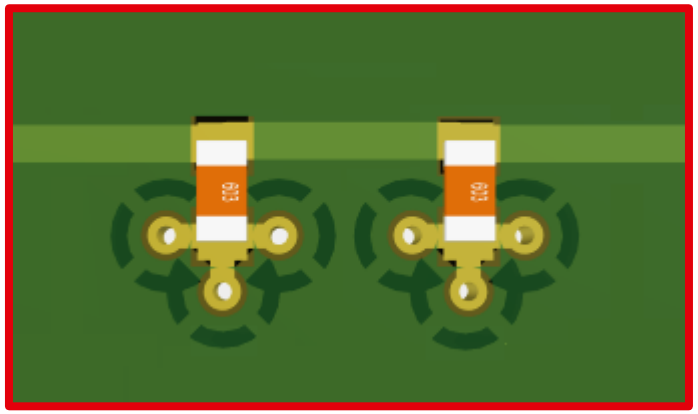


Filter Arrangement

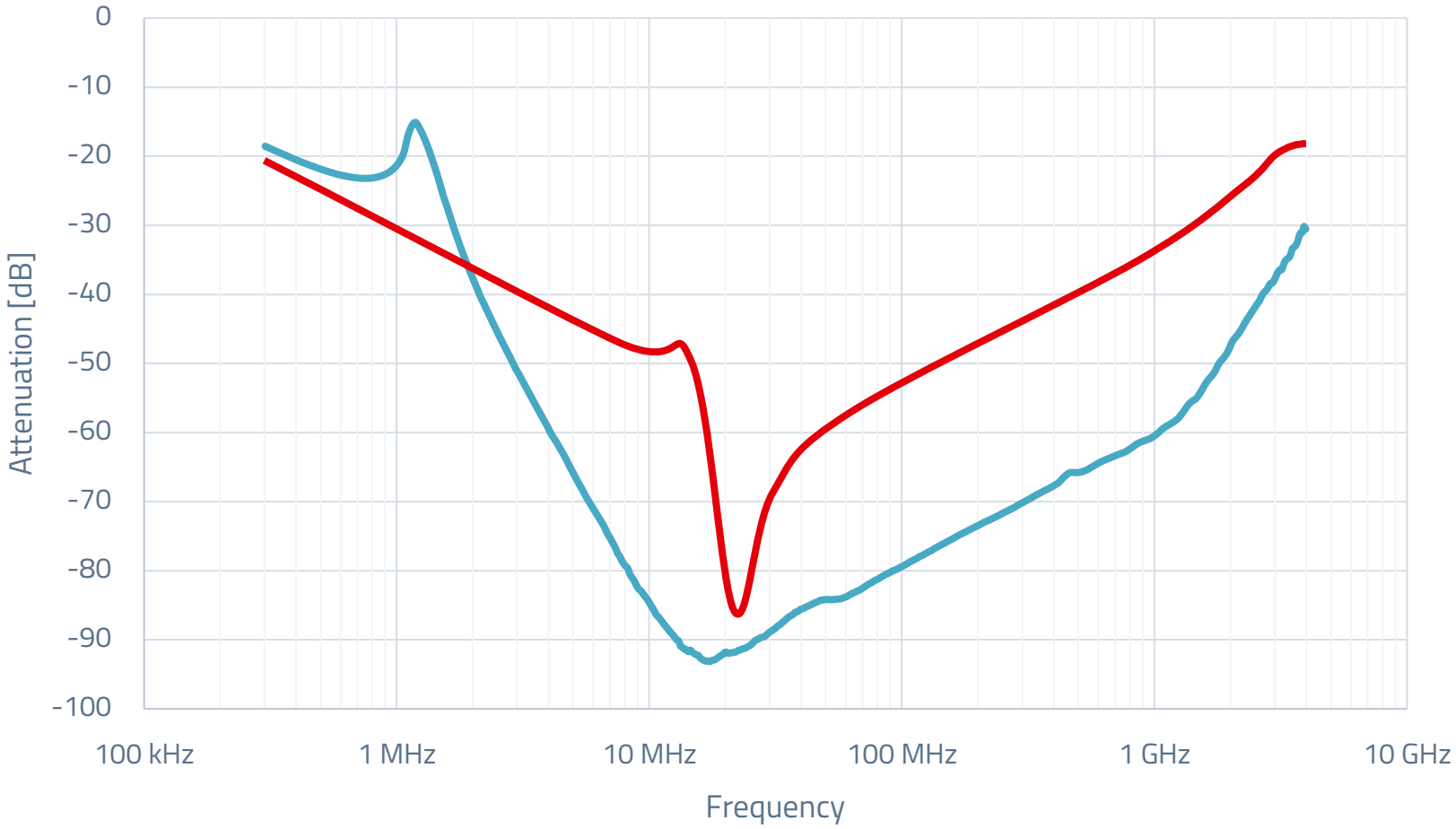
Caps vs. T-Filter: Influence on Insertion Loss



0603, with Ferrite

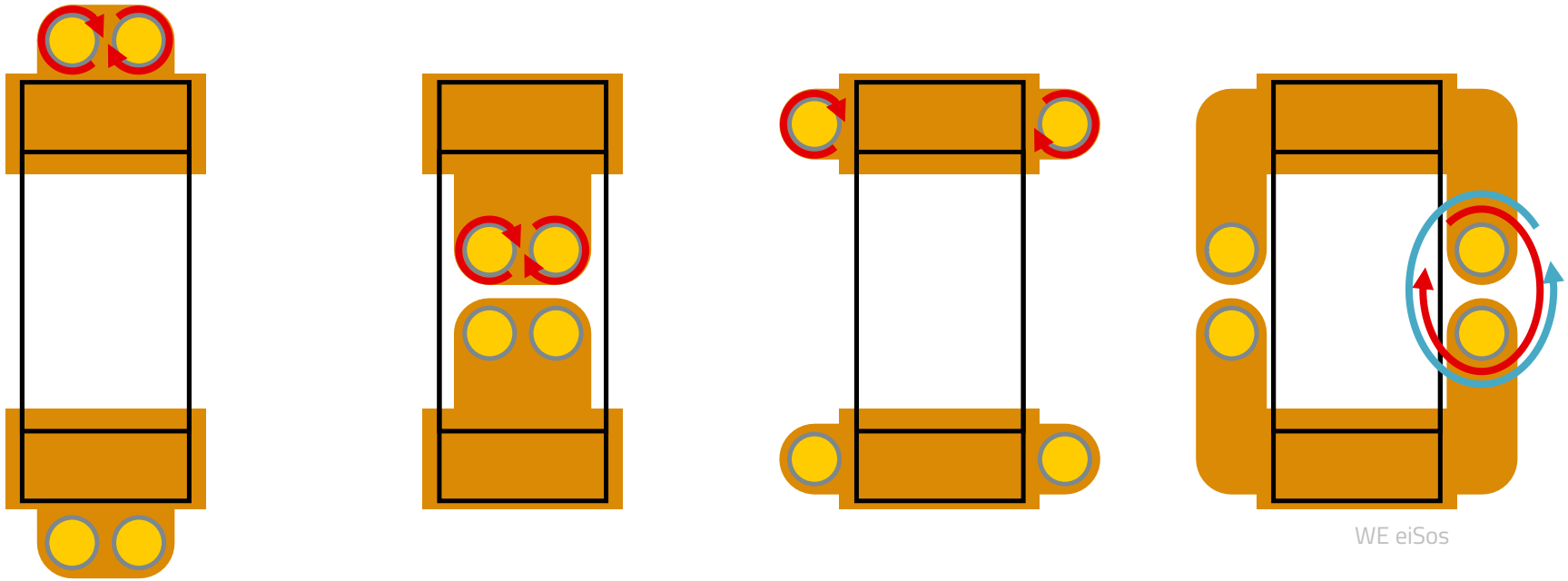


0603, without Ferrite



Parallel Vias

Arrangement of Vias



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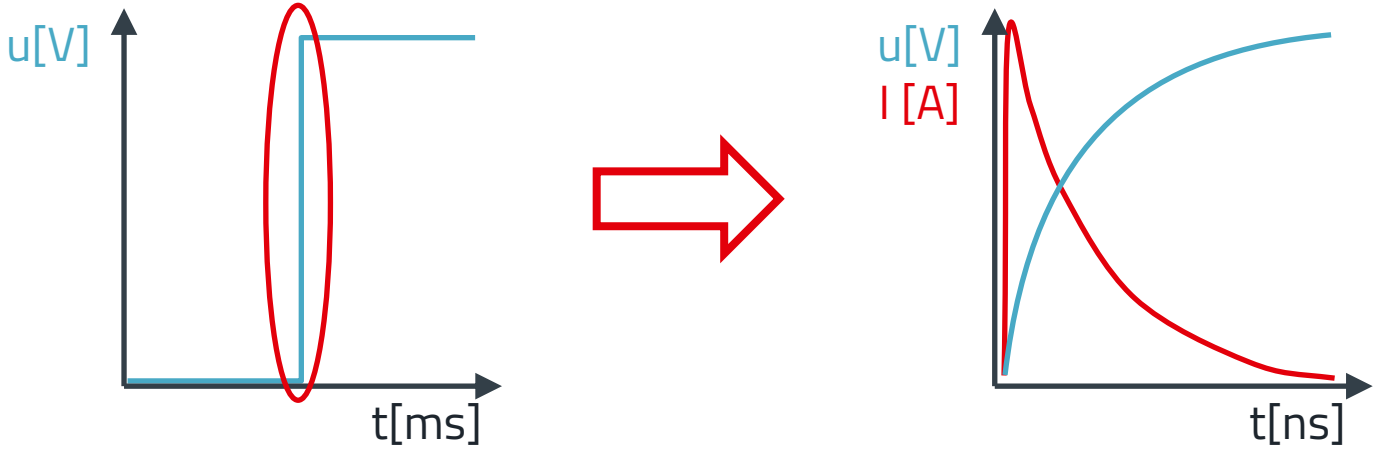
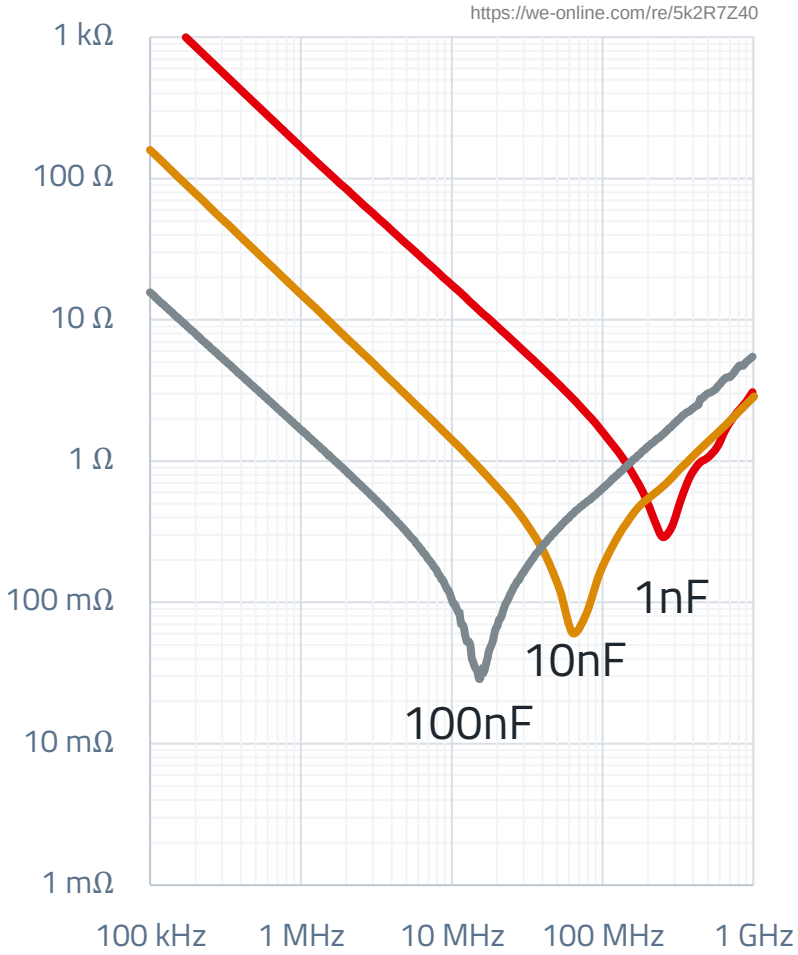
What is the best way to arrange Vias (theoretically) ?

Filter Capacitors

Selection Criteria

- For blocking capacitors, you have to consider the rise time of the signal
  - The steeper the edge, the higher the frequency that has to be blocked
- Transient loads lead to a high dI/dt
  - Not the voltage but the current is critical

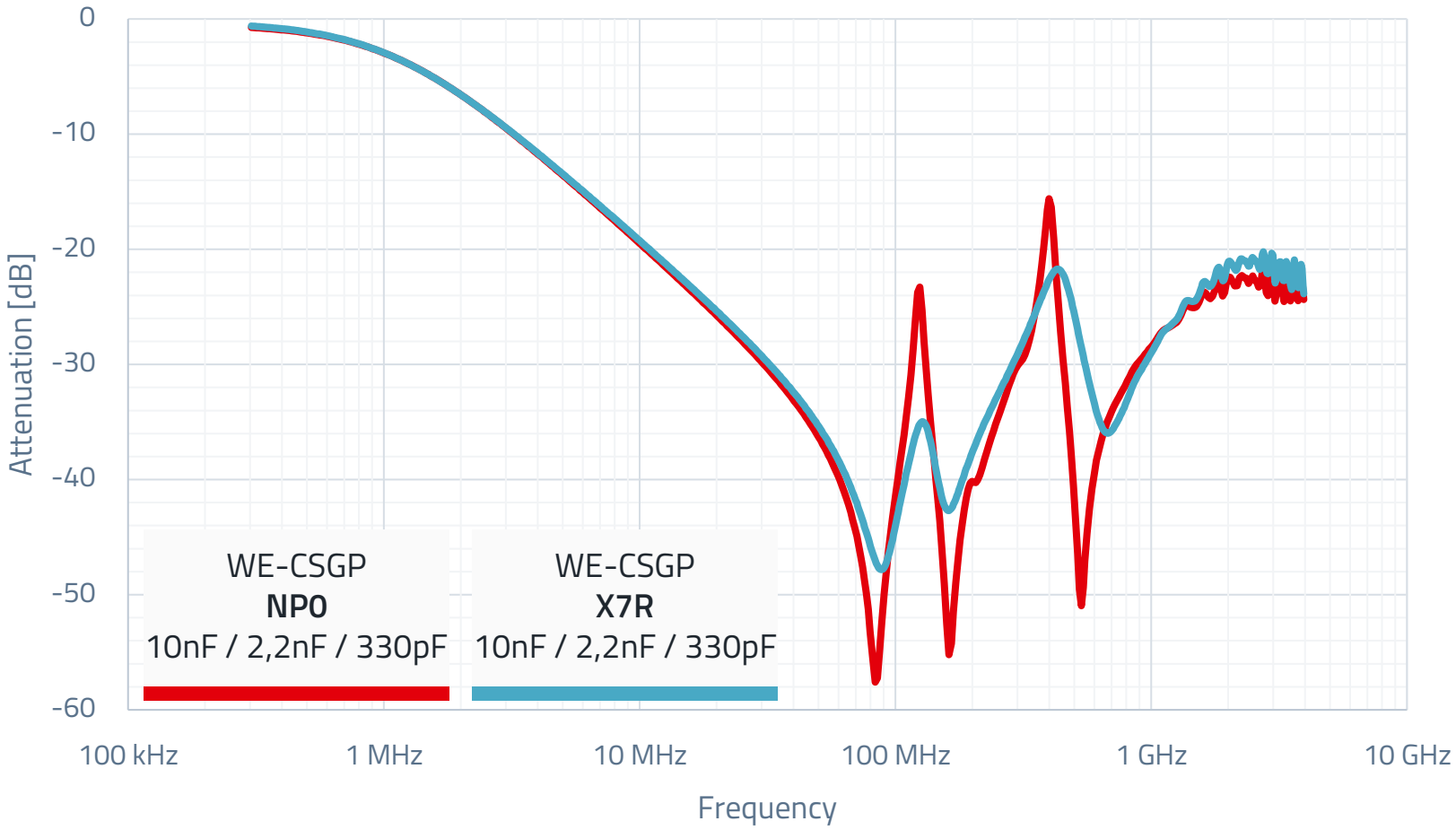




Filter Capacitors

Selection Criteria

- Ceramic Class of the blocking capacitor affects performance
- NP0 with high Q tends to resonate strongly
- X7R provides a smoother curve but has its downsides:
  - DC Bias
  - Temperature Stability
  - Aging



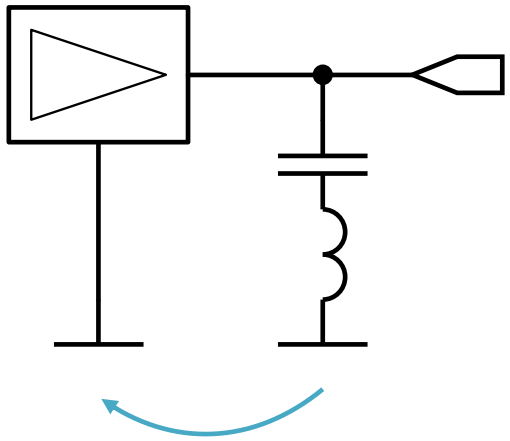
Filter Capacitors

General Considerations

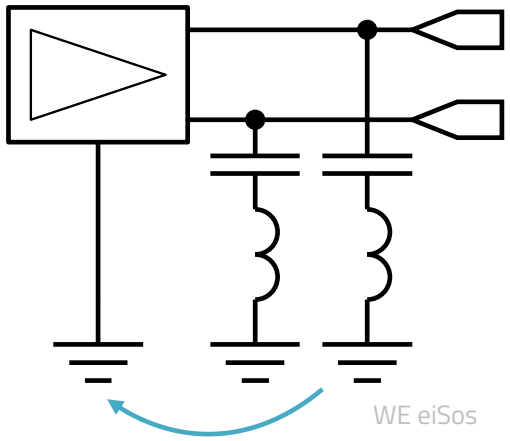
- For all capacitive Filters a low impedance connection to reference potential is key
  - For DM: (A/P) Ground
  - For CM: Earth / Chassis

- Additional Impedances decrease efficiency of RF short
  - THT contact pins
  - Inductance of PCB traces
  - Placement connection of steel spacers

Differential Mode Short



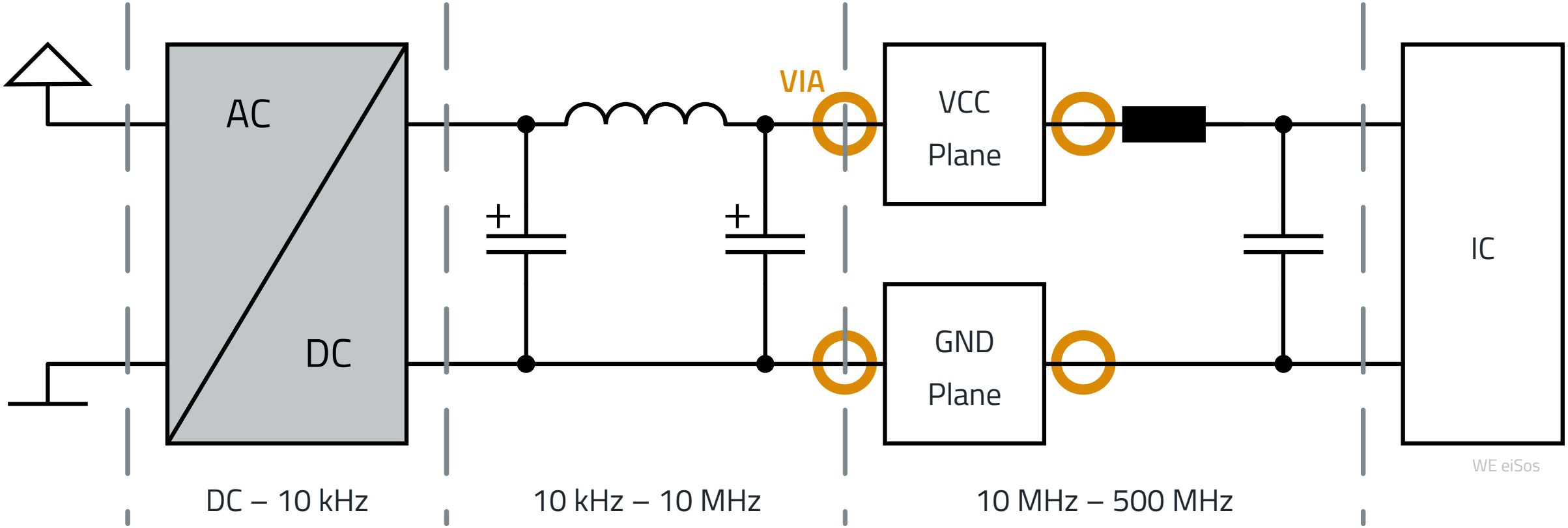
Common Mode Short



FILTER PLACEMENT

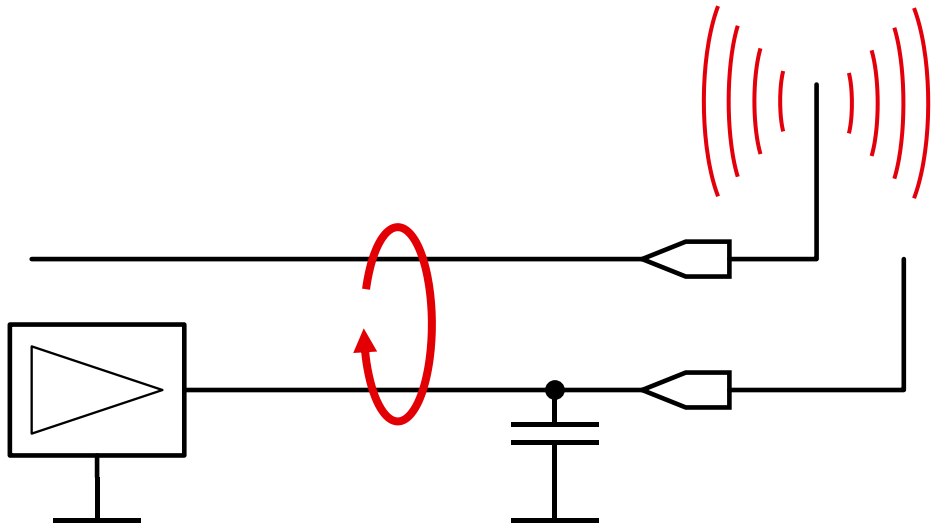
Filter Placement

Filter Bandwidth Requirements along the Power Path

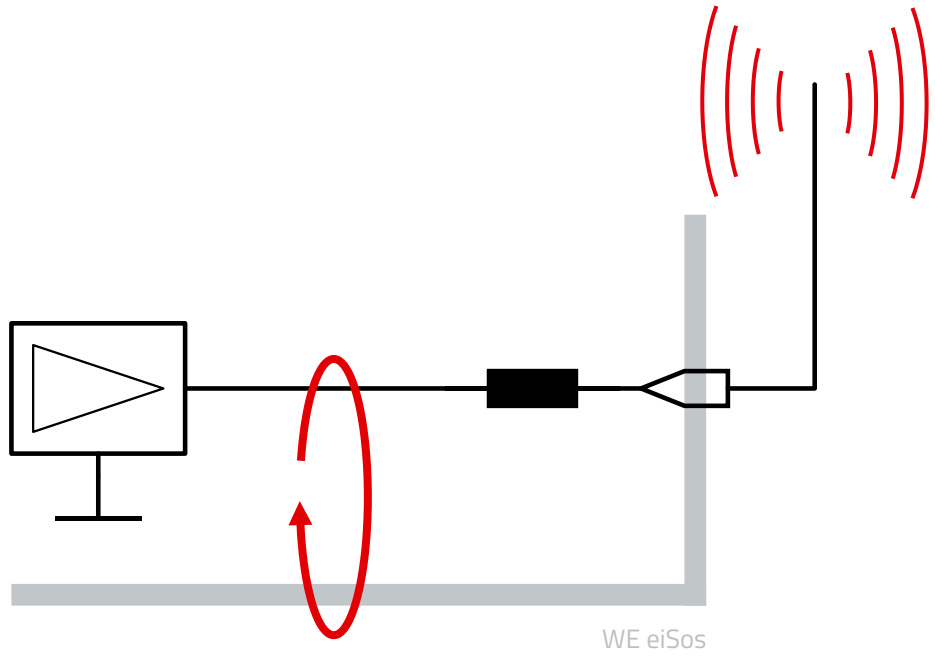


Filter Placement

Noise can bypass a misplaced Filter



Bypassing via parallel Lines

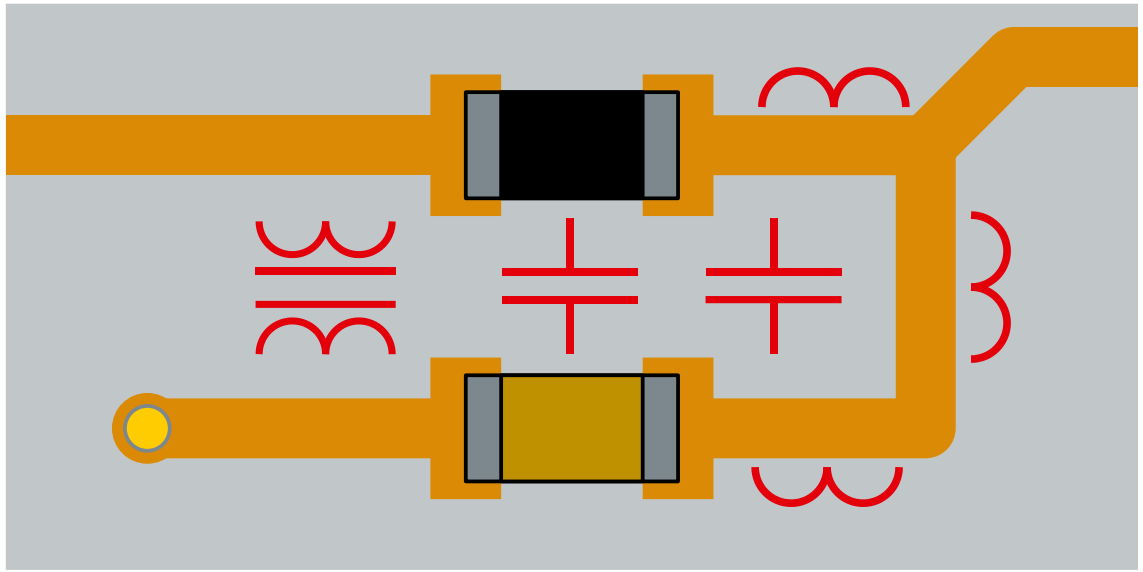


Bypassing via chassis parts

Filter Placement

Noise Coupling in Single-Ended Filters

- Inductive coupling between filter input and GND via
- Capacitive coupling – increases with frequency
- Conductor inductance – traces too long
  - 1nH per 1mm
  - 0.5nH per Via



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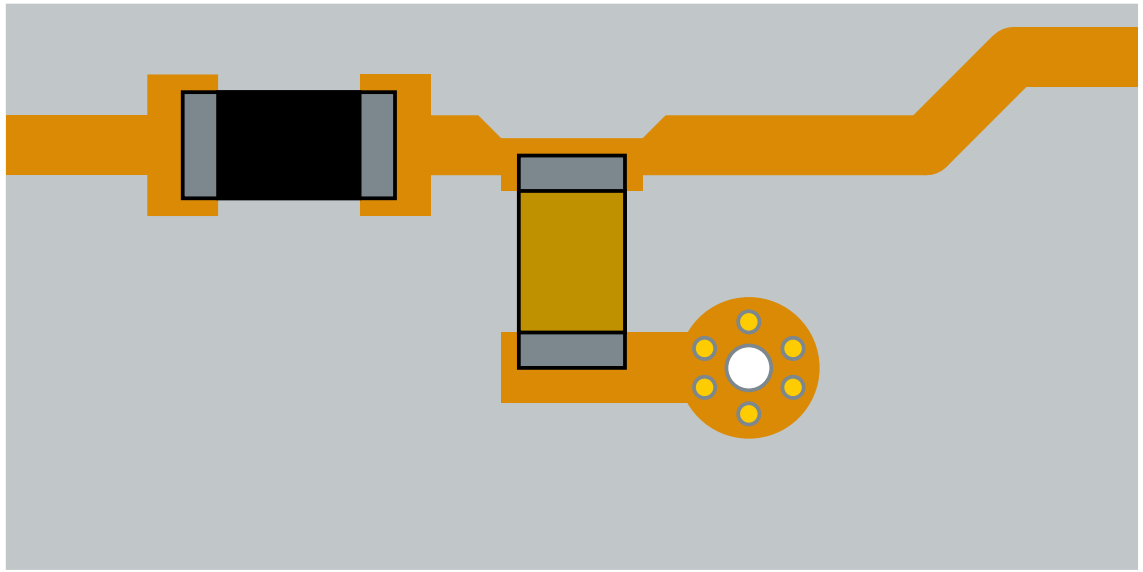
Filter Placement

Noise Coupling in Single-Ended Filters

- Constriction of the trace at the capacitor's connection reduces reflections in the GHz range (VSWR)
- Orthogonal arrangement of L and C to minimize capacitive coupling
- Vias to GND can be tied to PE using e.g. a steel spacer



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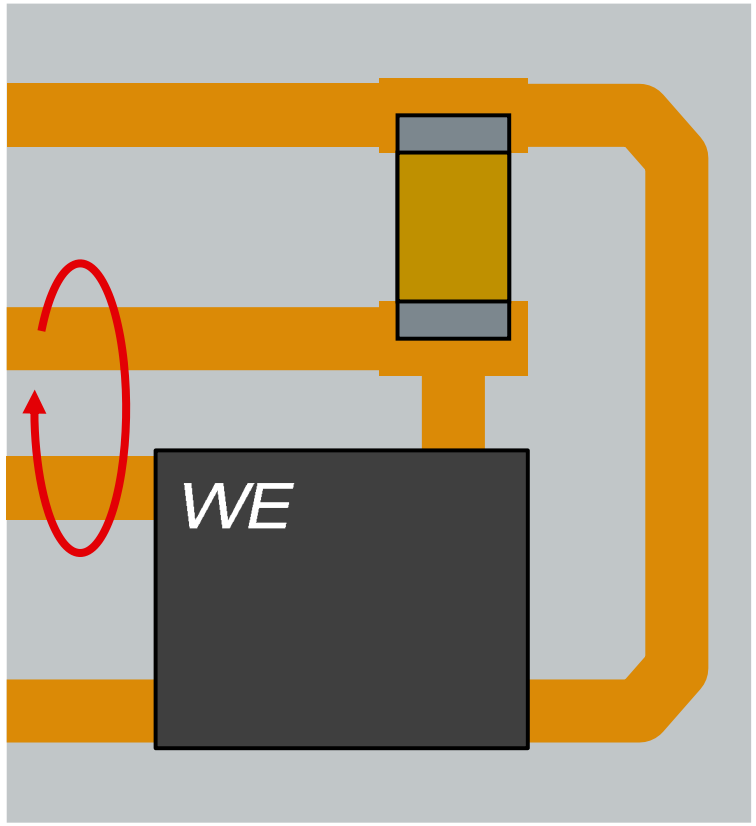
Filter Placement

Coupling Paths in Common Mode Filters

- CM-Filter as close to the connector as possible
  - Overvoltage is also running in CM!
- Avoid GND Plane beneath Choke
  - Possible coupling path / mode conversion
- Keep an eye on noise feedback from filter output to input



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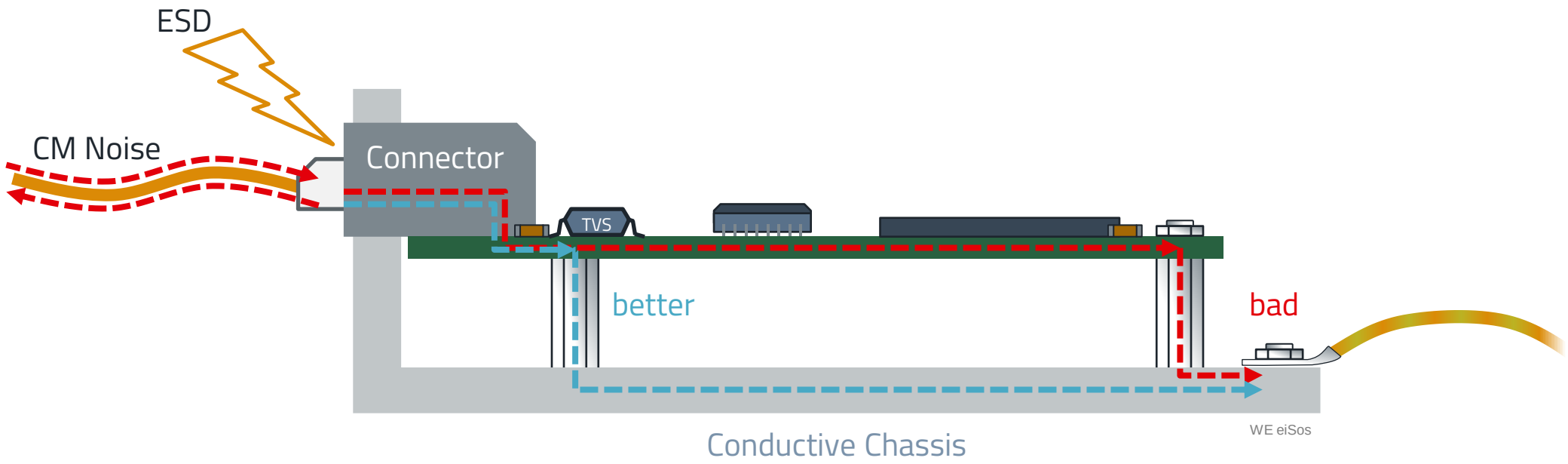
Inductive Coupling from CMC Output to Input

Filter Placement

Diverting Noise to Earth



- Grounding studs have to placed so that disturbances don’t affect the electronic parts
- Reference ground for ESD (and common mode noise) is earth potential

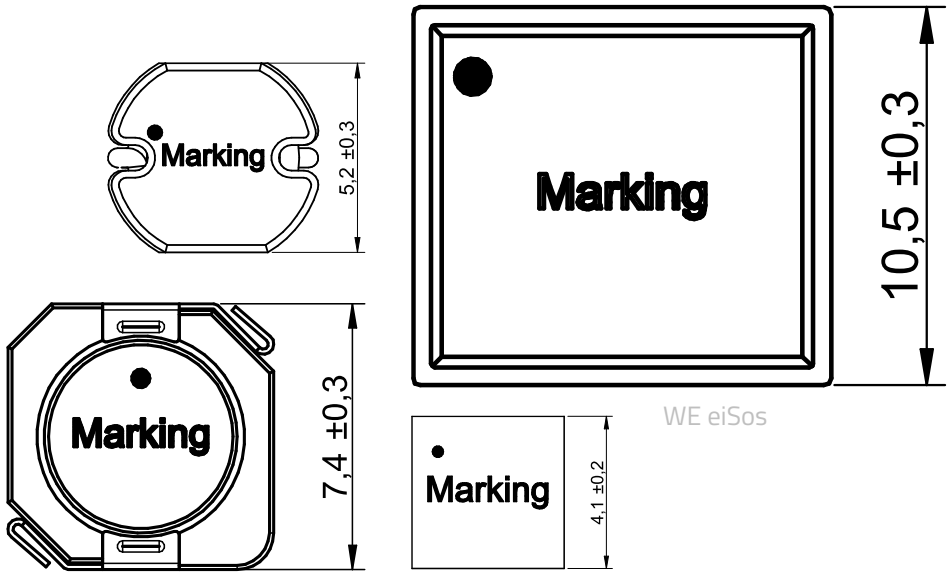
POWER INDUCTORS

Layout Considerations

Orientation of a Power Inductor

Keeping the Hot Node as small as possible

- Power Inductors with more than one layer of windings usually have marking indicating the start of winding
- Start of winding should be facing the Hot Node, so outer winding can act as a self shielding
- Even for Inductors with only one layer, orientation can make a difference (Height of terminal)
- Not every Inductor has a distinct start of winding due to the production process (e.g. Rod Cores)



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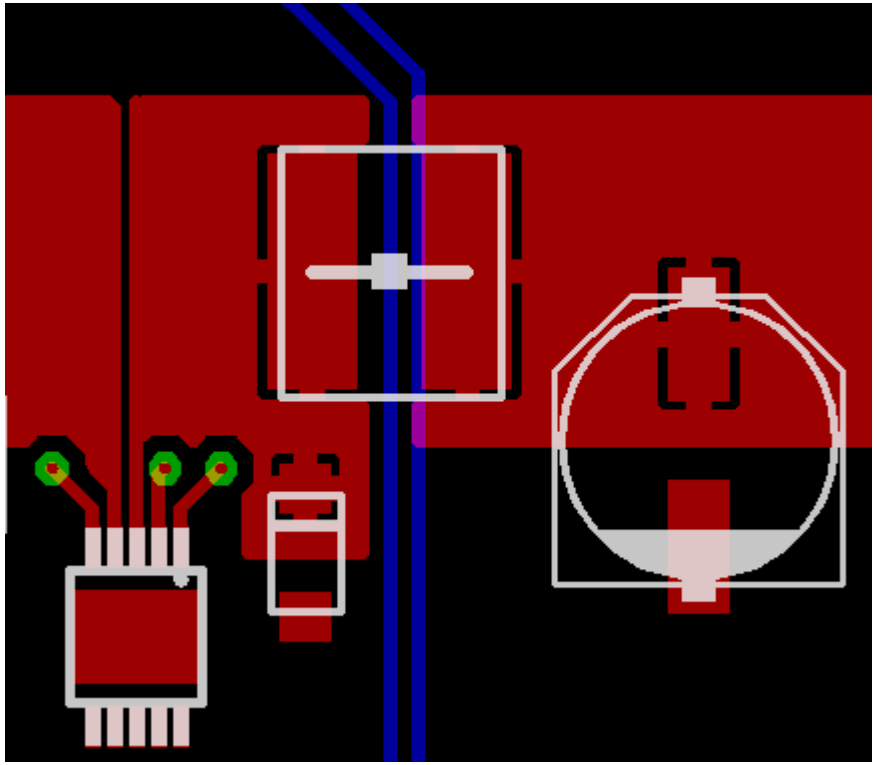
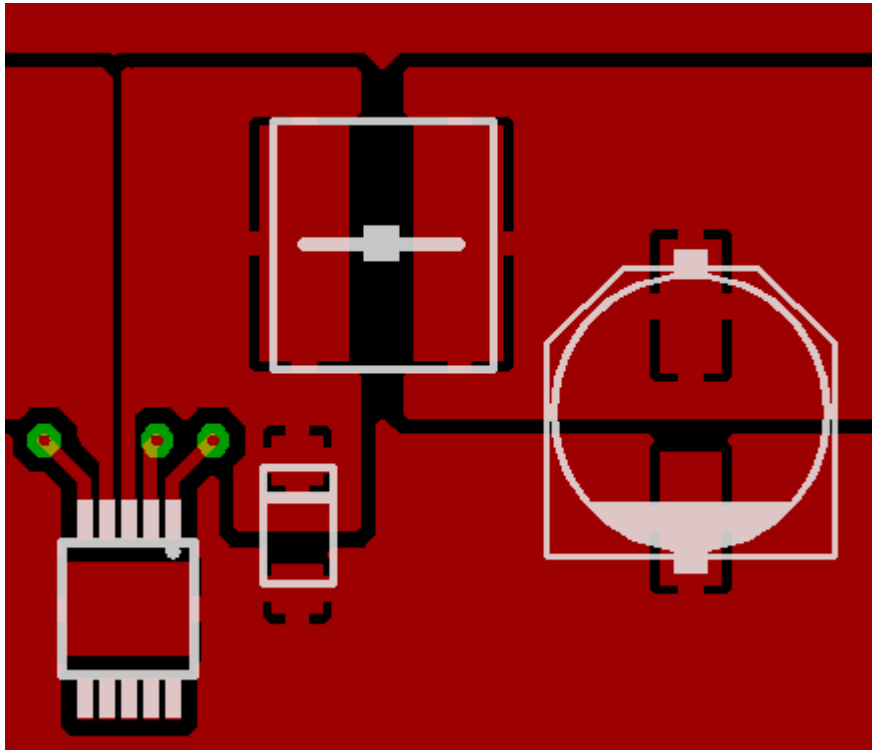
Traces below Power Inductors

Bottom side of Power Inductors is not shielded



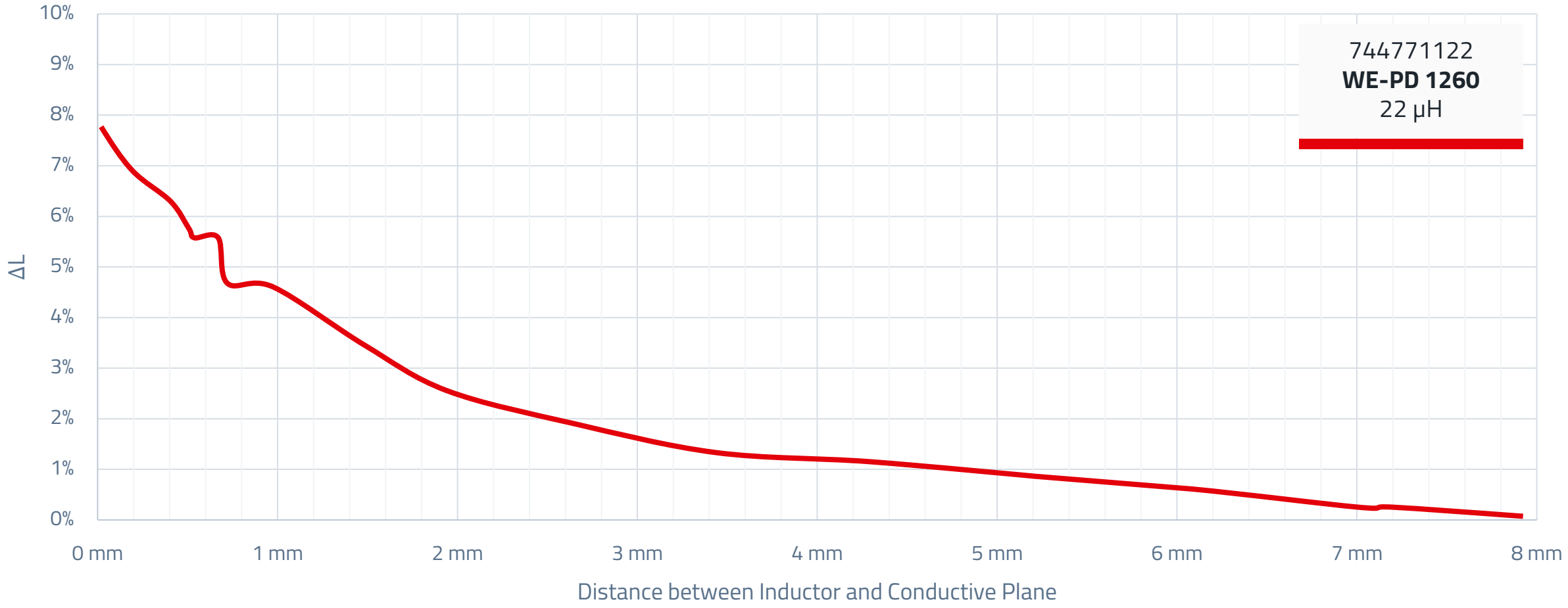
bad



good

Conductive Plane below Power Inductor

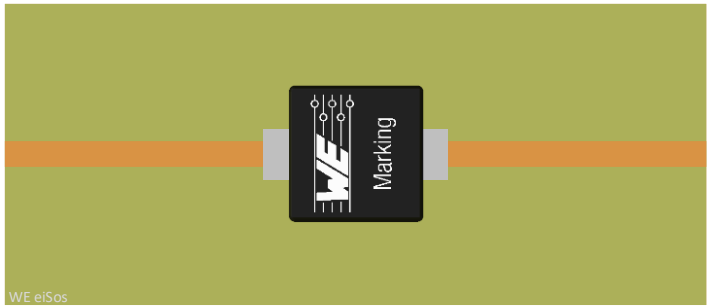
Influence on Inductance



Conductive Plane below Power Inductor

Layout Options

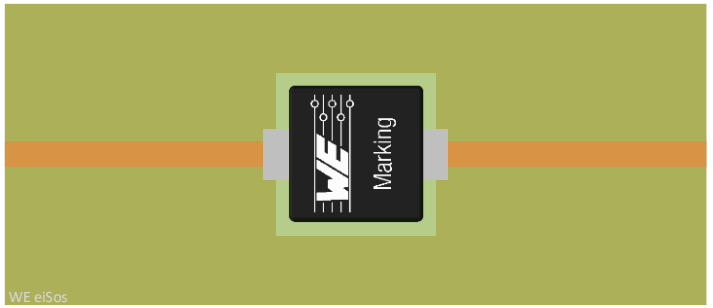
Continuous GND Plane



+ Shielding the electric Near Field

- Eddy Currents affect Inductance

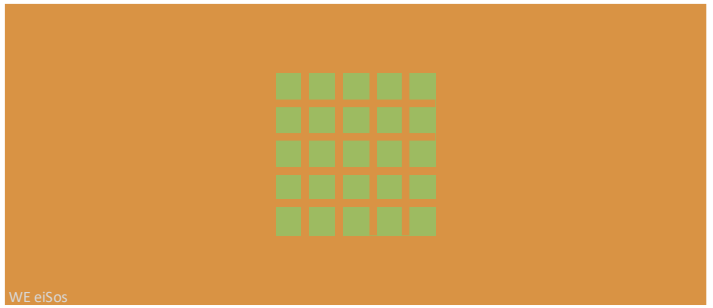
Opening in GND Plane



+ Reduced Eddy Currents

- Radiated Noise through PCB

Tradeoff - GND Grid



+ Reduced Eddy Currents

+ Reduced radiated Noise

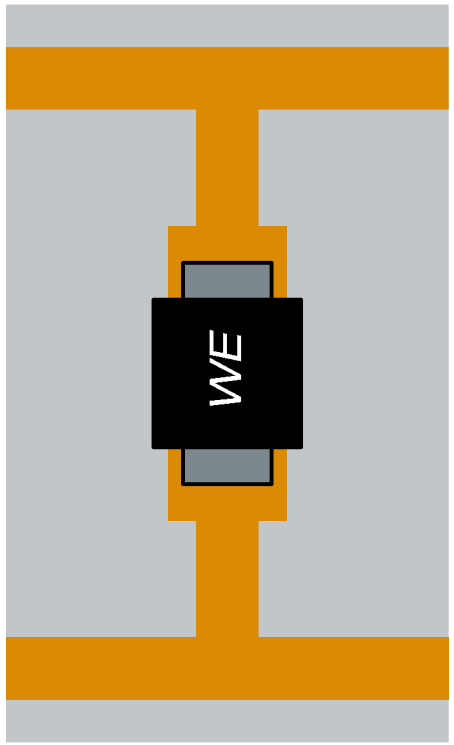
- Increased Layout Efforts

OVERVOLTAGE PROTECTION

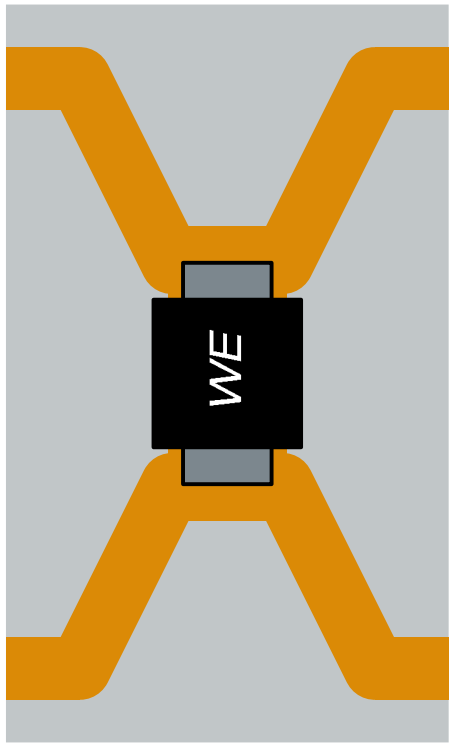
Layout Considerations

Routing OVP-Components

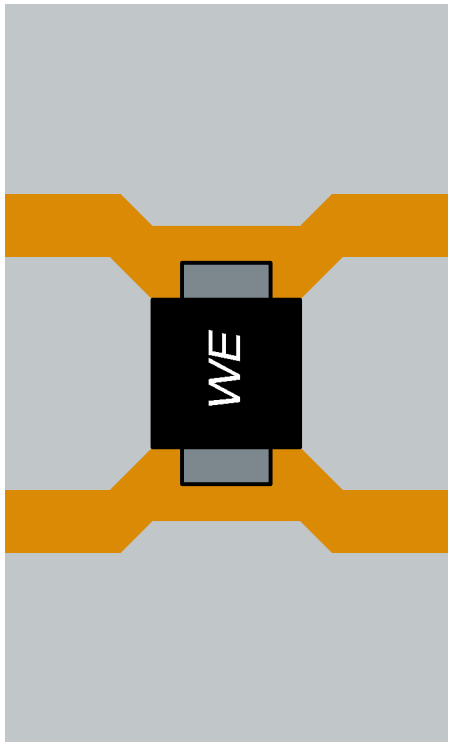
Keep Traces short and low impedance



Bad
Stub Traces



Good
Routing across SMD Pads



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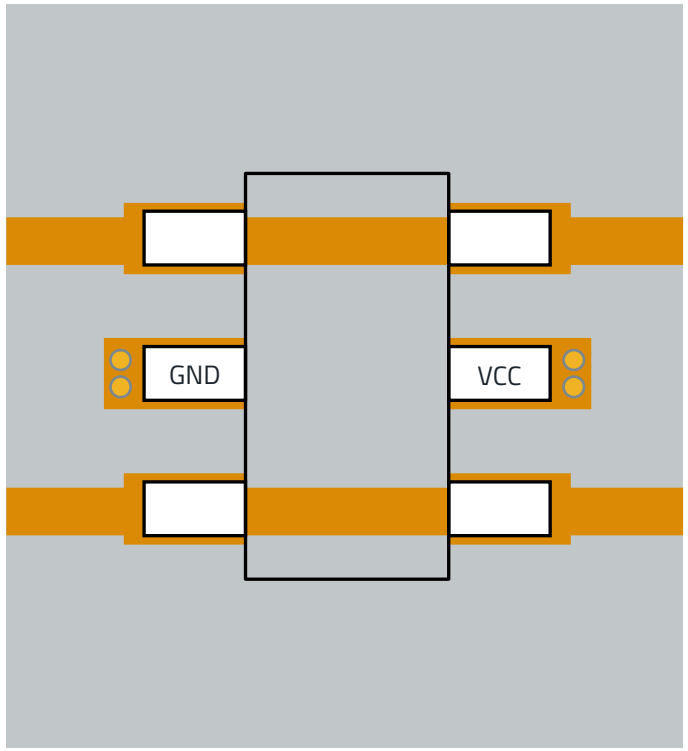
Best
Using Constictions at SMD Pads

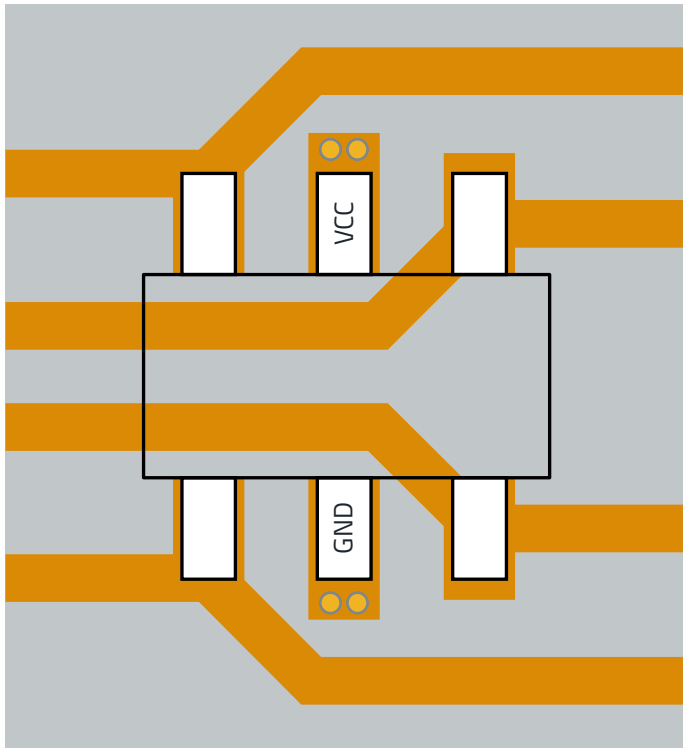
Routing OVP-Components

Keep Traces short and low impedance

- For TVS Diodes, multiple strips have to be coordinated across the component
- Parallel Vias to GND/ VCC plane for low impedant connection
- “Flow Through” design simplifies routing
- Impedance controlled traces and symmetrical routing for data lines



Routing for 2 Lines



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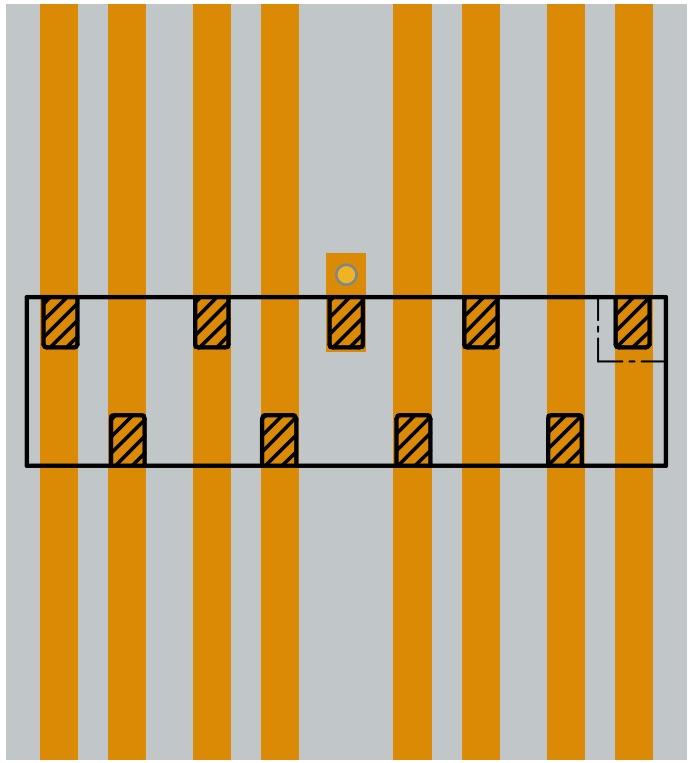
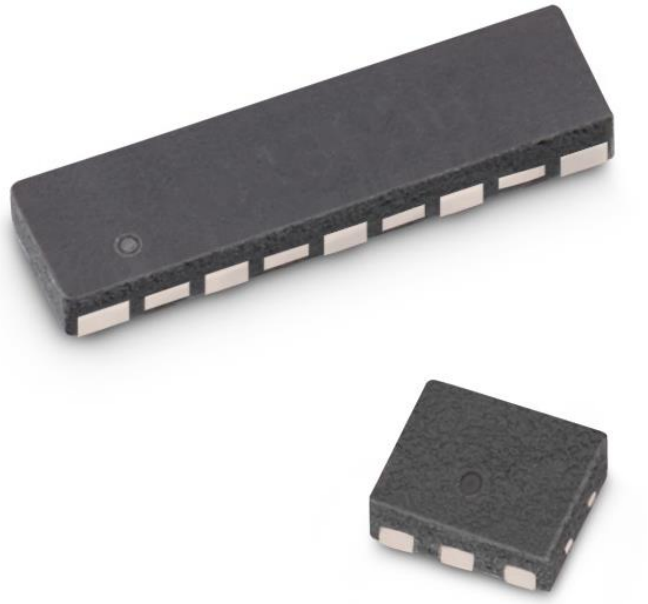
Routing for 4 Lines

Routing OVP-Components

Special Design for High Speed Interfaces

- Higher requirements on impedance controlled traces and symmetrical routing
- “Flow Through” design simplifies routing

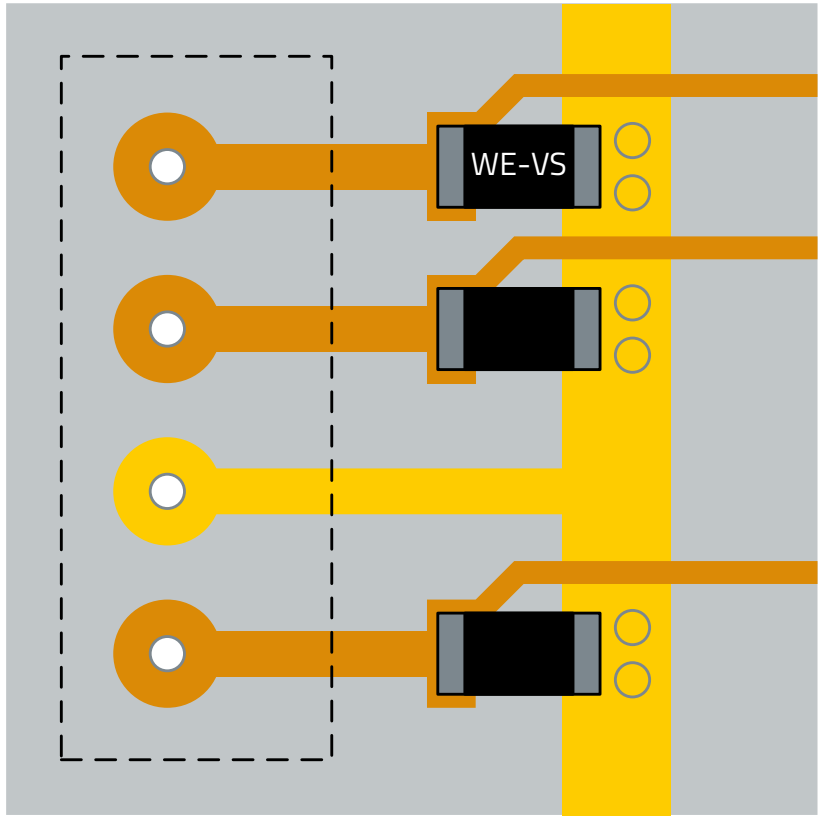




Connecting SMD Varistors

Separating Overvoltage Stressed Ports

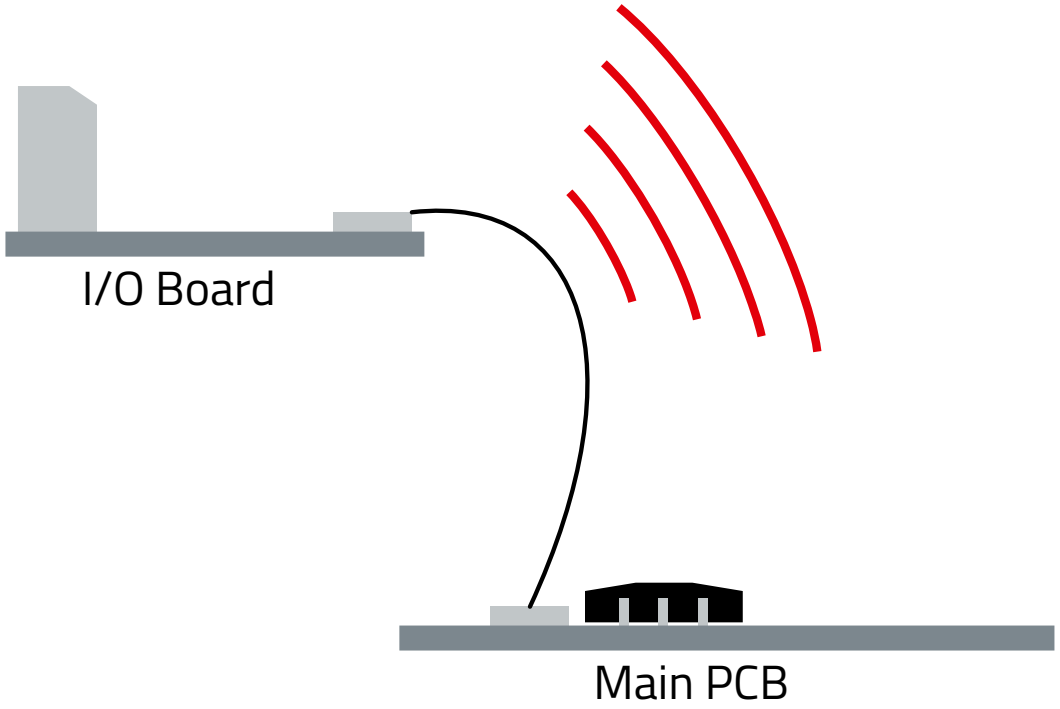
Wide traces to Varistor terminals



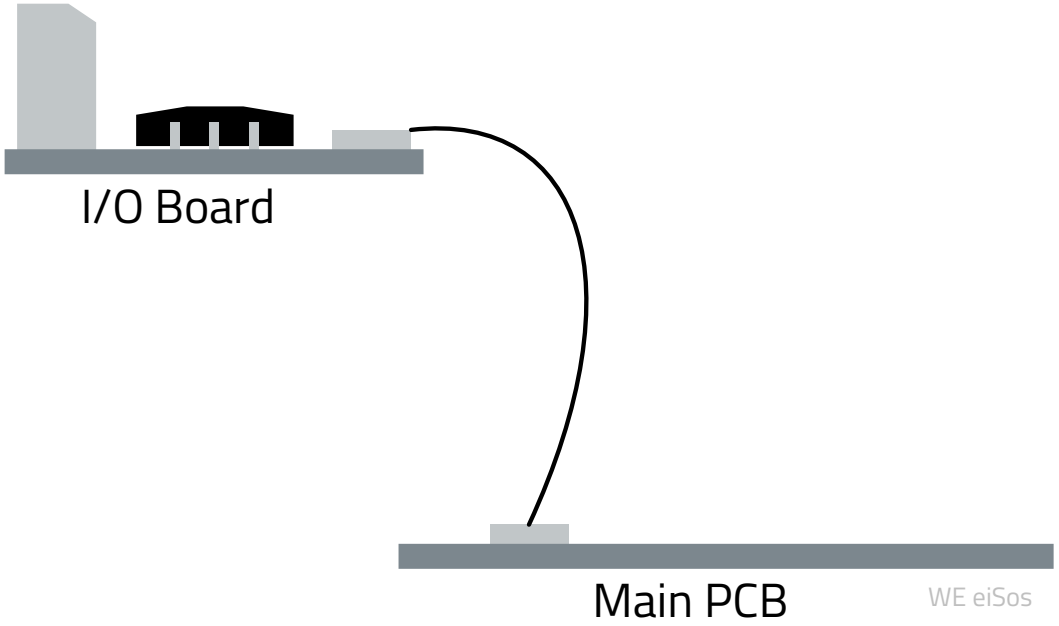
Regular traces for useful Signal

I/O Boards

Where to Place Overvoltage Protection



Placement on Main PCB



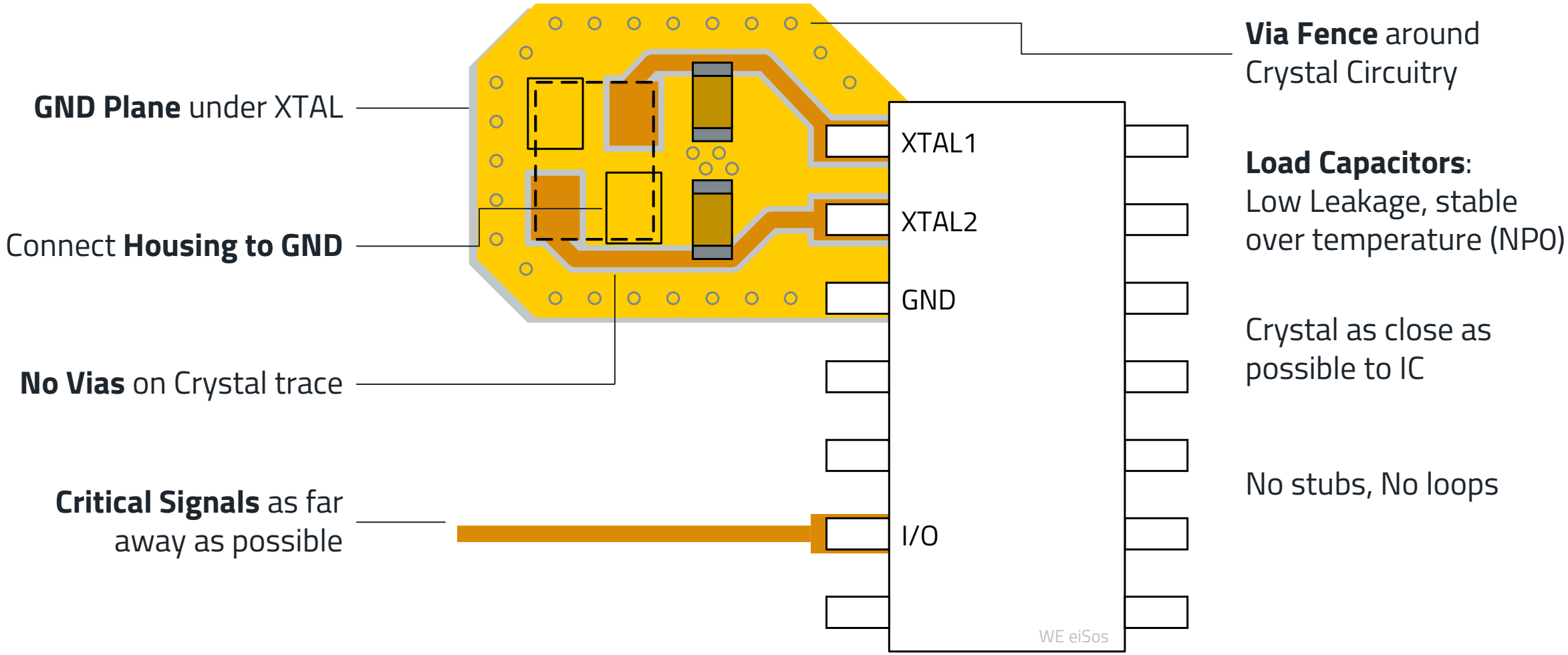
Placement on I/O Board

CRYSTALS & OSCILLATORS

Layout Considerations

Quartz Crystals

Layout Considerations



Crystal Oscillators

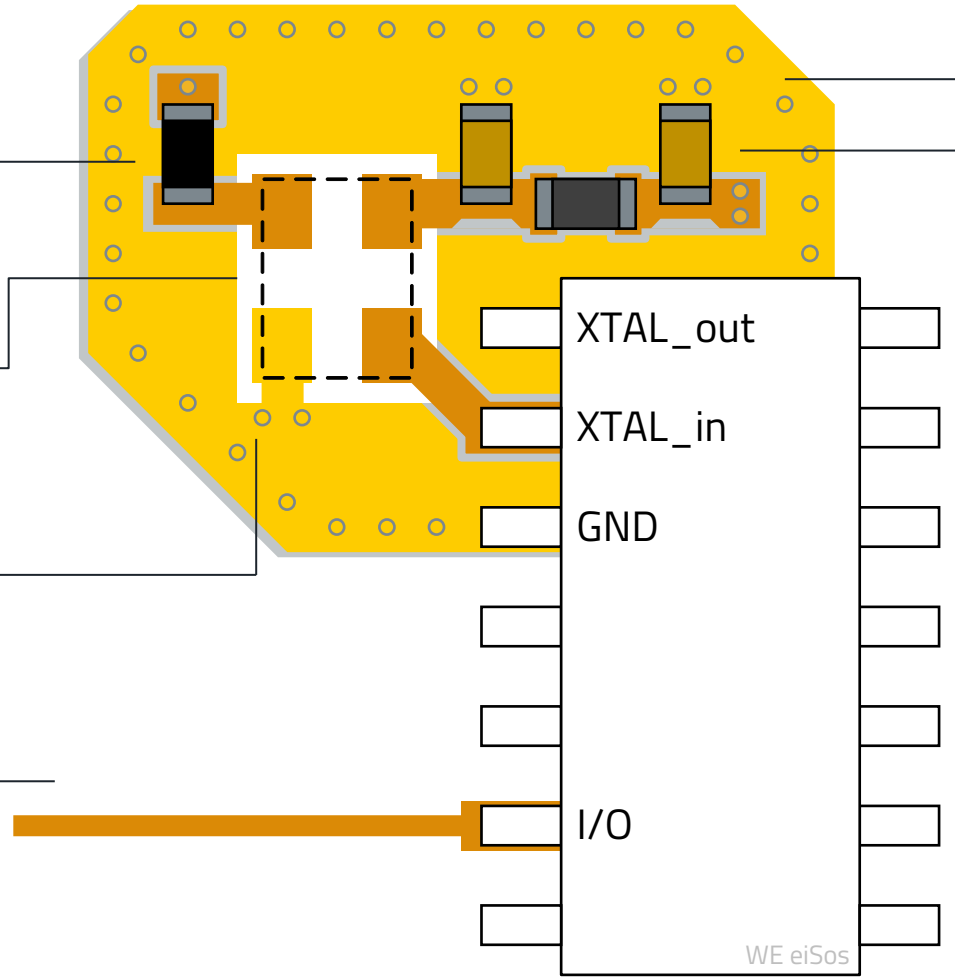
Layout Considerations

100kΩ Pull-Up
if EN is not required

Cut Out GND Plane
under Oscillator

Via to shorten GND Path

Critical Signals as far away as possible



Via Fence around Crystal Circuitry

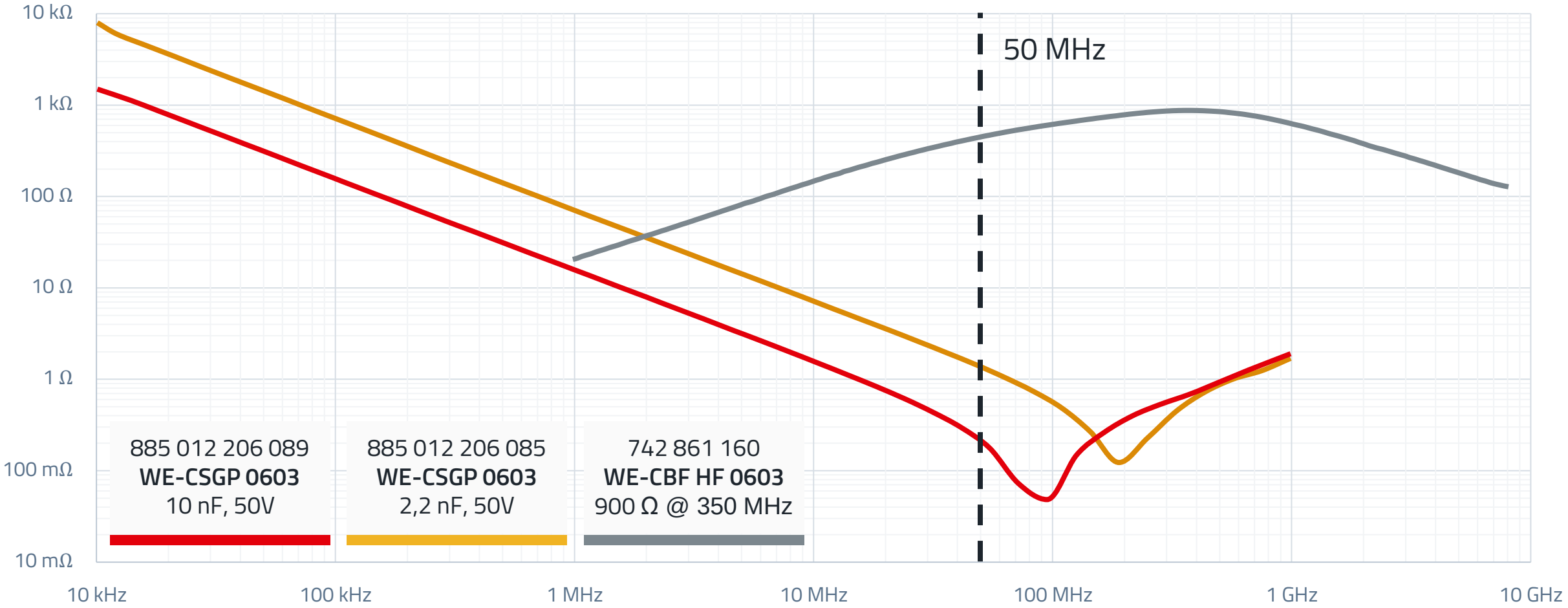
T-Filter for **RF Decoupling** of Supply Voltage

Keep **RF Lines** as short as possible

No Layer Jumps on RF Lines

T-Filter for RF Decoupling

For Crystal Oscillators @ 50MHz

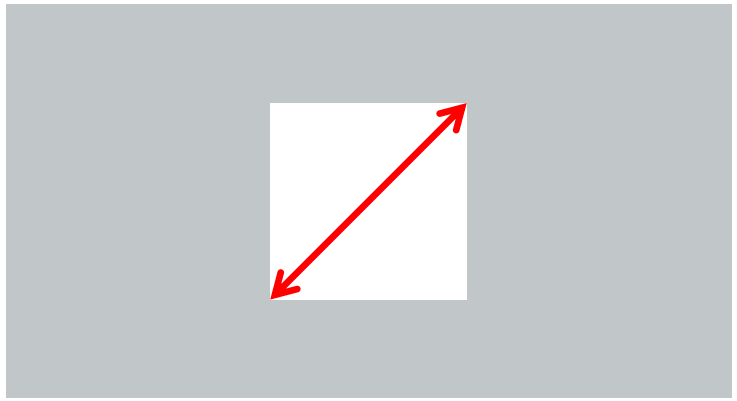


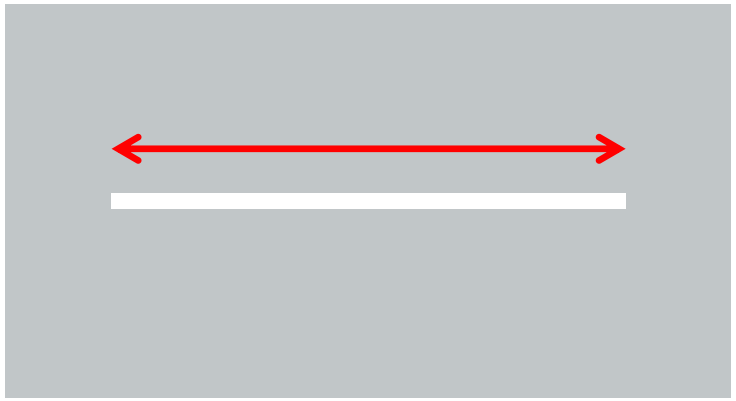
SHIELDING FOR CASINGS

Openings in PCB Housing

Apertures are Antennas, too

- No shielding is perfect, there will always be holes/ breaks
- Magnetic shielding is more affected than electric shielding
- The higher the frequency, the bigger is the impact of apertures compared to material properties
- The maximim linear dimension is crucial, not the area





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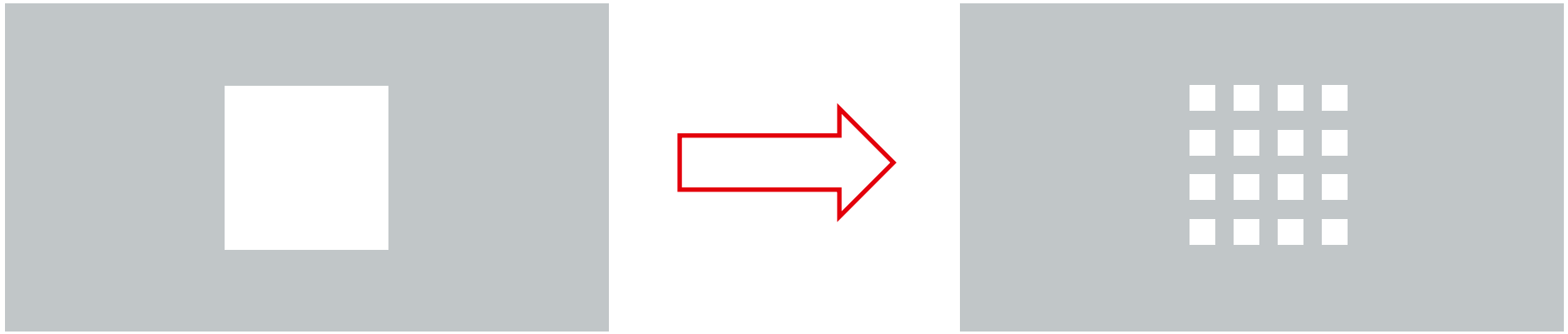
Openings in PCB Housing

Apertures are Antennas, too

- An aperture of $\ell = {}^{\lambda}/_{2}$ equals a half-wave dipole antenna
- If the vector of the electric field is perpendicular to the aperture, the shielding attenuation at the respective frequency is 0 dB
- If a bigger opening is needed, e.g. for ventilation, the area should be split up into many smaller ones



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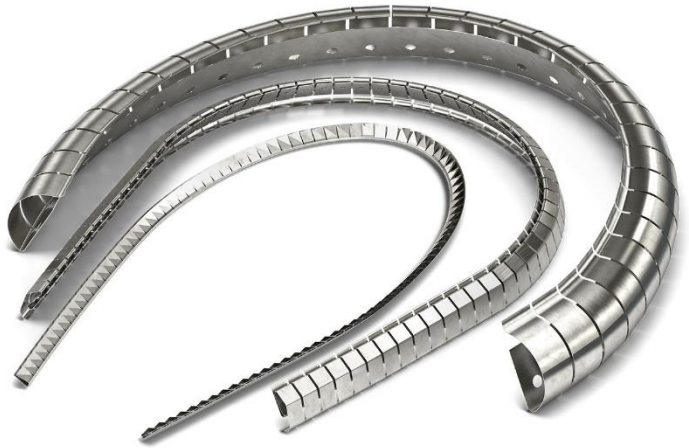
EMC Gaskets

Different Options



WE-CSGS
Contact Spring Gasket

WE-EGS
Conductive Elastomer Gasket

WE-LT
Conductive Mesh Gasket

Grounding

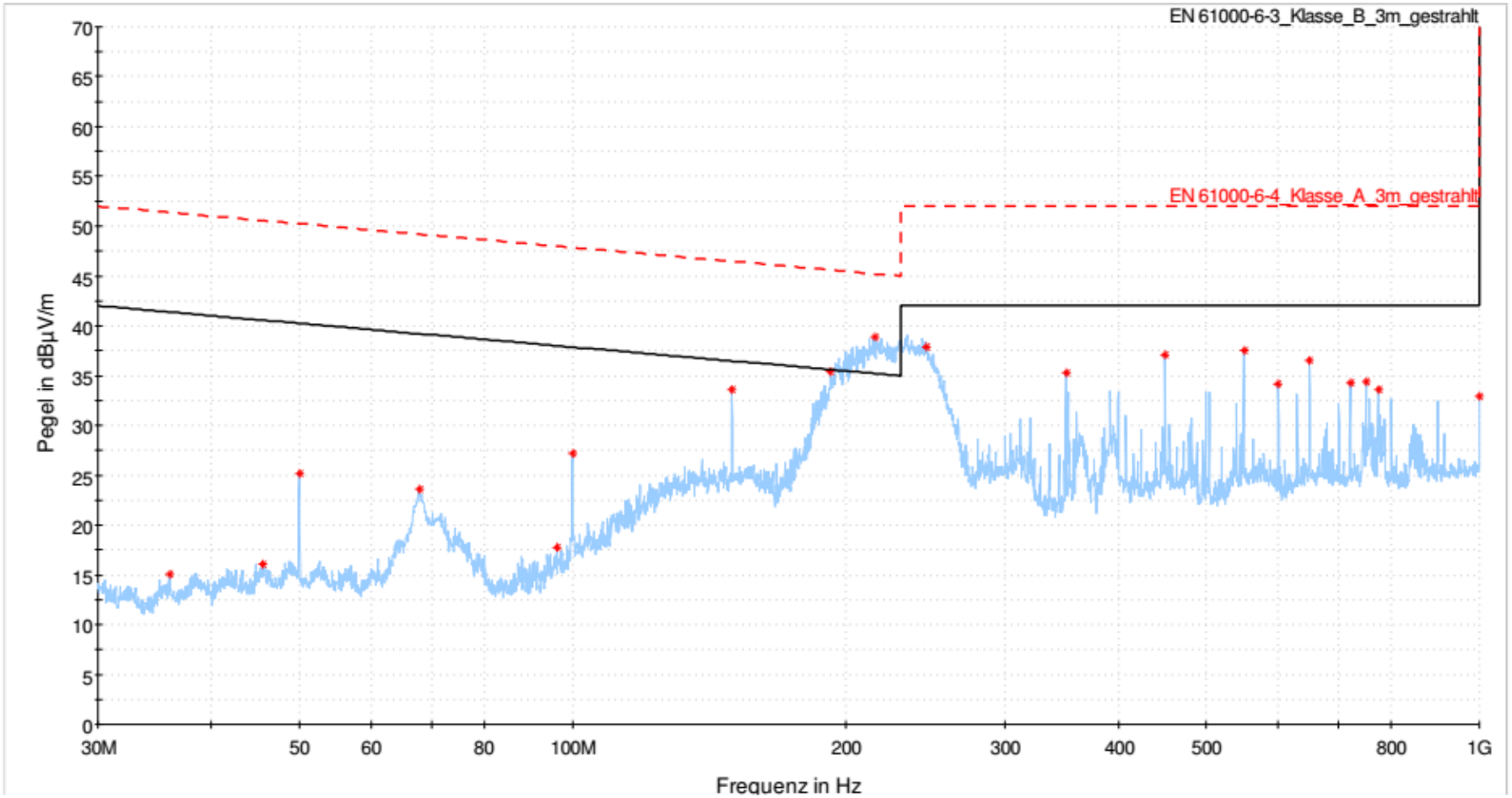
Connecting PCB to Casing

- For RF Currents (> 20 KHz)
  - Skin Effect forces Current to the surface of the conductor, increasing Impedance
  - Increasing influece of parasitic Inductance

- Connections have to
  - be as short as possible
  - have a maximum surface area
  - Low impedant for RF Frequencies

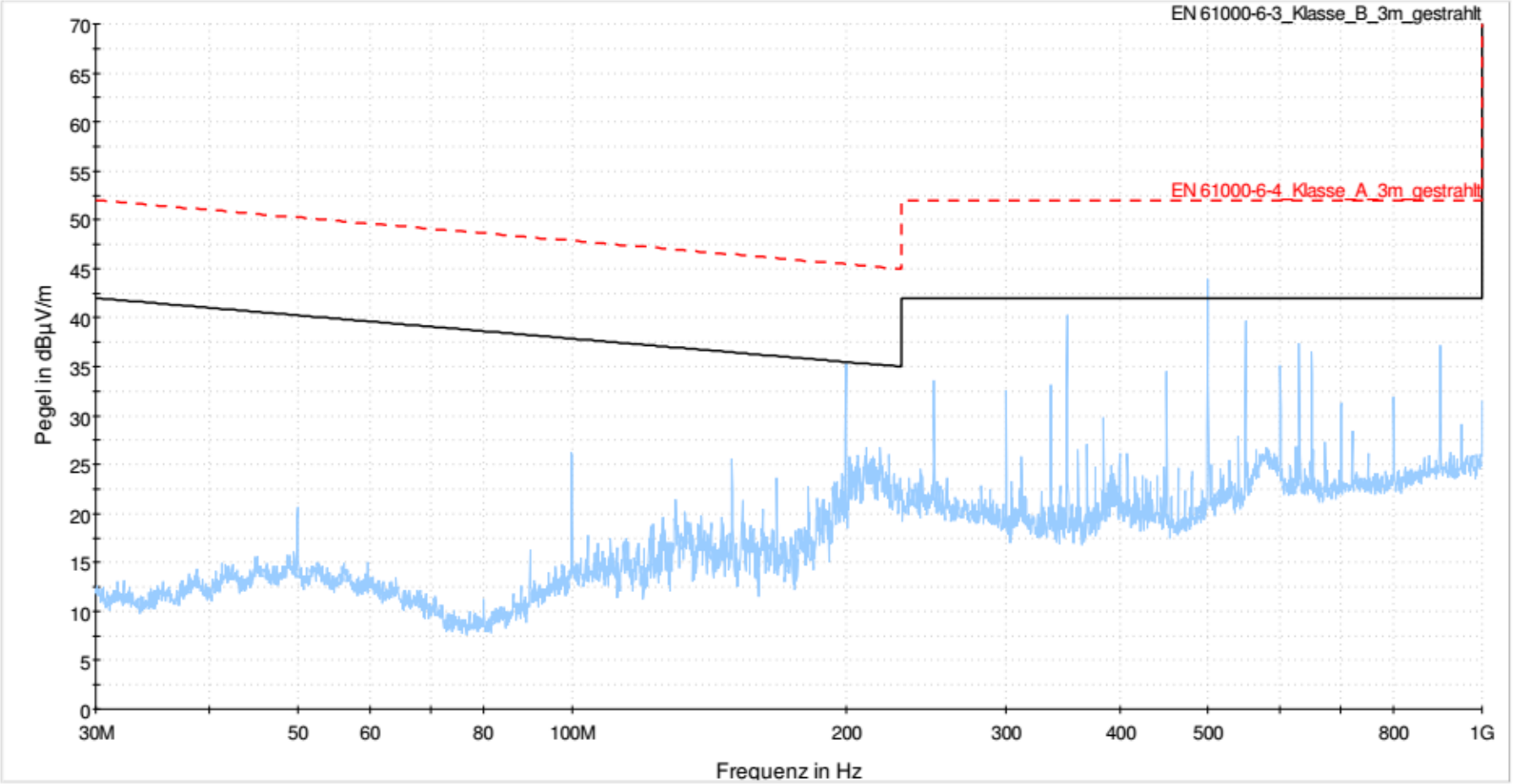
Example: Heatsink

Floating Potential, Dipole Antenna



Example: Heatsink

Bound directly to Power GND, Reduced Emission



Shielding on PCB Level

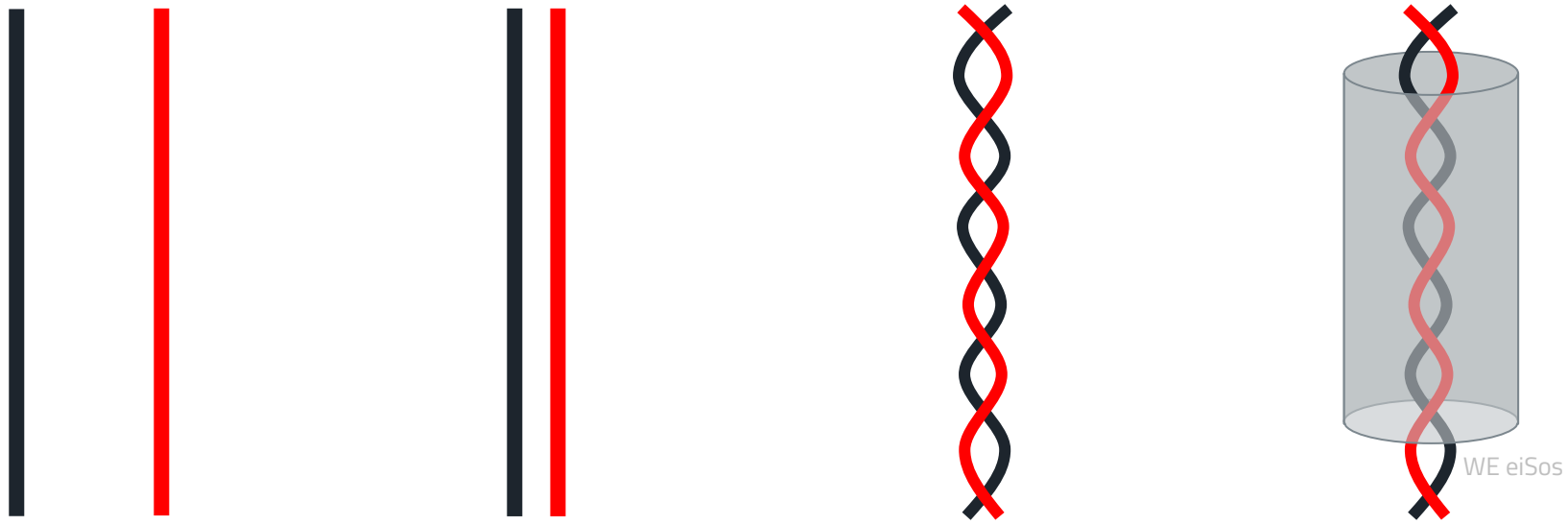
Shielding Cabinet WE-SHC

- Easy to pre-arrange with SMD-Pads
  - virtually no cost
- Place on PCB in case of susceptibility problems/ Radiating noise
- Go for standard sizes to reduce costs
- **Custom Solutions Possible**
  - ShielDIY for simple trials
  - *WE* can do special parts according to you drawings

SHIELDING FOR CABLES

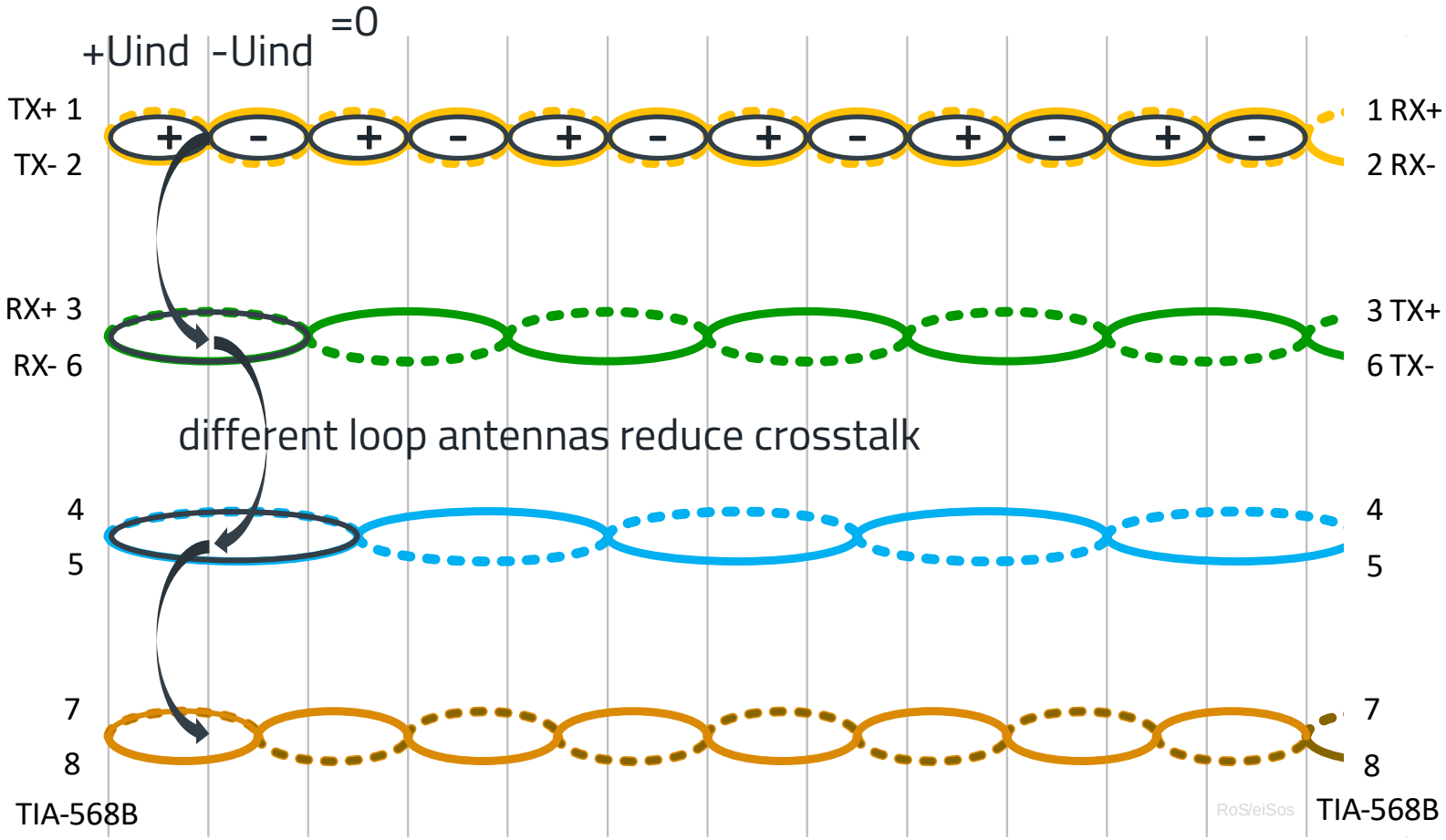
Cables are Antennas

Aim for small Loops and tight coupling



Cables are Antennas

Twisted pair for reduced Crosstalk

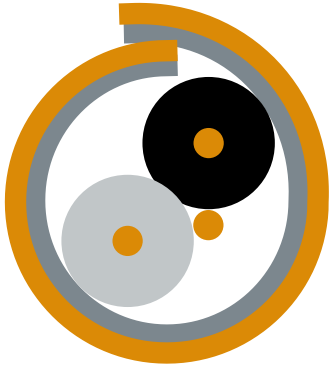


- e. g.: 1GBit S/FTP
  - 1st pair: 5,5 twists/10cm
  - 2nd pair: 6,5 twists/10cm
  - 3th pair: 7,5 twists/10cm
  - 4th pair: 8,5 twists/10cm
- The higher the count of twists the higher the quality of the cable, but with negative effects to cable bending and higher costs

Cable Shielding

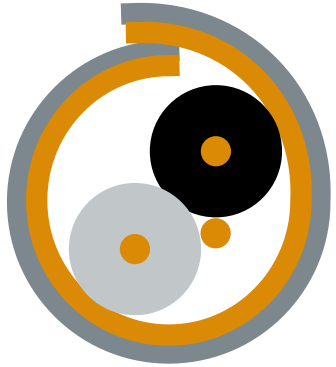
Faulty Overlap can lead to Radiation

- Depending on the Foil/Mesh, an opening can act as a Slot Antenna
- Check Overlap for non-conductive contact areas



Outside Metallized

No Conductive Overlap

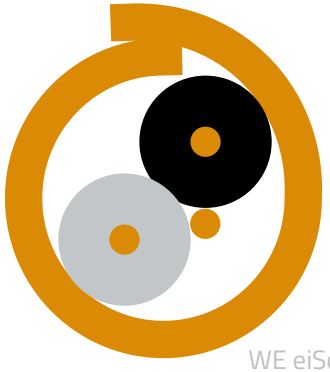


Inside Metallized

No Conductive Overlap

Inside Metallized, Wrapped

Fully Enclosed



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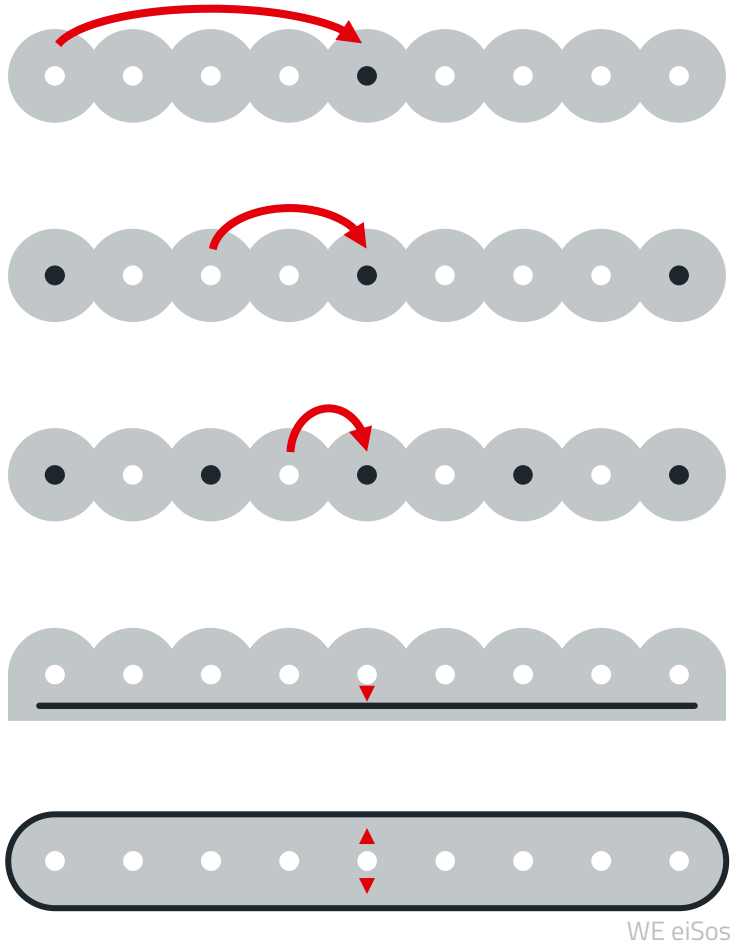
Aluminum Foil

Fully Enclosed

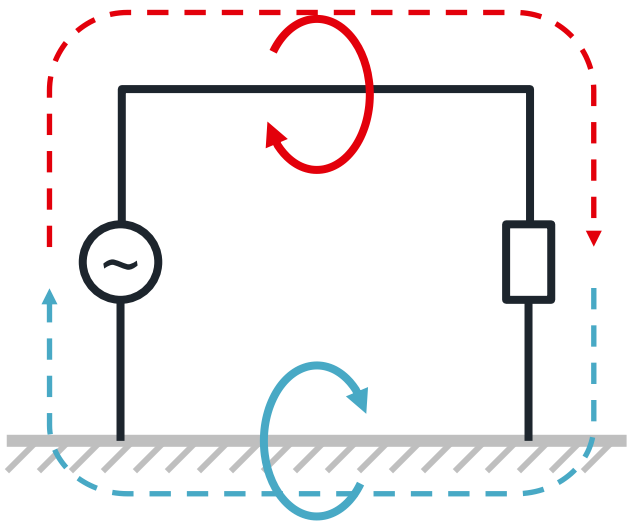
Signal Distribution on Flatwires

Keep an eye on GND Reference

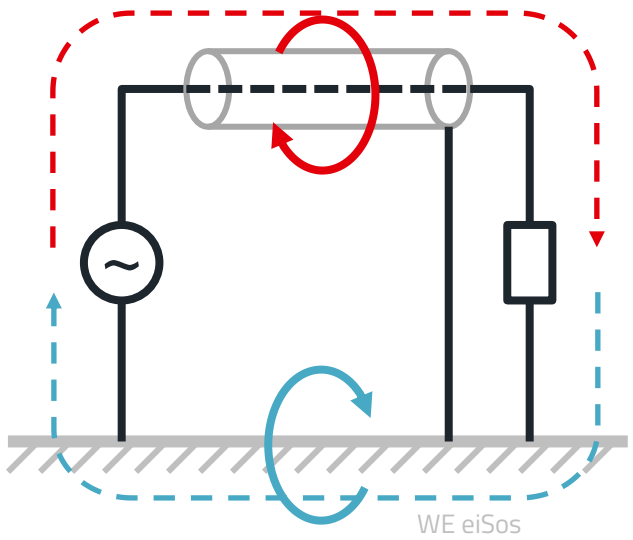
- For Flatwires you can alternate Signal and GND Lines
- Flex PCBs can have **GND Layers**
- Self-Adhesive Copper Foil connected to GND as **retrofit solution**



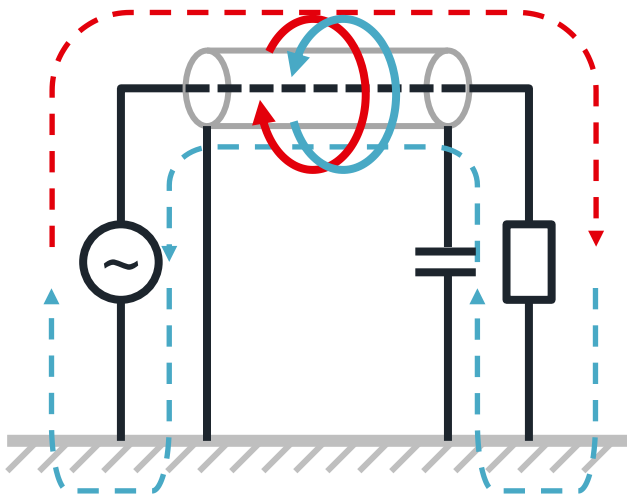
Cable Shielding



Radiating Noise



E-fields are shielded
H-fields radiating



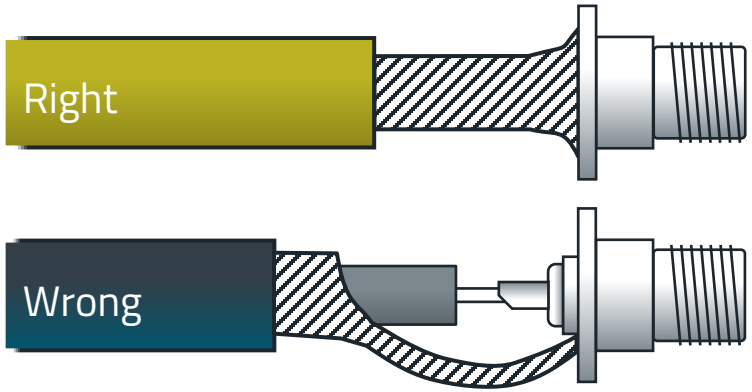
E-fields are shielded
H-fields are compensated

Cable Shielding

Shielding Mesh @ Connector

- Don’t break down shielding mesh
- Avoid Pigtails

- **Incomplete/ faulty termination is a source of CM Noise**



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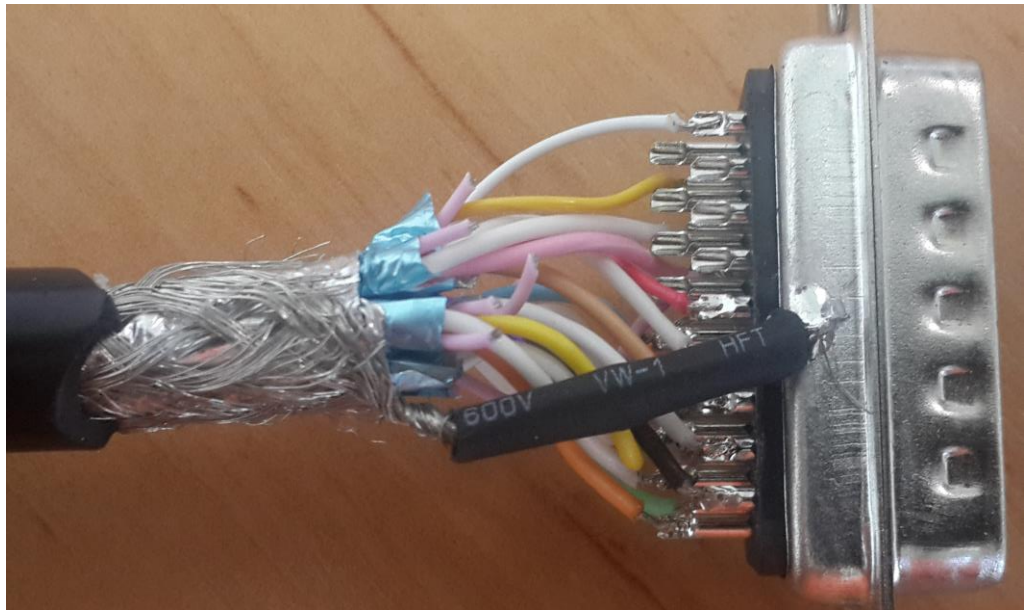
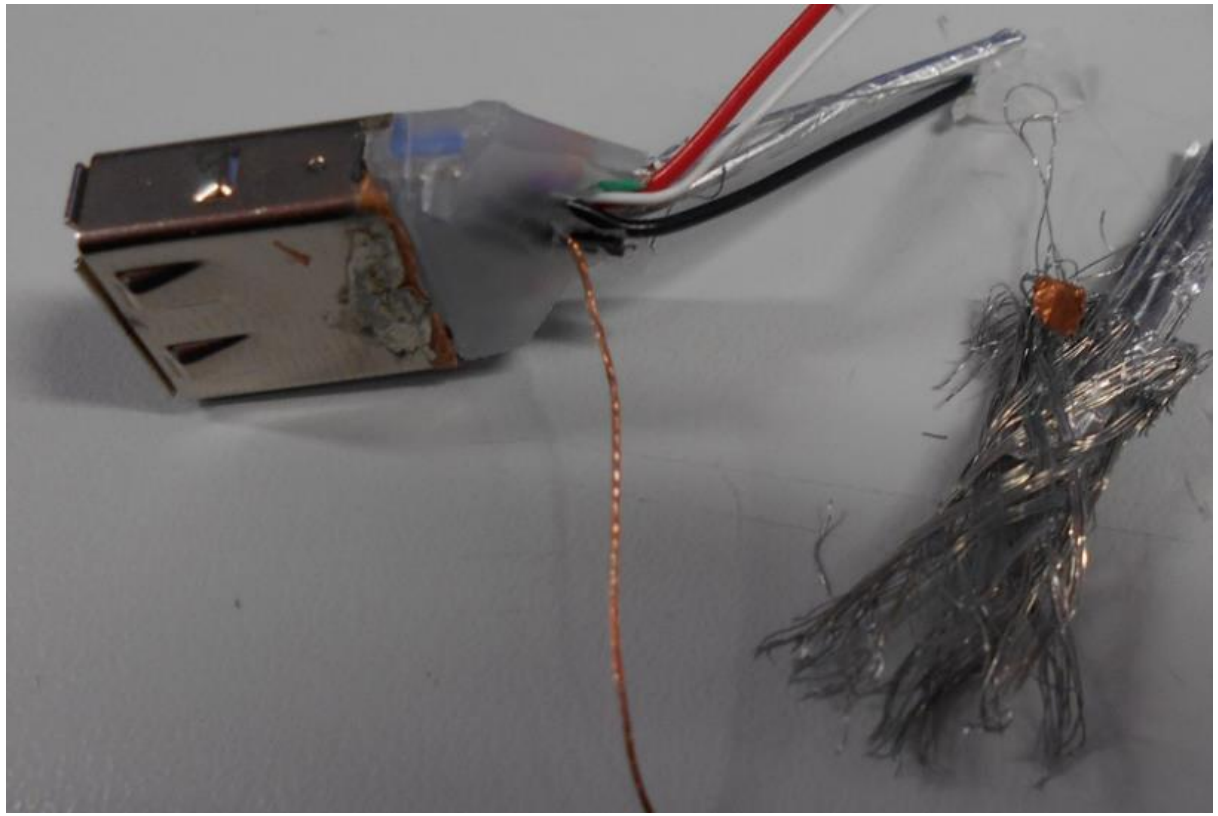


Cable Shielding

Example: USB 3 Cable – „High Quality“

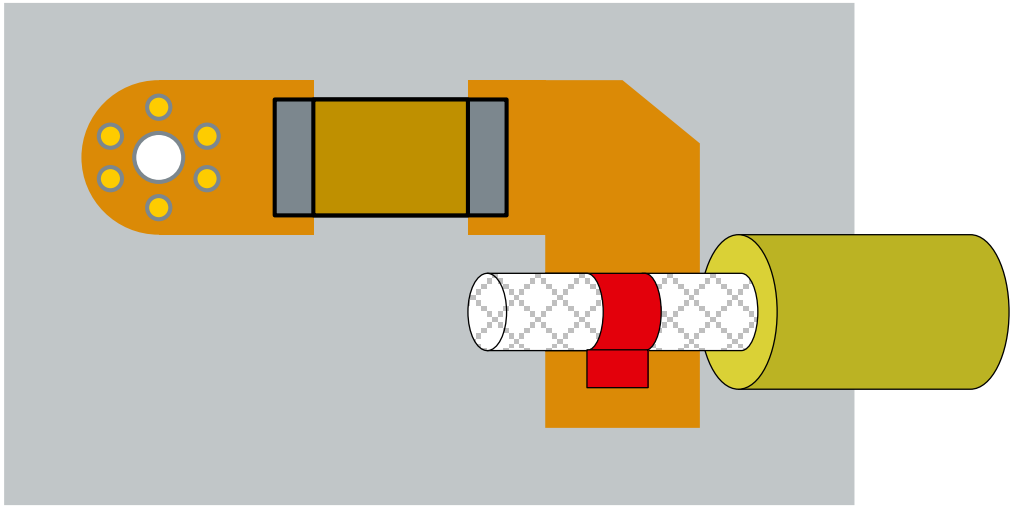


Cable Shielding

Shielding Mesh @ PCB Edge

- Go for 360° Coverage of the Mesh
- Earthing Clips of Metal or metalized Nylon are easily mounted on the PCB

- Use a Y-Capacitor and a Steel Spacer to open an RF Short to PE
  - If necessary, use a high impedance Resistor (~1MΩ) in parallel to circumvent shift of potential



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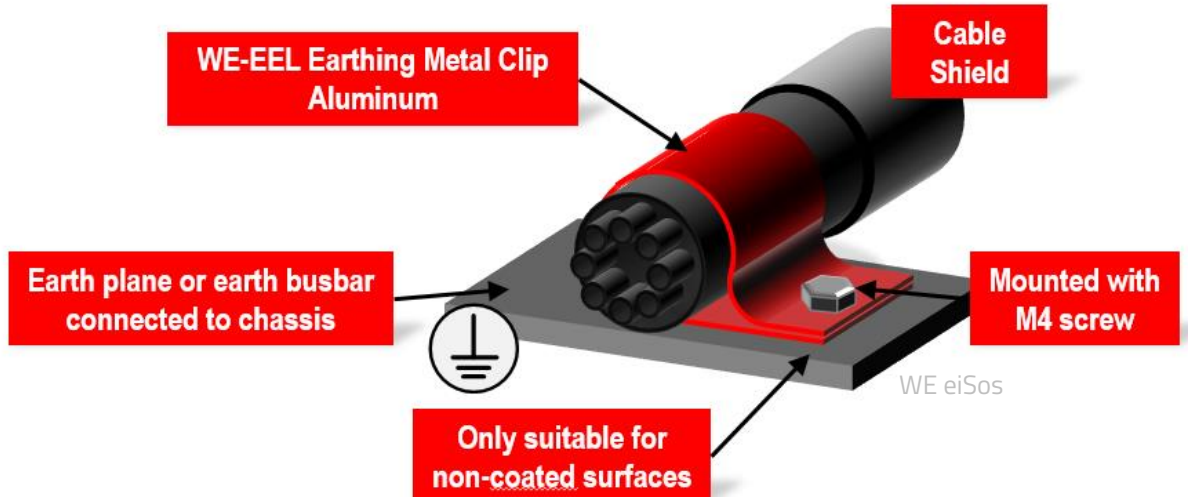

WE eiSos