- Currently, we have two modes, **SETUP** and **VRF**, for designs to do setup and verification operation respectively
  - Setup mode is **default using "yosys"** as a parser (yosysSETUP). If a user want to specify other tools to parse designs, for example, berkeley-abc and V3, one can use "*GV Set Engine*"" API to switch the setup engine
  - **Setup mode** is for parsing designs and storing design information
    - *GV Set Engine*, *GV Read Design*, *GV Print Info*, *GV File2Aig*
  - **Verify mode** is for verification operation, such as formal verification and random simulation
    - *GV Formal Verify*, *GV Random Simulate*

- Please notice that:
  - If one wants to switch mode, the "<mark>SEt SYStem &lt;mode&gt;</mark>" command is required
  - If one wants to switch to **VRF** mode but has not yet read in designs, GV tool will pop up an error message and the user is forbidden to enter **VRF** mode

- For example:
  yosysSETUP> SEt Engine abc
  abcSETUP> SET SYStem vrf
  vrf> SEt SYStem setup
  yosysSETUP>

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- There's another flow for *GV Formal Verify*. Since we use "abc" as the formal engine, it needs a recognizable file format to do formal verification. Here, we choose **AIG** format, and a user needs to construct it before doing formal verification

- A user can use "<mark>GV Read Design [-Aig]</mark>" or "<mark>GV File2Aig</mark>" in **SETUP** system mode to construct AIG format. After that, just type "<mark>Formal Verify [-bmc &lt;int_depth&gt; | -pdr | -itp]</mark>" will work, otherwise, an error message will pop out to remind one to read in AIG format

- For example, two ways to construct AIG format:
  - **1.**
    yosysSETUP> read design -v example.v
    yosysSETUP> file2 aig example.aig
    yosysSETUP> set system vrf
    vrf> formal verify -bmc 100
  - **2.**

```
yosysSETUP> set engine abc
abcSETUP> read design -aig example.aig
abcSETUP> set system vrf
vrf> formal verify -bmc 100
```