Lab4 Intro
Creating a Processor System

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Objectives

> **After completing this lab, you will be able to:**

>> Understand the steps and directives involved in creating an s_axilite IP-XACT hardware accelerator from a synthesized design in Vivado HLS

>> Create a processor system using IP Integrator in Vivado

>> Integrate the generated s_axilite IP-XACT hardware accelerator into the created processor system

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The Design

> **The design consists of a FIR filter to filter a 4 KHz tone added to a CD quality (48 KHz) music. This lab requires you to develop a peripheral core of the designed filter that can be instantiated in a processor system. The processor system will acquire a stereo music using on-board ADAU1761 CODEC chip from Analog Devices and I²S controller, process (bandstop filter) it through the designed filter, and output back to the speaker**

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Procedure

> **Create a Vivado HLS project for the FIR filter**

> **Run simulation and verify functionality**

> **Synthesize the design**

> **Run RTL/C Co-simulation**

> **Setup IP-XACT hardware accelerator**

> **Generate the IP-XACT hardware accelerator**

> **Create a Vivado project**

> **Generate bitstream and export to SDK**

> **Generate an application**

> **Verify in hardware**

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Summary

> **In this lab, you added RESOURCE directive to create an s_axilite IP-XACT hardware accelerator. You generated the s_axilite IP-XACT hardware accelerator. You then created a processor system using IP Integrator, integrated the generated ip core, and tested the system with the provided application**

Adaptable.
Intelligent.