# Course Intro
# High-Level Synthesis using Vivado HLS

# Course Objectives

- **After completing this course, you will be able to:**
  - Describe the high level synthesis flow
  - Understand the control and datapath extraction
  - Describe scheduling and binding phases of the HLS flow
  - Identify steps involved in validation and verification flows
  - State various directives which can be helpful in improving performance and resource utilization
  - Describe how to use OpenCV functions in the Vivado HLS tool
  - Perform system-level integration of blocks generated by the Vivado HLS tool

# Course Outline
# Day 1

## The course consists of the following modules:

- Introduction to High-Level Synthesis (HLS)
- Using Vivado HLS
- Lab 1: Creating Project and Understanding Reports
- Improving Performance
- Lab 2: Optimizing Performance through Pipelining
- Data Types

# Course Outline
# Day 2

- Improving Area and Resources Utilization
- Lab 3: Improving Area and Resources Utilization
- Handling Block- and Ports- Level Protocols
- Coding Considerations
- Creating a Processor System
- Lab 4: Creating a Processor System to filter Audio Signal

# Prerequisites

- Familiarity with the Xilinx Vivado Design Suite tool set
- Basic C programming
- Basic understanding of a processor-based system

# Platform Support

- **Vivado Design Suite: HLS 2018.2**
- **Xilinx University board**
  - PYNQ-Z2, PYNQ-Z1
- **Supported Operating Systems**
  - Windows 7 SP1 Professional (64 Bit)
  - Windows 10 Professional (64 Bit)
  - Red Hat Enterprise Linux 6.6 – 6.9 (64 Bit)
  - Red Hat Enterprise Linux 7.2 and 7.3 (64 Bit)
  - SUSE Linux Enterprise 11.4 and 12.2 (64 Bit)
  - Cent OS 7.2 and 7.3 (64 Bit)
  - Cent OS 6.7, 6.8, and 6.9 (64 Bit)
  - Ubuntu Linux 16.04.2 LTS (64 Bit)

# Adaptable.
# Intelligent.

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