ATmega168
Analog-to-Digital Converter

ADC0 - PC0
ADC1 - PC1
ADC2 - PC2
ADC3 - PC3
ADC4 - PC4
ADC5 - PC5
ADC6 *
ADC7 *

* Some Packages

System Clock

clk

Prescaler

Successive approximation
Analog to Digital Converter

ADCL and ADCH
ADC Data Register

ADCH — ADCL

ADLAR = 0

| - | - | - | - | - | - | ADC9 | ADC8 | ADC7 | ADC6 | ADC5 | ADC4 | ADC3 | ADC2 | ADC1 | ADC0 |

ADLAR = 1

| ADC9 | ADC8 | ADC7 | ADC6 | ADC5 | ADC4 | ADC3 | ADC2 | ADC1 | ADC0 | - | - | - | - | - | - |

ADCSRA

| ADIF |

UCSR0B

| ADIE |

SREG

| I |

ADC Conversion
Complete
Interrupt

(ADC)

Free Running Mode
Analog Comparator
External Interrupt Request 0
Timer/Counter0 Compare Match A
Timer/Counter0 Overflow
Timer/Counter1 Compare Match A
Timer/Counter1 Overflow
Timer/Counter1 Capture Event

(trigger)

ADMUX
ADC Multiplexer Selection Register

| REFS1 | REFS0 | ADLAR | . | MUX3 | MUX2 | MUX1 | MUX0 |

ADCSRB
ADC Control and Status Register B

| . | ACME | . | . | . | ADTS2 | ADTS1 | ADTS0 |

ADCSRA
ADC Control and Status Register A

| ADEN | ADSC | ADATE | ADIF | ADIE | ADPS2 | ADPS1 | ADPS0 |

REFS1	REFS0	Voltage Reference Selection
0	0	AREF (Internal V_{REF} off)
0	1	AV_{CC} *
1	0	Reserved
1	1	Internal 1.1V Reference *

* with external capacitor at AREF pin

MUX3	MUX2	MUX1	MUX0	Single Ended Input
0	0	0	0	ADC0
0	0	0	1	ADC1
0	0	1	0	ADC2
0	0	1	1	ADC3
0	1	0	0	ADC4
0	1	0	1	ADC5
0	1	1	0	ADC6
0	1	1	1	ADC7
1	0	0	0	(reserved)
1	0	0	1	(reserved)
1	0	1	0	(reserved)
1	0	1	1	(reserved)
1	1	0	0	(reserved)
1	1	0	1	(reserved)
1	1	1	0	1.1V (V_{BG})
1	1	1	1	0V (GND)

ADTS2	ADTS1	ADTS0	Trigger Source
0	0	0	Free Running Mode
0	0	1	Analog Comparator
0	1	0	External Interrupt Request 0
0	1	1	Timer/Counter0 Compare Match A
1	0	0	Timer/Counter0 Overflow
1	0	1	Timer/Counter1 Compare Match A
1	1	0	Timer/Counter1 Overflow
1	1	1	Timer/Counter1 Capture Event

ADPS2	ADPS1	ADPS0	Divison Factor
0	0	0	2
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128