1. Description

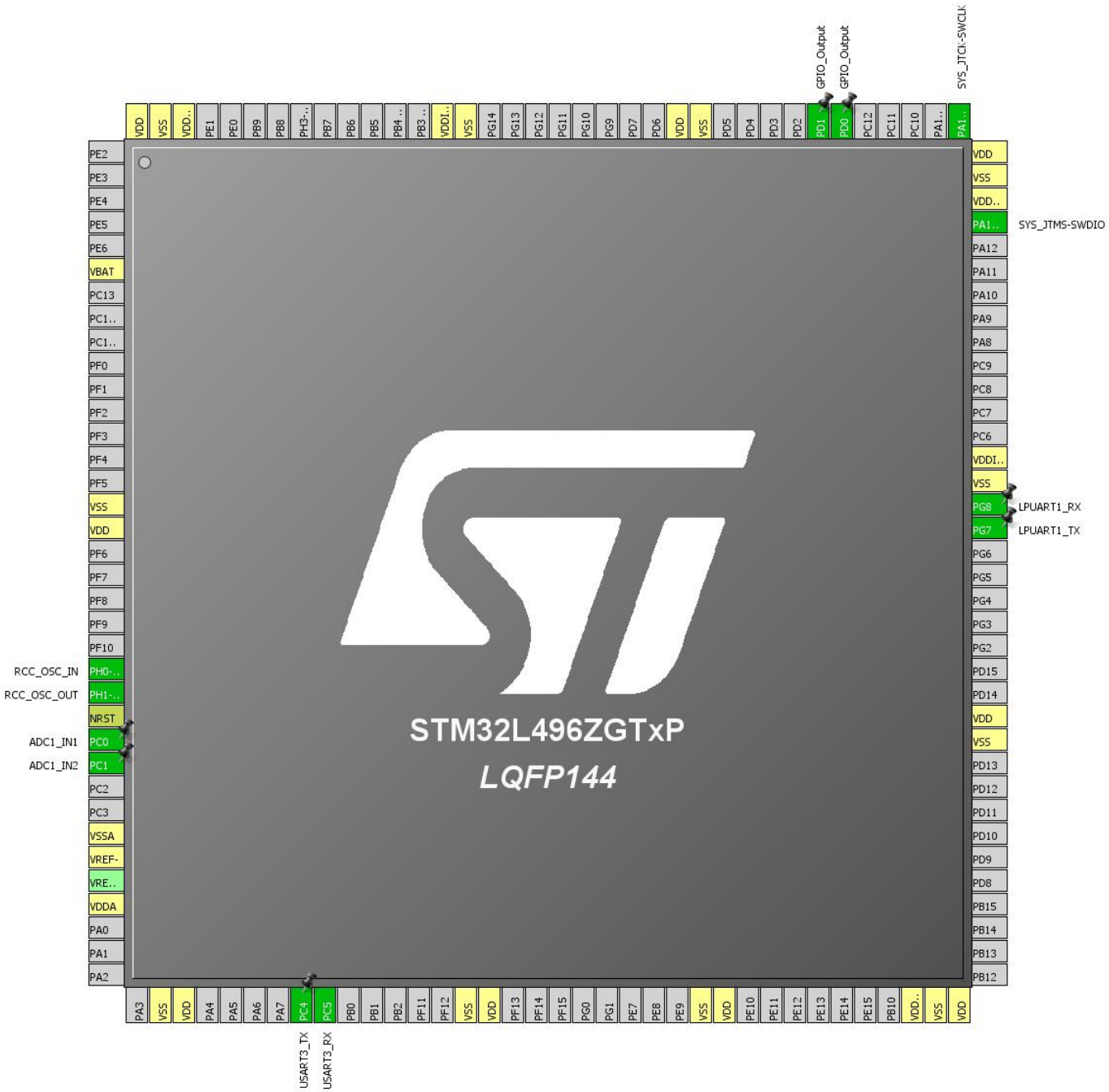
1.1. Project

Project Name	ADC_DMA_FFT_LPUART
Board Name	custom
Generated with:	STM32CubeMX 4.26.1
Date	11/18/2018

1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x6
MCU name	STM32L496ZGTxP
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration



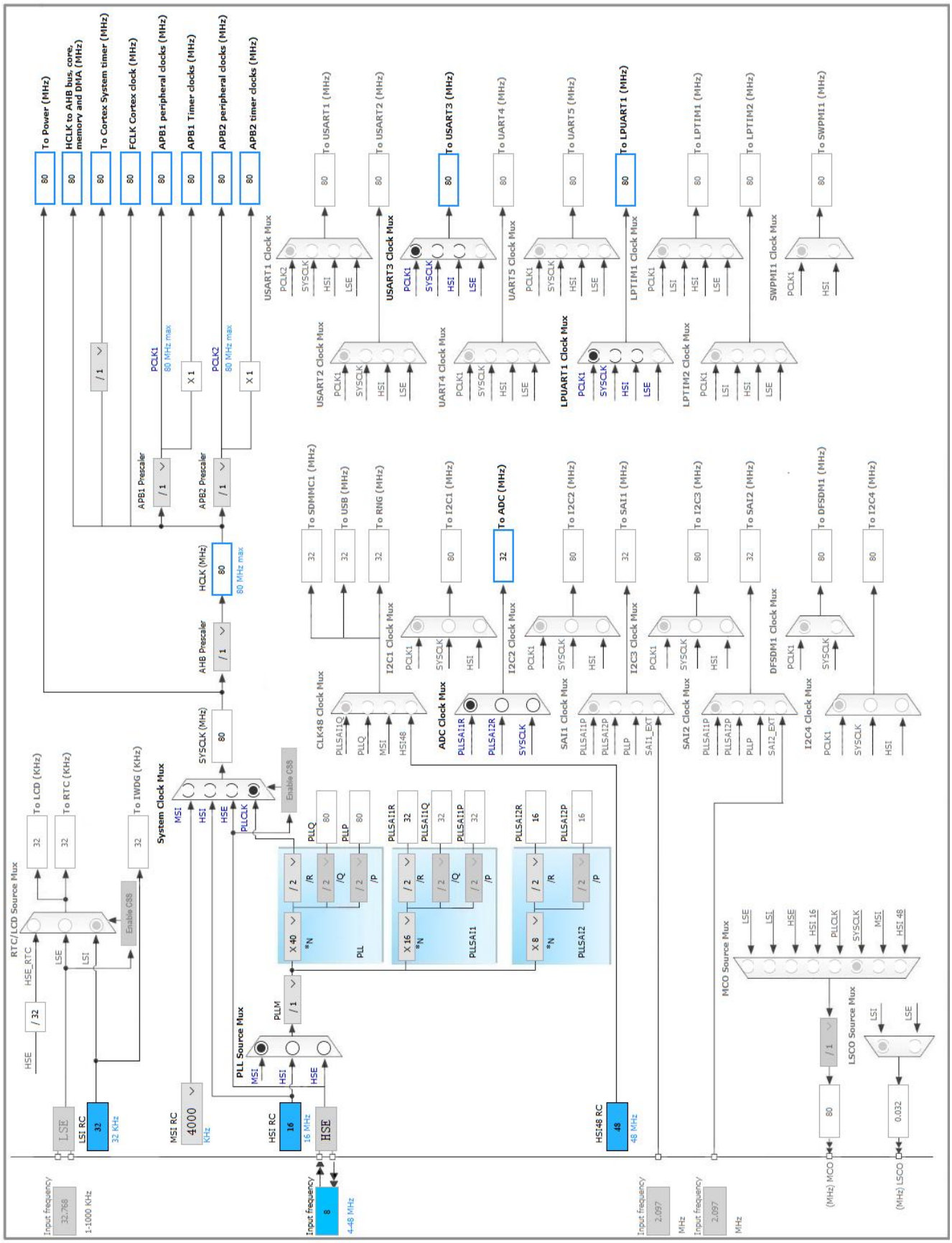
3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
16	VSS	Power		
17	VDD	Power		
23	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
24	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
25	NRST	Reset		
26	PC0	I/O	ADC1_IN1	
27	PC1	I/O	ADC1_IN2	
30	VSSA	Power		
31	VREF-	Power		
33	VDDA	Power		
38	VSS	Power		
39	VDD	Power		
44	PC4	I/O	USART3_TX	
45	PC5	I/O	USART3_RX	
51	VSS	Power		
52	VDD	Power		
61	VSS	Power		
62	VDD	Power		
70	VDD12	Power		
71	VSS	Power		
72	VDD	Power		
83	VSS	Power		
84	VDD	Power		
92	PG7	I/O	LPUART1_TX	
93	PG8	I/O	LPUART1_RX	
94	VSS	Power		
95	VDDIO2	Power		
105	PA13 (JTMS/SWDIO)	I/O	SYS_JTMS-SWDIO	
106	VDDUSB	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14 (JTCK/SWCLK)	I/O	SYS_JTCK-SWCLK	
114	PD0 *	I/O	GPIO_Output	
115	PD1 *	I/O	GPIO_Output	
120	VSS	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
121	VDD	Power		
130	VSS	Power		
131	VDDIO2	Power		
142	VDD12	Power		
143	VSS	Power		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

IN1: IN1 Single-ended

IN2: IN2 Single-ended

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	**2 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 1
Sampling Time	**12.5 Cycles ***
Offset Number	No offset
Rank	**2 ***
Channel	**Channel 2 ***
Sampling Time	**12.5 Cycles ***
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

5.2. LPUART1

Mode: Asynchronous

5.2.1. Parameter Settings:

Basic Parameters:

Baud Rate	**115200 ***
Word Length	**8 Bits (including Parity) ***
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Single Sample	Disable

Advanced Features:

Auto Baudrate Mode	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	4 WS (5 CPU cycle)

RCC Parameters:

HSI Calibration Value	64
MSI Calibration Value	0
MSI Auto Calibration	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

5.4. SYS

Debug: Serial Wire

Timebase Source: SysTick

5.5. TIM3

Clock Source : Internal Clock

5.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**40000-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**2-1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

5.6. USART3

Mode: Asynchronous

5.6.1. Parameter Settings:

Basic Parameters:

Baud Rate	**9600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN1	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PC1	ADC1_IN2	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
LPUART1	PG7	LPUART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PG8	LPUART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
RCC	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13 (JTMS/SWDIO)	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14 (JTCK/SWCLK)	SYS_JTCK-SWCLK	n/a	n/a	n/a	
USART3	PC4	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC5	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
GPIO	PD0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

6.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	**High ***
LPUART_RX	DMA2_Channel7	Peripheral To Memory	Low
LPUART_TX	DMA2_Channel6	Memory To Peripheral	Low

ADC1: DMA1_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	**Word ***

LPUART_RX: DMA2_Channel7 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

LPUART_TX: DMA2_Channel6 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	0
TIM3 global interrupt	true	0	0
USART3 global interrupt	true	0	0
DMA2 channel6 global interrupt	true	0	0
DMA2 channel7 global interrupt	true	0	0
LPUART1 global interrupt	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 interrupts	unused		
FPU global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x6
MCU	STM32L496ZGTxP
Datasheet	029173_Rev2

7.2. Parameter Selection

Temperature	25
Vdd	null

8. Software Project

8.1. Project Settings

Name	Value
Project Name	ADC_DMA_FFT_LPUART
Project Folder	E:\Documents\STM32L4\ADC_DMA_FFT_LPUART - +LoRa
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_L4 V1.12.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

9. Software Pack Report