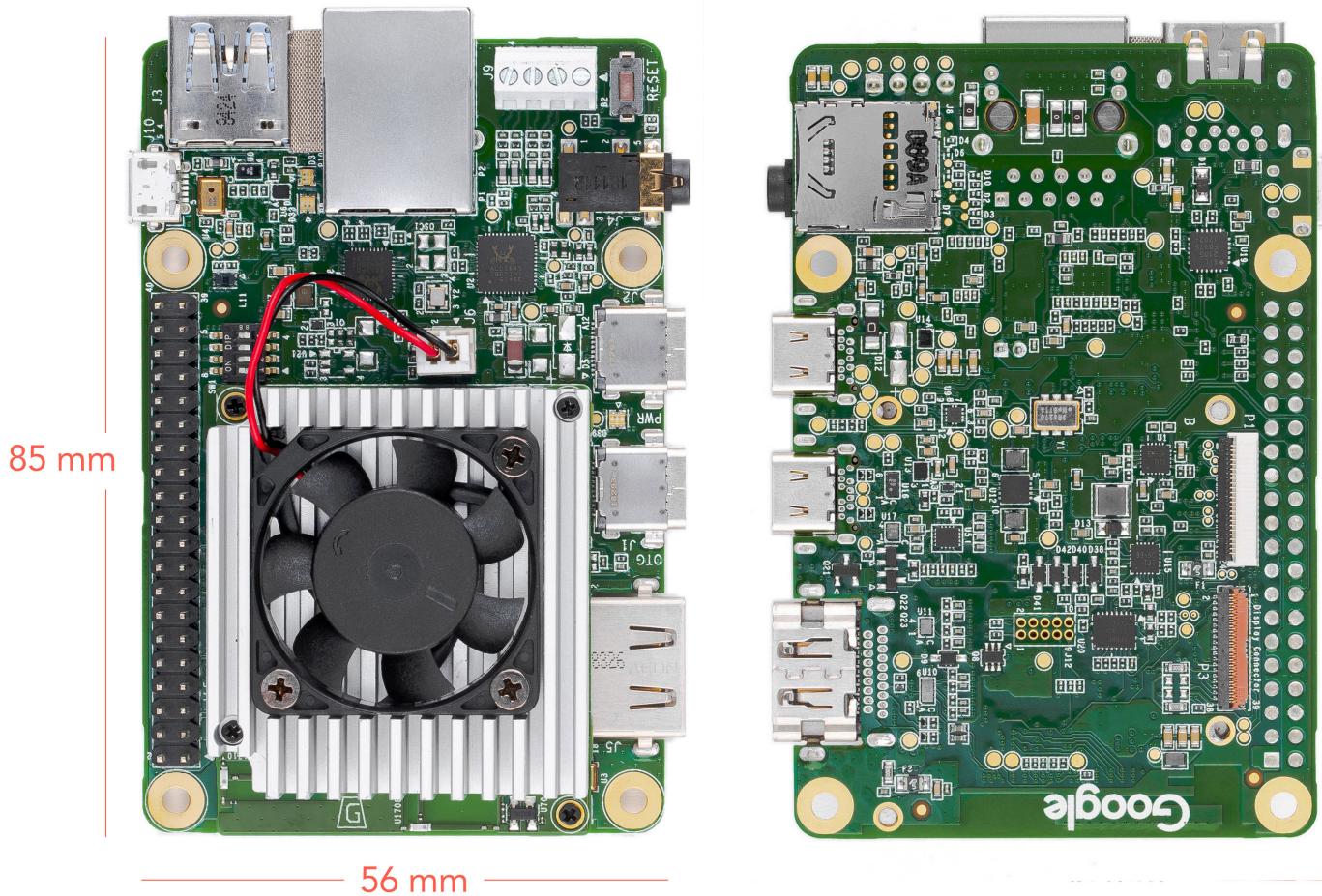


Coral

# Dev Board Datasheet

Beta version



# Features

- Edge TPU Module (SOM)
  - NXP i.MX 8M SOC (Quad-core Cortex-A53, plus Cortex-M4F)
  - Google Edge TPU ML accelerator coprocessor
  - Cryptographic coprocessor
  - Wi-Fi 2x2 MIMO (802.11b/g/n/ac 2.4/5GHz)
  - Bluetooth 4.1
  - 8GB eMMC
  - 1GB LPDDR4
- USB connections
  - USB Type-C power port (5V DC)
  - USB 3.0 Type-C OTG port
  - USB 3.0 Type-A host port
  - USB 2.0 Micro-B serial console port
- Audio connections
  - 3.5mm audio jack (CTIA compliant)
  - Digital PDM microphone (x2)
  - 2.54mm 4-pin terminal for stereo speakers
- Video connections
  - HDMI 2.0a (full size)
  - 39-pin FFC connector for MIPI-DSI display (4-lane)
  - 24-pin FFC connector for MIPI-CSI2 camera (4-lane)
- MicroSD card slot
- Gigabit Ethernet port
- 40-pin GPIO expansion header
- Supports Debian Linux

# Overview

The Coral Dev Board is a single-board computer with a removable system-on-module (SOM) that contains eMMC, SOC, wireless radios, and the Edge TPU. You can use the Dev Board as a single-board computer when you need accelerated ML processing in a small form factor, but it also serves as an evaluation kit for the SOM. You can use the dev board to prototype internet-of-things (IOT) devices and other embedded systems that demand fast on-device ML inferencing, and then scale to production using just the 40 mm × 48 mm SOM board combined with your custom PCB hardware using board-to-board connectors.

The SOM is based on NXP's iMX8M system-on-chip (SOC), but its unique power comes from the Edge TPU coprocessor. The Edge TPU is a small ASIC designed by Google that provides high performance ML inferencing with a low power cost. For example, it can execute state-of-the-art mobile vision models such as MobileNet v2 at 100+ fps, in a power efficient manner.

Edge TPU key benefits:

- High speed TensorFlow Lite inferencing
- Low power
- Small footprint

The baseboard includes all the peripheral connections you need to prototype a project, including USB 2.0/3.0 ports, DSI display interface, CSI2 camera interface, Ethernet port, speaker terminals, and a 40-pin GPIO header.

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# Hardware overview

The Coral Dev Board is composed of the Edge TPU Module (SOM) and a development baseboard. The SOM connects to the baseboard with three 100-pin connectors.

The SOM is based on NXP's iMX8M system-on-chip (SOC) provides an application processor to host your embedded operating system, Wi-Fi and Bluetooth connectivity, cryptographic security, and accelerated ML inferencing. The baseboard primarily serves as a prototyping board that allows you to connect other hardware peripherals to the system.

Figures 1 and 2 illustrate the core components on the baseboard and SOM.

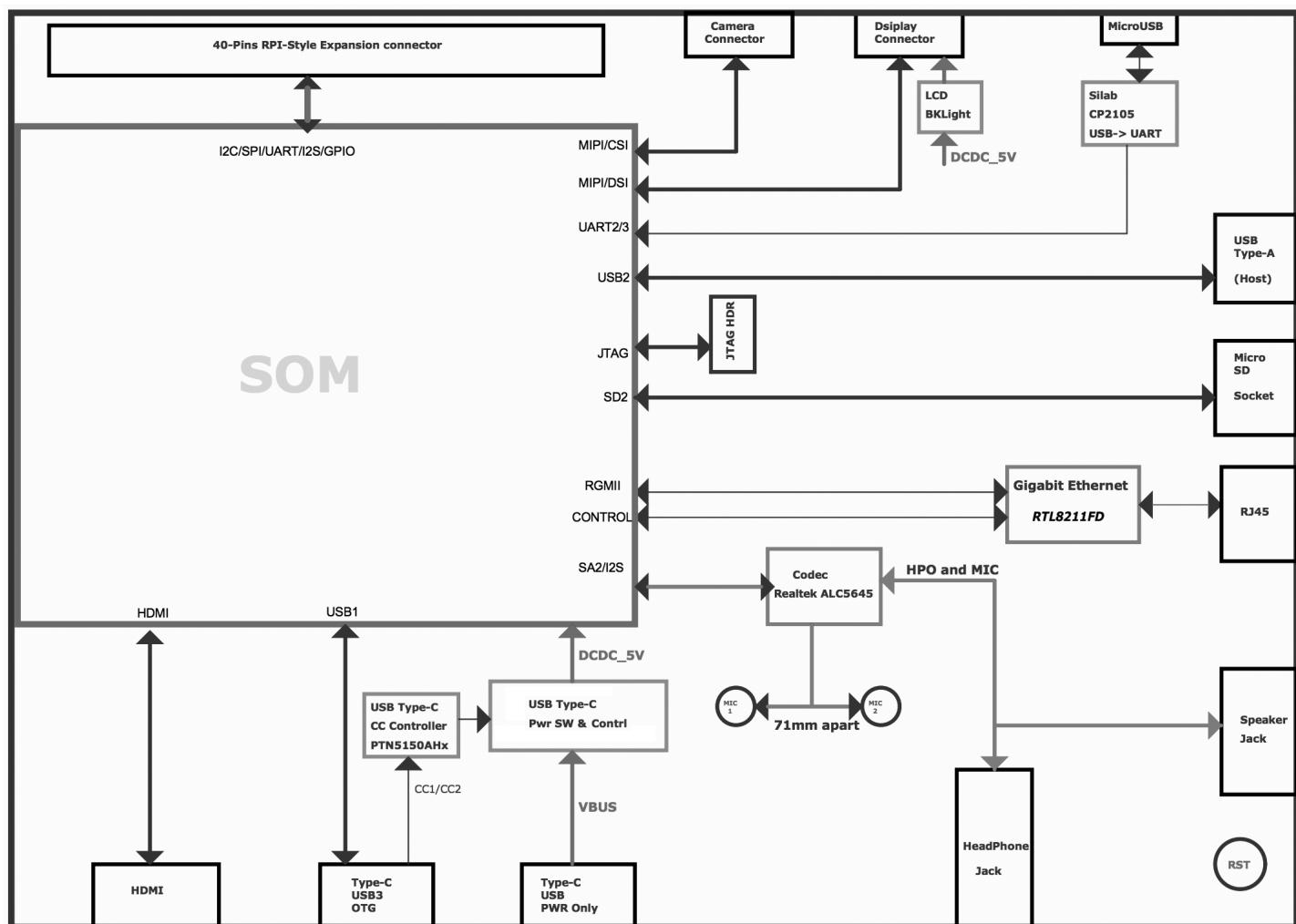


Figure 1. Block diagram of the baseboard components

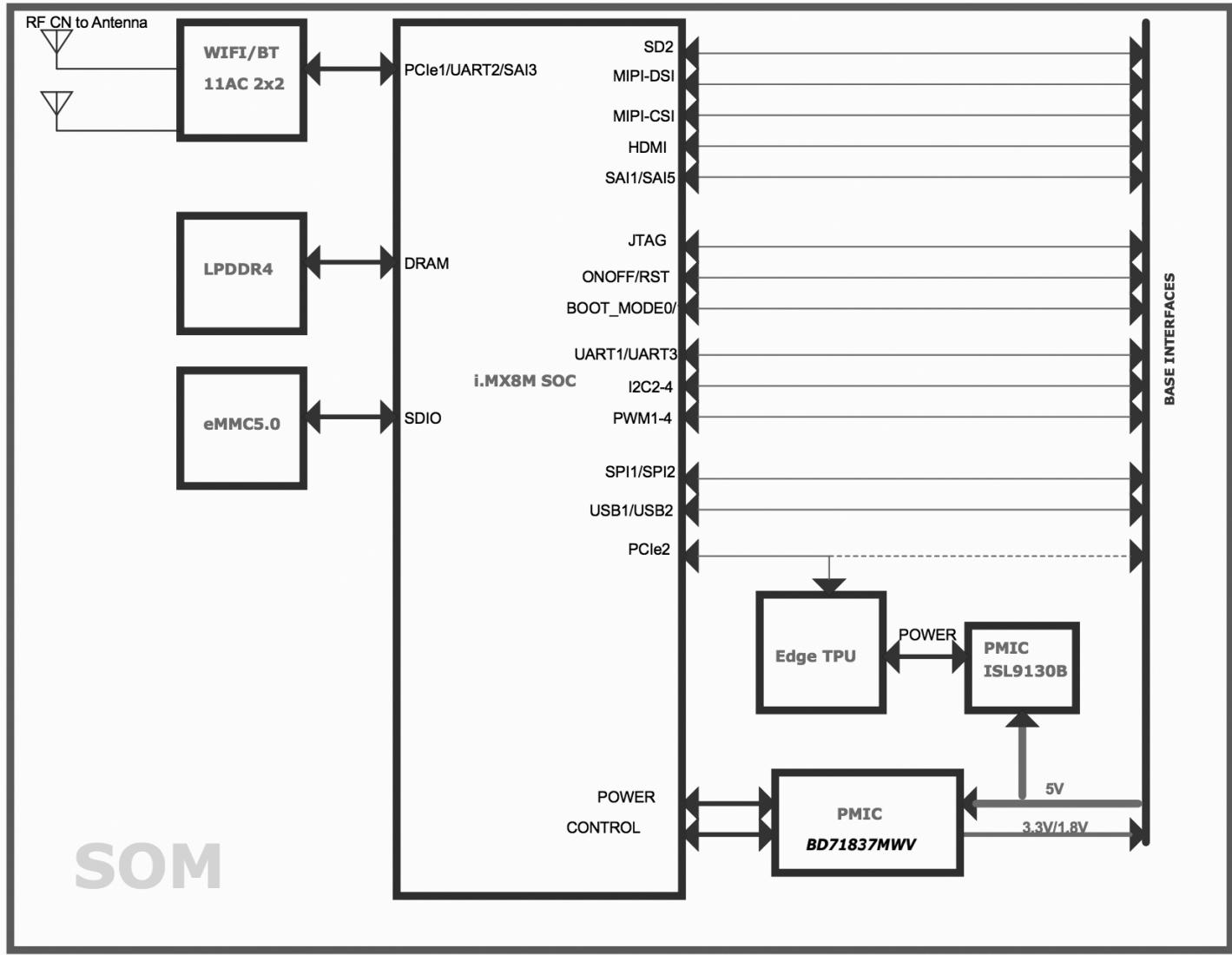


Figure 2. Block diagram of the SOM components

# Components overview

Feature	Details
Main system-on-chip (SOC) complex (i.MX8M SOC by NXP)	
Arm Cortex-A53 MPCore platform	<p>Quad symmetric Cortex-A53 processors:</p> <ul style="list-style-type: none"><li>• 32 KB L1 Instruction Cache</li><li>• 32 KB L1 Data Cache</li><li>• Support L1 cache RAMs protection with parity/ECC</li></ul> <p>Support of 64-bit Armv8-A architecture:</p> <ul style="list-style-type: none"><li>• 1 MB unified L2 cache</li><li>• Support L2 cache RAMs protection with ECC</li><li>• Frequency of 1.5 GHz</li></ul>
Arm Cortex-M4 core platform	<ul style="list-style-type: none"><li>• 16 KB L1 Instruction Cache</li><li>• 16 KB L1 Data Cache</li><li>• 256 KB tightly coupled memory (TCM)</li></ul>
Graphic Processing Unit	<ul style="list-style-type: none"><li>• 4 shaders</li><li>• 267 million triangles/sec</li><li>• 1.6 Gigapixel/sec</li><li>• 32 GFLOPs 32-bit or 64 GFLOPs 16-bit</li><li>• Support OpenGL ES 1.1, 2.0, 3.0, 3.1, Open CL 1.2, and Vulkan</li></ul>
Video Processing Unit	<ul style="list-style-type: none"><li>• 4Kp60 HEVC/H.265 main, and main 10 decoder</li><li>• 4Kp60 VP9 and 4Kp30 AVC/H.264 decoder (requires full system resources)</li><li>• 1080p60 MPEG-2, MPEG-4p2, VC-1, VP8, RV9, AVS, MJPEG, H.263 decoder</li></ul>

Feature	Details
I/O Connectivity	<ul style="list-style-type: none"> <li>Two PCI Express Gen2 interfaces</li> <li>Two USB 3.0/2.0 controllers with integrated PHY interfaces</li> <li>Two Ultra Secure Digital Host Controller (uSDHC) interfaces</li> <li>One Gigabit Ethernet controller with support for EEE, Ethernet AVB, and IEEE 1588</li> <li>Four Universal Asynchronous Receiver/Transmitter (UART) modules</li> <li>Four I2C modules</li> <li>Three SPI modules</li> <li>GPIO modules with interrupt capability</li> <li>Input/output multiplexing controller (IOMUXC) to provide centralized pad control</li> </ul>
On-chip memory	<ul style="list-style-type: none"> <li>Boot ROM (128 KB)</li> <li>On-chip RAM (128 KB + 32 KB)</li> </ul>
External memory	<ul style="list-style-type: none"> <li>32/16-bit DRAM interface: LPDDR4-3200, DDR4-2400, DDR3L-1600</li> <li>8-bit NAND-Flash</li> <li>eMMC 5.0 Flash</li> <li>SPI NOR Flash</li> <li>QuadSPI Flash with support for XIP</li> </ul>
Display	<p>HDMI Display Interface:</p> <ul style="list-style-type: none"> <li>HDMI 2.0a supporting one display up to 1080p</li> <li>Upscale and downscale between 4K and HD video (requires full system resources)</li> <li>20+ Audio interfaces 32-bit @ 384 kHz fs, with Time Division Multiplexing (TDM) support</li> <li>S/PDIF input and output</li> <li>Audio Return Channel (ARC) on HDMI</li> </ul> <p>MIPI-DSI Display Interface:</p> <ul style="list-style-type: none"> <li>MIPI-DSI 4 channels supporting one display, resolution up to 1920 x 1080 at 60 Hz</li> <li>LCDIF display controller</li> <li>Output can be LCDIF output or DC display controller output</li> </ul>

Feature	Details
Audio	<ul style="list-style-type: none"> <li>S/PDIF input and output</li> <li>Five synchronous audio interface (SAI) modules supporting I2S, AC97, TDM, and codec/DSP interfaces, including one SAI with 16 Tx and 16 Rx channels, one SAI with 8 Tx and 8 Rx channels, and three SAI with 2 Tx and 2 Rx channels</li> <li>One SAI for 8 Tx channels for HDMI output audio</li> <li>One S/PDIF input for HDMI ARC input</li> </ul>
Camera	<ul style="list-style-type: none"> <li>Two MIPI-CSI2 camera inputs (4-lane each)</li> </ul>
Security	<ul style="list-style-type: none"> <li>Resource Domain Controller (RDC) supports four domains and up to eight regions</li> <li>Arm TrustZone (TZ) architecture</li> <li>On-chip RAM (OCRAM) secure region protection using OCRAM controller</li> <li>High Assurance Boot (HAB)</li> <li>Cryptographic acceleration and assurance (CAAM) module</li> <li>Secure non-volatile storage (SNVS): Secure real-time clock (RTC)</li> <li>Secure JTAG controller (SJC)</li> </ul>
ML accelerator	
Edge TPU coprocessor	<ul style="list-style-type: none"> <li>ASIC designed by Google that provides high performance ML inferencing for TensorFlow Lite models</li> <li>Uses PCIe and I2C/GPIO to interface with the iMX8M SOC</li> </ul>
Memory and storage	
Random access memory (SDRAM)	<ul style="list-style-type: none"> <li>1GB LPDDR4 SDRAM (4-channel, 32-bit bus width)</li> <li>1600MHz maximum DDR clock</li> <li>Interfaces directly to the iMX8M build-in DDR controller</li> </ul>
Flash memory (eMMC)	<ul style="list-style-type: none"> <li>8GB NAND eMMC flash memory</li> <li>8-bits MMC mode</li> <li>Conforms to JEDEC version 5.0 and 5.1</li> </ul>
Expandable flash (MicroSD)	<ul style="list-style-type: none"> <li>Meets SD/SDIO 3.0 standard</li> <li>Runs at 4-bits SDIO mode</li> <li>Supports system boot from SD card</li> </ul>

Feature	Details
<b>Network &amp; wireless</b>	
Ethernet	<ul style="list-style-type: none"> <li>• 10/100/1000 Mbps Ethernet/IEEE 802.3 networks</li> </ul>
Wi-Fi	<ul style="list-style-type: none"> <li>• Wi-Fi 2x2 MIMO (802.11a/b/g/n/ac 2.4/5GHz)</li> <li>• Supports PCIe host interface for W-LAN</li> </ul>
Bluetooth	<ul style="list-style-type: none"> <li>• Bluetooth 4.1 (supports Bluetooth low-energy)</li> <li>• Supports UART interface</li> </ul>
<b>Security</b>	
Cryptographic coprocessor	<ul style="list-style-type: none"> <li>• Microchip ATECC608A cryptographic coprocessor</li> <li>• Asymmetric (public/private) key cryptographic signature solution based on Elliptic Curve Cryptography and ECDSA signature protocols</li> </ul>
<b>Baseboard</b>	
Connectors	<ul style="list-style-type: none"> <li>• 40-pin GPIO header (see pinout below)</li> <li>• USB Micro-B for serial console</li> <li>• USB 3.0 Type-A host</li> <li>• Gigabit Ethernet</li> <li>• 4-pin stereo terminal</li> <li>• 3.5mm audio jack</li> <li>• USB Type-C power</li> <li>• USB Type-C data</li> <li>• HDMI 2.0a (full size)</li> <li>• MicroSD slot</li> <li>• MIPI-DSI display (39-pin flat flex cable)</li> <li>• MIPI-CSI2 camera (24-pin flat flex cable)</li> </ul>

## Dev board dimensions

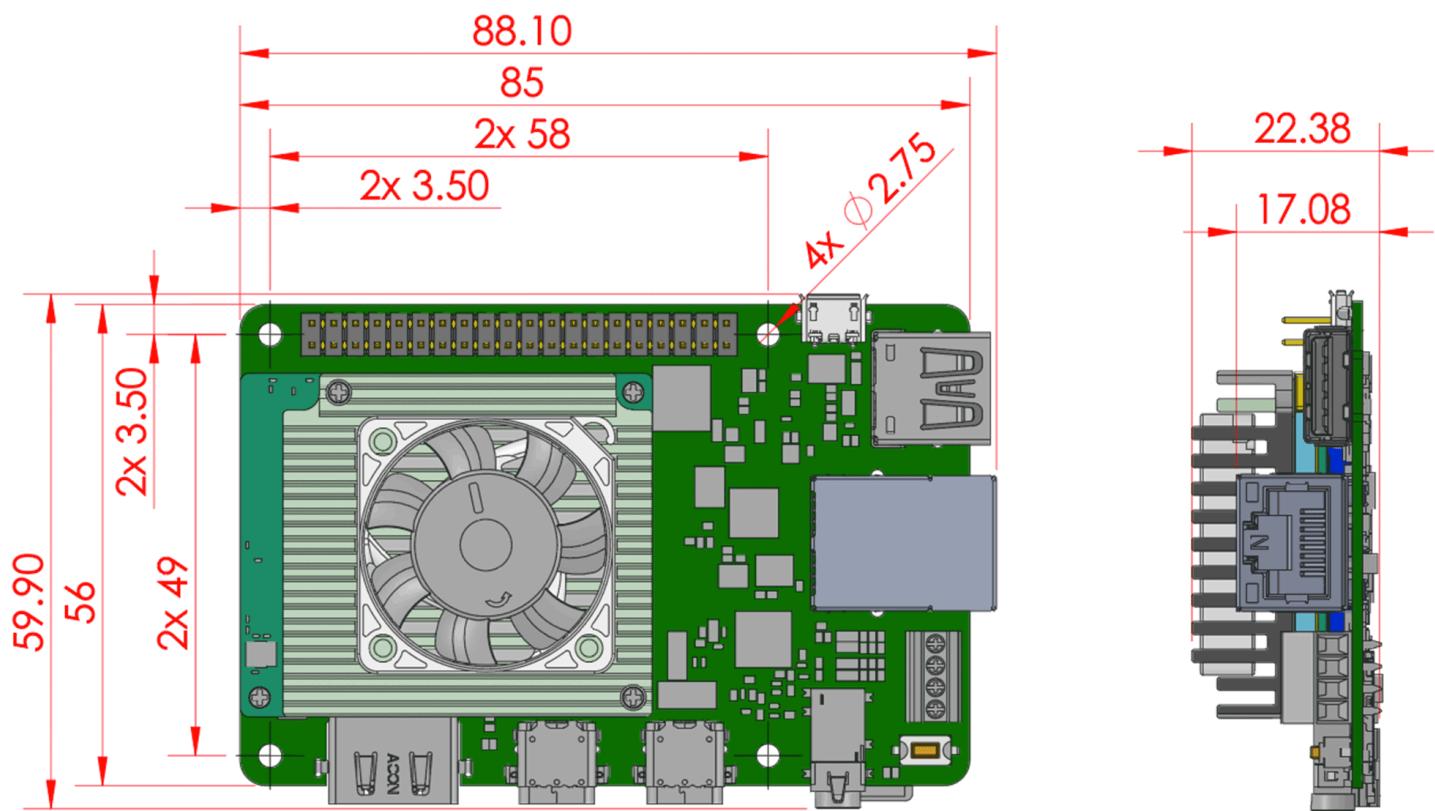


Figure 3. Coral Dev Board dimensions

# Baseboard connections

The baseboard on the Coral Dev Board provides a variety of connectors as shown in figure 4.

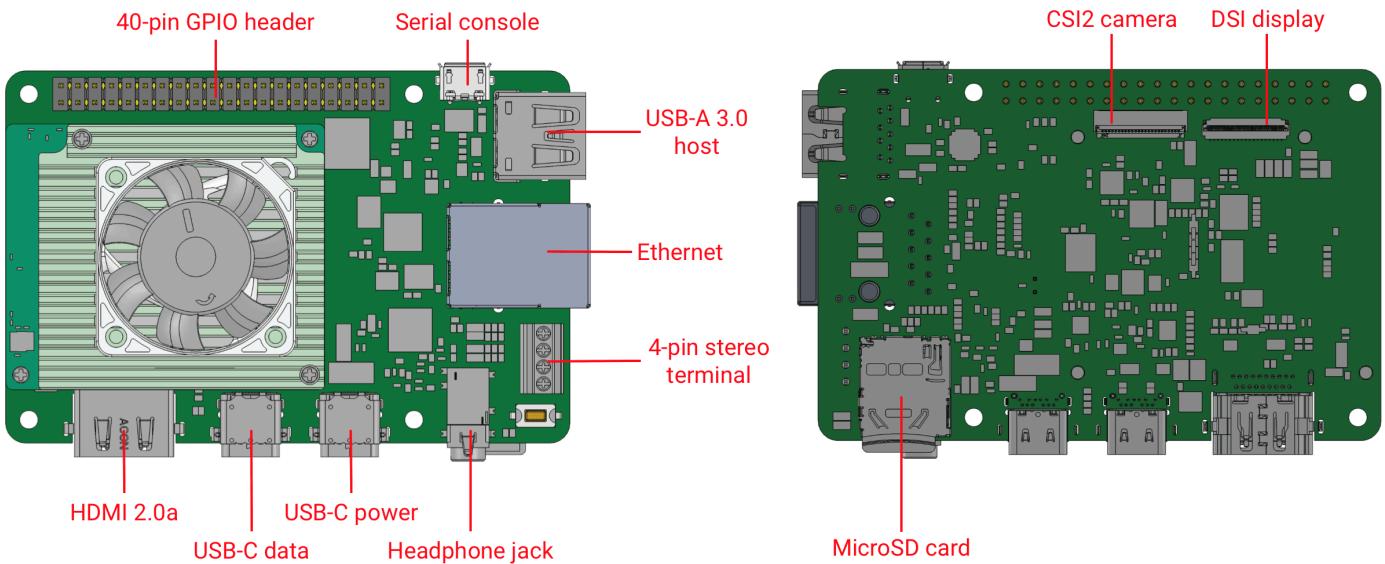


Figure 4. Connectors on the Coral Dev Board

## GPIO header pinout

All GPIO pins are powered by the 3.3V power rail, with a programmable impedance of 40 - 255 ohms, and a max current of ~ 82 mA. You can interact with each pin using standard Linux interfaces such as device files (/dev) and sysfs files (/sys).

All GPIO pins have a 90k pull-down resistor inside the iMX8M SOC that is used by default during bootup, except for the I2C pins, which instead have a pull-up to 3.3V on the SOM. However, these can all be changed with a device tree overlay that loads after bootup.

**Caution:** Do not connect a device that draws more than ~ 82 mA of power or you will brownout the system.

SOC SIGNAL	BASEBOARD SIGNAL		BASEBOARD SIGNAL	SOC SIGNAL
	3V3 power	1	2	5V power
I2C2_SDA	I2C2_SDA	3	4	5V power
I2C2_SCL	I2C2_SCL	5	6	Ground
UART3_TXD	UART3_TXD	7	8	UART1_TXD
	Ground	9	10	UART1_RXD
UART3_RXD	UART3_RXD	11	12	SAI1_TXC
GPIO6	GPIO_P13	13	14	Ground
PWM3	PWM3	15	16	GPIO_P16
	3V3 power	17	18	ECSPI2_SCLK
ECSPI1_MOSI	ECSPI1_MOSI	19	20	Ground
ECSPI1_MISO	ECSPI1_MISO	21	22	ECSPI2_MISO
ECSPI1_SCLK	ECSPI1_SCLK	23	24	ECSPI1_SS0
	Ground	25	26	ECSPI1_SS1
I2C3_SDA	I2C3_SDA	27	28	I2C3_SCL
GPIO7	GPIO_P29	29	30	Ground
GPIO8	GPIO_P31	31	32	PWM1
PWM2	PWM2	33	34	Ground
SAI1_TXFS	SAI1_TXFS	35	36	ECSPI2_SS0
NAND_DATA07	GPIO_P37	37	38	SAI1_RXD0
	Ground	39	40	SAI1_TXD0

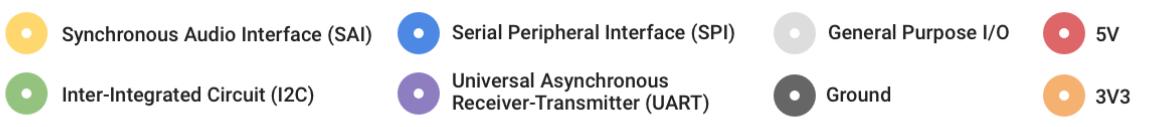


Figure 5. Pinout for the 40-pin GPIO header

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# Universal Asynchronous Receiver-Transmitter (UART)

Each UARTv2 module supports the following:

- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd, or none).
- Programmable baud rates up to 4 Mbps.
- 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud.

## Synchronous Audio Interface (SAI)

Each SAI module supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.

## Inter-Integrated Circuit (I2C)

Serial interface for external devices.

## Serial Peripheral Interface (SPI)

Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. Configurable to support Master/Slave modes, four chip selects to support multiple peripherals.

## Pulse Width Modulation (PMW)

Operates on a frequency of 0 - 66Mhz. Provides a 16-bit counter and is optimized to generate sound from stored sample audio images. It can drive motors and generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.

## Serial console port

The micro-USB port (see "serial console" in figure 4) provides access to the serial console based on the CP210x USB to UART Bridge Controller. Only Linux is officially supported for serial console connections, but you might have success from another platform if you install the appropriate [CP210x USB to UART Bridge Virtual COM Port \(VCP\) driver](#).

To connect, first determine the device filename for the serial connection by running this command on your Linux computer:

```
dmesg | grep ttyUSB
```

You should see two results such as this:

```
[ 6437.706335] usb 2-13.1: cp210x converter now attached to ttyUSB0  
[ 6437.708049] usb 2-13.1: cp210x converter now attached to ttyUSB1
```

Then use the name of the *first* filename listed as a `cp210x converter` to open the serial console connection (this example uses `ttyUSB0` as shown from above):

```
screen /dev/ttyUSB0 115200
```

You should now be connected.

**Tip:** You can also connect to the board via SSH over USB.

## HDMI port

This is a full-size HDMI 2.0a port.

By default, the output is locked at a resolution of 1920 x 1080 to avoid GPU pressure and power costs when driving higher resolution displays.

If your display does not support 1920 x 1080, you can change this setting by editing file at `/etc/xdg/weston/weston.ini`: In the `[output]` section, edit the line `mode=1920x1080` to be a resolution of your choice. You may also delete this line completely, and it will then use the highest resolution supported by the monitor (but doing so can degrade the overall system performance if it is higher than 1920x1080).

## USB 3.0 ports

There are three USB 3.0 ports:

- **USB Type-A host:** Operates as a USB 3.0 host that can provide power. Use this port for your peripherals, such as a USB camera.

**Caution:** Do not connect a device that draws more than 1 amp of power or you will brownout the system.

- **USB Type-C data:** Operates as a USB "on the go" (OTG) device port, so the Dev Board appears as a USB device to a connected host device. Use this port to [connect via SSH over USB](#) or to [flash the board](#).
- **USB Type-C power:** Use this to power the board with a 2 - 3A at 5V DC connection.

## Ethernet port

The Gigabit Ethernet port (RJ45) supports 10/100/1000 Mbps Ethernet/IEEE 802.3 networks.

## 4-pin stereo terminal

We recommend using a 4 Ohm, 3 watt speaker. A higher Ohmage results in a much quieter output.

The stereo terminal is a 4-pin 2.54mm-pitch terminal connector for stereo speakers. Wire functions are as follows (from left to right, as shown in figure 6):

- 1: Speaker left positive
- 2: Speaker left negative
- 3: Speaker right positive
- 4: Speaker right negative

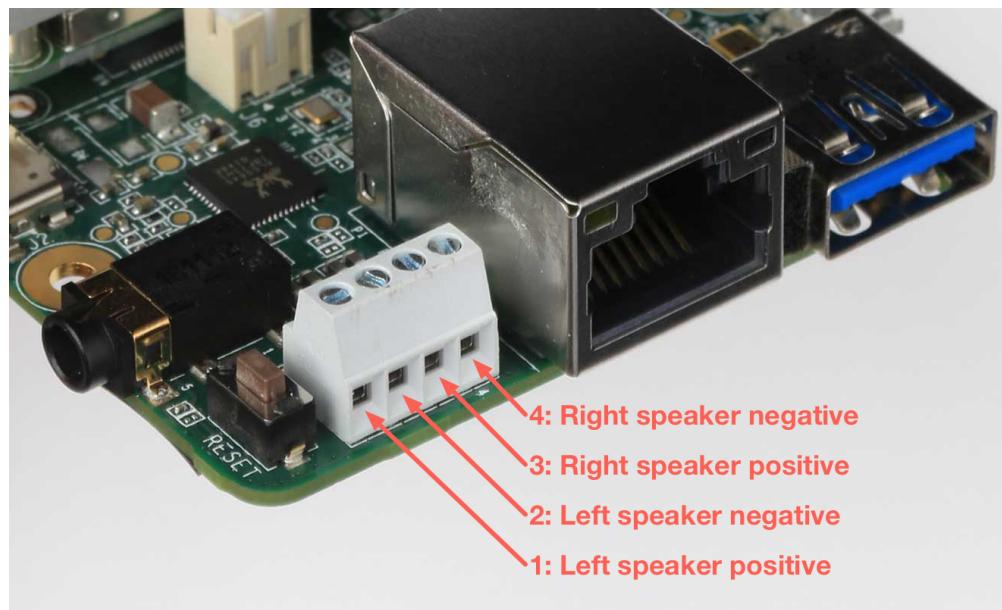


Figure 6. Stereo speaker terminals

## MicroSD slot

The MicroSD card meets the SD/SDIO standard, up to version 3.0. It can be used as expanded memory for the system or as the disk for the system image. If the entire system fails, you can use the SD card to reflash u-boot onto the board (see the [flashing instructions](#)).

## MIPI-DSI display connector

The MIPI-DSI display connector is a 39-pin flex cable connector that provides 4 lanes with resolution up to 1920x1080 at 60Hz. The connector pinout is as follows.

Pin #	Name
1	GND
2	---TP5
3	---TP20
4	---TP2
5	GND
6	MIPI_DSI_D2_P
7	MIPI_DSI_D2_N
8	GND
9	MIPI_DSI_D1_P
10	MIPI_DSI_D1_N
11	GND
12	MIPI_DSI_CLK_P
13	MIPI_DSI_CLK_N
14	GND
15	MIPI_DSI_D0_P
16	MIPI_DSI_D0_N
17	GND
18	MIPI_DSI_D3_P
19	MIPI_DSI_D3_N
20	GND

Pin #	Name
21	DSI_TE
22	---
23	V1V8
24	---
25	DISP_LEDA
26	DISP_LEDK1
27	DISP_LEDK2
28	VOP_5p5_CONN
29	VON_N5p5_CONN
30	LED_PWM
31	GND
32	GND
33	--- TP21
34	GND
35	DISPLAY_I2C_SCL_1V8
36	DISPLAY_I2C_SDA_1V8
37	DSI_VSP_EN
38	DSI_TS_nINT
39	DSI_RESETB

## MIPI-CSI2 camera connector pinout

The MIPI-CSI2 camera connector is a 24-pin flex cable connector that's designed for the Coral Camera Module. The connector pinout is as follows.

Pin #	Name
1	GND
2	MIPI_CSI_D0N
3	MIPI_CSI_D0P
4	GND
5	MIPI_CSI_D1N
6	MIPI_CSI_D1P
7	GND
8	MIPI_CSI_CLKN
9	MIPI_CSI_CLKP
10	GND
11	MIPI_CSI_D2N
12	MIPI_CSI_D2P

Pin #	Name
13	GND
14	MIPI_CSI_D3N
15	MIPI_CSI_D3P
16	GND
17	CAM_PWDNB
18	CAM_CLK
19	GND
20	CAM_I2C_SCL
21	CAM_I2C_SDA
22	VSYNC
23	CAM_RESETB
24	3V3

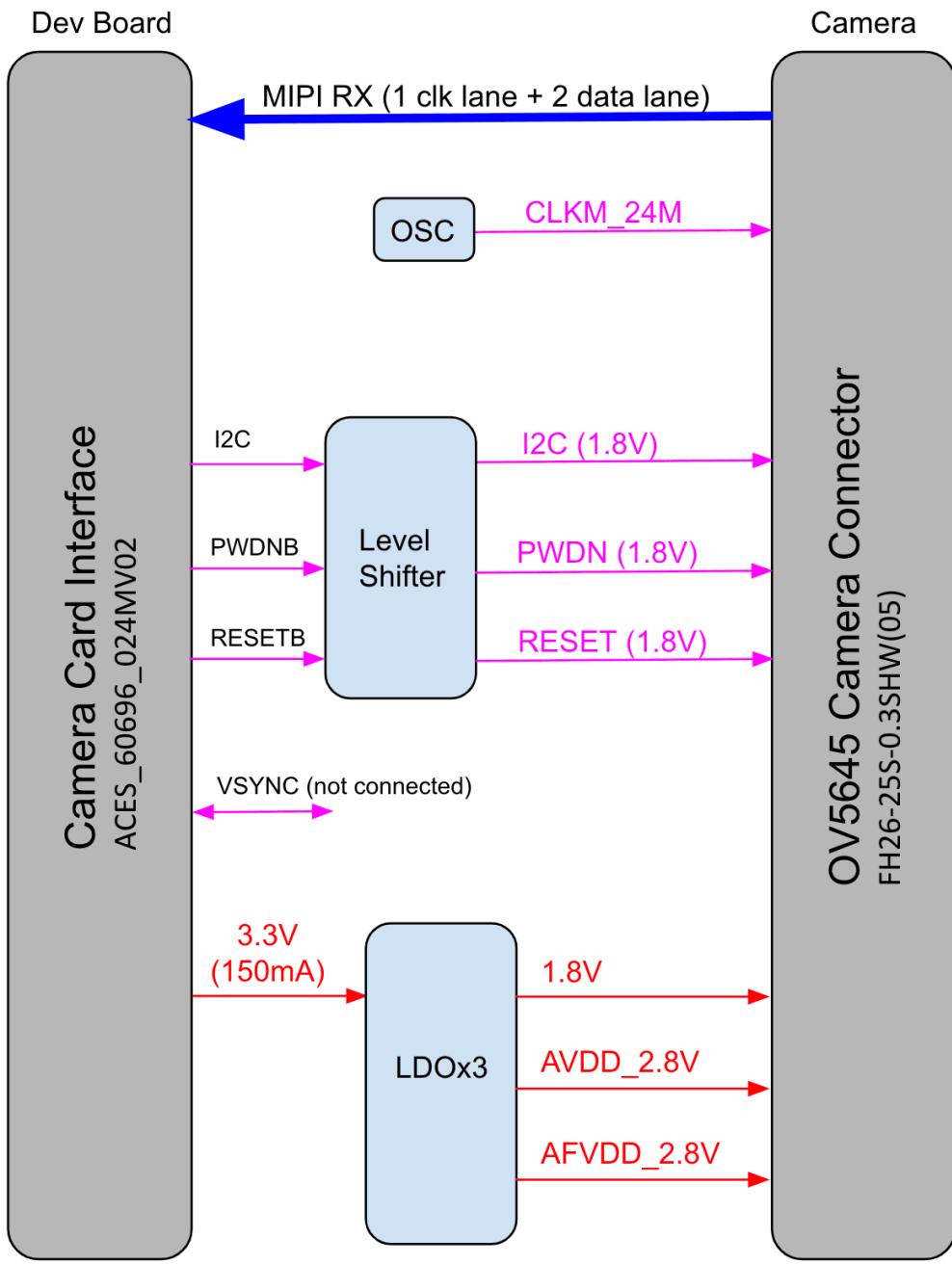


Figure 7. Camera adapter card diagram

# Power specifications

The Coral Dev Board must be powered by 2 - 3A at 5V DC using the USB Type-C power port (see figure 4).

**Caution:** Do not attempt to power the board by connecting it to your computer.

The SOM has one primary PMIC (BD71837MWV) from Rohm for the iMX8M SOC complex, LPDDR4, eMMC, and Wi-Fi/Bluetooth. It integrates 8 DC-DC buck regulators and 7 LDOs to provide all power rails required by iMX8M SOC and commonly used peripherals. It uses QFN package and pinout support low cost Type 3 (non-HDI) PCB. Programmable power sequencing and output voltages and flexible power state control ease system design.

There is a secondary PMIC ISL91301B exclusively for the Edge TPU ASIC.

## Boot mode

The baseboard includes 4 switches (indicated in figure 8) to control the boot mode. By default, they are set to boot from eMMC. You can change the boot mode as follows.

Boot mode	Switch 1	Switch 2	Switch 3	Switch 4
Serial download	Off	On	[Don't care]	[Don't care]
eMMC	On	Off	Off	Off
SD card	On	Off	On	On

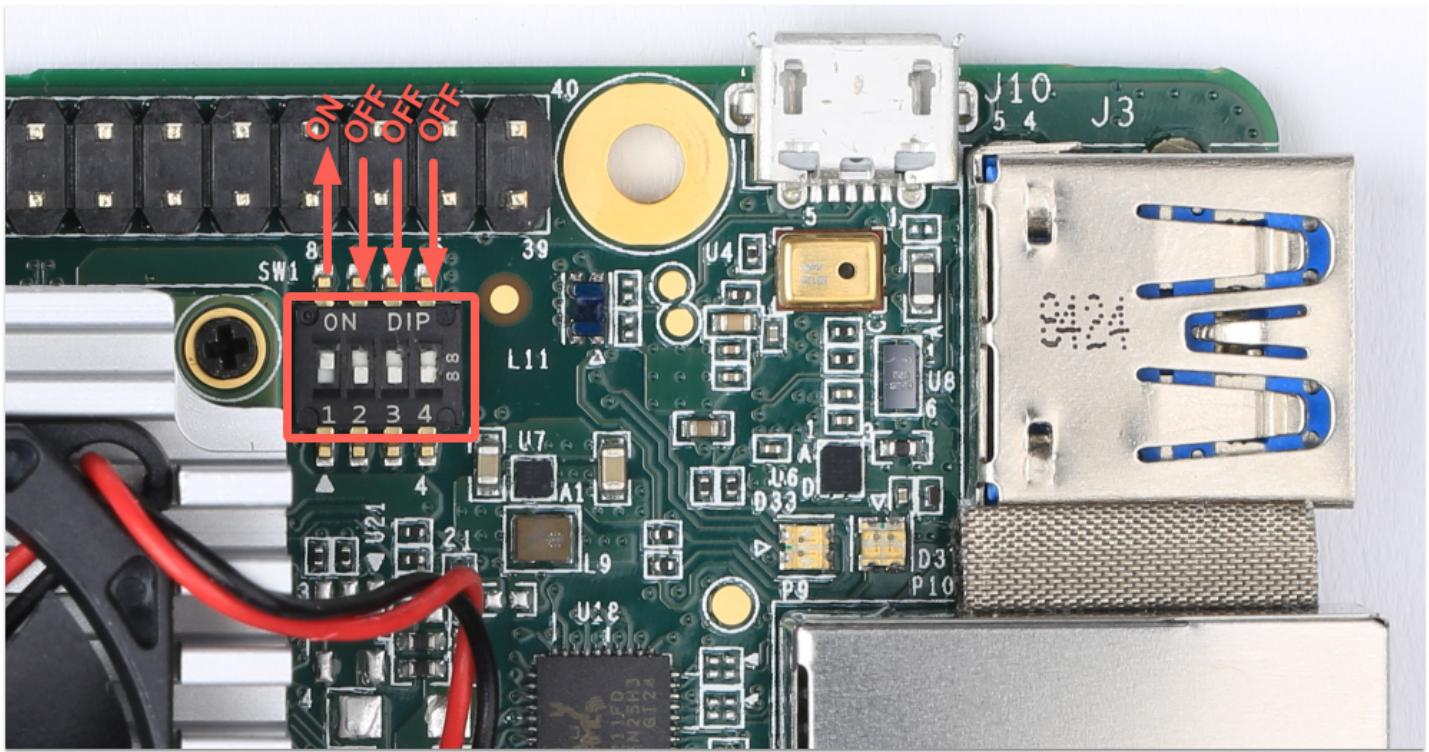


Figure 8. Boot mode switches, set to boot from eMMC

## System reset

You can restart the system with the RESET button shown in figure 9.

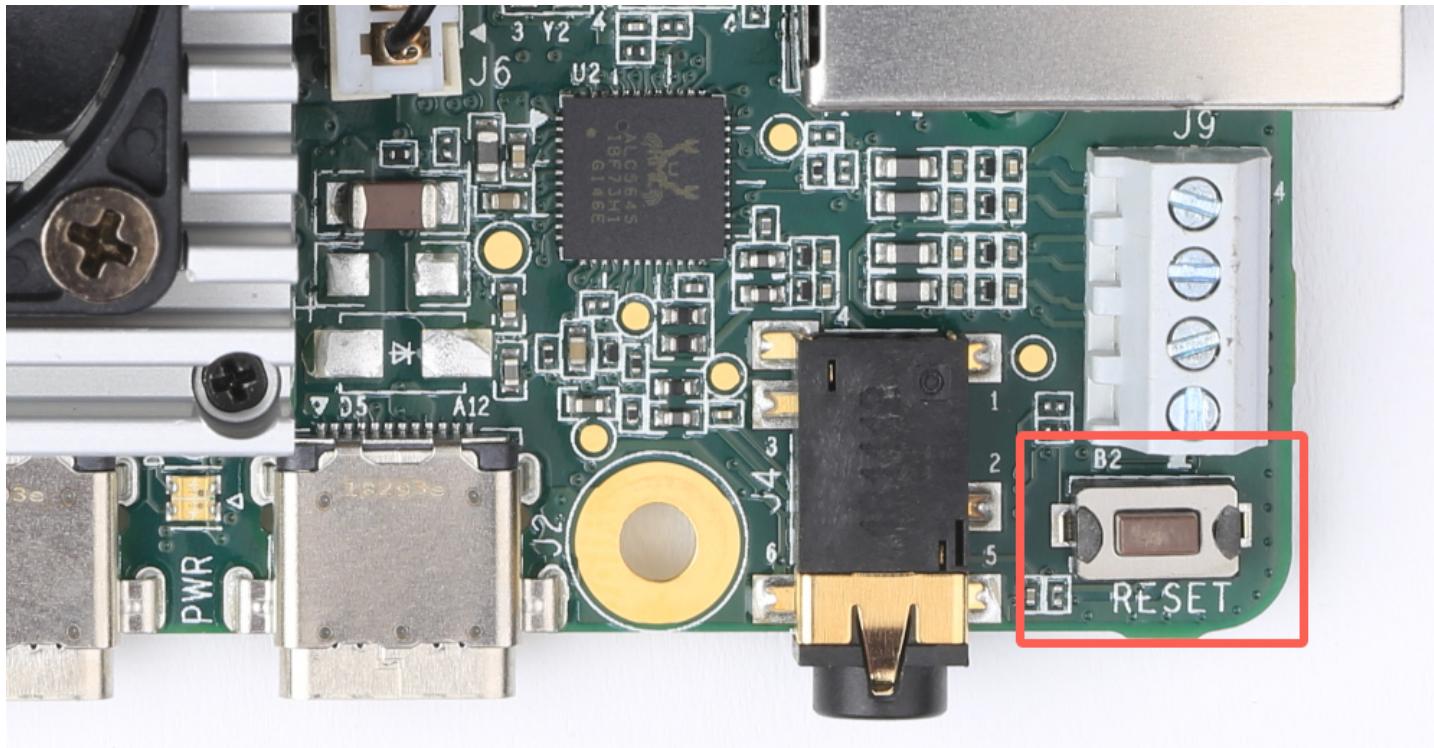


Figure 9. System reset button

# SOM hardware details

**Note:** This datasheet does not provide complete details on the SOM. The following information is primarily a look at the board-to-board connectors for those interested in using the SOM with custom PCB hardware. A more detailed SOM datasheet is available upon request.

The SOM is based on NXP's iMX8M system-on-chip (SOC) and contains all the essential hardware systems, including the Edge TPU and Wi-Fi/Bluetooth radios. It is attached to the Dev Board baseboard with three 100-pin board-to-board connectors.

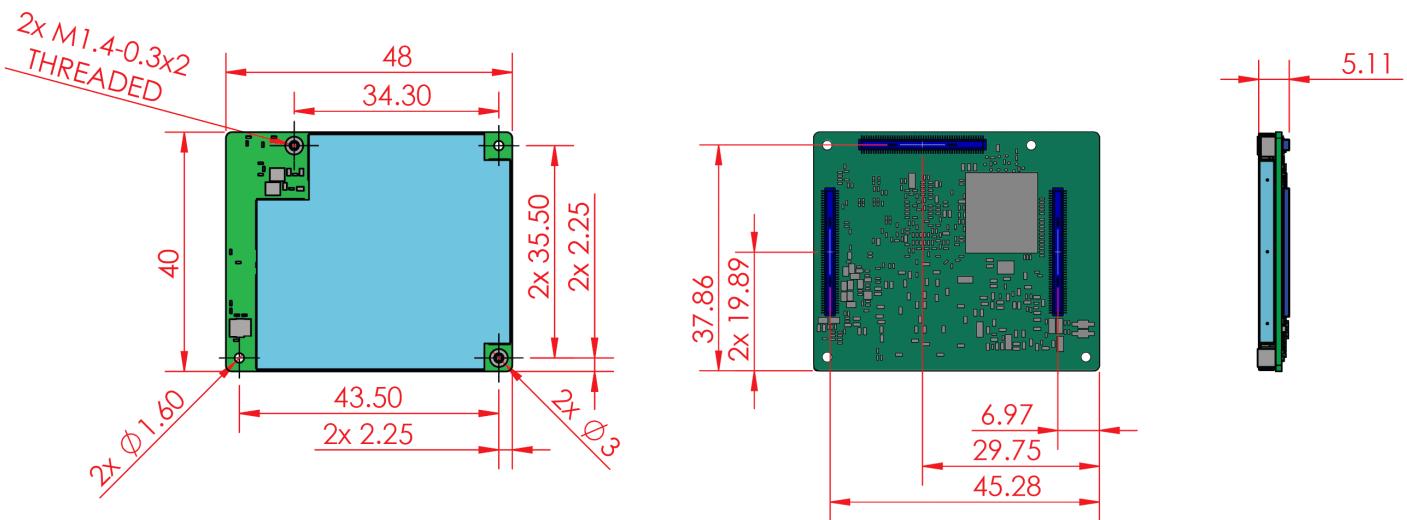


Figure 10. Edge TPU SOM dimensions without the fan

## Board to board connectors

The Edge TPU SOM connects to the host baseboard with three 100-pin connectors, as shown in figure 1.

These are Hirose Electric 100-position connector plugs (DF40C-100DP-0.4V(51)). They connect to the corresponding 100-position connector receptacles (DF40HC(3.0)-100DS-0.4V(51)) on the baseboard.

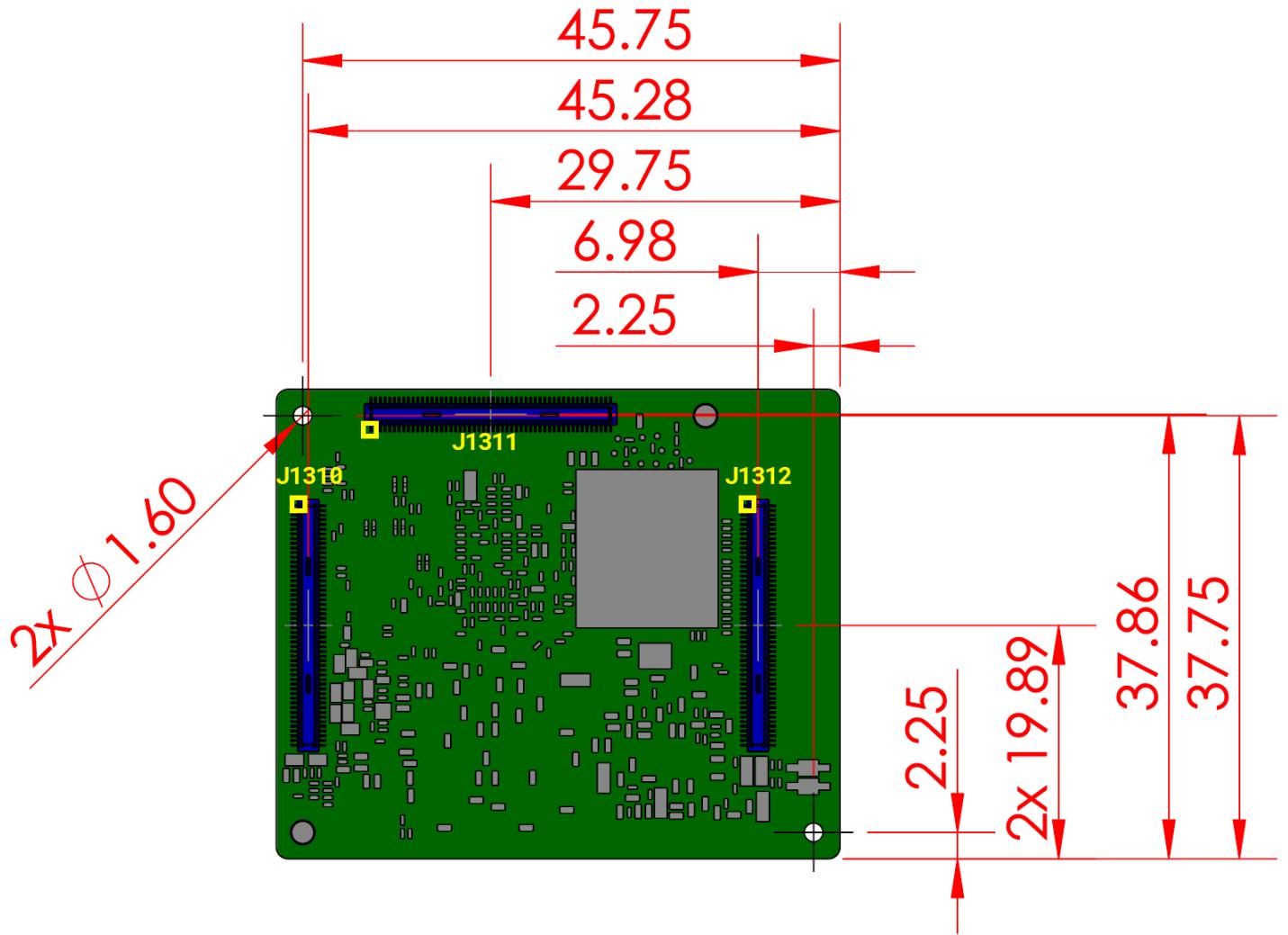


Figure 11. Module bottom with connector locations (in millimeters), the position for pin 1 on each connector is indicated with a yellow square

# Pinout schematic

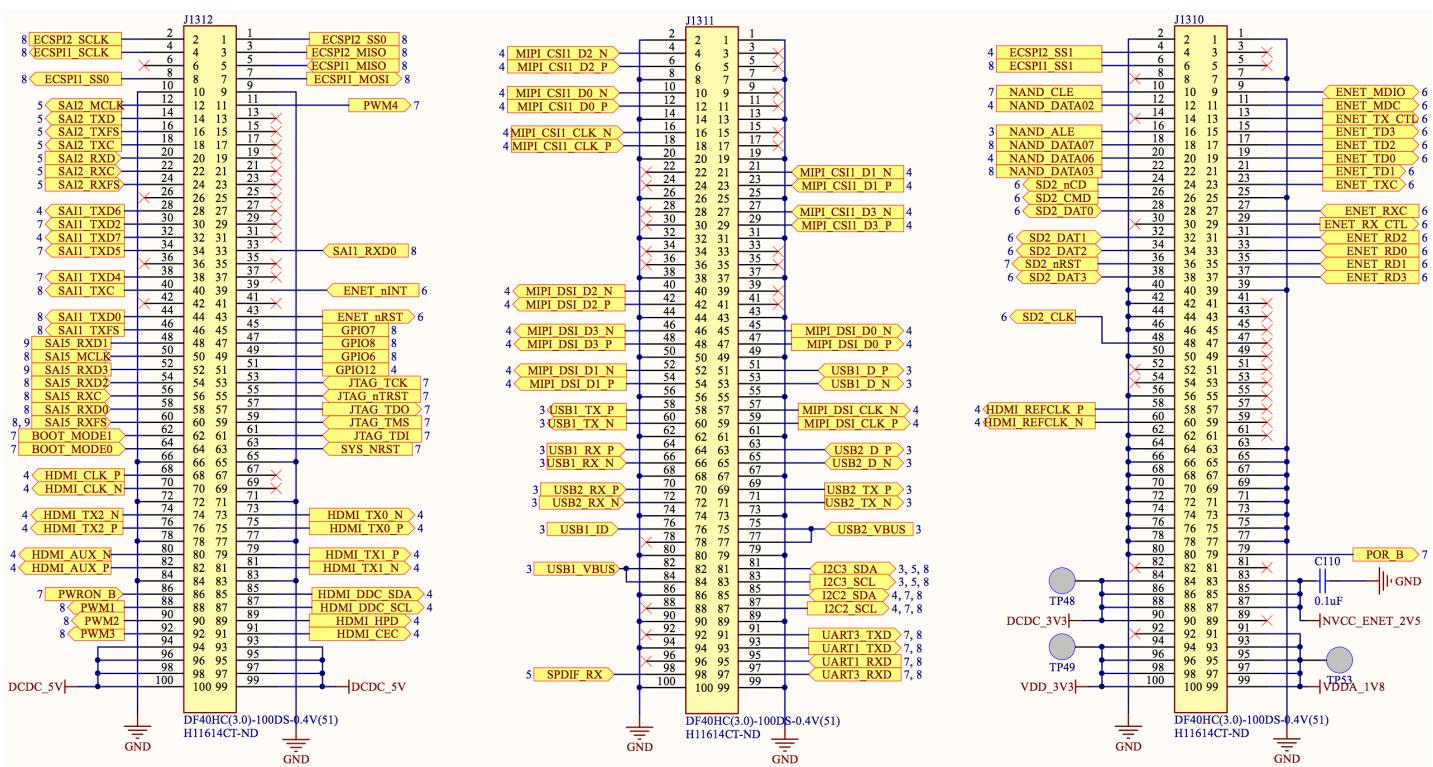


Figure 12. SOM board-to-board connector pinout

## Pinout by function

Signal Name	Direction (for SOM)	Source	Destination	Connector	Pins	Voltage	Description
<b>Power</b>							
VSYS_5V	IN	BaseBoard	PMIC	J1312	93, 94, 95, 96, 97, 98, 99, 100	5V	Main 5V Power source to SOM.
DCDC_3V3	OUT	PMIC/LDO1	N.C.	J1310	84, 86, 88, 90	3.3	Not used.
VDD_3V3	OUT	PMIC/SW6	Baseboard/PHY	J1310	94, 96, 98 100	3.3	Used for GPIO/pull-up for 3.3V rail.
VDDA_1V8	OUT	PMIC/LDO3	U12	J1310	91, 93, 95, 97, 99	1.8	Used for power-sequence BB_3V3.
NVCC_ENET_2V5	IN	Ethernet PHY	IMX8M SOC	J1310	83, 85, 87	2.5V	
<b>Ground</b>							
GND	IN			J1312	9, 10, 65, 66, 71, 72, 77, 78, 83, 84		

Signal Name	Direction (for SOM)	Source	Destination	Connector	Pins	Voltage	Description
GND	IN			J1311	1, 2, 7, 8, 13, 14, 19, 20, 25, 26, 31, 33, 37, 38, 43, 44, 49, 50, 55, 56, 61, 62, 67, 68, 73, 74, 79, 80, 86, 89, 90, 94, 99, 199		
GND	IN			J1310	1, 2, 7, 25, 39, 40, 42, 44, 45, 46, 50, 51, 56, 57, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 80		
<b>MIPI_CSI1</b>							
MIPI_CSI1_CLK_P/N	IN	Camera Interface	iMX8M.CSI1	J1311	18/16	0.2-1.2V	MIPI CSI1
MIPI_CSI1_D0_P/N	IN	Camera Interface	iMX8M.CSI1	J1311	12/10	0.2-1.2V	MIPI CSI1
MIPI_CSI1_D1_P/N	IN	Camera Interface	iMX8M.CSI1	J1311	23/21	0.2-1.2V	MIPI CSI1
MIPI_CSI1_D2_P/N	IN	Camera Interface	iMX8M.CSI1	J1311	6/4	0.2-1.2V	MIPI CSI1
MIPI_CSI1_D3_P/N	IN	Camera Interface	iMX8M.CSI1	J1311	29/27	0.2-1.2V	MIPI CSI1
<b>MIPI_CSI2</b>							
MIPI_CSI2_CLK_P/N	IN	NC	iMX8M.CSI2	J1311	36/34	0.2-1.2V	MIPI CSI2
MIPI_CSI2_D0_P/N	IN	NC	iMX8M.CSI2	J1311	35/33	0.2-1.2V	MIPI CSI2
MIPI_CSI2_D1_P/N	IN	NC	iMX8M.CSI2	J1311	30/28	0.2-1.2V	MIPI CSI2
MIPI_CSI2_D2_P/N	IN	NC	iMX8M.CSI2	J1311	24/22	0.2-1.2V	MIPI CSI2
MIPI_CSI2_D3_P/N	IN	NC	iMX8M.CSI2	J1311	41/39	0.2-1.2V	MIPI CSI2
<b>MIPI_DSI</b>							
MIPI_DSI1_CLK_P/N	OUT	iMX8M.DSI	Display Interface	J1311	59/57	0.2-1.2V	MIPI DSI
MIPI_DSI1_D0_P/N	OUT	iMX8M.DSI	Display Interface	J1311	47/45	0.2-1.2V	MIPI DSI
MIPI_DSI1_D1_P/N	OUT	iMX8M.DSI	Display Interface	J1311	54/52	0.2-1.2V	MIPI DSI
MIPI_DSI1_D2_P/N	OUT	iMX8M.DSI	Display Interface	J1311	42/30	0.2-1.2V	MIPI DSI
MIPI_DSI1_D3_P/N	OUT	iMX8M.DSI	Display Interface	J1311	48/46	0.2-1.2V	MIPI DSI
<b>HDMI</b>							
HDMI_REFCLKP/N	OUT	iMX8M.HDMI	HDMI Connector	J1310	58/60	3.3V	HDMI reference clock (27Mhz)
HDMI_CLKP/N	OUT	iMX8M.HDMI	HDMI Connector	J1312	68/70	3.3V	HDMI CLK
HDMI_TX0_P/N	OUT	iMX8M.HDMI	HDMI Connector	J1312	75/73	3.3V	HDMI TX0
HDMI_TX1_P/N	OUT	iMX8M.HDMI	HDMI Connector	J1312	81/79	3.3V	HDMI TX1
HDMI_TX2_P/N	OUT	iMX8M.HDMI	HDMI Connector	J1312	76/74	3.3V	HDMI TX2

Signal Name	Direction (for SOM)	Source	Destination	Connector	Pins	Voltage	Description
HDMI_AUX_P/N	OUT	iMX8M.HDMI	HDMI Connector	J1312	82/80	3.3V	HDMI AUX
HDMI_HPD	OUT	iMX8M.HDMI	HDMI Connector	J1312	89	3.3V	HDMI HPD
HDMI_DDC_SDA	OUT	iMX8M.HDMI	HDMI Connector	J1312	85	3.3V	HDMI DDC_SDA
HDMI_DDC_SCL	OUT	iMX8M.HDMI	HDMI Connector	J1312	87	3.3V	HDMI DDC_SCL
HDMI_CEC	OUT	iMX8M.HDMI	HDMI Connector	J1312	91	3.3V	HDMI CEC
<b>Ethernet/RGMII</b>							
ENET_RDO	IN	PHY on Base	iMX8M.ENET	J1310	33	1.8V	Ethernet RGMII RD
ENET_RD1	IN	PHY on Base	iMX8M.ENET	J1310	35	1.8V	Ethernet RGMII RD
ENET_RD2	IN	PHY on Base	iMX8M.ENET	J1310	31	1.8V	Ethernet RGMII RD
ENET_RD3	IN	PHY on Base	iMX8M.ENET	J1310	37	1.8V	Ethernet RGMII RD
ENET_RD_CTL	IN	PHY on Base	iMX8M.ENET	J1310	29	1.8V	Ethernet RGMII RD
ENET_RXC	IN	PHY on Base	iMX8M.ENET	J1310	27	1.8V	Ethernet RGMII RD
ENET_TD0	OUT	iMX8M.ENET	PHY on Base	J1310	19	1.8V	Ethernet RGMII TD
ENET_TD1	OUT	iMX8M.ENET	PHY on Base	J1310	21	1.8V	Ethernet RGMII TD
ENET_TD2	OUT	iMX8M.ENET	PHY on Base	J1310	17	1.8V	Ethernet RGMII TD
ENET_TD3	OUT	iMX8M.ENET	PHY on Base	J1310	15	1.8V	Ethernet RGMII TD
ENET_TD_CTL	OUT	iMX8M.ENET	PHY on Base	J1310	13	1.8V	Ethernet RGMII TD
ENET_TXC	OUT	iMX8M.ENET	PHY on Base	J1310	23	1.8V	Ethernet RGMII TD
ENET_MDC	OUT	iMX8M.ENET	PHY on Base	J1310	11	1.8V	Ethernet RGMII MDIO CLK
ENET_MDIO	OUT	iMX8M.ENET	PHY on Base	J1310	9	1.8V	Ethernet RGMII MDIO DATA
ENET_nRST	OUT	iMX8M.GPIO	PHY on Base	J1312	43	3.3V	Ethernet PHJY Reset
ENET_nINT	IN	PHY on Base	iMX8M.GPIO	J1312	39	3.3V	Ethernet PHY Interrupt
ENET_WoL	IN	PHY on Base	iMX8M.GPIO	J1312	41	3.3V	Ethernet PHY Wake-On-Lan

Signal Name	Direction (for SOM)	Source	Destination	Connector	Pins	Voltage	Description
CLKO_25M	OUT	iMX8M.GPIO_IO15	PHY on Base	J1310	54	3.3V	Reserved
<b>PCIe</b>							
PCIE1_REF_CLKP/N	OUT	iMX8M.CLK2	M2.KeyE	J1310	53/55	1.8V	PCIe-1 reference Clock from SOM to Baseboard
PCIE1_TXP/N	OUT	iMX8M.PCIE1	M2.KeyE	J1310	43/41	1.8V	PCIe-1 TX
PCIE1_RXP/N	IN	M2.KeyE	iMX8M.PCIE1	J1310	47/49	1.8V	PCIe-1 RX
PCIE1_nRST	IN	M2.KeyE	iMX8M.GPIO	J1310	59	3.3V	PCIe-1 RESET
PCIE1_nWAKE	IN	M2.KeyE	iMX8M.GPIO	J1310	61	3.3V	PCIe-1 Wake
PCIE1_nCLKREQ(I2C4_SCL)	OUT	iMX8M.GPIO	M2.KeyE			3.3V	Not connected to B2B connector.
PCIE2_REF_CLKP/N	OUT	Clock Source U1711	M2.KeyE	J1311	5/3	1.8V	PCIe-2 reference Clock from SOM to Baseboard
PCIE2_TXP/N	OUT	iMX8M.PCIE2	M2.KeyE	J1311	15/17	1.8V	PCIe-2 TX
PCIE2_RXP/N	IN	M2.KeyE	iMX8M.PCIE2	J1311	9/11	1.8V	PCIe-2 RX
PCIE2_nRST	IN	M2.KeyE	iMX8M.GPIO	J1310	3	3.3V	PCIe-2 RESET
PCIE2_nWAKE	IN	M2.KeyE	iMX8M.GPIO	J1310	5	3.3V	PCIe-2 Wake
PCIE2_nCLKREQ(I2C4_SDA)	OUT	iMX8M.GPIO	M2.KeyE	J1311	78	3.3V	PCIe-2 Clock Request
<b>USB</b>							
USB1_DP/N	In/Out	iMX8M.USB1	TypeC USB	J1311	51/53	3.3V	USB Port 1, USB2.0
USB1_TXP/N	OUT	iMX8M.USB1	TypeC USB	J1311	58/60	1.8V	USB Port 1, USB 3.0 TX
USB1_RXP/N	IN	TypeC USB	iMX8M.USB1	J1311	64/66	1.8V	USB Port 1, USB 3.0 RX
USB1_VBUS	IN	TypeC USB	iMX8M.USB1	J1311	82/84	5V	USB Port 1, VBUS detect
USB1_ID	IN	TypeC USB	iMX8M.USB1	J1311	76	3.3V	USB Port 1, USB ID
USB2_DP/N	In/Out	iMX8M.USB2	TypeA USB	J1311	63/65	3.3V	USB Port 2, USB2.0
USB2_TXP/N	OUT	iMX8M.USB2	TypeA USB	J1311	69/71	1.8V	USB Port 2, USB 3.0 TX
USB2_RXP/N	IN	TypeA USB	iMX8M.USB2	J1311	79/72	1.8V	USB Port 2, USB 3.0 RX

Signal Name	Direction (for SOM)	Source	Destination	Connector	Pins	Voltage	Description
USB2_VBUS	IN	TypeA USB	iMX8M.USB2	J1311	75/77	5V	USB Port 2, VBUS detect
USB2_ID	IN	TypeA USB	iMX8M.USB2	J1311	88	3.3V	USB Port 2, USB ID
Audio							
SAI2_TXD	OUT	iMX8M.SAI2	Codec on Baseboard	J1312	14	3,3V	SAI2
SAI2_RXD	IN	Codec on Base	iMX8M.SAI2	J1312	20	3,3V	SAI2
SAI2_TXC	OUT	iMX8M.SAI2	Codec on Base	J1312	18	3,3V	SAI2
SAI2_TXFS	OUT	iMX8M.SAI2	Codec on Base	J1312	16	3,3V	SAI2
SAI2_MCLK	OUT	iMX8M.SAI2	Codec on Base	J1312	12	3,3V	SAI2
SAI2_RXFS	IN	Codec on Base	iMX8M.SAI2	J1312	24	3,3V	SAI2
SAI2_RXC	IN	Codec on Base	iMX8M.SAI2	J1312	23	3,3V	SAI2
SAI1_MCLK	OUT	Reserved		J1312	26	3,3V	Reserved
SAI1_RXC	OUT	Reserved		J1312	17	3,3V	Reserved
SAI1_RXFS	OUT	Reserved		J1312	19	3,3V	Reserved
SAI1_RXD0	OUT	40-pin Header J15	IMX8M	J1312	33	3,3V	40-pin header for Audio: SAI1_RXD0
SAI1_RXD1	OUT	Reserved		J1312	35	3,3V	Reserved
SAI1_RXD2	OUT	Reserved		J1312	27	3,3V	Reserved
SAI1_RXD3	OUT	Reserved		J1312	31	3,3V	Reserved
SAI1_RXD4	OUT	Reserved		J1312	29	3,3V	Reserved
SAI1_RXD5	OUT	Reserved		J1312	21	3,3V	Reserved
SAI1_RXD6	OUT	Reserved		J1312	25	3,3V	Reserved
SAI1_RXD7	OUT	Reserved		J1312	23	3,3V	Reserved
SAI1_TXC	OUT	IMX8M	40-pin Header J15	J1312	40	3,3V	40-pin header for Audio: SAI1_TXC
SAI1_TXFS	OUT	IMX8M	40-pin Header J15	J1312	46	3,3V	40-pin header for Audio: SAI1_TXFS
SAI1_RXD0	OUT	IMX8M	40-pin Header J15	J1312	44	3,3V	40-pin header for Audio: SAI1_TxD0
SAI1_TxD1	I/O	Reserved		J1312	42	3,3V	

Signal Name	Direction (for SOM)	Source	Destination	Connector	Pins	Voltage	Description
SAI1_TXD2	OUT	Bit Switch SW1	iMX8M	J1312	30	3,3V	GPIO as BOOT_CFG10
SAI1_TXD3	IN	Reserved		J1312	36	3,3V	Reserved
SAI1_TXD4	IN	Bit Switch SW1	iMX8M	J1312	38	3,3V	GPIO as BOOT_CFG12
SAI1_TXD5	IN	Bit Switch SW1	iMX8M	J1312	34	3,3V	GPIO as BOOT_CFG13
SAI1_TXD6	OUT	iMX8M	Display Interface	J1312	28	3,3V	GPIO as DS1_TE for Display Interface
SAI1_TXD7	OUT	iMX8M	Display Interface	J1312	32	3,3V	GPIO as DS1_RESETB for Display Interface
SAI5_MCLK	IN	Baseboard pin-strap	iMX8M.SAI5	J1312	50	3,3V	GPIO: Base_Board_ID_0
SAI5_RXC	IN	Baseboard pin-strap	iMX8M.SAI5	J1312	56	3,3V	GPIO: Base_Board_ID_2
SAI5_RXD0	IN	Baseboard pin-strap	iMX8M.SAI5	J1312	58	3,3V	GPIO: Base_Board_ID_3
SAI5_RXD1	IN	SOM pin-strap	iMX8M.SAI5	J1312	48	3,3V	GPIO: SOM_Board_ID_0
SAI5_RXD2	IN	Baseboard pin-strap	iMX8M.SAI5	J1312	54	3,3V	GPIO: Base_Board_ID_1
SAI5_RXD3	IN	SOM pin-strap	iMX8M.SAI5	J1312	52	3,3V	GPIO: SOM_Board_ID_1
SAI5_RXFS	IN	SOM pin-strap	iMX8M.SAI5	J1312	60	3,3V	GPIO: SOM_Board_ID_2
SAI3_RXC		Reserved		J1312	13	3,3V	Reserved
SAI3_RXFS		Reserved		J1312	15	3,3V	Reserved
SPDIF_EXT_CLK	OUT	Reserved		J1311	92		
SPDIF_TX	OUT	Reserved		J1311	96	3,3V	
SPDIF_RX	IN	Codec U2	iMX8M	J1311	98	3,3V	GPIO: Interrupt from Codec U2.
<b>SDCard</b>							
SD2_CLK	OUT	iMX8M.SD1	uSD Card Slot	J1310	48	3,3V	Micro-SD Slot Interface
SD2_CMD	OUT	iMX8M.SD1	uSD Card Slot	J1310	26	3,3V	Micro-SD Slot Interface
SD2_nCD	OUT	iMX8M.SD1	uSD Card Slot	J1310	24	3,3V	Micro-SD Slot Interface

Signal Name	Direction (for SOM)	Source	Destination	Connector	Pins	Voltage	Description
SD2_DAT0	IO	iMX8M.SD1	uSD Card Slot	J1310	28	3.3V	Micro-SD Slot Interface
SD2_DAT1	IO	iMX8M.SD1	uSD Card Slot	J1310	32	3.3V	Micro-SD Slot Interface
SD2_DAT2	IO	iMX8M.SD1	uSD Card Slot	J1310	34	3.3V	Micro-SD Slot Interface
SD2_DAT3	IO	iMX8M.SD1	uSD Card Slot	J1310	38	3.3V	Micro-SD Slot Interface
SD2_nRST	OUT	iMX8M.SD1	uSD Card Slot	J1310	36	3.3V	Micro-SD Slot Interface
SDIO_WAKE	OUT	iMX8M.SD1	uSD Card Slot	J1310	30	3.3V	Micro-SD Slot Interface
<b>NAND</b>							
NAND_CE2_B	IO	Reserved		J1310	8	3.3V	Reserved
NAND_CLE	OUT	IMX8M	Fan Control	J1310	10	3.3V	GPIO: Fan Control: On/Off
NAND_DATA02	OUT	IMX8M	Cam Interface	J1310	12	3.3V	GPIO: CAM1_PWDN
NAND_CE0_B	IO	Reserved		J1310	14	3.3V	Reserved
NAND_ALE	IN	IMX8M	CC Controller U9	J1310	16	3.3V	GPIO: Interrupt from CC Controller U9
NAND_DATA07	IO	IMX8M	40-pin Header J15	J1310	18	3.3V	GPIO: GPIO_P37 at 40-pin header
NAND_DATA06	IN	Display Interface	IMX8M	J1310	20	3.3V	GPIO: DSL_TS_nINT from Display Interface
NAND_DATA03	IO	IMX8M	40-pin Header J15	J1310	22	3.3V	GPIO: GPIO_P16 at 40-pin header
<b>JTAG</b>							
JTAG_TMS	OUT	iMX8M.JTAG	J12	J1312	59	3.3V	JTAG for Debug use
JTAG_TDI	IN	iMX8M.JTAG	J12	J1312	61	3.3V	JTAG for Debug use
JTAG_TDO	OUT	iMX8M.JTAG	J12	J1312	57	3.3V	JTAG for Debug use
JTAG_TCK	OUT	iMX8M.JTAG	J12	J1312	53	3.3V	JTAG for Debug use
JTAG_nTRST	IN	iMX8M.JTAG	J12	J1312	55	3.3V	JTAG for Debug use

Signal Name	Direction (for SOM)	Source	Destination	Connector	Pins	Voltage	Description
<b>I2C</b>							
I2C2_SCL/SDA	In/Out	iMX8M.I2C2	Base: DSI/Audio/CSI1	J1311	87/85	3.3V	I2C Bus 2 from IMX8M
I2C3_SCL/SDA	In/Out	iMX8M.I2C3	Base: CSI2/PCIe.	J1311	83/81	3.3V	I2C Bus 3 from IMX8M
<b>UART</b>							
UART1_TXD	Out	iMX8M.UART1	40pin header	J1311	93	3.3V	UART1 from IMX8M
UART1_RXD	IN	40pin header	iMX8M.UART1	J1311	95	3.3V	UART1 from IMX8M
UART3_TXD	OUT	iMX8M.UART3	MicroUSB_Debug	J1311	91	3.3V	UART2 from IMX8M
UART3_RXD	IN	MicroUSB_Debug	iMX8M.UART3	J1311	97	3.3V	UART2 from IMX8M
<b>SPI</b>							
ECSPI1_MISO	IN	40pin header	iMX8M.SPI1	J1312	5	3.3V	SPI 1 Interface at 40 pin header
ECSPI1_MOSI	OUT	iMX8M.SPI1	40pin header	J1312	7	3.3V	SPI 1 Interface at 40 pin header
ECSPI1_SCLK	OUT	iMX8M.SPI1	40pin header	J1312	4	3.3V	SPI 1 Interface at 40 pin header
ECSPI1_SS0	OUT	iMX8M.SPI1	40pin header	J1312	8	3.3V	SPI 1 Interface at 40 pin header
ECSPI1_SS1	IO	iMX8M.SPI1	40pin header	J1310	6	3.3V	SPI 1 Interface at 40 pin header
ECSPI2_MISO	IN	40pin header	iMX8M.SPI2	J1312	3	3.3V	GPIO_P22 at 40 pin header
ECSPI2_MOSI	OUT	iMX8M.SPI2	Reserved	J1312	6	3.3V	Reserved
ECSPI2_SCLK	OUT	iMX8M.SPI2	40pin header	J1312	2	3.3V	GPIO_P18 at 40 pin header
ECSPI2_SS0	OUT	iMX8M.SPI2	40pin header	J1312	1	3.3V	GPIO_P36 at 40 pin header
ECSPI2_SS1	OUT	iMX8M.SPI2	Display Interface	J1310	4	3.3V	GPIO: GPIO as DSI_VSP_EN for Display Interface.
<b>GPIO</b>							
PWM1	OUT	iMX8M.GPIO1_IO01	40pin header	J1312	88		PWM1 at 40 pin header
PWM2	OUT	iMX8M.GPIO1_IO13	40pin header	J1312	90		PWM2 at 40 pin header

Signal Name	Direction (for SOM)	Source	Destination	Connector	Pins	Voltage	Description
PWM3	OUT	iMX8M.GPIO1_IO14	40pin header	J1312	92		PWM2 at 40 pin header
PWM4	OUT	iMX8M.SAI3_MCLK	40pin header	J1312	11		LED Status Control for LED D39
GPIO6	IO	iMX8M.GPIO1_IO06	40pin header	J1312	49		GPIO_P13 at 40 pin header
GPIO7	IO	iMX8M.GPIO1_IO07	40pin header	J1312	45		GPIO_P29 at 40 pin header
GPIO8	IO	iMX8M.GPIO1_IO08	40pin header	J1312	47		GPIO_P31 at 40 pin header
GPIO12	IO	iMX8M.GPIO1_IO12	CAM Interface	J1312	51		CAM_RESETB
<b>Misc</b>							
ONOFF	OUT	IMX8m.ONOFF	Reserved	J1310	52		Reserved
POR_B	IN	iMX8M.POR_B	Baseboard	J1310	79		Power_On_Reset from IMX8M
BOOT_MODE0	IN	Jumper	iMX8M.BOOT_MODE0	J1312	64		BOOTMODE0 from SW1
BOOT_MODE1	IN	Jumper	iMX8M.BOOT_MODE1	J1312	62		BOOTMODE0 from SW1
SYS_nRST	IN	Reset Button B2	PMIC	J1312	63		Power Reset from Reset Button B2
PWEON_B	IN	Reset Button B2	Reserved	J1312	86		Reserved
Spare				J1312	37,67,69		Reserved
Spare				J1310	81,82,89,92		

## Recommended operating conditions

To ensure reliable operation and performance, the board should operate in the following environment:

- Temperature: 0 - 50°C

## Thermal solution

To maintain functional heat levels the Dev Board includes a fan with the following specifications:

- Speed: 9k RPM

- Airflow: 138 LPM (4.9 CFM)
- Voltage: 5 V DC
- Power (peak): 0.65 W
- Static pressure: 42 Pa (0.17 in-H<sub>2</sub>O)

## Environmental and mechanical reliability tests

Test	Conditions	Verified
Temp cycling	Non-op, -40°C (LT) to 85°C (HT), 7 minute ramp, 23 minutes dwell, 60 minutes/cycle	200 cycles
Heat soak	Non-op, 85°C/85% RH	200 cycles
Audio jack cycling	50% manual plug/unplug, 50% uniaxial machine plug/ unplug	1000 cycles
HDMI cycling	Manual plug/unplug	100 cycles
MicroSD cycling	Manual plug/unplug	100 cycles
Vibration	3 axes (X, Y and Z), 15 minutes per axis, 10-500Hz. Amplitude: 2.16 Grms	45 minutes
USB-C connector cycling	Manual plug/unplug	1000 cycles
USB-A connector cycling	Manual plug/unplug	1000 cycles
Micro USB connector cycling	Manual plug/unplug	1000 cycles
Fan run life	40°C, 65% RH	70k hours

## Certifications

Market	Certifications
USA	FCC
European Union	CE