Traffic light controller using FPGA

FPGA Lab & IDP

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Why use FPGA?

- FPGA (Field Programmable Gate Array): This is an IC that contains an array of logic cells that can be programmed by user.
- FPGA has many advantages over microcontroller in speed, number of input and output ports & performance.
- FPGA is cheaper solution when compared to ASIC which is too costly and time consuming for small scale production
- In general, traffic lights on main roads are controlled with a fix-time control system which may lead to traffic congestions during rush hours
- VHDL is preferred especially for FPGA design because VHDL can be used to describe and simulate operation of ditial circuits

Objectives

- Transform word description of the protocol in to a Finite State Machine trasition diagram.
- Implement simple Finite State Machine using VHDL
- Simulate the operation of FSM
- Implement the design on to a FPGA

State Table

- The three lights (Green , Yellow , Red) cycle through the six states as shown in the table

State	North-South	East-West	Delay
0	Green	Red	5
1	Yellow	Red	1
2	Red	Red	1
3	Red	Green	5
4	Red	yellow	1
5	Red	Red	1

Table: Table showing different states and there corresponding delays

State Diagram

- If we use 3 Hz clock is used to drive this state diagram then a delay of one second is achieved by staying at one state for three clock seconds