EC 413

Lab 4 Write Up

Dabin Jang

1. 64 – bit Ripple Carry Adder

I used 4 \* 16 bit RCA to build 64 bit RCA. 16 bit RCA is made out of 4 \* 4 bit RCA and 4 bit RCA is mad out of 4 \* 1 bit full adders. Therefore, there are 64 full adders used to create a 64-bit RCA.

Graphical user interface

Description automatically generated

This is the result of the simulation of 64-bit RCA. I used 4 examples to test 64\_bit RCA. When all inputs are 0, a = 64’bF , b = 64’d1 (to create c\_out) and two random cases with and without c\_in. Everything worked properly.

The time delay for RCA was 128 ns. This is same as I expected. 1 full adder has 2 gate delay. Since we used 64 full adders, there is 128 ns gate delay.

1. 64-bit CSA

I used 3 \* 32 bit RCA and one 32 bit mux to create 64-bit CSA. One of the 32-bit RCA is to calculate from the least significant bit up to 31 and other two 32-bit RCA are to calculate the most significant 32-bit with and with c\_out. The values of c\_out will go into MUX as select input to choose which value will become the final output.

Graphical user interface

Description automatically generated with low confidence

I basically used the same examples for CSA. Every function of the system worked properly. The delay time for CSA is 64ns because three of the 32-bit RCA works concurrently. Therefore, the delay only takes as much as 32-bit RCA, 2\*16. It is same as I expected. I assumed that MUX has no gate delay. We used 32 more full adders to create CSA than to create RCA. Basically, used more space for efficiency.