EC 413

Lab 8 Write Up

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For this lab, most of the parts are already designed. What I had to modify was hazard unit to detect one ahead and two ahead. Therefore, I used this logic.

For one ahead hazard,

I expect hazard only when

1. Regwrite from control lines is 1 **and** (in execution stage)
2. Destination of the register of the instruction in execution stage is not equal to 0,
3. **and** one of the reading register numbers from next instruction matches with the #2 value, then there is one ahead hazard.

For Two Ahead Hazard,

I expect hazard only when

1. Regwrite from control lines is 1 **and** (in mem stage)
2. Destination of the register of the instruction in memory stage is not equal to 0,
3. **And** one of the reading register numbers from next instruction matches with the #2 value, then there is two ahead hazard.

Basically, for both hazards, the logic is the same. I just look at different stages to figure out either it’s one ahead or two ahead.

Simply adding this logic to hazard detection unit and wiring is all I have done for this lab.

Below is the result of the waveform. I used the given testbench.

A picture containing text, electronics, computer, screenshot

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