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Partial dynamic reconfiguration framework for FPGA: A survey with concepts, constraints and trends

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Highlights

- Partial reconfiguration is a design process, which allows a limited, predefined portion of an FPGA to be reconfigured while the remainder of the device continues to operate.
- Dynamic Partial Reconfiguration is a feature of modern FPGAs that allows runtime modification of an operating FPGA.
- Dynamic reconfiguration frameworks are high-performance reliable real time reconfigurable computing.
- FPGA framework is the agent system using dynamic partial reconfiguration.

- Dynamic reconfiguration frameworks are the supporting real-time applications on dynamic reconfigurable FPGAs.

Abstract

With demand for high performance and huge logic dense portable devices, the need for silicon area is increasing. A potential solution for the electronics industry to develop such huge logic demanding applications is the ability to reconfigure the system partially without altering the overall system operation. For more than two decades, reconfigurable computing has aided various applications and has seen tremendous technology transformation. The paper presents a survey of reconfigurable computing, its present state of existence, and a detailed report on state of art Partial Dynamic Reconfiguration Framework (PDRF) for reconfiguring FPGA designs partially and dynamically. A detailed analysis of the features, limitations, and performance of a wide range of PDRFs available in the literature are reported.

Introduction

Reconfigurable computing was first introduced [1], [2] during 1980 to accelerate the processing speed of General Purpose Processors (GPP). A GPP use generalized instruction set and hardware to execute a wide variety of algorithms with insignificant processing speed. Hence, a specialized Reconfigurable Hardware System (RHS) accelerator is complemented with GPP that can be customized by converting a part of the computation intensive code to hardware depending upon the task executed [3]. The RHS can be programmed to perform multiple tasks that can accelerate different portions of the software code running on a GPP. Depending on the code running on the GPP, one of multiple accelerators is programmed onto reconfigurable hardware. It usually takes an order of magnitude less time to evaluate a function when compared with the time required by assembly code executing on a GPP.

A RHS is divided into static region and dynamic region. Static region consists of primary functional unit of the system that doesn't need a reconfiguration and it continues to function even during reconfiguration. The region that can be reconfigured is Dynamic region / Dynamic Reconfiguration Region (DRR). Either static region or an external host

computer will control the reconfiguration process of DRR. The RHS is classified as either Coarse Grain RHS (CGRHS) or Fine Grain RHS (FGRHS) depending on the granularity of reconfigurable datapath used in DRR. DRR with datapath greater than 1-bit granularity are Course Grain DDR (CGDRR) [4]. CGDDR is mostly used along with a GPP as a hardware accelerator for a given application. A CGDDR consists of Programmable Functional Units (PFU) such as ALUs, Multipliers, Look-Up-Tables, Shifters, digital macro units etc connected as linear [5], [6], crossbar [7] or mesh arrays [8], [9] along with programmable routing.

The arrangement of these PFU depend on the data transfer network, type of reconfiguration used and the application for which it is designed for. Mesh based arrays are more efficient than the other two architectures as its 2D array structure supports better routing with 8 PFUs surrounding each PFU for efficient configuration and parallelism. The CGDDR provide efficient reconfiguration due to higher granularity of datapath, regular structures, less congestion routing, less complex placement and small configuration memory requirement.

While the CGDDR is efficient for reconfiguration, it offers less flexibility in altering the RHS to suit wide range of applications. The architecture of CGRHS is fixed before fabrication, while majority of FGRHS use Field Programmable Gate Array (FPGA) that provides a flexibility to alter DRR after fabrication also. The reconfiguration of CGRHS computer systems is done by dynamic alteration of interconnects through software control, variation of level of parallelism by dynamic resource partition and dynamic adaptation of instruction set architecture to support large variety of applications like digital signal processing, multimedia, software radio, wireless communications, general purpose loop acceleration etc. As the CGDRRs are mostly reconfigurable data paths and routes with hardwired CFB, the flexibility of these architectures to get adapted to other applications is less. Research in CGRHS is mainly focused on standard and distributed CGRHS structures. A standard CGRHS structure has a GPP as the primary processing unit and multiple DRRs supporting GPP while a distributed CGRHS structure has multiple DRRs without a GPP providing a high level of resource regularity and configuration generality. Any one of the DRRs can be configured and used as a primary GPP. Each PFU of either structure is interfaced with a configuration memory that holds configuration information for each different configuration. The structure of standard CGRHS and distributed CGRHS are shown in Fig. 1.

The configuration mapping framework of a RHS is dependent on the architecture, granularity, level of interconnect and selection of compiler. Compiler should be designed

for each different architectures. Higher the granularity less complicated is the mapping technology and routing algorithm.

Until the last decade, most of the designs were CGRHS owing to large routing overhead and huge resources required for routing configuration of FGRHS. However, multi-granular solutions are also developed to suit the application requirements. As the paper is mainly focused on the survey of research carried out on FGRHS using FPGA, the detailed discussion of CGRHS is beyond the scope of this paper. However few papers have contributed a detailed survey on CGRHS with substantial conclusions [4], [10], [11], [12]. The rest of the paper is organized as follows: FGRHS introduction is presented in Section II, basic information required to perform partial reconfiguration is detailed in Section III, and research work reported for the development of PDRF is surveyed in Section IV followed by discussions and conclusion in subsequent sections.

Section snippets

Fine grain reconfigurable hardware systems

Fine grain reconfiguration is a solution for high degree of flexibility to user. FGRHS use 1-bit granular Configurable Logic Block (CLB) as data path in DRR which can achieve vast functional transformation. The CGDDR are custom build for targeted application and therefore cannot be reused to suit a different application. But most of the early research is concentrated on CGRA due to high configuration overheads, low logic density and less support available for generic fine grain architectures …

Basics of partial reconfiguration

Current FPGA advancements support adaptation and upgradation of the design running on the FPGA without affecting the integrity of the entire system. Reconfiguration of entire FPGA is called as reconfiguration and reconfiguring a portion of FPGA is called Partial Reconfiguration. Each design reconfiguration needs to load bitstream into SRAM configuration memory that can configure all the programmable resources of FPGA like programmable interconnects, CLBs, DSP blocks, BRAM etc. A full …

Evolution of partial reconfiguration platforms

With the introduction of partial reconfiguration technology features into FPGAs, the research in reconfigurable computing have shifted from coarse grain to fine grain owing to the advantages of flexibility of adapting to any application, readily available platform to customize. These in-chip FGRHS were developed to support adaptive signal processing application, fault tolerant systems, software defined radio and other reconfigurable systems. Most of the research is concentrated on development …

Discussions on reconfiguration platforms

Though CGRHS are mainly used for GPP acceleration, FGRHS are being used for hardware acceleration [46], [47], run time design adaptability, evolvable hardware systems [34], [48], [49], fault tolerant designs [50], [51], hardware update and maintenance without suspending the system operation.

From the above reviewed systems and Table 2, it is evident that the RHS using embedded processor [30], [31], [33], [34], [36], [37], [45] couldn't achieve the theoretical throughput of ICAP port. This is due …

Conclusions

An overview of reconfigurable computing is presented, while describing the architectural evolution in CGRHS and FGRHS, with an emphasis on FGRHS and PDRF for FPGA. From the above discussions, it is observed that a good amount of work is done in improving reconfiguration throughput of a FGRHS. To use reconfiguration to all dimensions of applications, high flexibility in choosing the DRR and generating configuration data is essential while using reasonable physical resources in comparison with …

CRediT authorship contribution statement

T. Siva Sankar Phani: Investigation, Resources, Visualization. **Anitha Arumalla:** Conceptualization, Investigation, Resources, Data curation, Writing - original draft, Writing - review & editing, Supervision. **M. Du rga Prakash:** Conceptualization, Investigation, Resources, Writing - original draft, Writing - review & editing, Supervision. …

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper. …

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2024, Journal of Systems Architecture

> *Citation Excerpt :*
> ...In dynamic reconfiguration, the architecture can dynamically change the functionality on the fly during the operation. This capability allows adaptability to new operational requirements or optimization of resources at run-time [78]. However, this also results in high design complexity and reconfiguration overhead as compared to static reconfiguration....

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