

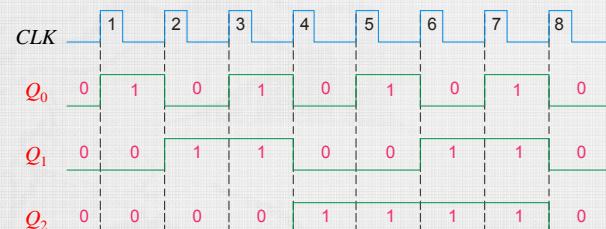
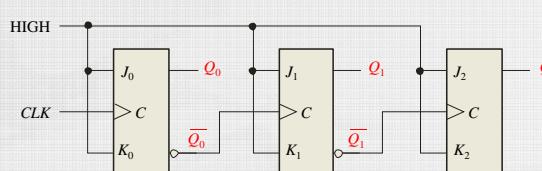
논리회로 및 설계

Chapter 8

일부 이미지 저작권:
Wikipedia, Creative Commons
Pearson Educations

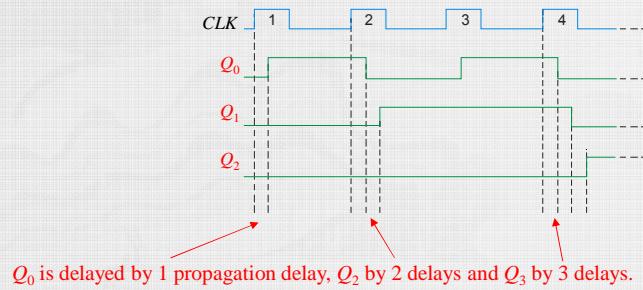
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Asynch. counter



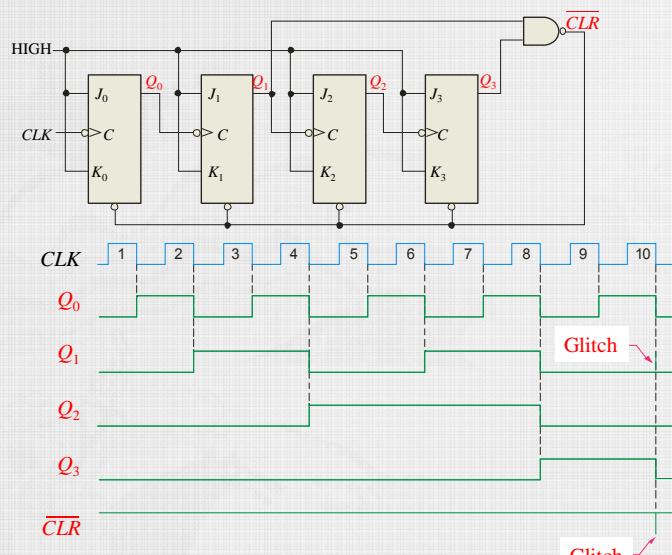
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Delay of Async. Counter



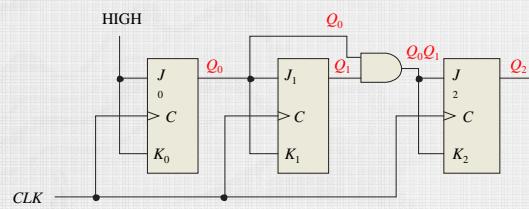
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Asynch. Decade Counter



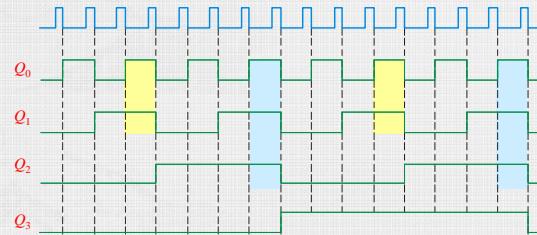
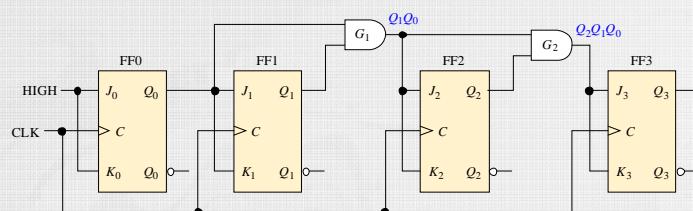
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Synch. Counter



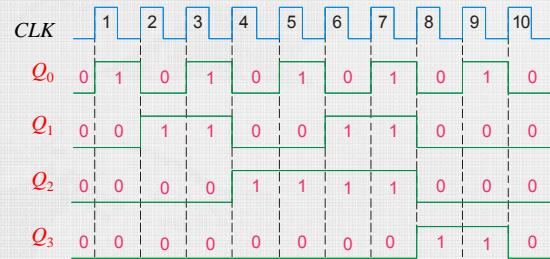
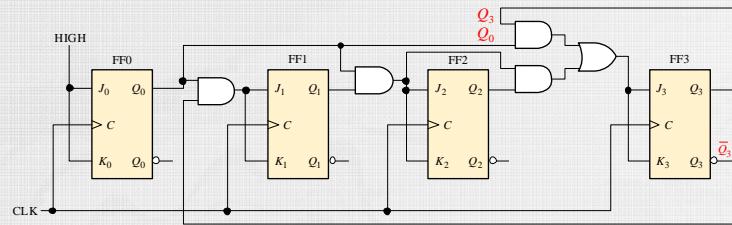
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4 Bit Synch Counter



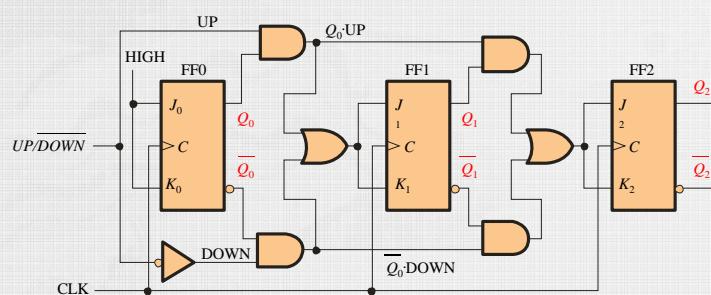
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Sync. BCD Decade Counter



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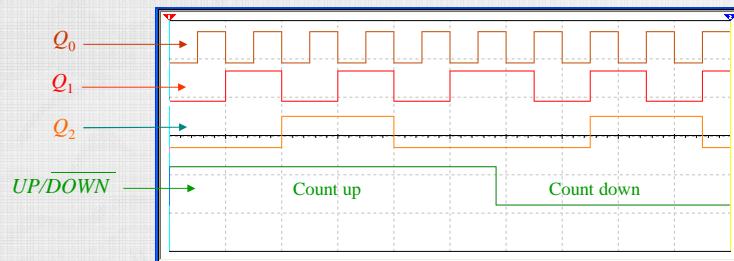
Up/Down Counter



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Summary

Up/Down Synchronous Counters



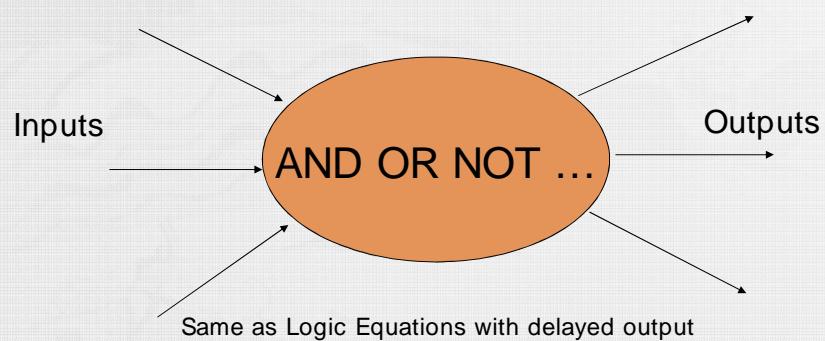
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State Machine

- Combinational Logic : Using Logic gates
- Synch. Sequential Logic : FF+Comb, with feedback

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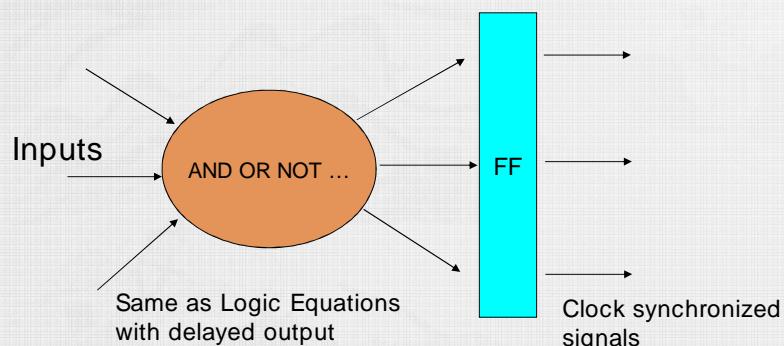
Combinational Logic



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Synchronizing

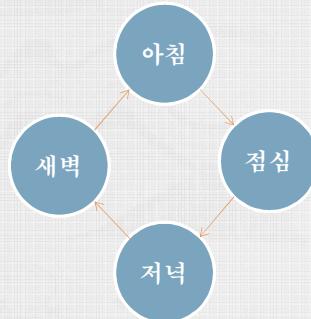
- Sync. Signals with clock



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State Machine

- Process steps from predefined steps

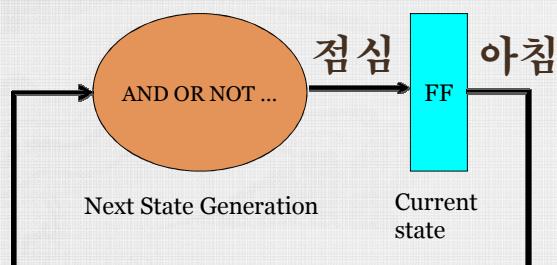


Simplest state machine

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State Machine

- Clock synchronized state machine

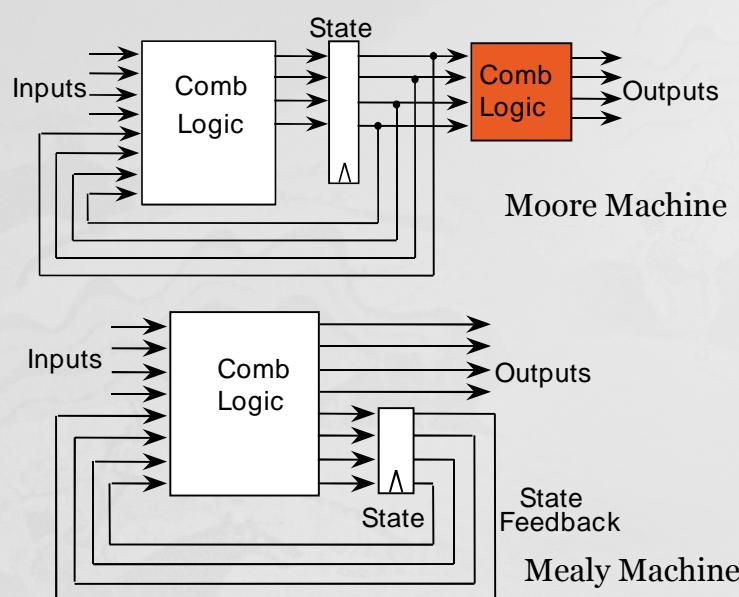


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State Machine

- Moore Machine
 - Outputs : Function of the current state
 - Outputs synchronized with state (and clock)
- Mealy Machine
 - Outputs : Function of the state & inputs
 - Output can change by input changes
 - Asynchronous outputs

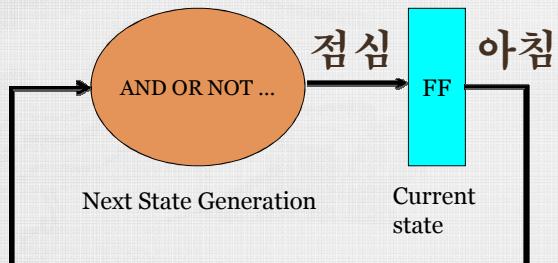
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State Machine

- Clock synchronized state machine



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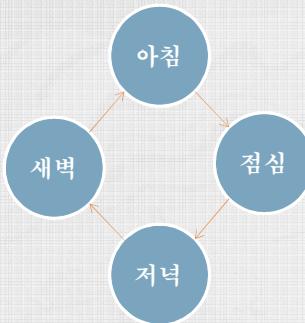
State Machine

- State : Stored values in the FF
- State mapping to the stored values
 - One bit hot encoding
 - Assign unique FF for each state
 - Binary encoding
 - Assign unique and sequential value for each state

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State Machine (one bit hot encoding)

- Assign each states to unique value



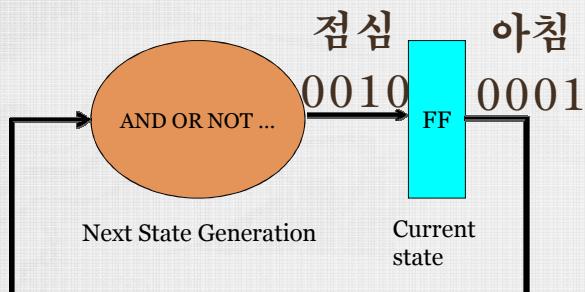
상태명	값(binary)
아침	0001
점심	0010
저녁	0100
새벽	1000

- 4 states : requires 4 FF (4 bits)
- N states : requires N FFs (N bits)

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State Machine (one bit hot encoding)

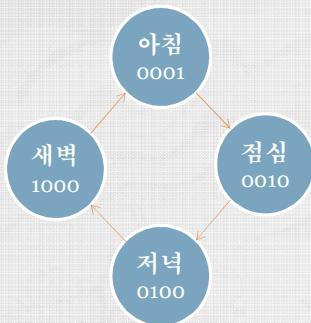
- Clock synchronized state machine



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State Machine (one bit hot encoding)

- Convert the state transition to a table



Current	Next
0001	0010
0010	0100
0100	1000
1000	0001

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State Machine (one bit hot encoding)

C ₃	C ₂	C ₁	C ₀	N ₃	N ₂	N ₁	N ₀
0	0	0	1	0	0	1	0
0	0	1	0	0	1	0	0
0	1	0	0	1	0	0	0
1	0	0	0	0	0	0	1

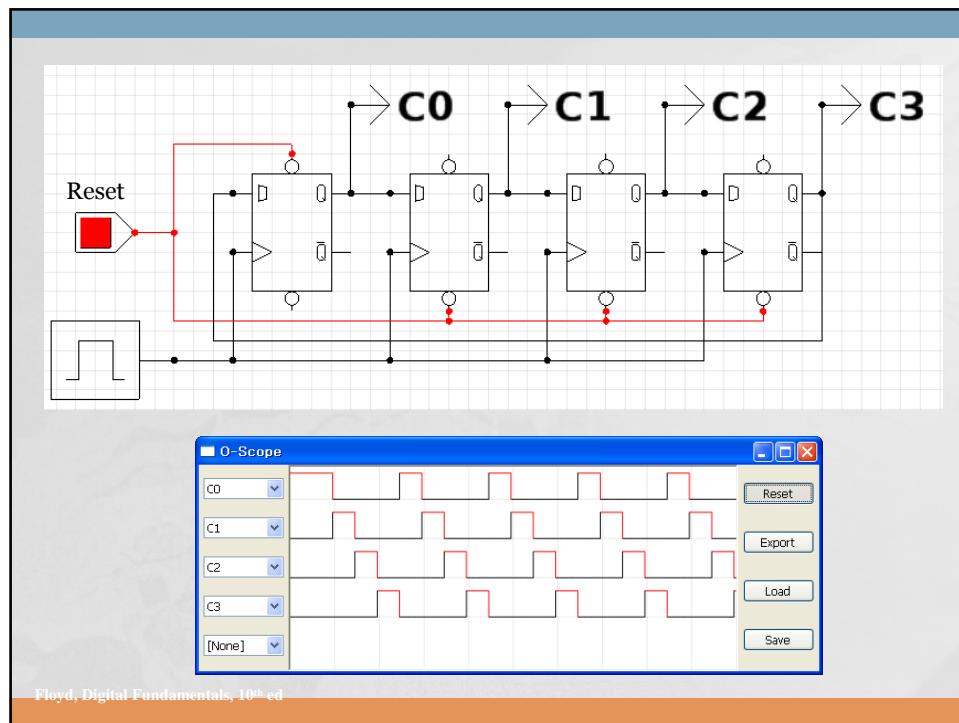
$$N_3 = C_2$$

$$N_2 = C_1$$

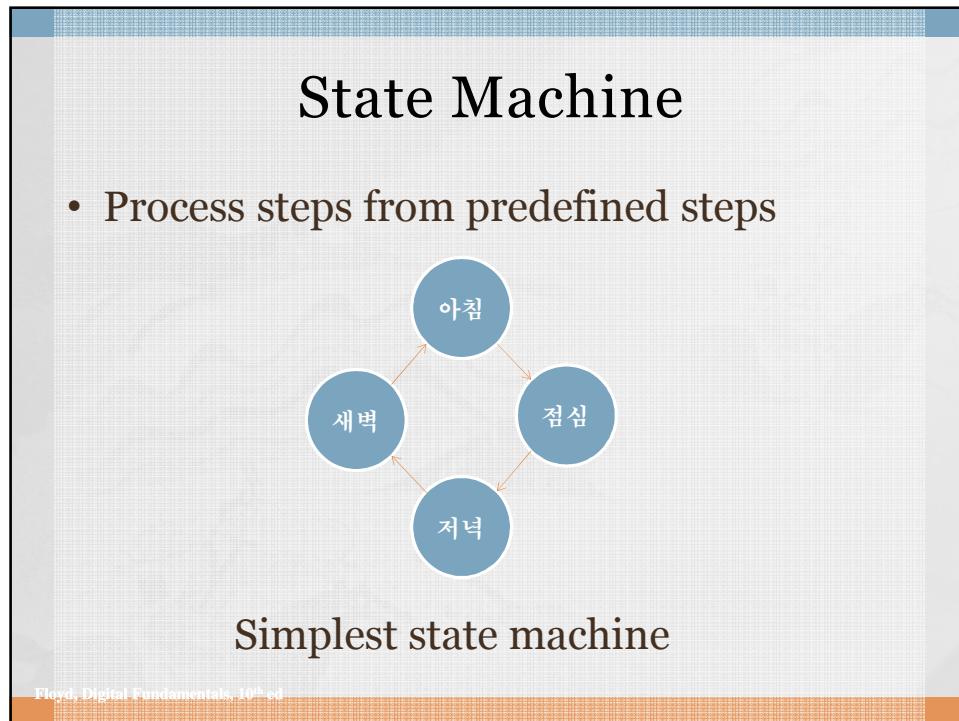
$$N_1 = C_0$$

$$N_0 = C_3$$

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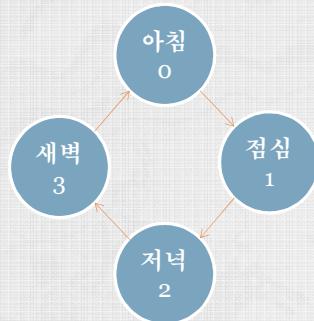
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State Machine (binary encoding)

- Assign each states to unique value
- Convert the state transition to a table

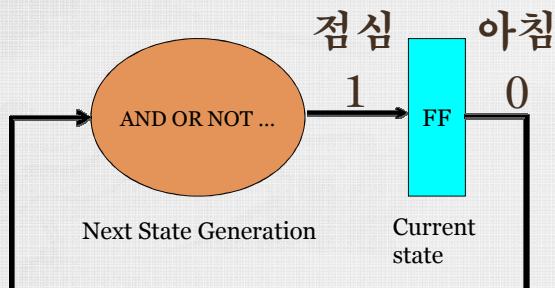


Current	Next
0	1
1	2
2	3
3	0

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State Machine (binary encoding)

- Clock synchronized state machine



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State Machine (binary encoding)

- Convert the sequence table to a binary table

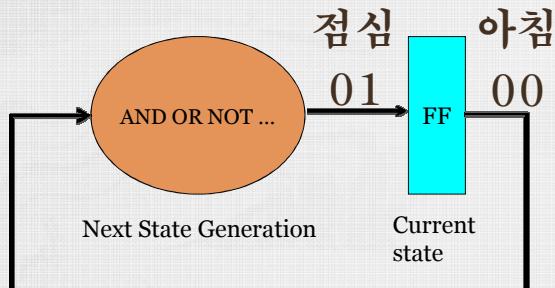
Current	Next	Current 1	Current 0	Next 1	Next 0
0	1	0	0	0	1
1	2	0	1	1	0
2	3	1	0	1	1
3	0	1	1	0	0

- 4 states : requires 2 FF (2 bits)
- N states : requires $\lceil \log_2 N \rceil$ FFs

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State Machine (binary encoding)

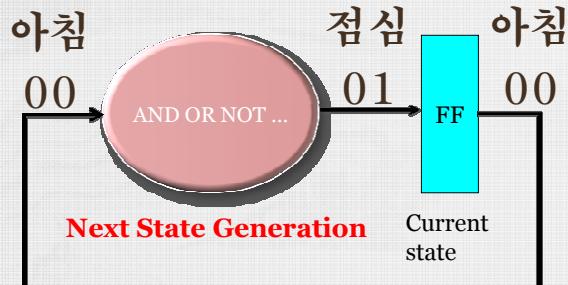
- Clock synchronized state machine



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State Machine (binary encoding)

- Clock synchronized state machine



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State Machine (binary encoding)



Next State Generation

Inputs		Outputs	
Current 1	Current 0	Next 1	Next 0
0	0	0	1
0	1	1	0
1	0	1	1
1	1	0	0

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State Machine (binary encoding)

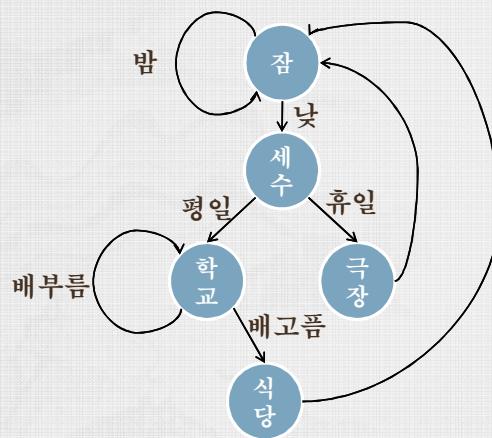
Inputs		Outputs	
Current 1	Current 0	Next 1	Next 0
0	0	0	1
0	1	1	0
1	0	1	1
1	1	0	0

$$\text{Next}0 = \sim\text{Current}0$$

$$\text{Next}1 = \text{Current}0 \oplus \text{Current}1$$

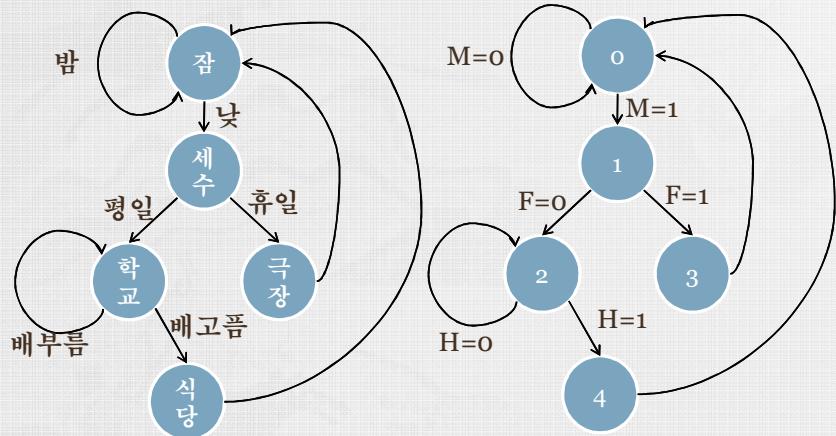
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State Machine 2



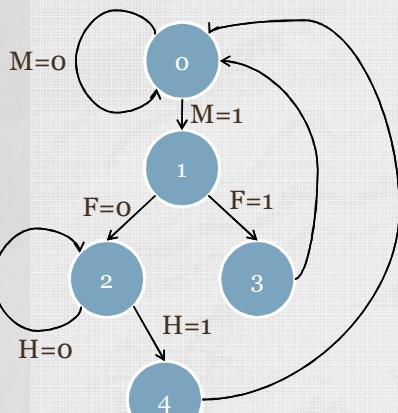
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State Machine 2



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State Machine 2



Current	M	F	H	Next
0	0	x	x	0
0	1	x	x	1
1	x	0	x	2
1	x	1	x	3
2	x	x	0	2
2	x	x	1	4
3	x	x	x	0
4	x	x	x	0

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State Machine 2

Current	M	F	H	Next	C2	C1	Co	M	F	H	N2	N1	No
0	0	x	x	0	0	0	0	0	x	x	0	0	0
0	1	x	x	1	0	0	0	1	x	x	0	0	1
1	x	0	x	2	0	0	1	x	0	x	0	1	0
1	x	1	x	3	0	0	1	x	1	x	0	1	1
2	x	x	0	2	0	1	0	x	x	0	0	1	0
2	x	x	1	4	0	1	0	x	x	1	1	0	0
3	x	x	x	0	0	1	1	x	x	x	0	0	0
4	x	x	x	0	1	0	0	x	x	x	0	0	0

$$N2 = \sim C2 * C1 * \sim C0 * H$$

...

...

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JK FF

Inputs			Outputs		Comments
J	K	CLK	Q	\bar{Q}	
0	0	\uparrow	Q_0	\bar{Q}_0	No change
0	1	\uparrow	0	1	RESET
1	0	\uparrow	1	0	SET
1	1	\uparrow	\bar{Q}_0	Q_0	Toggle

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JK FF

FF Value		JKFF Input	
Current	Next	J	K
0	0	0	1
		0	0
0	1	1	0
		1	1
1	0	0	1
		1	1
1	1	1	0
		0	0

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JK FF

FF Value		JKFF Input	
Current	Next	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

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State Machine 2

C ₂	C ₁	C ₀	M	F	H	N ₂	J ₂	K ₂	N ₁	No
0	0	0	0	x	x	0	0	X	0	0
0	0	0	1	x	x	0	0	X	0	1
0	0	1	x	0	x	0	0	X	1	0
0	0	1	x	1	x	0	0	X	1	1
0	1	0	x	x	0	0	0	X	1	0
0	1	0	x	x	1	1	1	X	0	0
0	1	1	x	x	x	0	0	X	0	0
1	0	0	x	x	x	0	X	1	0	0

$$J_2 = \sim C_2 * C_1 * \sim C_0 * H$$

$$K_2 = 1$$

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State Machine 2

C ₂	C ₁	C ₀	M	F	H	N ₂	J ₂	K ₂	N ₁	J ₁	K ₁	No	J ₀	K ₀
0	0	0	0	x	x	0	0	X	0	0	X	0	0	X
0	0	0	1	x	x	0	0	X	0	0	X	1	1	X
0	0	1	x	0	x	0	0	X	1	1	X	0	X	1
0	0	1	x	1	x	0	0	X	1	1	X	1	X	0
0	1	0	x	x	0	0	0	X	1	X	0	0	0	X
0	1	0	x	x	1	1	1	X	0	X	1	0	0	X
0	1	1	x	x	x	0	0	X	0	X	1	0	X	1
1	0	0	x	x	x	0	X	1	0	0	X	0	0	X

$$J_1 = C_0, K_1 = \sim(C_1 * \sim C_0 * \sim H)$$

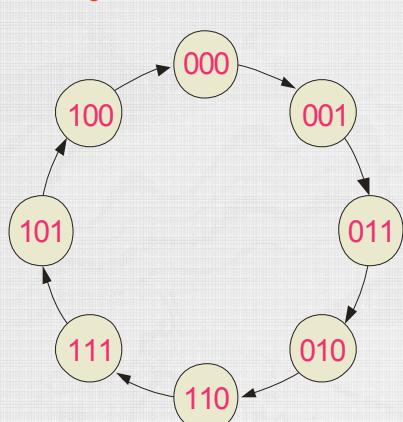
$$J_0 = \sim C_2 * \sim C_1 * M$$

$$K_0 = \sim(\sim C_1 * C_0 * F)$$

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Counter Design

State diagram:



Next state table:

Present State			Next State		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	0	0	1
0	0	1	0	1	1
0	1	1	0	1	0
0	1	0	1	1	0
1	1	0	1	1	1
1	1	1	1	0	1
1	0	1	1	0	0
1	0	0	0	0	0

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Counter Design

C ₂	C ₁	C ₀	N ₂	N ₁	N ₀
0	0	0	0	0	1
0	0	1	0	1	1
0	1	1	0	1	0
0	1	0	1	1	0
1	1	0	1	1	1
1	1	1	1	0	1
1	0	1	1	0	0
1	0	0	0	0	0

N₂

C ₂ C ₁	C ₀ = 0	C ₀ = 1
00		
01	X	
11	X	X
10		X

$$N_2 = C_1 * \sim C_0 + C_2 * C_0$$

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Counter Design

C ₂	C ₁	Co	N ₂	N ₁	No
0	0	0	0	0	1
0	0	1	0	1	1
0	1	1	0	1	0
0	1	0	1	1	0
1	1	0	1	1	1
1	1	1	1	0	1
1	0	1	1	0	0
1	0	0	0	0	0

N1

C ₂ C ₁	Co = 0	Co = 1
00		X
01	X	X
11	X	
10		

$$N1 = C1 * \sim C0 + \sim C2 * C0$$

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Counter Design

C ₂	C ₁	Co	N ₂	N ₁	No
0	0	0	0	0	1
0	0	1	0	1	1
0	1	1	0	1	0
0	1	0	1	1	0
1	1	0	1	1	1
1	1	1	1	0	1
1	0	1	1	0	0
1	0	0	0	0	0

N0

C ₂ C ₁	Co = 0	Co = 1
00	X	X
01		
11	X	X
10		

$$N0 = \sim C2 * \sim C1 + C2 * C1$$

$$= C2 \text{ xnor } X1$$

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Counter Design

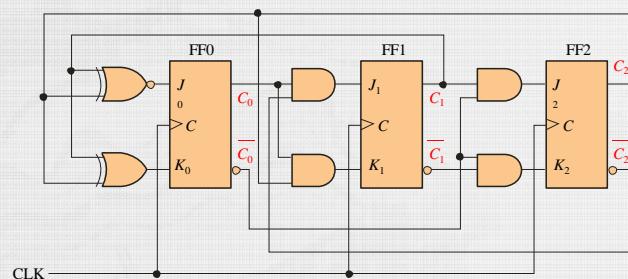
C ₂	C ₁	C ₀	N ₂	N ₁	No	J ₂	K ₂	J ₁	K ₁	J ₀	K ₀
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	1	0	X	1	X	X	0
0	1	1	0	1	0	0	X	X	0	X	1
0	1	0	1	1	0	1	X	X	0	0	X
1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	1	0	1	X	0	X	1	X	0
1	0	1	1	0	0	X	0	0	X	X	1
1	0	0	0	0	0	X	1	0	X	0	X

$$J_2 = C_1 * \sim C_0, K_2 = \sim C_1 * \sim C_0$$

$$J_1 = \sim C_2 * C_0, K_1 = C_2 * C_0$$

$$J_0 = C_2 \text{ xnor } C_1, K_0 = C_2 \text{ xor } C_1$$

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Check point

- Asynchronous & Synchronous
- Counters
- State Machine
 - Moore
 - Mealy
- State Machine
 - One bit hot encoding
 - Binary encoding
- State Machine using D FF
- State Machine using JK FF

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