

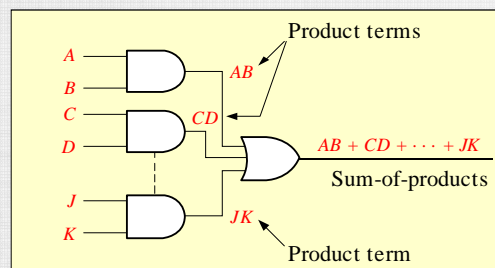
논리회로 및 설계

Chapter 5

일부 이미지 저작권:
Wikipedia, Creative Commons
Pearson Educations

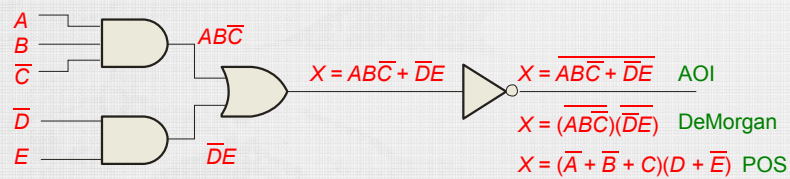
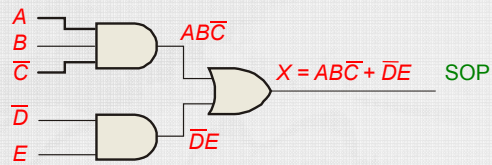
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SoP Circuit



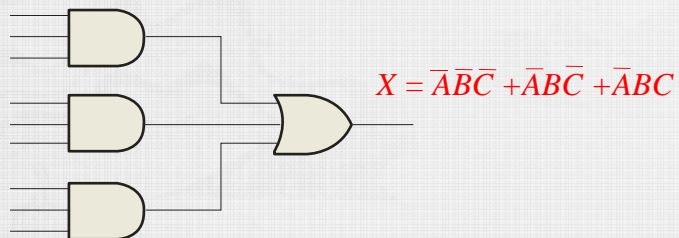
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$$\text{SoP} = \sim \text{PoS}$$



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SoP standard reduction



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Karnaugh Map & Truth Table

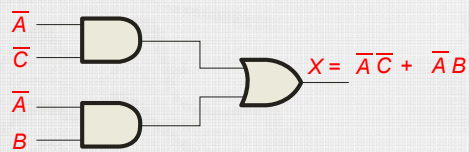
$\backslash C$	0	1
AB		
00	1	
01	1	1
11		
10		

$$X = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}BC$$

Inputs			Output
A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

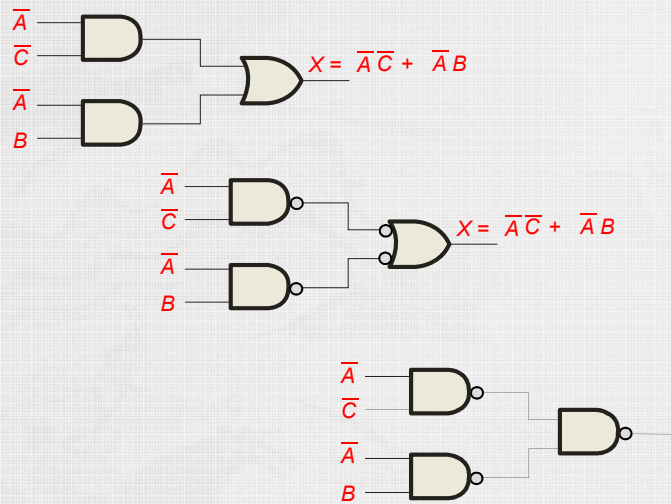
$$X = \bar{A}\bar{C} + \bar{A}B$$

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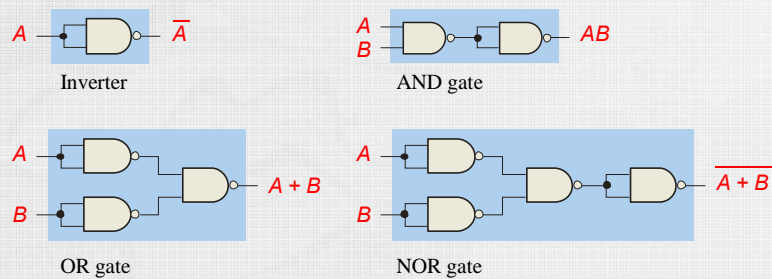
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NAND Logic : from SoP



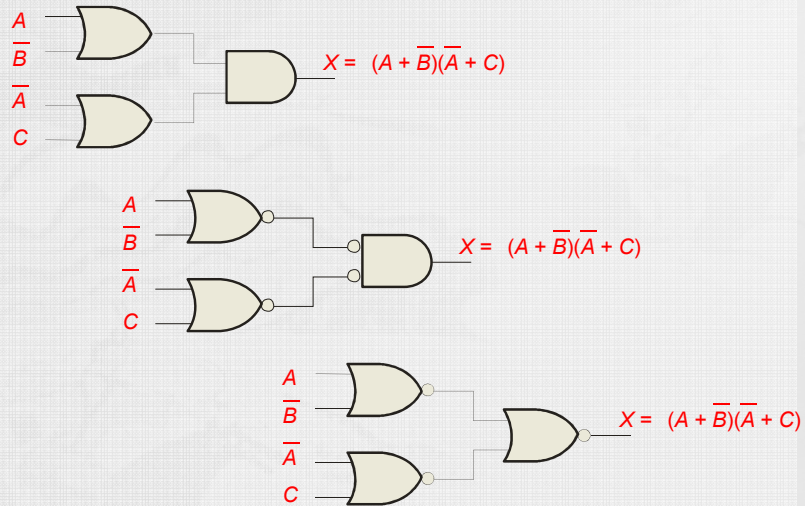
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NAND : Universal Gate



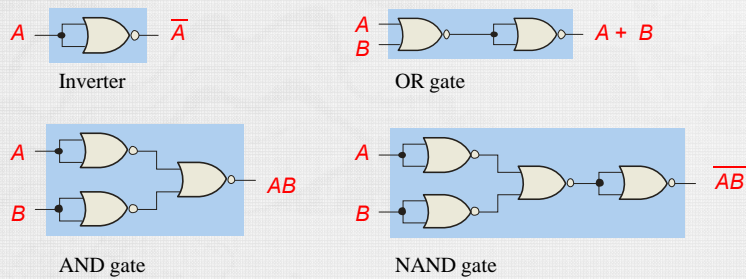
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NOR Logic : from PoS



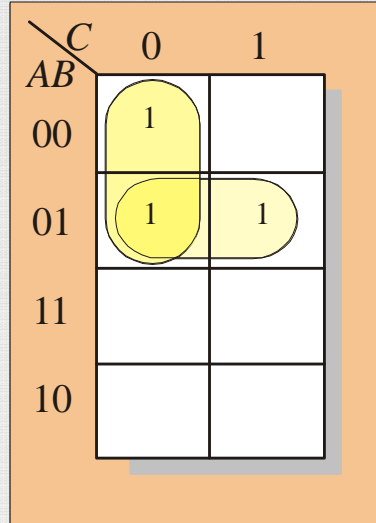
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NOR : Universal Gate



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PoS from Karnaugh Map



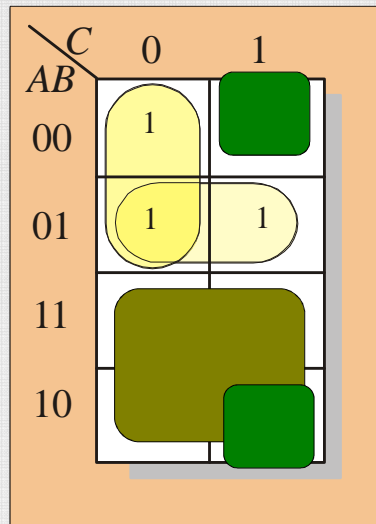
$$X = \overline{A}\overline{B}\overline{C} + \overline{A}B\overline{C} + \overline{A}BC$$

Inputs			Output
A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

$$X = \overline{A}\overline{C} + \overline{A}B$$

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PoS from Karnaugh Map



$$X = \overline{A}\overline{B}\overline{C} + \overline{A}B\overline{C} + \overline{A}BC$$

Inputs			Output
A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

$$\overline{X} = A + \overline{B}C$$

$$X = \overline{A} (B + \overline{C})$$

$$X = \overline{A}\overline{C} + \overline{A}B$$

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Check point

- SoP = NAND Logic (Universal)
- PoS = NOR Logic (Universal)
- Truth Table = Karnaugh Map = SoP = PoS

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