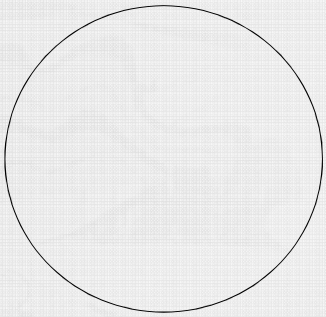
논리회로 및 설계

Chapter 7

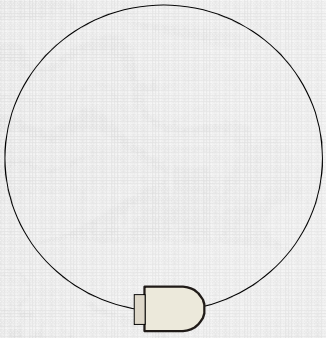
Storage elements

- Latch
- FlipFlop

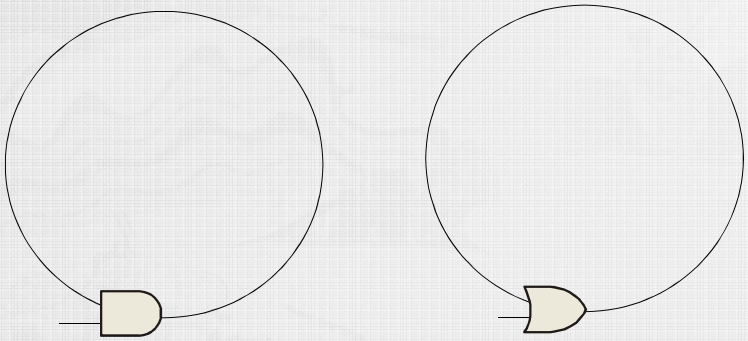
Store of Electron



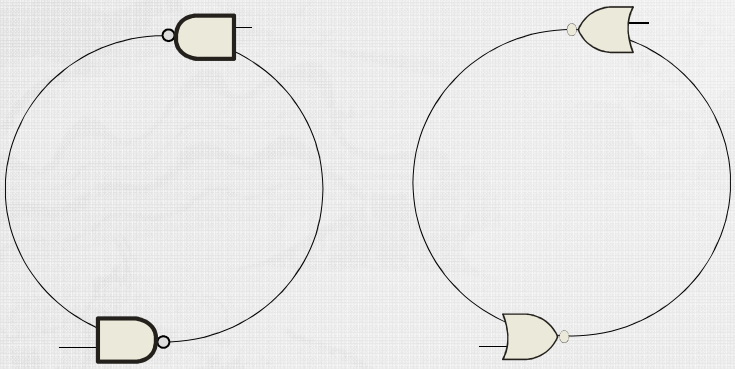
Store of Electron



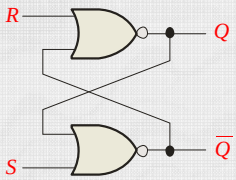
Store of Electron : memory?



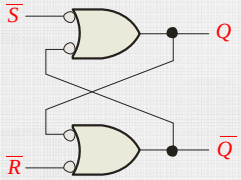
Save State



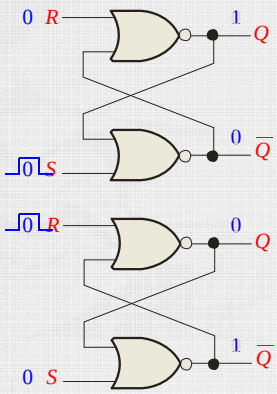
Latch

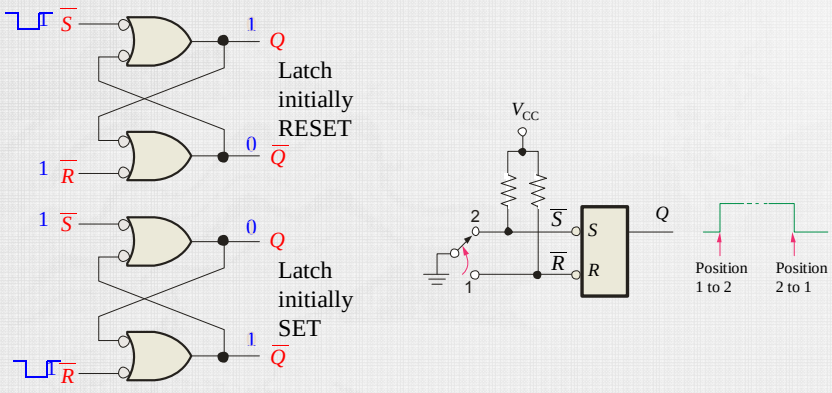


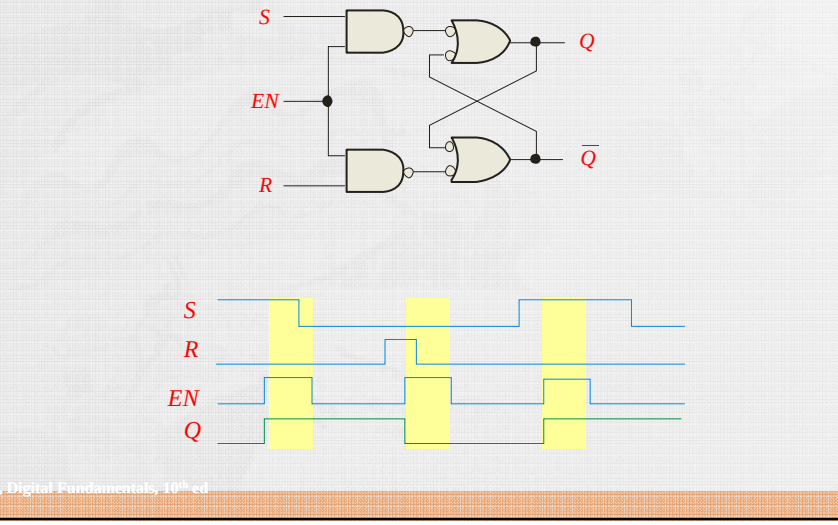
NOR Active-HIGH Latch



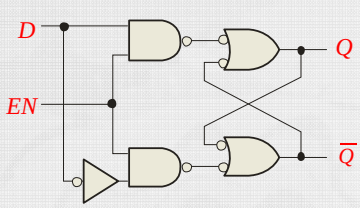
NAND Active-LOW Latch

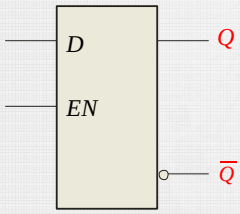



$\overline{S}$
1
Q
Latch initially RESET
0
$\overline{Q}$
1
$\overline{R}$
1
$\overline{S}$
0
Q
Latch initially SET
1
$\overline{Q}$
$\overline{R}$
V_{CC}
2
1
$\overline{S}$
S
Q
$\overline{R}$
R
Position 1 to 2
Position 2 to 1

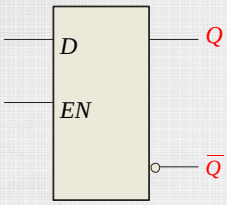

S
EN
R
Q
$\overline{Q}$
S
R
EN
Q

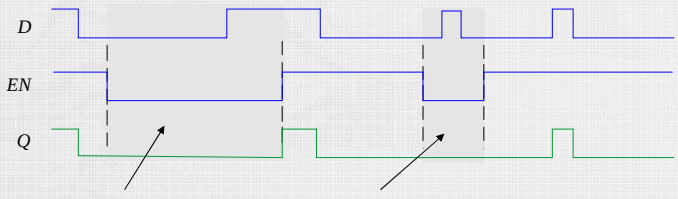
D Latch



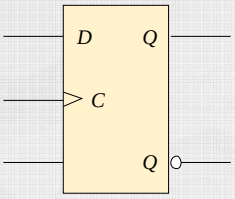


Inputs		Outputs		
D	*EN*	*Q*	$\overline{Q}$	Comments
0	1	0	1	RESET
1	1	1	0	SET
X	0	Q_0	$\overline{Q}_0$	No change

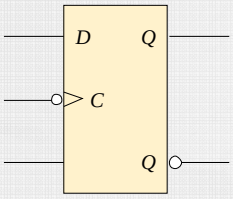




Flip-Flop



(a) Positive edge-triggered



(b) Negative edge-triggered

Inputs		Outputs		
D	CLK	*Q*	$\overline{Q}$	Comments
1	↑	1	0	SET
0	↑	0	1	RESET

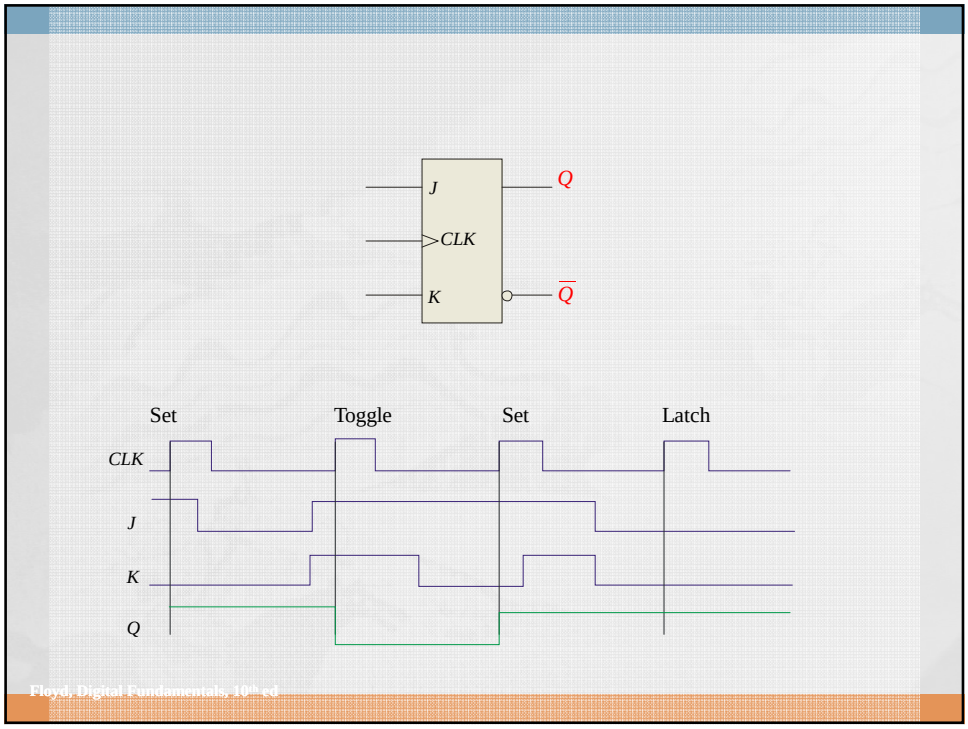
(a) Positive-edge triggered

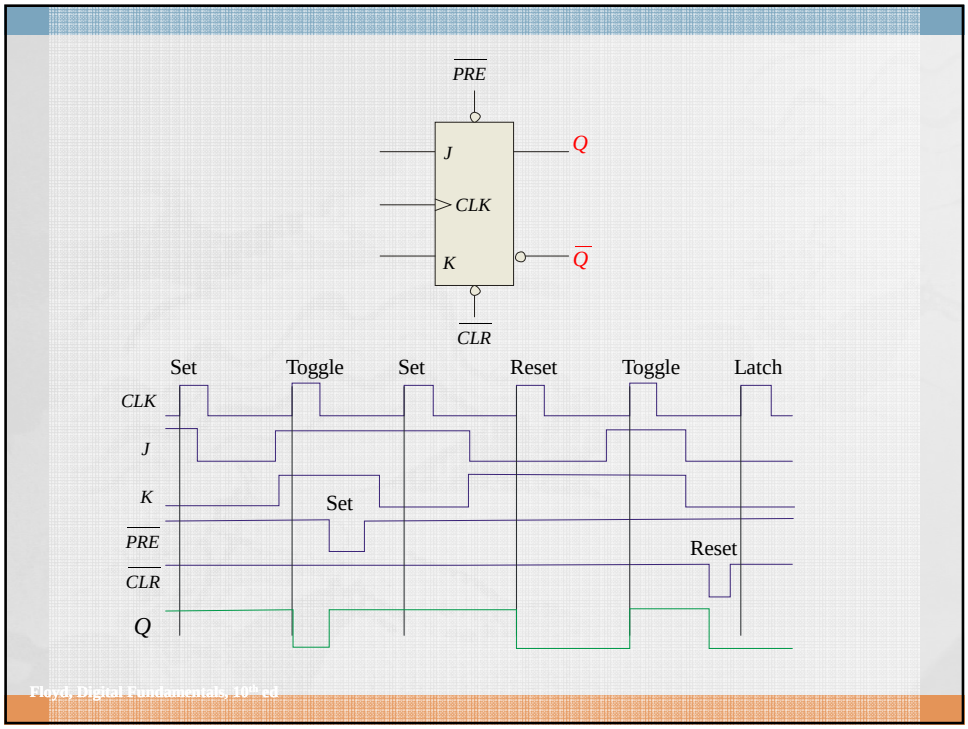
Inputs		Outputs		
D	CLK	*Q*	$\overline{Q}$	Comments
1	↓	1	0	SET
0	↓	0	1	RESET

(b) Negative-edge triggered

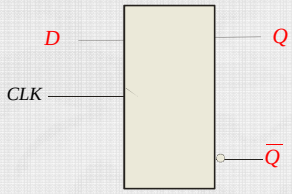
JK FF

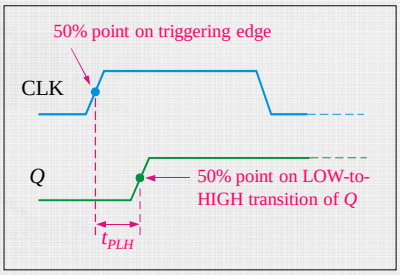
Inputs			Outputs		
J	*K*	CLK	*Q*	$\overline{Q}$	Comments
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle


J
CLK
K
Q
$\overline{Q}$
Set
Toggle
Set
Latch
CLK
J
K
Q


$\overline{PRE}$
J
CLK
K
Q
$\overline{Q}$
$\overline{CLR}$
Set
Toggle
Set
Reset
Toggle
Latch
CLK
J
K
$\overline{PRE}$
$\overline{CLR}$
Q
Set
Reset

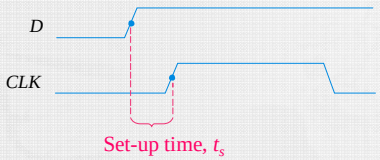
D FF



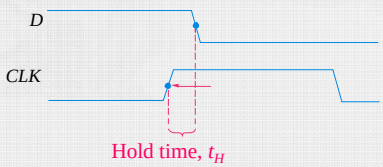


Setup & Hold time

Setup time is the minimum time for the data to be present *before* the clock.



Hold time is the minimum time for the data to *remain* after the clock.



Check point

- Latch
- FlipFlop : Sync. with Clock
- Propagation Delay
- Setup time
- Hold time