

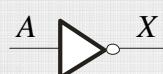
# 논리회로 및 설계

## Chapter 3

일부 이미지 저작권:  
Wikipedia, Creative Commons  
Pearson Educations

Floyd, Digital Fundamentals, 10th ed.

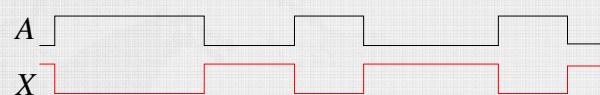
## Inverter



**Inverter : NOT operation.**

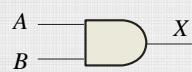
Input	Output
A	X
LOW (0)	HIGH (1)
HIGH (1)	LOW(0)

$$X = \sim A$$



Floyd, Digital Fundamentals, 10th ed.

AND

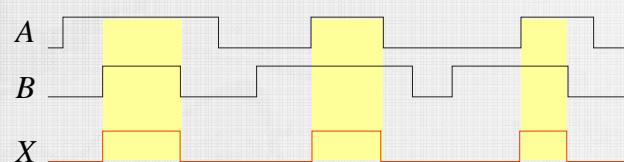


Inputs		Output
A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

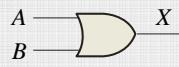
$$X = A \cdot B$$

$$X = AB$$

Floyd, Digital Fundamentals, 10<sup>th</sup> ed.



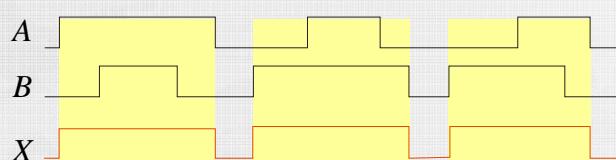
# OR



Inputs		Output
A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

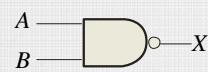
$$X = A + B$$

Floyd, Digital Fundamentals, 10th ed



Floyd, Digital Fundamentals, 10th ed

# NAND



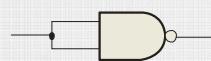
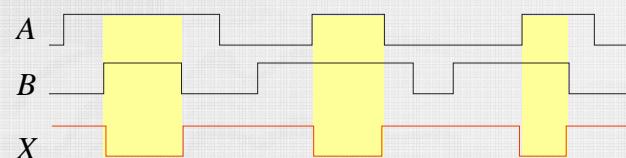
Inputs		Output
A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

$$X = \sim(A \cdot B)$$

$$X = \sim(AB)$$

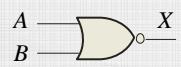
Floyd, Digital Fundamentals, 10th ed

# NAND



Floyd, Digital Fundamentals, 10th ed

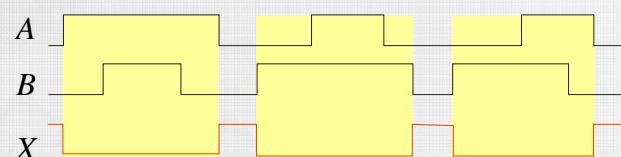
# NOR



Inputs		Output
A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

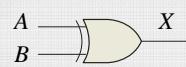
$$X = \sim(A + B)$$

Floyd, Digital Fundamentals, 10th ed



Floyd, Digital Fundamentals, 10th ed

# XOR

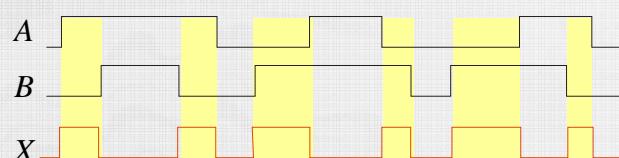


Inputs		Output
A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

$$X = \sim AB + A\sim B$$

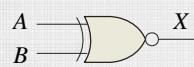
$$X = A \oplus B$$

Floyd, Digital Fundamentals, 10<sup>th</sup> ed



Floyd, Digital Fundamentals, 10<sup>th</sup> ed

# XNOR

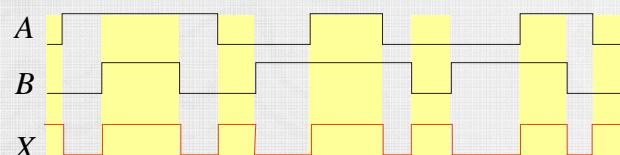


Inputs		Output
A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

$$X = \sim A \sim B + AB$$

$$X = A \odot B$$

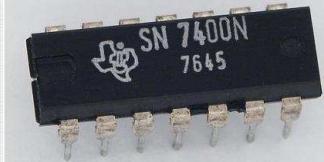
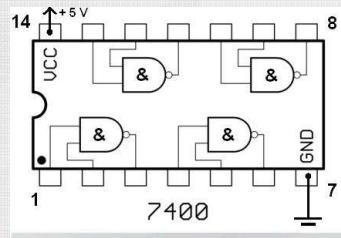
Floyd, Digital Fundamentals, 10<sup>th</sup> ed



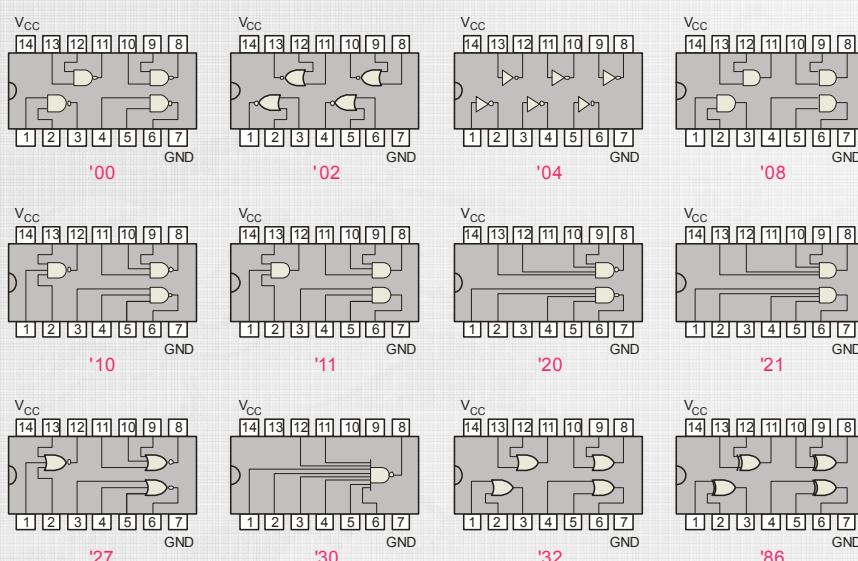
Floyd, Digital Fundamentals, 10<sup>th</sup> ed

# 74 series

## Fixed Function Logic



Floyd, Digital Fundamentals, 10<sup>th</sup> ed

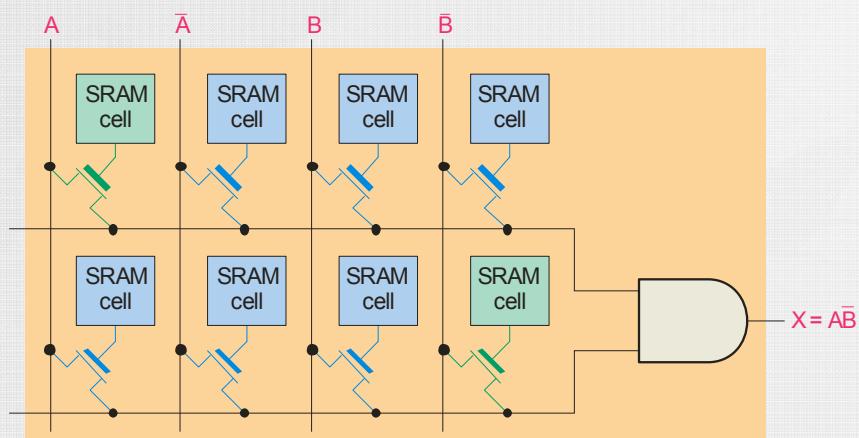


Floyd, Digital Fundamentals, 10<sup>th</sup> ed

Part number	Description
7400	quad 2-input NAND gate
741G00	single 2-input NAND gate
7401	quad 2-input NAND gate with open collector outputs
741G01	single 2-input NAND gate with open drain output
7402	quad 2-input NOR gate
741G02	single 2-input NOR gate
7403	quad 2-input NAND gate with open collector outputs
741G03	single 2-input NAND gate with open drain output
7404	hex inverter
741G04	single inverter
7405	hex inverter with open collector outputs
741G05	single inverter with open drain output
7406	hex inverter buffer/driver with 30 v open collector outputs
741G06	single inverting buffer/driver with open drain output
7407	hex buffer/driver with 30 v open collector outputs
741G07	single non-inverting buffer/driver with open drain output
7408	quad 2-input AND gate
741G08	single 2-input AND gate
7409	quad 2-input AND gate with open collector outputs
741G09	single 2-input AND gate with open drain output
7410	triple 3-input NAND gate

Floyd, Digital Fundamentals, 10th ed

## Programmable Logic



Floyd, Digital Fundamentals, 10th ed

# VHDL

```
entity NandGate is
    port(A, B: in bit;
         LED: out bit);
end entity NandGate;

architecture GateBehavior of NandGate is
    signal A, B: bit;
begin
    X <= A nand B;
    LED <= X;
end architecture GateBehavior;
```

Floyd, Digital Fundamentals, 10th ed

## Check point

- Basic Gates : NOT, AND, OR, NAND ...
- Truth Table (진리표)
- Standard IC (74 series)
- PLD
- VHDL

Floyd, Digital Fundamentals, 10th ed