

논리회로 및 설계

Chapter 11

일부 이미지 저작권:
Wikipedia, Creative Commons
Pearson Educations

Floyd, Digital Fundamentals, 10th ed.

Programmable Logic Devices

$\text{PLD} = \text{FF} + \text{Basic Gates}$

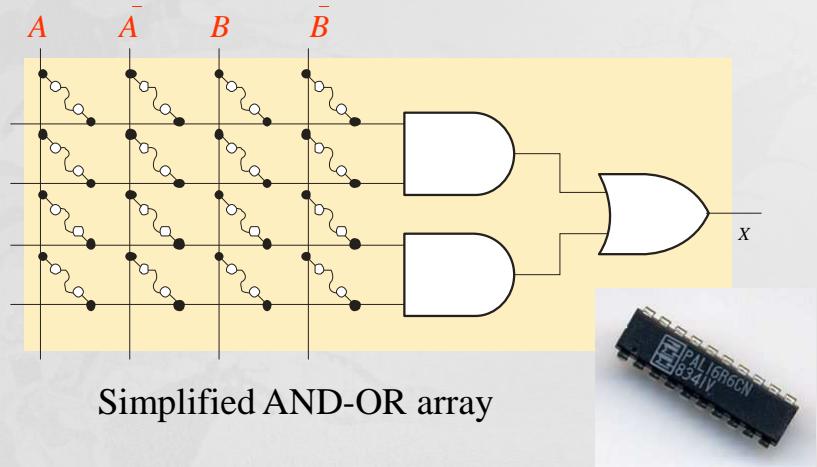
SPLD: (Simple PLDs) ~ 20 Gates with FF, PAL, GAL

CPLD: (Complex PLDs) ~ hundreds Gates with FF

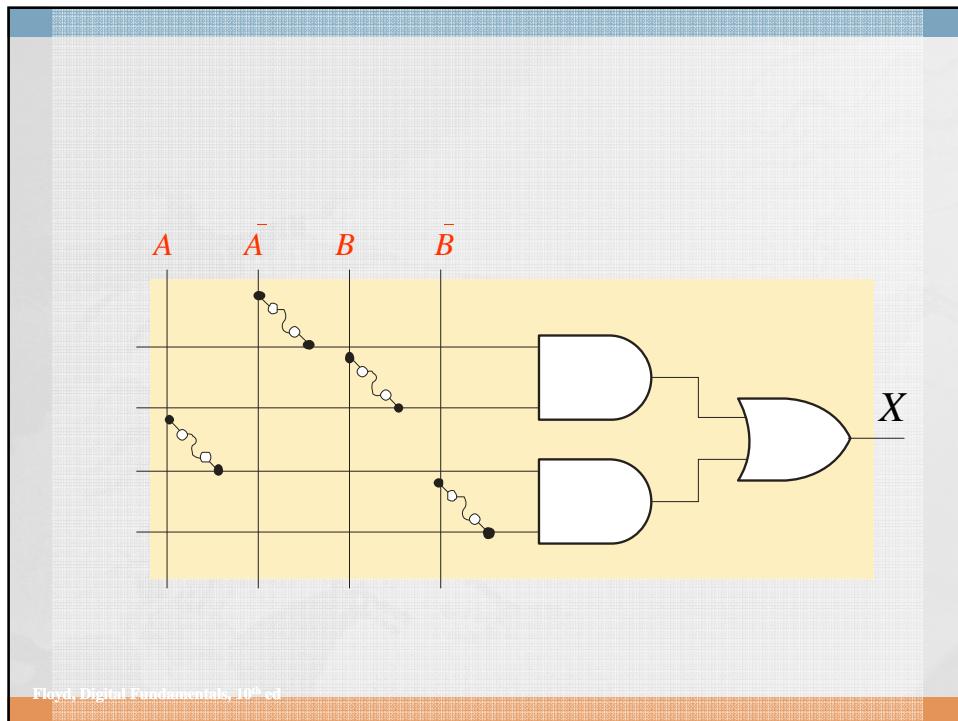
FPGA: (Field Programmable Gate Array) ~ hundreds of millions Gates with FF

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PAL(Programmable Array Logic)



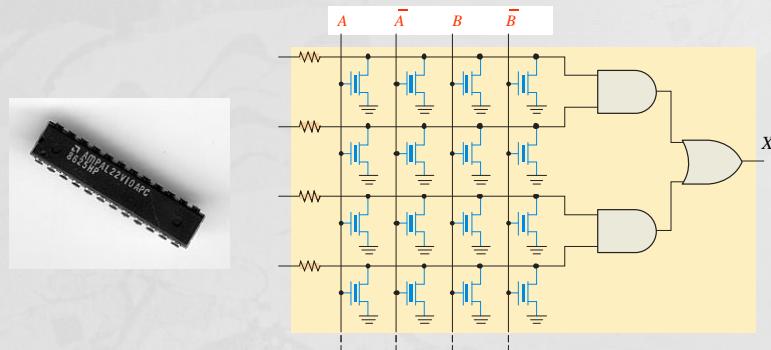
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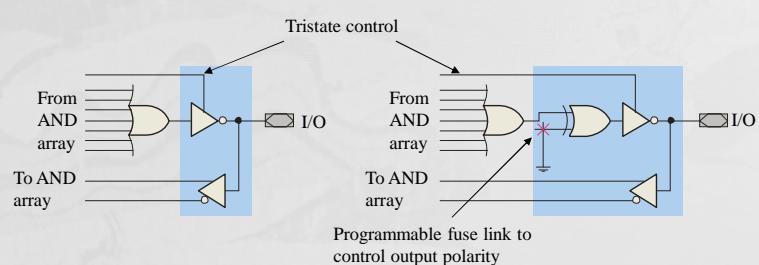
GAL(Generic Array Logic)

EEPROM , Erasable



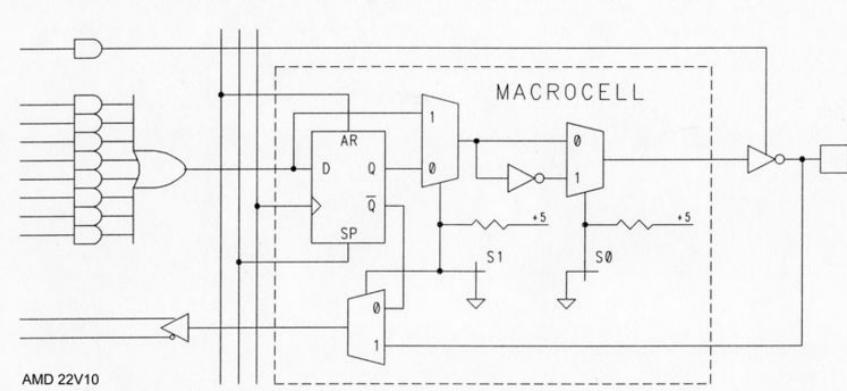
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PAL, GAL : I/O part

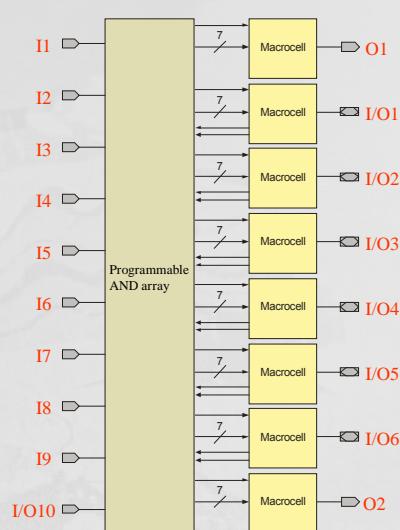


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PAL, GAL : macrocell



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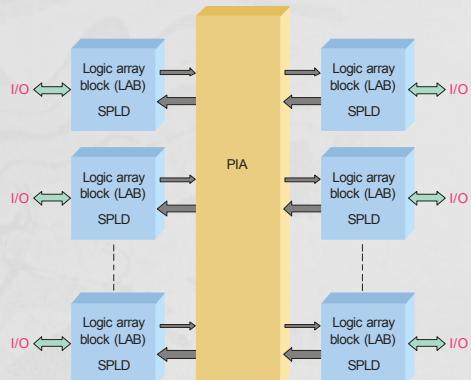
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CPLD

(Complex programmable logic device)

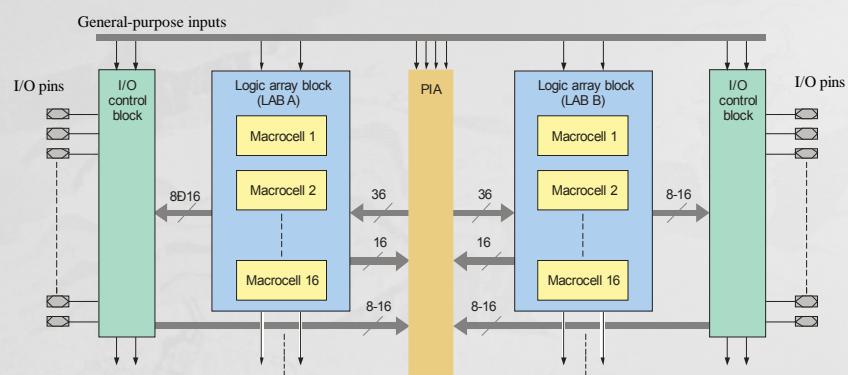
Multiple logic array blocks (**LAB** = SPLD)

LABs are connected via a programmable interconnect array (**PIA**)



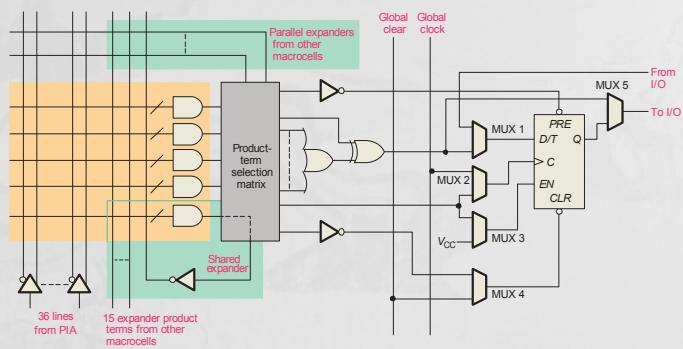
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CPLD example : Altrera MAX7000



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MAX7000 macrocell

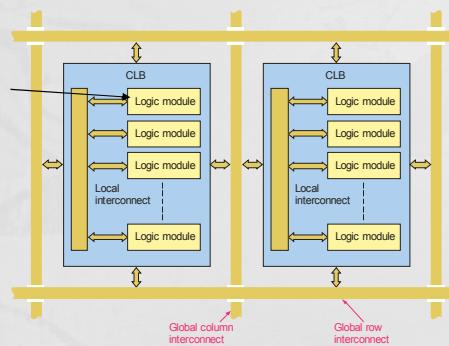


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FPGA (Field programmable gate array)

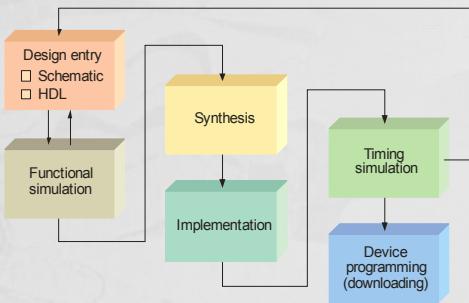
The configurable logic block (**CLB**) : basic element

logic modules : look-up table (LUT), flip-flop, MUX



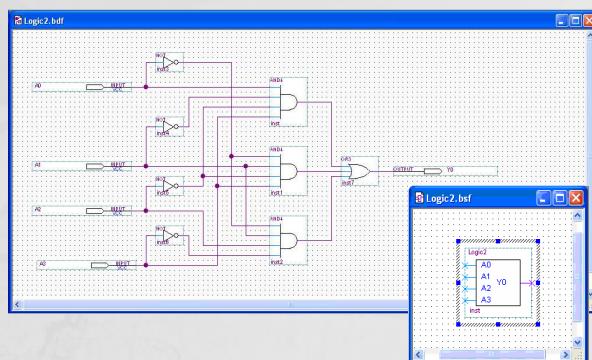
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Programming procedure



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Schematic Design



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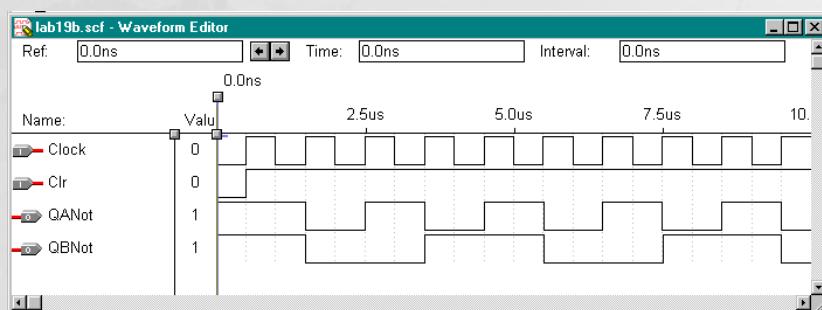
HDL Design : VHDL

```
entity NandGate is
    port(A, B: in bit;
         LED: out bit);
end entity NandGate;

architecture GateBehavior of NandGate is
    signal A, B: bit;
begin
    X <= A nand B;
    LED <= X;
end architecture GateBehavior;
```

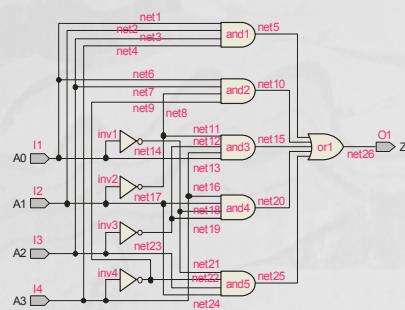
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Functional Simulation



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Synthesis

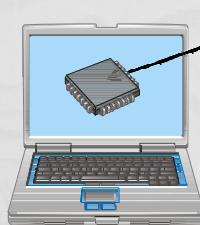


Netlist

```
Netlist (Logic3)
net<name> instance<name> <from>; <to>;
instances: and1, and2, and3, and4, and5, or1, inv2,
inv3, inv4;
Input/outputs: I1, I2, I3, I4, O1;
net1: and1, input1; I1;
net2: and1, input2; I2;
net3: and1, input3; I3;
net4: and1, input4; I4;
net5: and1, output1; or1, input1;
net6: and2, input1; I1;
net7: and2, input2; I3;
net8: and2, input3; inv2.output1
net9: and2, input4; inv4.output1
net10: and2, output1; or1.input2;
net11: and3, input1; inv2.output1
net12: and3, input2; inv3.output1
net13: and3, input3; I4;
net14: and3, input4; inv4.output1
net15: and3, output1; O1;
net16: and4, input1; inv3.output1
net17: and4, input2; inv4.output1
net18: and4, input3; I3;
net19: and4, input4; I1;
net20: and4, output1; or1.input2;
net21: and5, input1; I1;
net22: and5, input2; I3;
net23: and5, input3; inv2.output1
net24: and5, input4; inv4.output1
net25: and5, output1; O1;
```

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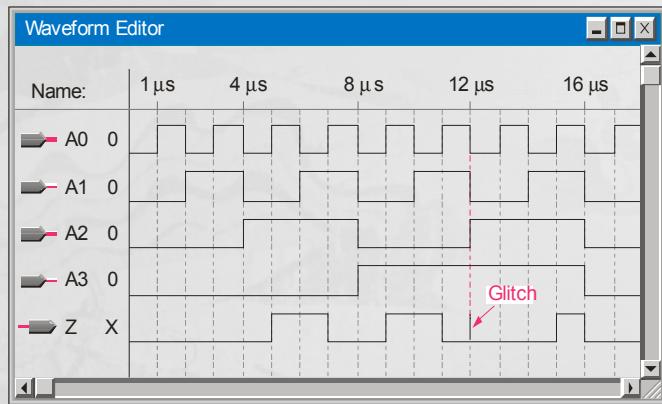
Implementation : device fitting



Specifying device &
I/O Pin assignment

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Timing Simulation



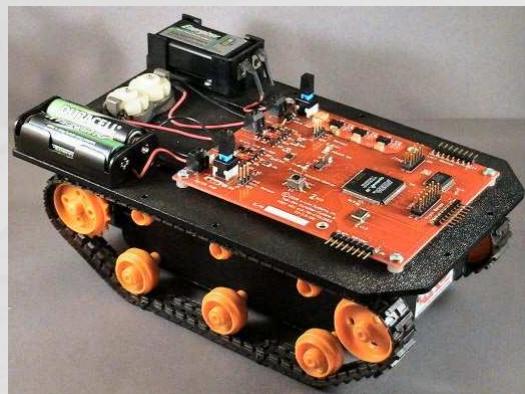
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Device Programming



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Test Operation



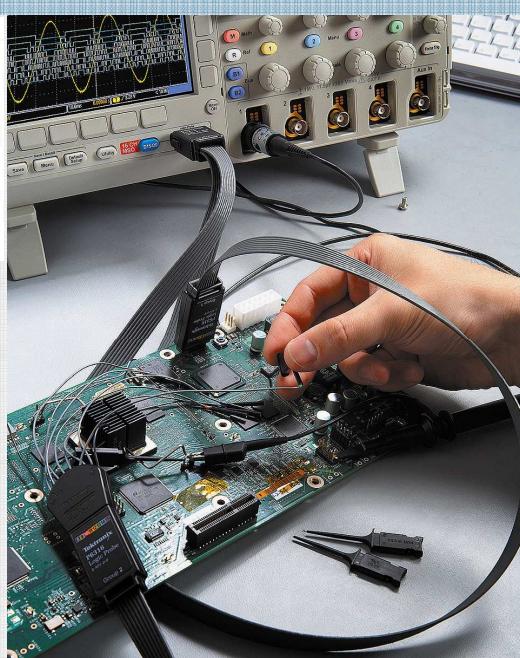
*image from **c-Link Systems Trak-Bot C3**

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Debugging

*image from
Eetimes,
Electronic Specifier

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Check point

- PAL, GAL, CPLD, FPGA
- Design Flow
- Schematic Design
- VHDL Coding
- Functional Simulation
- Timing Simulation
- Device Programming
- Debugging