**A REPORT**

**ON**

**DESIGN AND ANALYSIS OF PLL AND ITS SUB BLOCKS**

**By**

Abhishek Bhagat 2012A3PS145G

**AT**



**STMicroelectronics, Greater Noida**

A Practice School II Station of



##### BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI

**December, 2015**

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&Electronics Engineering

## Prepared in the partial fulfillment of the

Practice School II Course

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December, 2015

**BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE**

**PILANI (RAJASTHAN)**

**Practice School Division**

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**Title of the Project:** Design and Analysis of PLL and its sub blocks

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**Key Words:** Phase Locked Loop, Level shifter, Voltage controlled oscillator

**Project Areas:** Clock Generation

**Abstract:** The Phase Locked Loop (PLL) is a prime component in generation of clock. The most important applications of a PLL are generation of frequencies in multiples of the input frequency and distribution of timely clocked pulses in digital logic circuits such as microprocessors. This project involves the analysis of the blocks that make up such a complex yet important system. The standard charge pump PLLs analyzed in this project was designed in 90nm technology. Simulations were carried out on specific blocks separately to understand their working and henceforth characterizing them as per the given specifications at all process, voltage and temperature corners.

Signature(s) of Student(s) Signature of PS Faculty

Date

**BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE**

**PILANI (RAJASTHAN)**

**PRACTICE SCHOOL DIVISION**

# Response Option Sheet

**Station**: STMicroelectronics **Center**: Greater Noida

**Name**: Abhishek Bhagat **ID No**. : 2012A3PS145G

**Title of the Project**: Design and Analysis of PLL and its sub blocks

Usefulness of the project to the on-campus courses of study in various disciplines. Project should be scrutinized keeping in view the following response options. Write Course No. and Course Name against the option under which the project comes.

|  |  |  |
| --- | --- | --- |
| Code No. | Response Option | Course No.(s) & Name |
| 1. | A new course can be designed out of this project. | NO |
| 2. | The project can help modification of the course content of some of the existing Courses | YES |
| 3. | The project can be used directly in some of the existing Compulsory Discipline Courses (CDC)/ Discipline Courses Other than Compulsory (DCOC)/ Emerging Area (EA), etc. Courses | NO |
| 4. | The project can be used in preparatory courses like Analysis and Application Oriented Courses (AAOC)/ Engineering Science (ES)/ Technical Art (TA) and Core Courses. | NO |
| 5. | This project cannot come under any of the above mentioned options as it relates to the professional work of the host organization. | YES |

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Date: Date:**Acknowledgement**

The successful completion of this project depends largely on the encouragement and guidelines of many others. I take this opportunity to express my heartfelt gratitude to the people who have been instrumental in the successful completion of this project.

I want to start by thanking my mentor, **Mr. Nitin Gupta**, whose constant supervision was invaluable. His knowledge in this domain and his commitment towards work were always a source of motivation for me. I would also like to thank my group manager, **Mr. Anand Kumar**, for his encouragement throughout the project. I am deeply indebted to the employees of the PLL team, particularly **Mr. Jeet Narayan Tiwari** for his unending patience and guidance all along without which the project could not have been completed in a systematic manner.

I am thankful to **STMicroelectronics**, Greater Noida for providing me with an opportunity to work on latest tools and technology and alongside such talented people.

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**1. INTRODUCTION**

Phase locked loop, popularly known as PLL is one of the important constituent of modern electronic systems. Having wide range of applications over a broad frequency spectrum PLL has become one of the most essential element in microprocessor boards of complex systems, wired and wireless communication systems and many other systems.

PLL is widely used in communications, multimedia and in many other applications. It is essentially a feedback loop that locks the on-chip clock phase to that of an input clock or signal. Because the on-chip clock toggles a large capacitive load, a series of clock buffers efficiently increases the drive strength of the PLL output to drive the load. High-performance PLLs and clock buffers are widely used within a digital system for two purposes: clock generation, and timing recovery.

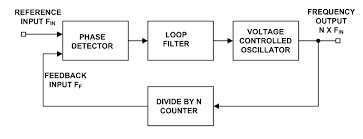
High frequency clocks are used to sequence operations and synchronize between functional units and between ICs. Clock frequencies and data rates have been increasing with each generation of processing technology and processor architecture. Within these digital systems, well-timed clocks are generated with PLLs and then distributed on-chip with clock buffers. Also, for some applications such as high speed parallel links and distributed synchronous clocking, multiple PLLs are employed to minimize the timing uncertainty. Therefore, demand for low-power PLLs has been increasing. The low-power requirement makes the design of a low-jitter PLL even more challenging.

My project mainly focuses on analysis of PLLs and its sub blocks with particular attention to implementations in VLSI technologies. I was assigned the work of analyzing different PLL blocks at all Process Voltage Temperature corners and checking for departure from ideal behavior, like duty cycle variation in the level shifter. Various simulations have been done to get behavior and robustness of the circuits and the whole PLL itself.

**2. BASICS OF PLL**

A PLL is a closed loop feedback system that sets fixed phase relationship between its output clock phase and the phase of a reference clock. It is capable of tracking the changes that are within its bandwidth. It also multiplies a low frequency reference clock to produce a high frequency clock at the output.

The basic block diagram of PLL:



**Fig1**: Basic Block Diagram of PLL

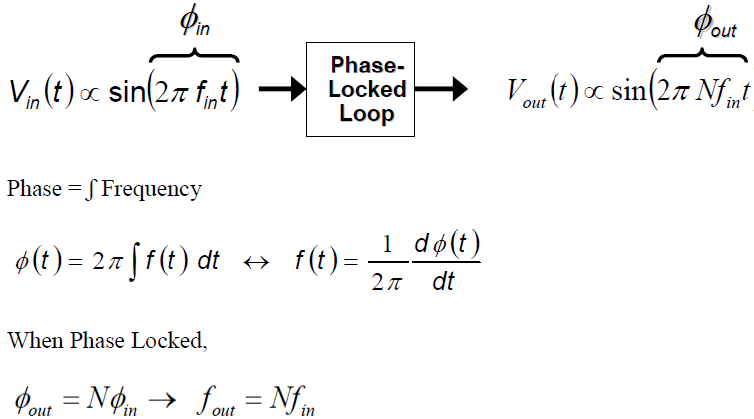
**Working:**

The basic operation of a PLL is as follows. The phase detector (comparator) produces an error output signal based on the phase difference between the phase of the feedback clock and the phase of the reference clock. Over time, small frequency differences accumulate as an increasing phase error. The difference or error signal is low-pass filtered and fed as input to the oscillator. The filtered error signal acts as a control signal (voltage or current) of the oscillator and adjusts the frequency of oscillation to align phase of feedback clock with the phase of the reference clock.

If two frequencies are sufficiently close, the PLL feedback mechanism forces the two PD input frequencies to be equal and the VCO is locked with incoming frequency. This is called as **locked state of PLL**. Once the loop is in locked state, there will be small phase difference between the two PD input phase signals. This phase difference results in a dc voltage at the phase detector output which is required to shift the VCO from its free running frequency to input frequency and keeps the loop in locked state. 

**Fig2**: Operation of PLL

**Equations governing PLL:**



**3. TERMINOLOGIES**

**Locking:**

When VCO output is in phase as well as in frequency with the reference input signal.

**LOCK RANGE:**

Lock range is the range of input frequencies over which the oscillator can stay in lock once lock was achieved. This is a wider range than capture range since the comparator is already in lock, so incoming frequency variations are dealt with incrementally.

**CAPTURE RANGE:**

The capture range is the incoming signal frequency range over which the phase comparator and oscillator can react fast enough so that phase lock is achieved before the phase comparator goes through another cycle.

Capture range depends on the amount of the gain in a loop itself and the loop filter bandwidth. Reducing the loop filter bandwidth thus improves the rejection of the out-of-band signals, but at the same time the capture range decreases, pull in time becomes larger and phase margin becomes poor.

**FREE RUNNING FREQUENCY:**

VCO running frequency when no input applied.

**Bandwidth of PLL:**

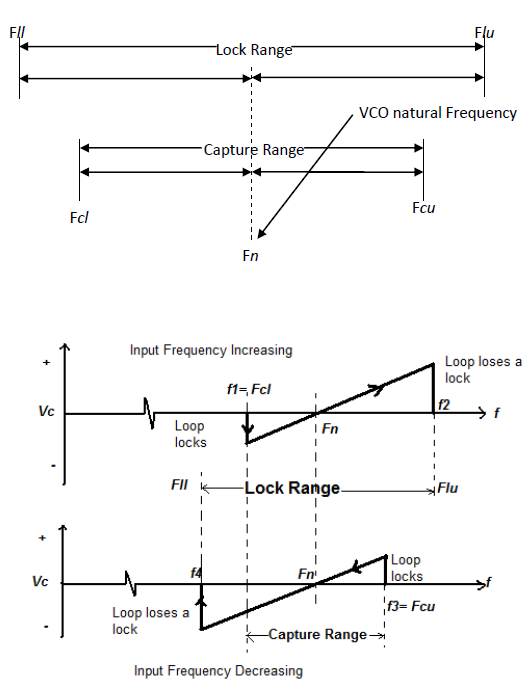
The bandwidth of a PLL is the measure of the PLL's ability to track the input clock and jitter. The closed loop gain 3-dB frequency of the PLL determines the PLL bandwidth. The bandwidth is approximately the unity gain point for PLL open loop response.

**Acquisition Time:**

Pull-in time + settling time: Time required for the PLL to lock itself on to the reference clock.

**Phase Offset or Phase Error (Steady State):**

When PLL is locked, the phase difference between input and output.



**Fig3**: Lock Range and Capture Range of PLL

In the upper part of the above figure, the loop frequency is being gradually increased. The loop does not respond to the signal until it reaches a frequency f1, corresponding to the lower edge of the capture range. Then, the loop suddenly locks on the input, causing a negative jump of the loop-error voltage. Next, Vd varies with frequency with a slope equal to the reciprocal of the VCO voltage-to-frequency conversion gain, and goes through zero as fs = fo. The loop tracks the input until the input frequency reaches *f2,* corresponding to the upper edge of the lock range. The PLL then loses lock, and the error voltage drops to zero.

If the input frequency is now swept slowly back, the cycle repeats itself as shown in the lower part of the preceding figure. The loop recaptures the signal at *f3* and traces it down to *f4*. The frequency spread between *(f1, f3)* and (*f2, f4*) corresponds to the total capture and lock ranges of the system; that is, *f3 - f1* = capture range and *f4 - f2* = lock range. The PLL responds only to those input signals sufficiently close to the VCO frequency *fo* to fall within the lock or capture range of the system. Its performance characteristics, therefore, offer a high degree of frequency selectivity, with the selectivity characteristics centered about *fo*.

If an incoming frequency is far removed from that of the VCO, so that their difference exceeds the pass band of the low-pass filter, it will simply be ignored by the PLL. Thus, the PLL is a frequency-selective circuit.

**4. TYPES OF PLL**

There are several types of PLL available. The architecture broadly ranges according to the application. PLL can be broadly classified as **analog** and **digital PLLs**.

PLL can also be classified according to the order of loop filter used in architecture. The order of loop filter is the type of PLL. For example, if 1st order loop filter is used, then it is called as type I PLL. If 2nd order filter is used, it is called as type II PLL and so on.

If PLL uses simple ‘Phase detector’ in its architecture, it is called as simple PLL. But if PLL uses ‘Phase Frequency Detector’ accompanied with ‘Charge Pump.’, it is called as “Charge Pump PLL”.

Following types of PLL are classified according to their application.

* **Programmable PLL:** This type of PLL can be programmed for wide range of signals.
* **Single and multi-phase PLL:** These can control a single or many phases. They are used in digital clock networks.
* **Digital Phase Locked Loop:** They are used digital input signals for application like Manchester coding.
* **PLL with lock detector:** It uses a lock on one of the pins and is used in frequency modulation.
* **PLL frequency synthesizer:** These are used to synthesize the frequency of different range and band.
* **PLL FM/AM demodulator:** The FM/AM radio frequencies are modulated and demodulated using this type of PLL.
* **Single RF/ Multi RF PLL:** It is used for controlling single or multiple radio frequencies.
* **Super PLL:** It is used for frequency synthesizing of radios, networks of GSM, cordless phones, etc.

**5. APPLICATIONS OF PLL**

The demand of the PLL circuit increases day by day because of its wide application in the area of electronics, communication and instrumentation. The recent applications of the PLL circuits are

in memories, microprocessors, hard disk drive electronics, RF and wireless transceivers, clock recovery circuits on microcontroller boards and optical fiber receivers. Some of the PLL applications are mentioned below.

**FREQUENCY SYNTHESIS AND MULTIPLICATION:** Many electronic systems include processors of various sorts that operate at hundreds of megahertz. Typically, the clocks supplied to these processors come from clock generator PLLs, which multiply a lower-frequency reference clock (usually 50 or 100 MHz) up to the operating frequency of the processor. Say the multiplication factor is M. Just like a voltage divider is used in feedback in voltage amplifier, output frequency of PLL is divided by *M* and applied to the phase detector, we get**, *fout=M fin****.* Also, since fin and fD must be equal, PLL multiplies fin by M.

Some systems require a periodic waveform whose frequency (a) must be very accurate and (b) can be varied in very fine steps. Hence to synthesize a required frequency, a channel control word (digital) is applied to divider block in feedback that varies the value of M. Since ***fout= M fREF*,** the relative accuracy of fout is equal to that of fREF. It is also notable that fout varies in steps equal to fREF if M changes by one each time.

**CLOCK RECOVERY:** Some data streams, especially high-speed serial data streams (such as the raw stream of data from the magnetic head of a disk drive), are sent without an accompanying clock. The receiver generates a clock from an approximate frequency reference, and then phase-aligns to the transitions in the data stream with a PLL. This process is referred to as clock recovery.

**SKEW REDUCTION:** This is one of the very popular and earliest uses of PLL. Suppose synchronous pair of data and clock lines enter a large digital chip. Since clock typically drives a large number of transistors and logic interconnects, it is first applied to large buffer. Thus, the clock distributed on chip may suffer from substantial skew with respect to data. This is an undesirable effect which reduces the timing budget for on-chip operations.

**JITTER AND NOISE REDUCTION:** One desirable property of all PLLs is that the reference and feedback clock edges be brought into very close alignment. The average difference in time between the phases of the two signals when the PLL has achieved lock is called the static phase offset. The variance between these phases is called tracking jitter. Ideally, the static phase offset should be zero, and the tracking jitter should be as low as possible.

**6. CHARGE PUMP PLL**

Charge pump is one of the important parts of PLL which converts the phase or frequency difference information into a voltage, used to tune the VCO. Before arriving at the concept of charge pump, the problem of simple PLL which uses phase detector is discussed here.

**LIMITATIONS OF SIMPLE PLL ARCHITECTURE**

For type I PLL there are always trade-offs between damping ratio of loop filter, loop filter bandwidth and the phase error. Hence the performance of PLL cannot improve beyond certain limit. Apart from this, a simple PLL suffers from a critical drawback i.e. limited acquisition range.

**Dynamics of simple PLL**

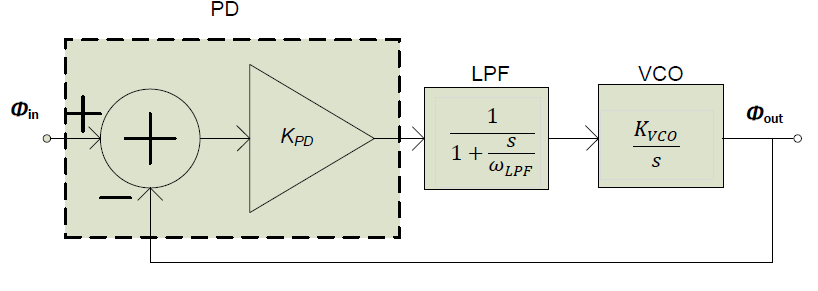
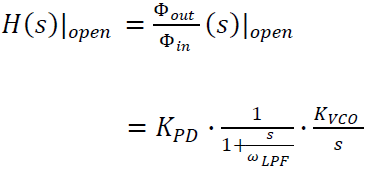
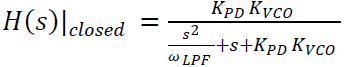


Fig4: Linear Model of Type I PLL

The open Loop transfer function of Type I PLL is:



Closed Loop transfer function of Type I PLL is:



𝜁𝜔𝑛=1/2(𝜔𝐿𝑃𝐹)

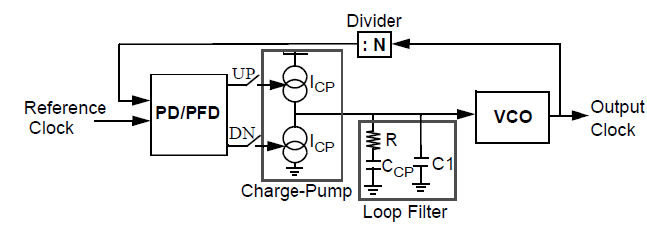
Where, 𝜔𝑛 = (𝜔𝐿𝑃𝐹.𝐾𝑃𝐷.𝐾𝑉𝐶𝑂)^1/2

𝜁 = 0.5 (𝜔𝐿𝑃𝐹 / (𝐾𝑃𝐷.𝐾𝑉𝐶𝑂)) ^1/2

When the PLL circuit is turned on, its oscillator operates at a frequency far from the input frequency, i.e., the loop is not locked. Now PLL starts acquiring a lock. The transition of the loop from unlocked to locked condition is very nonlinear process because phase detector senses unequal frequency. Also for this kind of PLL, the “acquisition range” is on the order of ωLPF, that is, the loop locks only if the difference between ωin and ωout is less than roughly ωLPF. If ωLPF is reduces to suppress the ripple on control voltage, the acquisition range decreases. Even if the input frequency has a precisely controlled value, a wide acquisition range is often necessary because the VCO frequency may vary considerably with the process and temperature.

Hence in order to remove this problem, frequency detection is also incorporated in addition to phase detection. The concept is such that let the two frequencies (reference and VCO output frequency) be equal, once these two frequencies are equal, phases are compared and VCO is tuned such that phases of reference and feedback waveform are equal. Frequencies are compared using frequency detector which generates a dc voltage equal to the difference of two input frequency and drives the VCO such that ωin = ωout. When |ωin - ωout| is sufficiently small, phase locked loop takes over, acquiring lock. Such scheme increases the acquisition range to the tuning range of VCO.

For smooth transition and minimum ripples at the output of the LPF, a type II charge pump PLL is used. The block diagram of one such PLL is as follows.



**Fig5**: Type II PLL

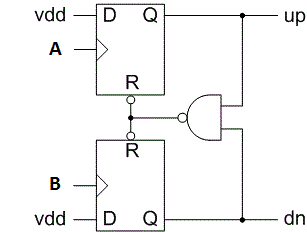
The addition of capacitor C1 prevents large jumps in the value of Vcont due to I1 and I2 mismatches and charge injection and clock feed through effects of S1 and S2. However, this capacitor adds another pole to the system thereby degrading its stability.

**7. PLL COMPONENTS**

**7.1. PHASE FREQUENCY DETECTOR:**

The phase detector (PD) compares the phase difference between two input signals and produces an error signal that is proportional to the phase difference. In the presence of a large frequency difference, a pure phase detector does not always generate the correct direction of phase error. To remedy the problem of inadequate acquisition range, a phase-frequency detector (PFD) is used that can detect both phase and frequency differences.

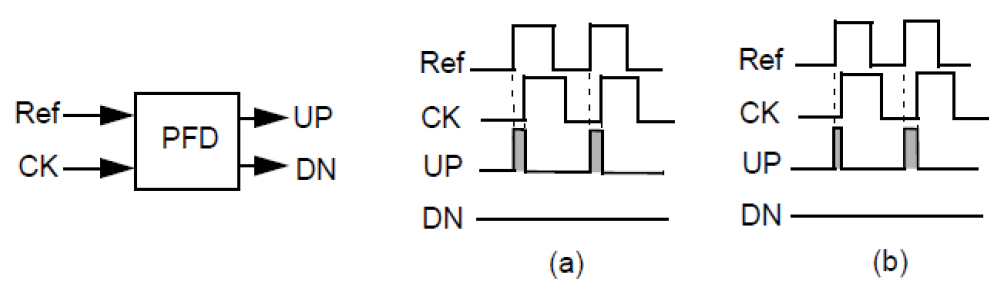
The diagram of a simple Phase Frequency detector is shown below



**Fig6**: Phase Frequency Detector

The Phase Frequency Detector consists of two edge triggered resettable D flip-flops with their D inputs tied to logical ONE. Inputs A and B serve as clock of flip-flops. If QA=QB=0 and A goes high, QA rises. If this event is followed by a rising transition on B, QB also goes high and the AND gate resets both flip-flops. In other words, QA and QB are simultaneously high for a short time but the difference between their average values still represents the input phase or frequency difference correctly.

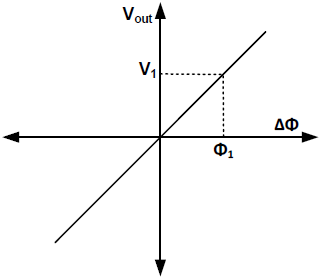
There are generally two outputs of a Phase Frequency Detector- UP and DOWN, which are useful to suggest which frequency, A or B, is higher and also to map the phase difference between the two if their frequency of operation are equal.



**Fig7**: Operation of PFD (A) FRef =FCK, ᶲRef #ᶲCK AND (B) FRef >FCK

An ideal phase detector (PD) produces an output signal whose value is linearly proportional to the difference between the phases of two periodic inputs:

Vout = KPD. 𝛥 ɸ



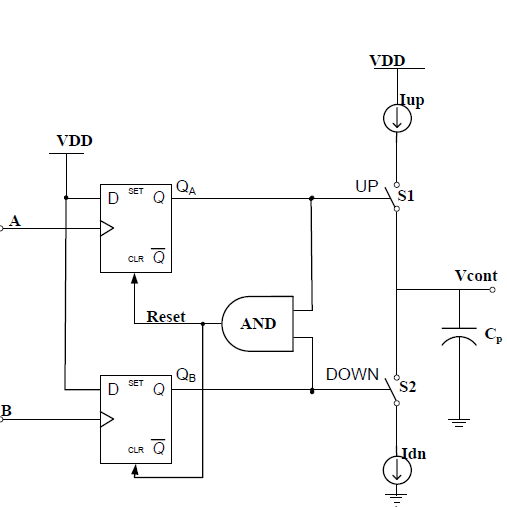
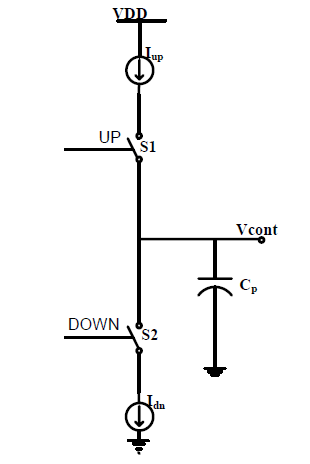
**Fig8**: Ideal Phase detector Behavior

There are several types of phase detectors in the two main categories of analog and digital. Different types of phase detectors have different performance characteristics.

In PLL applications it is frequently required to know when the loop is out of lock. The more complex digital phase-frequency detectors usually have an output that allows a reliable indication of an out of lock condition.

**7.2. CHARGE PUMP:**

The basic diagram of a charge pump is as follows.



1. (b)

**Fig9**: (a) Charge Pump Architecture (b) PFD-CP-Loop Filter Combination

QA and QB produce UP and DOWN pulses respectively. The charge pump operates in three states-

1. S1 ON, S2 OFF: This happens when UP pulse is in the high state. In such a case, I1 charges the capacitor CP.

2. S1 OFF, S2 ON: This happens when DOWN pulse is in the high state. In such a case, I2 discharges the capacitor CP.

3. S1 ON, S2 ON: This happens when both UP and DOWN pulses are in the high state. This takes place for a very short duration until the reset signal becomes high again to reset the values of QA and QB. In such a case, the voltage on CP remains constant since there is direct path for I1 to flow from VDD to ground.

Generally, I1 and I2 are almost equal to each other.

The combination of charge-pump and CP is an integrator that generates the average of UP (or DN) pulses. This average voltage on CP, after passing through the low pass filter serves as the control voltage for the oscillator. Since the VCO introduces another integrator, the loop gain of a charge-pump PLL has two poles at origin; thus, the closed loop system is unstable. To stabilize the system, a zero, ωz = 1/RCP, is introduced in the loop gain by adding a resistor, R, in series with CP.

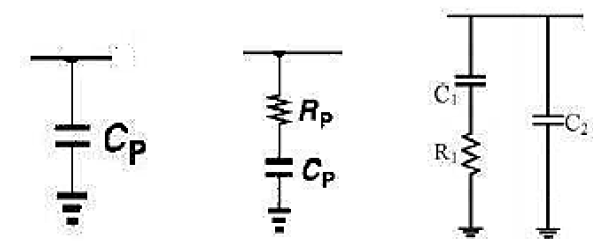
The PFD, charge pump and filter are often modeled with a linear continuous-time model. In reality, the PFD acts as a pulse modulator system and drives the charge-pump for the duration of pulse width which is equal to PFD input phase difference, Δ φ. The actual phase response is not linear because phase is cyclical. Furthermore, the phase information is discrete, sampled at the clock reference frequency.

However, a linear continuous-time approximation is often used to model the stability of an operating point. The error due to approximation is negligible if the PLL bandwidth is 1/10th or smaller than the reference clock frequency. The reference frequency determines the rate that PFD output is refreshed.

With a linear approximation, Vctrl is equal to:

𝑉𝑐𝑡𝑟𝑙/𝛥𝜑 = ((𝐶𝑃)/2𝜋).F(s), where F(s) is the transfer function of the loop filter.

**7.3. LOOP FILTER:**



(A) (B) (C)

**Fig10**: Types of Passive Loop Filter (A) Basic Type I (B) Type I with zero (C) Type II with zero

The block commonly called the PLL loop filter (usually a low pass filter) generally has two distinct functions.

The primary function is to determine loop dynamics, also called stability. This is how the loop responds to disturbances, such as changes in the reference frequency, changes of the feedback divider, or at start-up. Common considerations are the range over which the loop can achieve lock (pull-in range, lock range or capture range), how fast the loop achieves lock (lock time, lock-up time or settling time) and damping behavior. Loop parameters commonly examined for this are the loop's gain margin and phase margin. Common concepts in control theory including the PID controller are used to design this function.

The second common consideration is limiting the amount of reference frequency energy (ripple) appearing at the phase detector output that is then applied to the VCO control input. This frequency modulates the VCO and produces FM sidebands commonly called "reference spurs". The low pass characteristic of this block can be used to attenuate this energy, but at times a band reject "notch" may also be useful.

The design of this block can be dominated by either of these considerations, or can be a complex process juggling the interactions of the two. Typical trade-offs are: increasing the bandwidth usually degrades the stability or too much damping for better stability will reduce the speed and increase settling time. Often also the phase-noise is affected.

**7.4. Voltage controlled oscillator:**

An oscillator is an autonomous system that generates a periodic output without any input. For the oscillator to oscillate on a given frequency, the system includes a resonant circuit to ensure that the oscillation occurs on a given frequency. The resonant circuit can be one of a number of configurations from an LC resonant circuit in either series or parallel resonance dependent upon the circuit, or a quartz crystal, etc. Voltage controlled oscillator is a type of oscillator where the frequency of the output oscillations can be varied by varying the amplitude of an input voltage signal. Voltage controlled oscillators are commonly used in frequency (FM), pulse (PM) modulators and phase locked loops (PLL). Another application of the voltage controlled oscillator is the variable frequency signal generator itself. Within a phase locked loop, PLL, or frequency synthesizer, the performance of the voltage controlled oscillator, VCO is of paramount importance. This is because the VCO Voltage Controlled Oscillator performance determines many of the overall performance characteristics of the overall synthesizer. An ideal voltage-controlled oscillator is a circuit whose output frequency is a linear function of its control voltage.

***ωo + Kvco\*Vcont = ωout***

where ωo is the free-running frequency (output frequency when Vcont is 0) and Kvco is the VCO gain.

Most widely used architecture for implementing a CMOS Ring Oscillator is Current controlled Oscillator where current is used for frequency control. Figure 11 shows the block diagram of a complete VCO circuit. V TO I Converter is a bias circuit which provides current to the ring oscillator followed by a level shifter which aligns the oscillator output with the digital domain.

Since the phase of a PLL is adjustable, the frequency of oscillation must be tunable. In the example of an inverter ring oscillator, the frequency could easily be adjusted with controlling the supply (voltage or current) of inverters. The slope of frequency versus control signal curve at the oscillation frequency is called voltage-to-frequency (or current to-frequency) conversion gain, KVCO.

Voltage to current

Converter

Vctrl

Ibias

VCO Buffer

Current controlled

Oscillator

Fvco

**Fig11**: Basic diagram of Voltage controlled oscillator

**OSCILLATORS:**

An oscillator is a system employing positive feedback. It is constructed from an amplifier block and a frequency-selective network connected in a positive-feedback loop.

According to the standard oscillator definition, this system must have a finite output even in the absence of an input signal. The magnitude of the loop gain should be equal to unity and the phase of the loop gain should be an integer multiple of 2π for the feedback loop to provide stable oscillations. This condition is called Barkhausen criterion. This criteria guarantee that oscillation will be sustained after it starts but it does not guarantee that oscillation will start. Practically, the magnitude of the loop gain should be designed to be slightly larger than unity for the oscillation to start.

**CMOS RING OSCILLATORS:**

The most basic ring oscillator employs single-ended inverters in place of the amplification stages. In this case, an odd number N of inverter stages is needed for steady oscillations. Otherwise the oscillation latches up at a DC level which corresponds to the satisfaction of barkhausen criterion at zero frequency. Frequency of the oscillation will be 1/ (2\*N\*Td) where Td is the propagation delay of a single stage for this case.

Frequency domain analysis:

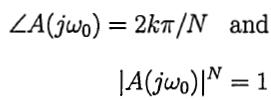
L(s) = A1(s)A2(s)……..AN(s)

Where A1(s), A2(s) and AN(s) are the s-domain transfer functions of individual delay stages. For most practical applications, the gain stages are identical so that the loop gain reduces to

L(s) = AN(s)

Where N is the number of stages and A(s) = A1(s) = A2(s) = A3(s) = AN(s).

Now according to the barkhausian criterion, the total phase difference to a multiple of 2π and the magnitude of the loop function should be one. This implies that



Phase Shift provided by each stage is given by 180/N, where N represents the number of stages in the oscillator. Ring oscillator with even number of stages can employed by configuring one stage that does not invert.

**7.5. LOOP DIVIDER:**

PLLs may include a divider between the oscillator and the feedback input to the phase detector to produce a frequency synthesizer. A programmable divider is particularly useful in radio transmitter applications, since a large number of transmit frequencies can be produced from a single stable, accurate, but expensive, quartz crystal–controlled reference oscillator. Some PLLs also include a divider between the reference clock and the reference input to the phase detector.

If the divider in the feedback path divides by N and the reference input divider divides by M, it allows the PLL to multiply the reference frequency by N/M. It might seem simpler to just feed the PLL a lower frequency, but in some cases the reference frequency may be constrained by other issues, and then the reference divider is useful. Frequency multiplication can also be attained by locking the VCO output to the Nth harmonic of the reference signal. Instead of a simple phase detector, the design uses a harmonic mixer (sampling mixer). The harmonic mixer turns the reference signal into an impulse train that is rich in harmonics. The VCO output is coarse tuned to be close to one of those harmonics. Consequently, the desired harmonic mixer output (representing the difference between the N harmonic and the VCO output) falls within the loop filter pass band.

The digital divider circuits used in Analog PLLs have to be made fully custom since there is a tight constraint on power consumption and frequency of operation. Most of the divider blocks are made asynchronous to save power.

In a synchronous counter, each flip flop is running at the clock frequency. So for a 3 bit counter, in effect, 3 flip flops are running. In an asynchronous counter, on the contrary, only the first flip flop runs at the clock frequency and the subsequent ones run at half frequencies.

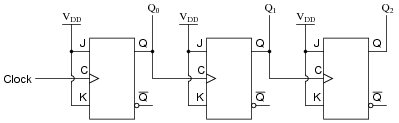


Fig12: Asynchronous Counter

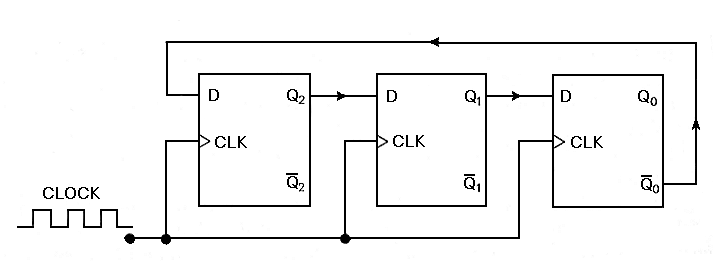


Fig13: Synchronous Counter

So, Freq\*(1+1/2+ 1/4+1/8 ….. infinity) = Freq\*2

That is, only 2 flip flops are clocked at the input frequency effectively, thus saving power.

Pdyn = C\*(V^2)\*freq

**8. AREAS OF ANALYSIS AND BLOCK DESIGNING**

**8.1. LEVEL SHIFTER**

Level shifters are used when the signal goes from one voltage domain to another voltage domain. It will amplify the signal for low power domain so that high voltage domain cells can read logic-1 or logic-0 correctly. It has been implemented using a differential pair with active load.

**Block diagram**

INPUT OUTPUT

Inverter Differential pair with active load Inverter

**Fig14**: Level Shifter Basic diagram

**Transient analysis**

Many transient simulations has been done to understand the working of the level shifter and to know about its robustness. There are basically two modes normal mode of operation and power done mode of operation. All the parameters like duty cycle, slope of the output waveform were checked at normal mode. Also the maximum current which flows through the circuit is found at the worst corner when the circuit is operating in normal mode. Power down simulations were carried to find the leakage current of the circuit at various corners and temperature.

**MONTE CARLO SIMULATION**

Performance parameters are most comprehensively observed by using Monte Carlo simulations on the circuit.

Monte Carlo methods (or Monte Carlo experiments) are a broad class of computational algorithms that rely on repeated random sampling to obtain numerical results; i.e., by running simulations many times over in order to calculate those same probabilities heuristically. They are often used in physical and mathematical problems and are most suited to be applied when it is impossible to obtain a closed-form expression or infeasible to apply a deterministic algorithm.

Monte Carlo methods are mainly used in three distinct problems: optimization, numerical integration and generation of samples from a probability distribution.

In level shifter it works by simulating for output duty cycle at a large number of samples by varying certain process parameters, to eventually observe the nature of variation of duty cycle with variation of samples.

Some changes were made to the circuit to reduce the leakage current of the circuit. A PMOS which acted as a switch was connected at the top of the circuit to control the leakage of the circuit.

PMOS

INPUT OUTPUT

Inverter Differential pair with active load Inverter

**Fig15**: Level Shifter Basic diagram with some changes

Leakage was reduced at the cost of some normal mode performances of the circuit.

**8.2. PHASE FREQUENCY DETECTOR**

**SIMULATIONS**

Normal mode and power down simulations were carried out to understand the working of the circuit and to find the leakage current respectively.

**RESET PULSE WIDTH**

Reset Pulse width helps to decide the operating frequency of the circuit. If the frequency is circuit is increased beyond its operating frequency it can be observed that some edges of the signal are missed which leads to improper functioning of the phase frequency detector. It is measured at low operating voltage supply of the circuit.

**FLIPFLOP MISMATCH**

**DUTY CYCLE**

Duty cycle was both increased and decreased to check the performance of the circuit. It was done to find how the circuit responded when duty cycle is varied from one extreme to other.

**LOAD CAPACITANCE**

Capacitance was increased using lumped capacitor to check the circuit’s performance. It was done to check the circuit’s response to increase in capacitance value and study the problems that may occur .

**DELAY BETWEEN UP AND NUP (MISMATCH)**

UP and NUP two outputs were compared to check the mismatch between them. Width of the transistors was changed to decrease the delay but it was observed that delay can’t be reduced further. If delay was decreased it leads to increase in the slope (rise time and fall time) of the output signal which can cause further problems.

**SWITCH USAGE TO DECREASE LEAKAGE CURRENT**

Same idea as the level shifter was used here to reduce the leakage current of the circuit but because of the PMOS connected at the top of the circuit created some issues and hence no changes were made in the circuit.

**8.3. LOCK CIRCUIT**

**SIMULATION AND ANALYSIS**

Normal mode and power down simulations were carried out to check the performance of the circuit and to find out normal and leakage current. Locking and unlocking frequencies were calculated. In one simulation input frequency was increased and in another simulation input value was decreased. The output waveforms showed a hysteresis behavior in the circuit. Also, it can be observed that the accuracy of the lock circuit can be increased at the cost of time taken by the circuit to lock itself.

Suppose the accuracy of circuit is X%. Then

Voltage Voltage

Time Time

1. When Frequency is Increased (**B**) When Frequency is Decreased

**Fig16**: Hysteresis behavior of the lock circuit

**8.4. FRACTIONAL LOCK CIRCUIT**

**SIMULATIONS AND ANALYSIS**

Normal mode simulations were done to understand the working of the circuit and to check its robustness. Power down simulations was also carried out to check the leakage current of the circuit.

**8.5. VOLTAGE CONTROLLED OSCILLATOR**

**FINDING VCONT RANGE**

Some work was to be done to find out the Vcontrol range of the voltage controlled oscillator. These were:

1. Maintain the mosfet used for converting voltage to current must remain in saturation.
2. Mosfet of the previous stage which generate the value of vcont must also remain in saturation.

Mosfet used to convert the voltage to current was also operated in sub threshold region to check whether that can be done. It was found that the variation across temperature and corners were very high when operated in sub threshold region hence it must operate in saturation.

Also the slope of the VCO was found. It was measured in GHz/V.

**UNDERSTANDING RING OSCILLATOR**:

Simulations were carried out to study the behavior of ring oscillator. Input current is varied to see the variation of frequency with input current. Also, the gain of each stage was measured and varied to find out the minimum gain after which the oscillator stops to oscillate.

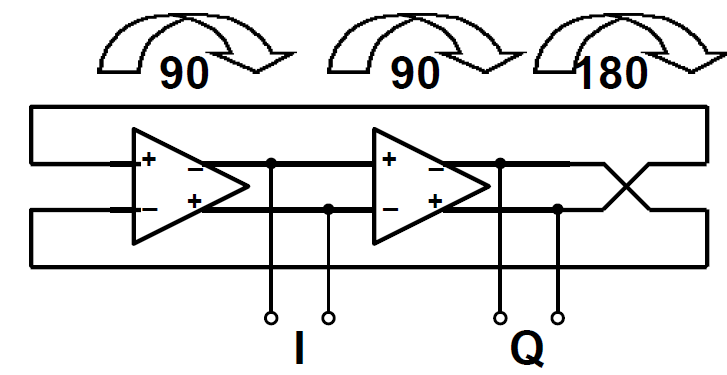
**DESIGNING OF 90 DEGREE PHASE SHIFT RING OSCILLATOR**

**Two stage ring oscillator**

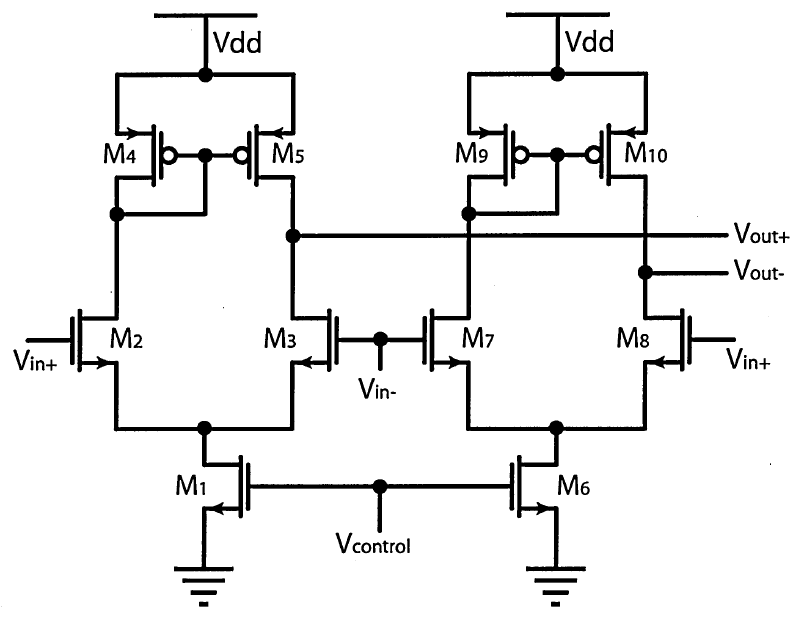
To satisfy Barkhausian oscillation criteria a minimum of three stages for a ring oscillator with single pole system should be used. Figure below shows a ring oscillator employing a double differential delay stage to supply the required extra phase and gain.

The small-signal characteristics of the half-circuit are similar to a differential amplifier with a current mirror load. The current mirror load doubles the gain of the differential amplifier by folding the small signal current of the other side. When compared to the standard differential pair stage, this design inhibits an additional pole-zero pair resulting from the extra nodes created at the drain/gates of the unbalanced current mirror loads. This supplies the required extra phase shift to sustain a steady oscillation.

Two differential pair with active current mirror load is connected and as a pair they act as a differential amplifier. Now two pairs are connected back to back to get a 90 degree phase shift. Tail current was used to vary the frequency of operation.



**Fig17**: Design of a 90 degree phase shift ring oscillator



**Fig18**: Double Differential delay stage

In total four differential pair with active load is used. Two of them are used as a pair so that they act as a differential pair. Hence two differential pairs are made and a phase shift of 90 degree is obtained.

**9. CONCLUSION**

Working with complex electronic systems like PLLs is in itself a very challenging task. The limited time frame was utilized in the best manner possible to get familiar with the design perspective and get insight about the performance affecting parameters by simulation of the circuit. The blocks of the PLL that were studied were simulated using Eldo and redesigned accordingly to meet the given specifications. In 90nm technology, design and analysis was done on VCO, level shifter, phase frequency detector, lock circuit and fractional lock circuit. All the blocks mentioned were characterized successfully and verified across all process corners.

The simulation results, schematics and waveforms cannot be disclosed as they are considered confidential to the company.

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**10. References**

[1] Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, Tata-McGraw Hill 2002, Ch. 15, pp. 532-578

[2] Ben G. Streetman & Sanjay Banerjee, “Solid State Electronic Devices”.

[3] Eugene R. Hnatek, “Applications of Linear Integrated Circuits”, John Wiley & Sons, 1975.

[4] H.Djahanshahi and C. Salam, “Differential CMOS circuits for 622-MHz/933-MHz clock and data recovery applications,” IEEE J. Solid-State Circuits, vol. 35, no. 6, pp. 847-855, June 2000.

[5] STMicroelectronics confidential execution guides and tutorials about the build flow and details of tools used.