Computer organization and architecture exit exam model questions

1. Among the given options choose correct one
   I. Von Neumann Architecture shares common memory for instructions and data.
   II. Harvard Architecture has separate memory for instruction and data
   A. Only I is true
   B. I and II are true
   C. Only II is true
   D. I and II are false
2. Suppose we want to compute the value y^6, $\sqrt{y}$, $y^{1/3}$ using the value of y. which of the following among Flynn's CPU classification will be best suited for above calculation?
   A. SISD Stream
   B. SIMD Stream
   C. MISD Stream
   D. MIMD Stream
3. Vector and Array belongs to which class of Flynn's classification.
   A. SISD Stream
   B. SIMD Stream
   C. MISD Stream
   D. MIMD Stream
4. Choose the correct statement(s) below:
   S1: CISC supports Fixed Length Instruction Format
   S2: RISC supports Variable Length Instruction Format
   S3: CISC supports Immediate Operand
   S4: RISC Allows only register operand
   A. S1
   B. S2
   C. S3
   D. S4
5. Assembly language
   A. Uses alphabetic codes in place of binary numbers used in machine language
   B. Is the easiest language to write programs
   C. Need not be translated into machine language
   D. None of these
6. In computers, subtraction is generally carried out by
   A. 9's complement
   B. 1's complement
   C. 2's complement
   D. 10's complement
7. The amount of time required to read a block of data from a disk in to memory is composed of seek time, rotational latency, and transfer time. Rotational latency refers to
   A. The time it takes for the platter to make a full rotation
   B. The time it takes for the read-write head to move into position over the appropriate track
   C. The time it takes for the platter to rotate the correct sector under the head
   D. None of the above
8. The circuite used to store one bit of data is known as
   A. Register
   B. Encoder
   C. Flip Flop
   D. Decoder
9. The average time required to reach a storage location in memory and obtain its content is called
   A. Seek time
   B. Access time
   C. Transfer time
   D. Turnaround time
10. The idea of cache memory is based
    A. On the property of locality of reference
    B. On the heuristic 90-10 rule
    C. On the fact that references generally tend to cluster
    D. All of the above

11. Which of the following is lowest in memory hierarchy?
    A. Cache memory
    B. RAM
    C. Register
    D. Secondary memory
12. Which of the following best characterize a computer that uses memory-mapped I/O?
    A. the computer provides special Instruction for manipulating the I/O port
    B. I/O ports are placed at addresses on bus and are accessed just like other memory location
    C. to perform an I/O operation, it is sufficient to place the data in an address and call the channel to perform the operation
    D. ports are reference only by memory-mapped Instruction of the computer and are located hard-wired memory location
13. Suppose, after analyzing a new cache design, you discover that the cache has far too many conflict misses, and this needs to be resolved. You know that you must increase associativity in order to decrease the number of cache misses. What are the implications of increasing associativity?
    A. Slower cache access time
    B. Increase index bits
    C. Increase block size
    D. All of these
14. Identify the false statements:
    S1: Separate I/O address space does not necessarily mean that I/O address lines are physically separated.
    S2: Address decoder is an essential part of the I/O interface.
    A. Only S1
    B. Only S2
    C. Both S1 and S2
    D. Neither S1 nor S2
15. In 2's compliment addition, the overflow
    A. Is flagged whenever there is carry from sign bit addition
    B. Cannot occur when a +ve value is added to a –ve value
    C. Is flagged when the carriers from sign bit and previous bit match
    D. None of the above
16. The value of a float type variable is represented using the single-precision 32-bit floating point format of IEEE-754 standard that uses 1 bit for sign, 8 bits for biased exponent and 23 bits for mantissa. A float type variable X is assigned the decimal value of 14.25. The representation of X in hexadecimal notation is
    A. C1640000H
    B. 416C0000H
    C. 41640000H
    D. C16C0000H
17. DMA interface unit eliminates the need to use CPU registers to transfers data from
    A. MAR to MBR
    B. MBR to MAR
    C. I/O units to memory
    D. Memory to I/O units
18. Compared to RISC processors, CISC processors contain _____.
    A. More registers and smaller instruction set
    B. Larger instruction set and fewer registers
    C. Fewer registers and smaller instruction set
    D. More transistor elements
19. For the given Sequence of micro-operations.
    MBR ← PC
    MAR ← X
    PC ← Y
    Memory ← MBR

Which among the following is a possible operation performed by this Sequence?

A. Instruction fetch
B. Operand fetch
C. Conditional branch
D. Initiation of Interrupt

20. Which of the following miss is definite to occur in cache memory?
A. Cold-start miss
B. Capacity miss
C. Conflict miss
D. All of these

21. Which of the following are not considered as part of the I/O interface which connects bus and I/O device?
(i) Address decoder
(ii) Control circuitry
(iii) Data and status register
A. Only (i) and (iii)
B. Only (ii) and (iii)
C. (i), (ii) and (iii)
D. None of these

22. A computer has a cache memory of size 256 Kbyte, and it is a 4-way set associated with a block size of 32 Bytes. The processor sends 32-bit addresses to the cache controller. Each cache tag directory entry contains, in addition, to address tag, two valid bits, one modified bit, and 1 replacement bit.
The number of bits in the tag field of an address is

A. 11
B. 14
C. 16
D. 27

23. Consider the following statements:
I.Time taken for a single instruction on a pipelined CPU is less than or equal to the time taken on a non-pipe lined (identical) CPU.
II. In a uniform delay pipeline, the execution time for a single instruction is equal to the execution time in the non-pipelined processor. (Assume no buffer delay)
Which of the above statement(s) is correct?

A. Only I
B. Only II
C. Both I and II
D. Neither I nor II

24. The amount of ROM needed to implement a 4-bit multiplier is
A. 64 bits
B. 128 bits
C. 1 K bits
D. 2 K bits

25. Register renaming is done in pipeline processors
A. as an alternative to registering allocation at compile time
B. For efficient access to function parameters and local variables
C. to handle certain kinds of hazards
D. as part of address translation

26. A two-way **set-associative cache** has lines of 16 bytes and a total cache size of 8 K bytes. The 256 M byte main memory is Byte addressable. Which one of the following main memory blocks are mapped onto the set ‘0’ of the cache memory?
A. (CFED09B)16
B. (FCED90C)16
C. (CFED00B)16
D. (FECD10C)16

27. Which of the following operation is mainly performed by RAM?
A. Read only
B. Read and write
C. Write only
D. Depends on the system

28. Match the computer storage type in the left column with their example in the right column:

1. Flash Drive	i. CD
2. Cloud Storage	ii. Dropbox
3. Optical Storage	iii. SSD
4. Hard Drive	iv. SD card

A. 1 – iii, 2 – i, 3 – ii, 4 – iv
B. 1 – iv, 2 –ii, 3 – i, 4 – iii
C. 1 – iii, 2 – i, 3 – iv, 4 – ii
D. 1 – iv, 2 – iii, 3 – i, 4 – ii

29. Computer architecture CISC is used mostly in which computers?
A. Supercomputers
B. Automation computers
C. Analog computers
D. Mainframe computers

30. EBCDIC coding scheme uses ___ bits to code different characters.
A. 4
B. 8
C. 16
D. 32

31. Which of the following is used in main memory
A. DDR
B. DRAM
C. SRAM
D. PRAM

32. The first instructor of bootstrap loader program of an operating system is stored in
A. RAM
B. Hard Disk
C. BIOS
D. None

33. Which of the following is fastest memory?
A. Secondary Memory
B. Cache Memory
C. Auxiliary Memory
D. None of the above

34. What is computer architecture?

A. set of categories and methods that specify the functioning, organisation, and implementation of computer systems

B. set of principles and methods that specify the functioning, organisation, and implementation of computer systems

C. set of functions and methods that specify the functioning, organisation, and implementation of computer systems

D. None of the mentioned

35. What is computer organization?

A. structure and behaviour of a computer system as observed by the user

B. structure of a computer system as observed by the developer

C. structure and behaviour of a computer system as observed by the developer

D. All of the mentioned

36. To reduce the memory access time we generally make use of _____
A. SDRAM's
B. Heaps
C. Cache's
D. Higher capacity RAM's

37. Which of the following is world's first general-purpose Intel microprocessor
A. 8086
B. 8080

C. 4004 D. 8008

38. A processor performing fetch or decoding of different instruction during the execution of another instruction is called _____ .
    A. Pipe-lining C. Parallel Computation
    B. Super-scaling D. None of these
39. CPU does not perform the operation ……
    A. data transfer C. arithmetic operation
    B. logic operation D. all of the above
40. The load instruction is mostly used to to hold temporarily operands and results of ALU operations.
    A. Accumulator C. Program counter
    B. Instruction Register D. Memory address Register
41. Which of the following registers is used to keep track of address of the memory location where the next instruction is located?
    A. Memory Address Register C. Instruction Register
    B. Memory Data Register D. Program counter
42. The interconnection structure must support the following types of transfers except
    A. Memory to processor C. I/O to processor
    B. I/O to memory D. None
43. $(2FAOC)_{16}$ is equivalent to
    A. $(195\ 084)_{10}$ C. Both (A) and (B)
    B. $(00101111101000001100)_2$ D. None of these
44. The average time required to reach a storage location in memory and obtain its contents is called the
    A. seek time C. access time
    B. turnaround time D. transfer time
45. The idea of cache memory is based
    A. on the property of locality of reference
    B. on the heuristic 90-10 rule
    C. on the fact that references generally tend to cluster
    D. all of the above
46. Cache memory acts between
    A. CPU and RAM C. CPU and Hard Disk
    B. RAM and ROM D. None of these
47. Which one of the following is not visible to user
    A. General Purpose registers C. Instruction registers
    B. Data register D. Address register
48. A Stack-organised Computer uses instruction of
    A. Indirect addressing C. Zero addressing
    B. Two-addressing D. Index addressing
49. In computers, subtraction is carried out generally by
    A. 1's complement method C. signed magnitude method
    B. 2's complement method D. BCD subtraction method
50. A group of bits that tell the computer to perform a specific operation is known as
    A. Instruction code C. Accumulator
    B. Micro-operation D. Register
51. (-27) can be represented in a signed magnitude format and in a 1’s complement format as

A. 111011 & 100100
B. 100100 & 111011
C. 011011 & 100100
D. 100100 & 011011

52. When CPU is executing a Program that is part of the Operating System, it is said to be in _____.
A. Interrupt mode
B. System mode
C. Half mode
D. Simplex mode

53. The multiplicand register & multiplier register of a hardware circuit implementing booth's algorithm have (11101) & (1100). The result shall be _____.
A. $(812)_{10}$ B. $(-12)_{10}$ C. $(12)_{10}$ D. $(-812)_{10}$

54. Cache memory-
A. has greater capacity than RAM
B. is f aster to access than CPU Registers
C. is permanent storage
D. faster to access than RAM

55. Which memory unit has lowest access time?
A. Cache
B. Registers
C. Magnetic Disk
D. Main Memory

56. Which of the following memory unit communicates directly with the CPU?
A. Auxiliary memory
B. Main memory
C. Secondary memory
D. None of the above

57. What is the content of stack pointer (SP)?
A. Address of the top element in the stack
B. Address of current instruction
C. Address of next instruction
D. None of the above

58. What does a computer bus line consists of?
A. Set of parallel lines
B. Accumulators
C. Registers
D. None of the above

59. In which of the following term the performance of cache memory is measured?
A. Chat ratio
B. Hit ratio
C. Copy ratio
D. Data ratio

60. In which of the following addressing mode the instruction itself contains the value to be used
A. Implicit
B. Immediate
C. Direct
D. Register

61. The most important fundamental instruction design issues include the following except
A. Instruction formats
B. Registers
C. Addressing mode
D. None of the above

62. Write through technique is used in which memory for updating the data

A. Virtual memory
B. Auxiliary memory
C. Cache memory
D. Main memory

63. Which of the architecture is power efficient?
A. RISC
B. ISA
C. IANA
D. CISC

64. Both the CISC and RISC architectures have been developed to reduce the _____
A. Time delay
B. Semantic gap
C. Cost
D. All of the mentioned

65. The difference in the address and data connection between DRAM's and SDRAM's is _____
A. The requirement of more address lines in SDRAM's
B. The usage of a buffer in SDRAM's
C. The usage of more number of pins in SDRAM's
D. None of the mentioned

66. During a write operation if the required block is not present in the cache then _____ occurs.
A. Write miss
B. Write latency
C. Write hit
D. Write delay

67. The number successful accesses to memory stated as a fraction is called as _____
A. Access rate
B. Success rate
C. Hit rate
D. Miss rate

68. . The two phases of executing an instruction are _____
A. Instruction decoding and storage
B. Instruction fetch and instruction execution
C. Instruction execution and storage
D. Instruction fetch and Instruction processing

69. _____ is used to choose between incrementing the PC or performing ALU operations.
A. Conditional codes
B. Multiplexer
C. Control unit
D. None of the mentione

70. The pipelining process is also called as _____
A. Superscalar operation
B. Assembly line operation
C. Von Neumann cycle
D. None of the mentioned