National Taiwan University
Graduate Institute of Electronics Engineering
Department of Electrical Engineering
Physical Design for Nanometer ICs, Spring 2017

May 28, 2017
Handout #17
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Programming Assignment #4: Steiner-Tree Construction (due 6pm, June 17th, 2017 on-line)

Submission URL:

http://eda.ee.ntu.edu.tw/~yslu/pd17/pa4_submission/

Online Resources:

http://eda.ee.ntu.edu.tw/~yslu/pd17/arearouting.tar.gz

Modified form Problem #2 of the 2017 IC/CAD Contest @ ICCAD.

1. Problem Statement

This programming assignment asks you to construct a Steiner-tree router that can connect pins for a single net on a single-layer chip. Given a set of pins for a single net, the Steiner-tree router routes all pins within a chip. The pins are connected by horizontal lines (H-line) and/or vertical lines (V-line). Steiner points are allowed to be used during routing.

The objective of Steiner-tree routing is to minimize the total routing wirelength. The total routing wirelength W of a set of P can be computed by

$$C = \sum_{p_i \in P} w(p_i) + Disjoint\ \ cost$$

where p_i denotes an H-line or a V-line in the line segment set P, and $w(p_i)$ denotes the real routing wirelength of p_i. The disjoint cost is evaluated by

$$Disjoint\ \ cost = 2 \times (\#unconnected\ \ pins) \times (half\ \ perimeter\ \ of\ \ the\ \ chip\ \ boundary)$$

Note that a route which has any net routed out of the chip boundary is a failed result.

2. Input

Input Format	Sample Input
Boundary = *(LLx,LLy),(URx,URy)* NumPins = *number* PIN *name (x,y)* …	Boundary = (0,0), (100,100) NumPins = 3 PIN p1 (20, 30) PIN p2 (50, 30) PIN p3 (50, 90)

The input file starts with the chip boundary, followed by the description of pins. The description of each pin contains the keyword PIN, followed by the name and the coordinate of the pin. See the sample input for the format of a net with three pins.

3. Output

Output Format	Sample Output
NumRoutedPins = *number* WireLength = *number* H-line (x1,y) (x2,y) V-line (x,y1) (x,y2) …	NumRoutedPins = *3* WireLength = 90 V-line (50,30) (50,90) H-line (20,30) (50,30)

In the program output, you are asked to give the number of pins, the routing wirelength, and the coordinates of routed net segments. Note that you can output the H-line/V-line in any order.

4. Language/Platform

- Language: C or C++. **Please specify your programming language.**
- Platform: Linux. **Please develop your programs on a server in the EDA Union Lab**

5. Submission

You need to submit the following materials in a .tar or a .zip file (e.g., f04943094-p3.zip)

at the course submission website by the deadline: (1) all source codes in the src/ directory, (2) executable binaries named as legalizer, (3) a text readme file named as readme.txt, and (4) a report named as report.doc on the algorithm used in your program. Note that any wrong terminology or file format will cause a severe penalty.

6. Evaluation

This programming assignment will be graded based on the (1) correctness of the program, (2) solution quality, (3) running time (restricted to one hour for each case), (4) report.doc and (5) readme.txt. Please check these items before your submission.

7. Online Resources

Benchmarks, readme.txt, and report.doc can be found at the submission website.

8. References

You may refer to these previous works to find some algorithms for Steiner-tree routing.

[1] C.-W. Lin, S.-Y. Chen, C.-F. Li, Y.-W. Chang, and C.-L. Yang, "Obstacle-Avoiding Rectilinear Steiner Tree Construction Based on Spanning Graphs," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, Vol. 27, No. 11, pp. 2007-2016, November 2008.

[2] C. Chu and Y.-C. Wong, "FLUTE: Fast Lookup Table Based Rectilinear Steiner Minimal Tree Algorithm for VLSI Design," in *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, Vol. 23, No. 11, pp. 696-701, November 2004.