ENSC 450
VLSI Design - Phase 04

Daimon Gill
Siavash Rezghi
Zi Zhou Qu

For Dr. Anita Tino and Sheida Alan

Purpose of Lab 4

- Obtain an accurate description of core, take into account P&R, replace models with implementation
- Perform a full back-end design flow for our chosen core using a single .tcl script
  - Import design files and technology libraries to Cadence Innovus
  - Setup floor planning parameters such as density
  - Build power ring and power net around block for power distribution
  - Perform cell placement and post-placement optimization
  - Synthesize clock tree and perform post CTS optimization
  - Route connections between cells
  - Generate final Verilog file

- Compare back-end results with lab 1 front-end results in terms of floor area, clock tree timing and operating frequency, average power and testbench vcd power.

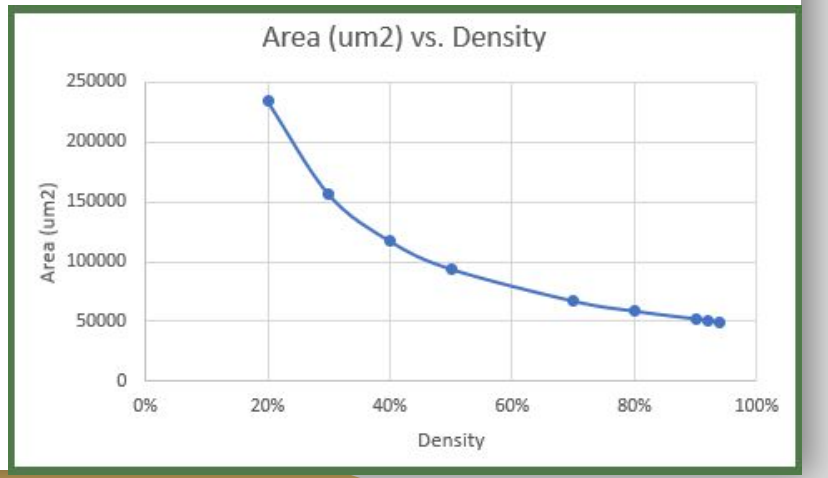
- Verify functionality of core is preserved after back-end implementation using testbench

Procedure

1. Ensured that various P&R scripts worked with our core and created a single script.
2. Fixed input transition time violations.
3. Ran the master script at periods of 6.67ns - 12.5ns, at densities ranging from 0.2 - 0.94 (35 times).
4. Made comparisons of timing, area, and power from our results.
5. Selected an optimal frequency.
6. Ensured correct functionality of our core at the new optimal frequency via post-synthesis simulation.
7. Made comparisons with lab 1.

Notes

- As density increased, area decreased.
- Area was substantially larger than lab 1.
- Higher frequencies were prone to DRC violations.
- Densities larger than 0.92 were prone to DRC violations.
- The master script took ~6 minutes to run.



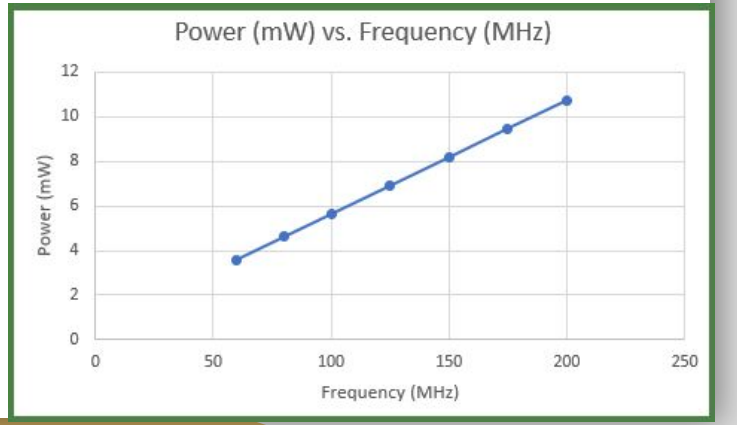
AES-128 core - Post P&R Netlist

Area	Density	Frequency	Slack	Average Power	VCD Power
52,012 um^2	0.9	125 MHz	1.324	6.9 mW	1.5 mW

Max Skew	Latency	Number of Levels	Number of Clock Buffers	Number of Sinks
89.5ps	89.5ps - 89.5ps = 0ps	0	169	262

Post Layout Simulation:

- Verified correct functionality on the aeskey128.final.v netlist

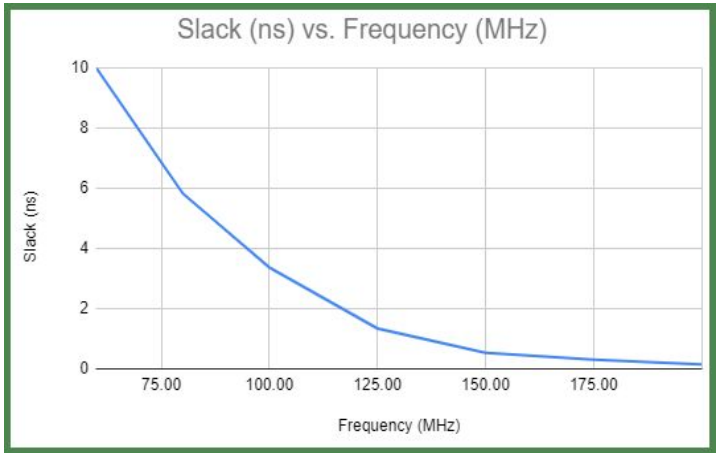


Critical Path:

- Contains 55 cells
- 8 Clock buffers
- Involved in a substitution operation

Comparison of Lab 4 vs Lab 1

Libraries Used	FreePDK	Lab 4 (0.9)	Lab 4 (0.8)
Area (um^2)	46,773	52,012	58,012
Slack (ns)	Slack Met (0.14)	Slack Met (1.32)	Slack Met (0.136)
Frequency	200 MHz	125 MHz	200 MHz
Average Power	0.9 mW	6.9 mW	7.1 mW
VCD Power	1 mW	1.5 mW	1.7 mW



- Substantial degradation in timing, area, and power
- Lab 4 at density 0.8 contained DRC violations