ENSC 450
VLSI Design - Phase 02

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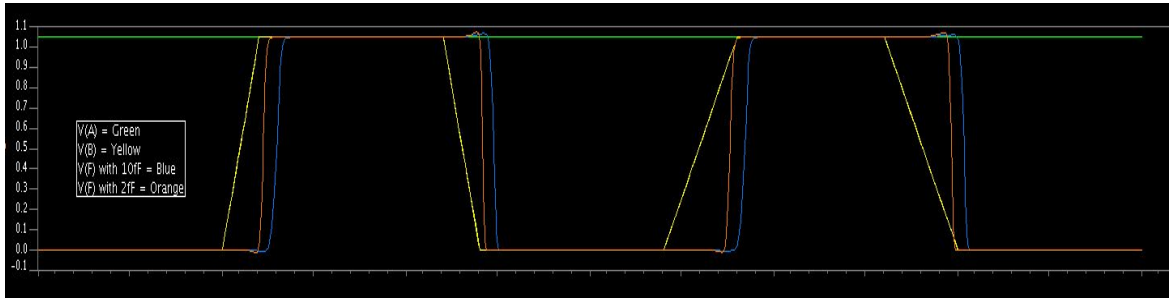
Standard Cell Area and Capacitance

- Area of cell = (sum of transistor areas in cell) * (drive strength) * (unit area)
- Capacitance of cell = (single terminal input capacitance) * (drive strength) * (unit capacitance)
- Data values for worst case transitions for rise propagation delay Tpdr
  - NOT: “1” to “0”
  - NAND: “11” to “10”
  - NOR: “10” to “00”
  - AND: “10” to “11”

X1	NOT	NAND	NOR	AND	X4	NOT	NAND	NOR	AND
Area (um^2)	3	8	10	11	Area (um^2)	12	32	40	44
Gate Cap (fF)	3	4	5	4	Gate Cap (fF)	12	16	20	16

AND_X1 Results




```
  *** parameter load =    2.000E-15 ***

******
and_x1

 ******  transient analysis tnom=  25.000 temp= 125.000 *****
  tpdf_1ns=  5.7701E-10  targ=  1.2077E-08   trig=  1.1500E-08
  pdf_2ns=  8.2140E-10  targ=  2.4821E-08   trig=  2.4000E-08
  tpdr_1ns=  6.1136E-10  targ=  6.1114E-09   trig=  5.5000E-09
  tpdr_2ns=  8.0889E-10  targ=  1.8809E-08   trig=  1.8000E-08
  ttr_1ns=  1.0123E-10  targ=  6.1602E-09   trig=  6.0589E-09
  ttr_2ns=  1.1450E-10  targ=  1.8860E-08   trig=  1.8745E-08
  ttf_1ns=  2.6928E-10  targ=  6.1000E-09   trig=  5.8308E-09
  ttf_2ns=  3.6217E-10  targ=  1.8812E-08   trig=  1.8450E-08

        ***** job concluded

  *** parameter load =    1.000E-14 ***

******
and_x1

 ******  transient analysis tnom=  25.000 temp= 125.000 *****
  tpdf_1ns=  8.7823E-10  targ=  1.2378E-08   trig=  1.1500E-08
  pdf_2ns=  1.1617E-09  targ=  2.5162E-08   trig=  2.4000E-08
  tpdr_1ns=  9.8153E-10  targ=  6.4815E-09   trig=  5.5000E-09
  tpdr_2ns=  1.2075E-09  targ=  1.9207E-08   trig=  1.8000E-08
  ttr_1ns=  1.6542E-10  targ=  6.5531E-09   trig=  6.3877E-09
  ttr_2ns=  1.6438E-10  targ=  1.9282E-08   trig=  1.9118E-08
  ttf_1ns=  6.2630E-10  targ=  6.5939E-09   trig=  5.9676E-09
  ttf_2ns=  6.7341E-10  targ=  1.9321E-08   trig=  1.8648E-08
```

HSpice Simulation:

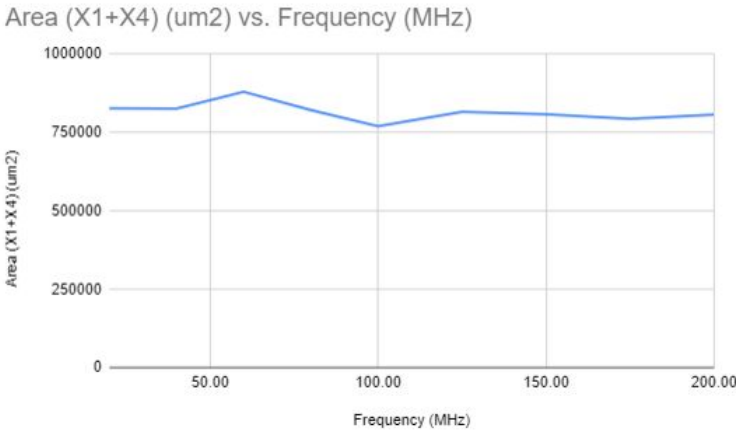
- T_{tran} = 1ns, C_{load} = 2fF
- T_{tran} = 1ns, C_{load} = 10fF
- T_{tran} = 2ns, C_{load} = 2fF
- T_{tran} = 2ns, C_{load} = 10fF
- Collected values for T_{PDF}, T_{PDR}, T_{tf}, T_{tr}

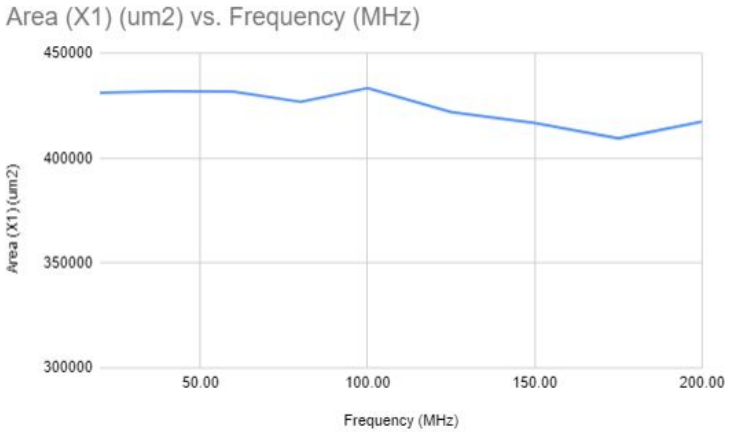
Waveform Comments:

- C_{load} = 2fF in Orange
- C_{load} = 10fF in Blue
- Rise Transitions: ‘10’ -> ‘11’
- Fall Transitions: ‘11’ -> ‘10’
- Higher load capacitance results in slower transitions

- X1 vs X4:
- X4 cells had expected behaviour of less delay

X1 and X1+X4 Area vs. Frequency





Synthesis Result Comparison

Libraries Used	FreePDK	X1 only	X1 and X4
Area (um^2)	46,773	431,859	826,802
Critical Path (ns)	Slack Met (0.14)	Slack Met (0.0)	Slack Met (0.67)
Data Arrival (ns)	4.70	16.67	24.33
Period (ns)	5	16.67	25
Frequency	200 MHz	60 MHz	40 MHz