ENSC 450
VLSI Design - Phase 03

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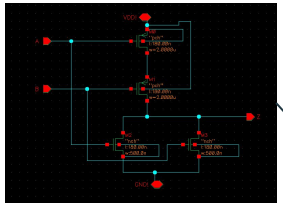
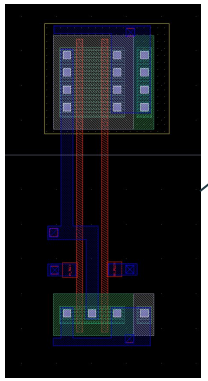
Purpose of Lab 3

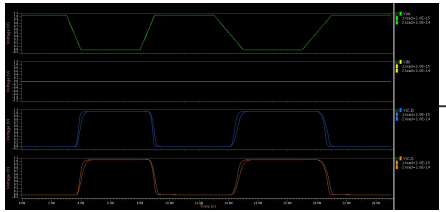
- Manually create cell layout for use with synthesis
  - Create LVS matching schematic and layout in Cadence Virtuoso according to DRC rules
  - Extract Hspice circuit from layout
- Compare synthesis results using FreePDK, Lab 2 Hspice cells, Lab 3 Virtuoso cells
  - Repeat synthesis using only Lab 3 cells
  - Repeat synthesis using both Lab 2 and Lab 3 cells
  - Compare slack, area, and static power consumption

Process for each standard cell

1. Schematic was created and functionality was verified by observing waveforms by the extracted netlist
2. Layout was created and LVS performed against the schematic to ensure correct functionality
3. HSpice simulations conducted on the extracted netlists
4. Timing, power, and area measurements were included in liberty files
5. Synthesis conducted with new liberty files





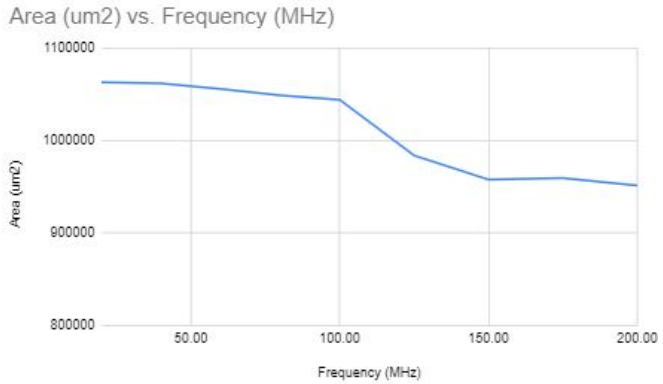


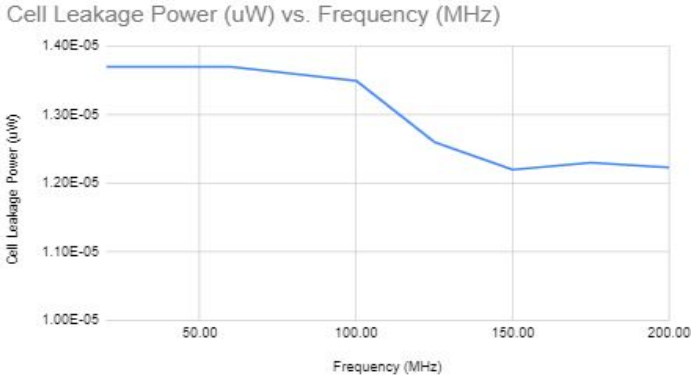
HSpice

.lib File

All standard cells completely passed LVS and DRC checks.

Lab 3 Performance and Power

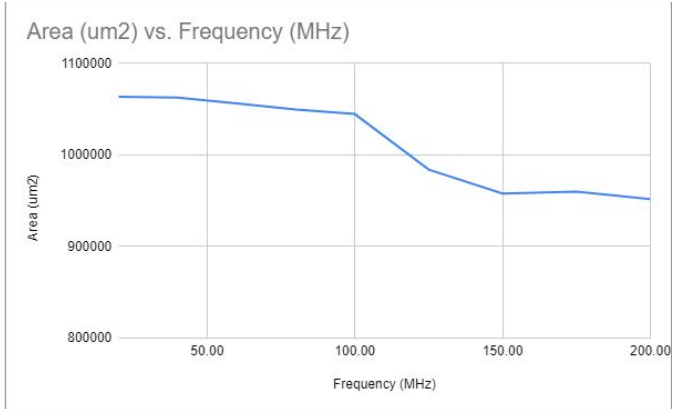


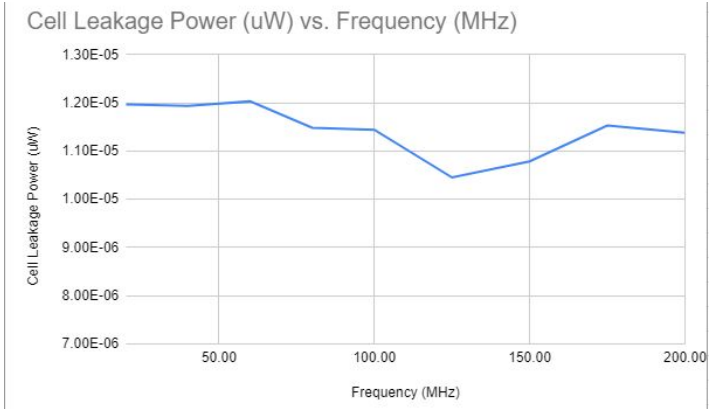


Operational Frequency: 100 MHz

- Slack violated at frequencies greater than 150 MHz
- Slack first met at 125 MHz
- 100 MHz selected to provide a margin

Lab 2 + Lab 3 Performance and Power





Operational Frequency: 100 MHz

- Slack violated at 150 MHz (-0.06 ns)
- Slack first met at 125 MHz (0 ns)
- 100 MHz selected to provide a margin

Comparison of Libraries

Libraries Used	FreePDK	Lab 2	Lab 3	Lab 2 + Lab 3
Area (um^2)	46,773	752,864	1044660	1345315
Slack (ns)	Slack Met (0.14)	Slack Met (0.0)	Slack Met (0.0)	Slack Met (0.0)
Frequency	200 MHz	80 MHz	100 MHz	100 MHz