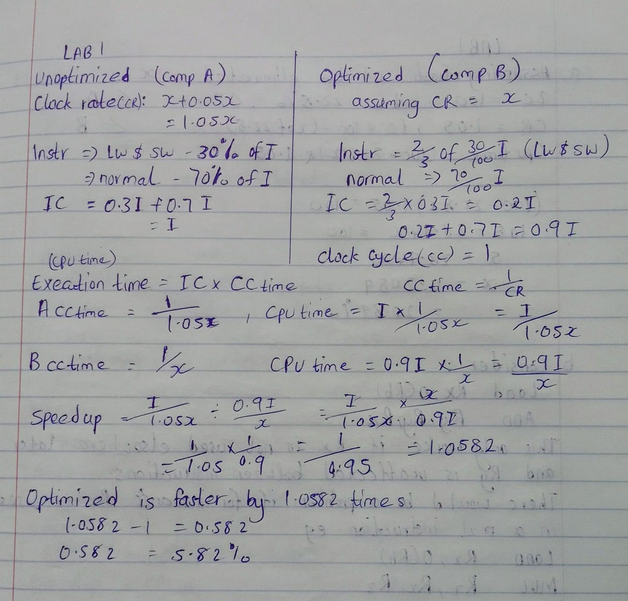
Daisy Opanga

SCT212-0052/2021

LAB 1

**E1.**

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**E2**.

A notebook with writing on it

AI-generated content may be incorrect.

**D1.** RISC in the 1980s had few instructions, load/store architecture, simple encoding and fixed-size instructions.

Modern RISC (e.g. ARMv8, RISC-V) on the other hand, has many instructions (e.g. SIMD, cryptographic ops), load/store, mostly fixed instruction size and mostly simple register-to-register instructions.

In Conclusion, modern RISC processors still embody RISC principles (regular encoding, register-based ops, simplicity in decoding), but they’ve evolved to include performance-enhancing features. Complexity has moved from ISA design to microarchitecture.

**D2.** ISA: x86 is CISC because it comprises variable-length instructions, many addressing modes and complex instructions. However, its microarchitecture internally decodes x86 to RISC-like micro-operations which are fixed-length, pipeline-friendly and register-based.

ISA complexity is best measured at compiler interface level since internals don’t define the ISA rather its the implementation. Intel processors are CISC by ISA but RISC-like by microarchitecture, hence complexity should be measured at the software-visible level.