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LAB 3

**E1.**

1. Data Hazard (Read After Write), DADD reads R1 before LD writes to it.
2. Name Dependency, in out-of-order execution (Write After Write), both instructions write to R1. This wouldn’t be allowed if it occurs In-order but since it’s out-of-order, it causes hazards.
3. Structural Hazard, since there is only one MULT unit, both instructions cannot execute in parallel.
4. Data Hazard (Read After Write), SD needs the value of R1, but DADD hasn’t finished writing it yet.
5. Address Calculation (Read After Write), SD uses R1 to compute the memory address, but DADD hasn’t completed writing to R1.

**E2.**

1. A 2-bit saturating counter is a simple finite state machine used to predict whether a branch will be taken or not taken. It uses 2 bits to represent the state of the branch prediction, allowing 4 states and better resilience to occasional mispredictions compared to 1-bit predictors.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| State | Transition | Prediction | Transition on Taken | Transition on Not Taken | T- Taken  N - Not  S - strongly  W - weakly |
| SNT | 00 | NT | 01 | 00 |
| WNT | 01 | NT | 10 | 00 |
| WT | 10 | T | 11 | 01 |
| ST | 11 | T | 11 | 10 |



|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Iteration | X[i] | Actual Outcome | Counter Before | Prediction | Correctness Evaluation | Counter After |
| 0 | 0 | NT | 00 / SNT | NT | True | 00 |
| 1 | != 0 | T | 00 / SNT | NT | False | 01 |
| 2 | 0 | NT | 01/ WNT | NT | True | 00 |
| 3 | != 0 | T | 00 / SNT | NT | False | 01 |
| 4 | 0 | NT | 01/ WNT | NT | True | 00 |
| 5 | != 0 | T | 00 / SNT | NT | False | 01 |

The predictor keeps bouncing between 00 and 01 states, never reaching Taken (states 10 or 11), because the input pattern keeps alternating thus resulting in a misprediction on every Taken branch.