MIDWESTERN STATE UNIVERSITY

DEPARTMENT OF COMPUTER SCIENCE
CMPS 3023: Logic Design
Spring semester 2020

Project Assignment
03/05/2019 - due on April 30, 2020

RISC-V is an open source hardware instruction set originally developed at UC Berkeley. It supports 3 word widths, 32, 64, 128 bits. One of its characteristics is to have a subset of compressed instructions utilizing 16 bits, used to reduce program size when intermixed with the regular instructions. In this project, tour team will design the hardware component (Thumb mini micro processor) required to execute some of these instructions. This project is to be performed either individually or by a group of at most 4 students. Use the VHDL compiler or the graphical designer and simulator to design tiny processor able to execute a subset of the compressed RISC-V instruction set in accordance with the specifications below.

For this project, you are to design (using VHDL and components design or schematics capture) and simulate an 8-bit processor (8-bit registers), which includes two registers R1 and R2, able to execute the instruction set shown on table 1.

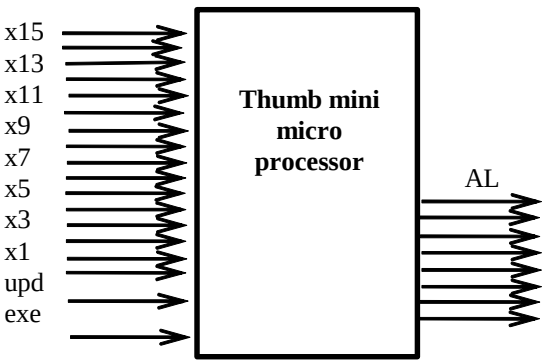
Table RISC-V Compressed Instruction subset

Mnemonic		**Action**	**15 14 13**	**12**	**11 10**	**9 8 7**	**6 5**	**4 3 2**	**1 0**
LI	**Rd,imm**	Load Rd with immediate	010	imm5	rd		imm4:0		01
SRLI	**Ri,imm**	Shift right Ri by imm bits	100	imm5	00	rs/rd	imm4:0		01
ANDI	**Ri,imm**	Logical product Ri with imm	100	imm5	10	rs/rd	imm4:0		01
SUBW	**Rd,Rs2**	Subtract Rd minus Rs2	100	1	11	rs/rd	00	rs2	01
OR	**Rd,Rs2**	Logical sum of Rd and Rs2	100	0	11	rs/rd	10	rs2	01
SLLI	**Ri,imm**	Shift left Ri by imm bits	000	imm5	rs/rd		imm4:0		10
ADDW	**Rd,Rs2**	Add Rd plus Rs2	100	1	11	rs/rd	01	rs2	01
MV	**Rd,Rs**	Copy Rs to Rd	100	0	rd		rs		10
OUT	**Rs**	Displays contents of Rs*	100	0	00	000	rs		11

Rs: source register; Rd: destination register; Ri = 001, 010
*Not part of the RISC-V standard

The block diagram of the micro RISC-V processor is shown on Figure 1. The machine has 18 input signals and 8 output signals. The 18 input signals consist of 16 bits used for instructions and 2 extra bits used to clock the operations: one clock signal will command the execution of the operation (EXE) and the other will update the destination register (UPD) (these two bits cannot be zero at the same time). The 8 output bits should show the value contained in R1 (in binary format), except when instructed to do it differently by the instruction OUT.

Coding example: LI R1,5 in binary 0100 0000 1001 0101
LI R2,13 in binary 0100 0001 0011 0101



ADD R1,R2,R1 in binary 1001 1100 1010 1001

VERY IMPORTANT:

1. Clock signals activate circuit components when they are zero.

Project report:

Use computer word processing and drawing tools of your choice to generate your report. It must consist of the following items:

1. Block diagram (planned drawing) of the circuit implementation (show major components like registers, logic units, multiplexers, connections, etc.).

2. Printout of the circuit schematics (from Quartus) or VHDL code used to implement the design.

3. Electronic copy of the .vhd or the .bdf file required to run the simulation.

4. Brief report on the simulation results (which instructions were simulated and success or not of the functionality of the design). Make sure to run a simulation that loads values in the registers before trying any operation such as ADD or SHIFT.

Your project is due on April 30, 2020. You need to start working NOW!!!! Anything that you try to do in the last week before the due date will not work for sure. Time is an important factor in this project. **If you write your solution in VHDL and the entire solution has less than 3 entities described, then your maximum grade is 50.** If your project does not work or you cannot justify why it does not work, then your grade will be zero. Acceptable justifications are based on software limitations only, and in this case you must show you had every component defined and tested and only the integration failed. Failure in reporting the simulation experiment will reduce your grade by ten points. **NO EXTENSIONS!!**