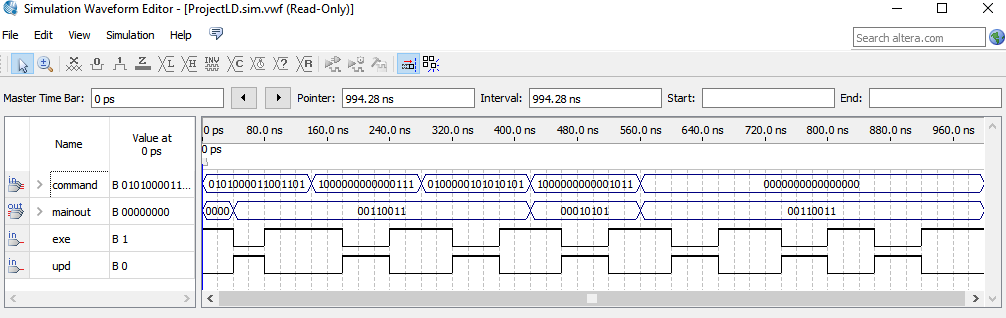
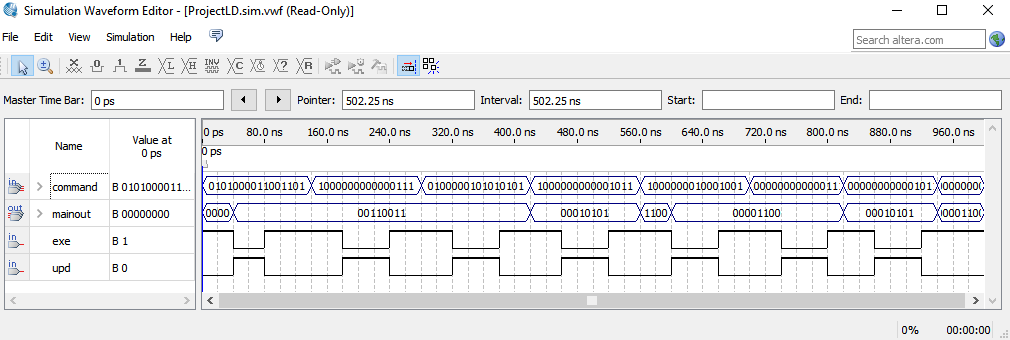
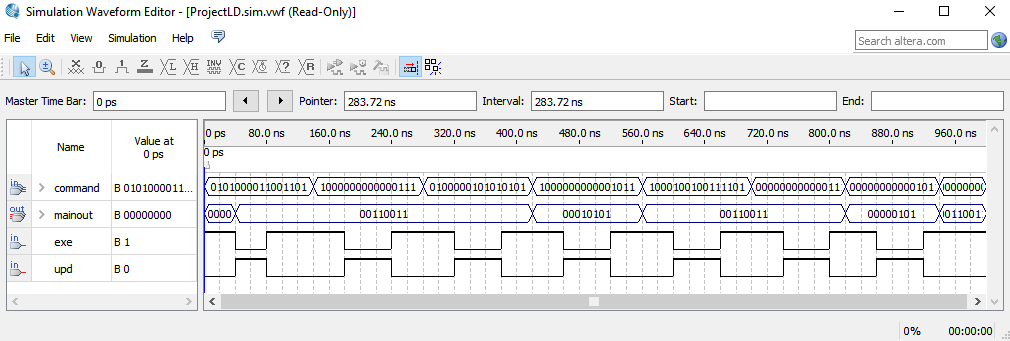
**REPORT:**

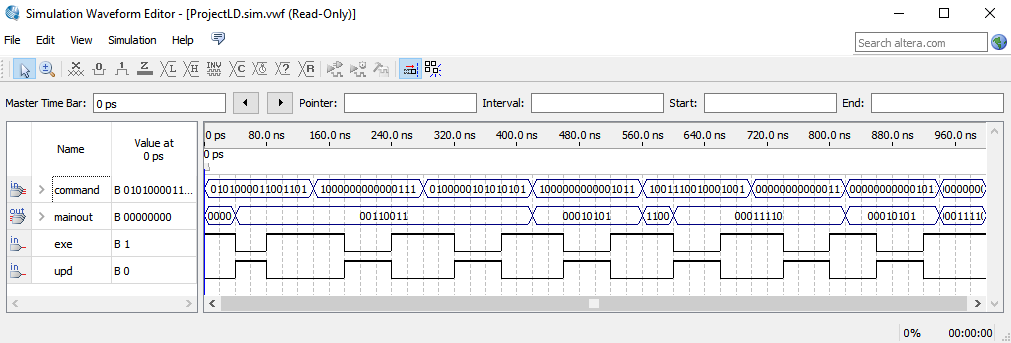
**All but first: LI R1,110011->OUT R1->LI R2, 10101->OUT R2->COMMAND->OUT R1->OUT R2**

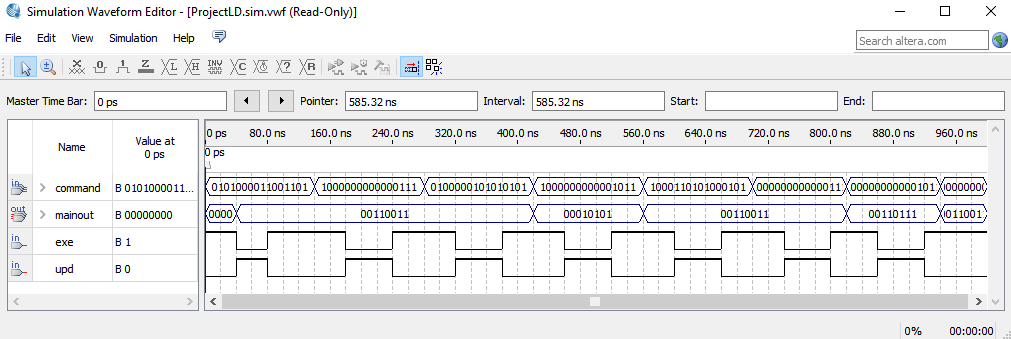
We think for the most part the program works! However, we don’t think we correctly used the upd signal correctly, our register updates on the falling clock (which is essentially the same as upd rising we think). Also, we think that a command can only be used in one clock cycle but aren’t sure if that’s true so we coded for such.

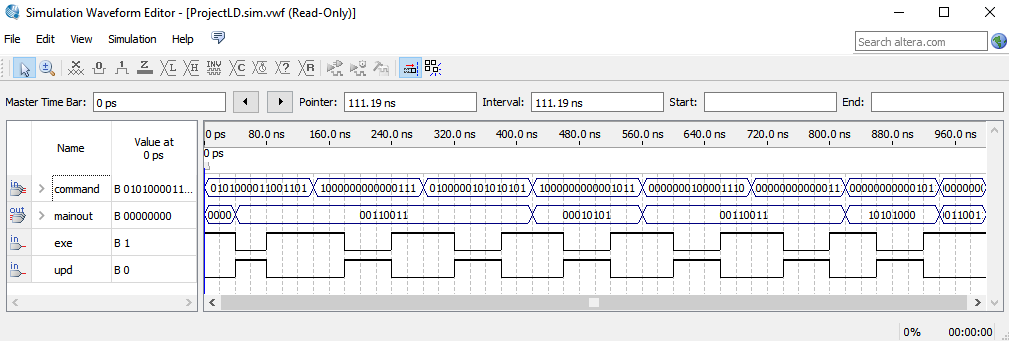
**Loads r1 and r2 then outputs them:**

**Loads r1 and r2 then shifts r1 right by 2:**

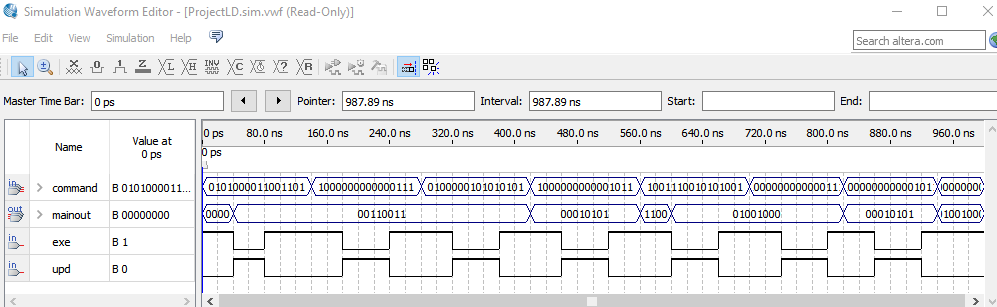
**Loads r1 and r2 then “ands” r2 by ‘15’:**

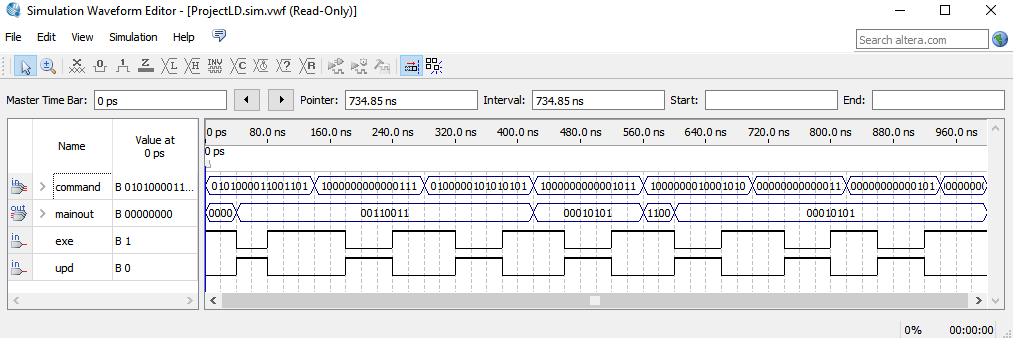
**Loads r1 and r2 then does r1 = r1-r2:**

**Loads r1 and r2 then “ors” r2 by r1:**



**Loads r1 and r2 then shifts r2 by 3:**

**Loads r1 and r2 then does r1=r1+r2:**

**Loads r1 and r2 then does r1=r2(move):**