UNIVERSITÄT OSNABRÜCK

- NeuromorChip -
A comparison between the neuromorphic chips Loihi and SpiNNaker

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Introduction

Neuromorphic computing is an emerging field that aims to design hardware and software systems that mimic the structure and function of the brain. One approach to neuromorphic computing involves the use of neuromorphic chips, specialized hardware devices that can process and store data like how neurons and synapses function in the brain. Two examples of neuromorphic chips are Loihi and SpiNNaker.

Loihi is a neuromorphic chip developed by Intel Labs that was first introduced in 2018 (Lines et al., 2018). Loihi is designed to implement spiking neural networks (SNNs), a type of artificial neural network that operates using discrete events called "spikes" rather than continuous-valued signals. Loihi is notable for its ability to implement SNNs in an asynchronous manner, which allows it to operate at high efficiency and low power consumption. In a recent survey of results and outlook for neuromorphic computing with Loihi (Davies et al., 2021), the authors highlighted the chip's ability to perform various tasks, including pattern recognition, object classification, and control tasks.

SpiNNaker is a neuromorphic chip developed by the University of Manchester (Furber et al., 2014). Like Loihi, SpiNNaker is designed to implement SNNs and is optimized for low-power operation. SpiNNaker utilizes a massively parallel architecture consisting of multiple chips connected, allowing it to process large amounts of data in parallel.

In this essay, we will compare Loihi and SpiNNaker with respect to their capabilities as neuromorphic chips and their potential for modeling the human brain. While both chips have demonstrated the ability to perform various tasks using SNNs, it is important to consider their differences in architecture and design when evaluating their suitability for different applications. Through a review of the available literature and analysis of their respective strengths and limitations, we aim to determine which chip represents a better approach to neuromorphic computing and brain modeling.

Key Features and Architecture of the Neuromorphic chips Loihi and SpiNNaker

Loihi

The digital SNN chip Loihi (named after the emerging Hawaiian undersea volcano set to surface one day) was released by Intel for public use in March 2018 and has been used for research ever since (Davies et al., 2021). In the sense of brain-inspired computing, Loihi consists of an asynchronous SNN where connections are highly time-based. One chip has a total of 130.000 artificial neurons and 130 million synapses. It consists of 128 neuromorphic cores, which are arranged in a mesh, three embedded x86 processor cores that communicate via an asynchronous network-on-chip, and an off-chip communication interface (Davies et al., 2018). When put together, several chips form a system, i.e.,the USB stick-sized “Kapoho Bay” (2 chips and 262 thousand neurons) or a greater system like “Pohoiki Springs” (768 chips and 100 million neurons).

Because of an integrated learning engine in each core, Loihi has uniquely high learning capabilities and programmability regarding the synaptic process (Davies et al., 2018).

Apart from research, multiple promising applications have been demonstrated on Loihi i.e., event-based sensing and perception, odor recognition and learning, closed-loop control for robotics, and simultaneous localization and mapping (Davies et al., 2021).

In September 2021, Intel introduced the second-generation chip Loihi 2, a successor of Loihi, which has a total of 1.048.576 artificial neurons and 120 million synapses. The main difference is the manufactured base material. Loihi is fabricated on Intel's 14 nm process, while Loihi 2 is fabricated on Intel 4 process. In comparison to Loihi, Loihi 2-based systems can have a larger scale with less resources i.e., the card-sized "Oheo Gulch" (1 chip and 1 million neurons) or the 4-inch by 4-inch factor board "Kapoho Point" (8 chips and 8 million neurons). The aim is to optimize the architecture and implementation of the chip and still be commercially viable (Davies et al., 2018). First experimental results also promise greater flexibility and extended range in exploring novel SNN models, mainly because of the improved programmable neural engine (Orchard et al., 2021; Frady et al., 2022).

SpiNNaker

The SpiNNaker, short for "Spiking Neural Network Architecture", is a processor platform that is optimized for the simulation of neural networks in order to run neuroscience applications, but can also be used for other distributed computing, such as ray tracing and protein folding (Mayr, Hoeppner & Furber, 2019; Garside & Plana, 2020). The first generation of SpiNNaker was designed by a small team of academic researchers and postgraduate students at the University of Manchester (Garside & Plana, 2020). The SpiNNaker1 with 18 cores is put together to the SpiNNaker1 board containing 864 ARM cores. The large scale SpiNNaker1 machine is operational at its intended maximum system size, i.e. one Million ARM processors, which allow it to model a billion spiking neurons with biologically realistic connectivity (1,000 to 10,000 synapses per neuron) and simulate 1% of the human brain (Young et al., 2019; Mayr, Hoeppner & Furber, 2019).

Since 2013, the Technische Universität Dresden and the University of Manchester have been cooperating to develop the next-generation SpiNNaker2 system in the framework of the Human Brain Project. The common goal is to scale the number of cores by a factor of 10, while staying within the same power budget, leading to an overall increase in system capacity to simulate the entire human brain (Yan et al, 2021). In other words, the current SpiNNaker1 system, a one Million core machine in 130nm CMOS (Complementary metal-oxide- semiconductor) will soon be replaced by SpiNNaker2, a 10 Million core machine (56 chips with 144 cores each x 25 boards x 5 racks x 10 cabinets ≈ 10 Million processors) in 22nm FDSOI (Fully Depleted Silicium on Insulator) (Mayr, Hoeppner & Furber, 2019). SpiNNaker2 encompasses a range of novel features like dynamic power management, floating-point support, synchronous memory sharing to neighboring cores, multiple- accumulate accelerators, and other numeric accelerators (Yan et al., 2019).

The performance of the SpiNNaker system is enhanced through massive parallel-processing, i.e. the usage of a large array of processors. High power consumption is tackled by employing power-efficient rather than fast microprocessors (Garside & Plana, 2020). This is crucial for training machine learning models as many iterations of the learning process need to be computed simultaneously. To benefit from the asynchronous, naturally parallel and independent sub computations of biological neurons, each core simulates neurons independently and uses a lightweight, spike-optimized asynchronous protocol for communication (Furber et al., 2013). Still, the greatest bottleneck in terms of performance lies in the communications between processors. This is why SpiNNaker has been optimized for short multicast messages (spikes) associated with neural network simulation. Experimental results demonstrated that for parallel neural network simulations, the customized multi-core architecture is energy efficient while keeping the flexibility of software-implemented neuronal and synaptic models, which other neuromorphic chips are still lacking (Garside & Plana, 2020). SpiNNaker's energy efficient simulation of neural network models happens in real time, thereby outperforming conventional high performance computing significantly (Mayr, Hoeppner & Furber, 2019).

In the following, the communication systems of the presented neuromorphic hardware Loihi and SpiNNaker will be compared based on a review from 2019 by Young et al. with respect to routing, global communication, scalability, and synchronization. The comparison criterion of efficiency is related to current experimental studies.

Comparing Loihi and SpiNNaker

It should be noted that the communication patterns in spiking neuromorphic networks are very different from the patterns of communication found in traditional computing. While in traditional memory transfer the CPU performance has outpaced memory throughput and speed, leading to the need to infer what information will be relevant for the processor ahead of time, memory in SNNs is stored locally in the form of synaptic weights, allowing the memory to be located alongside the computation elements. Various communication channels and routing methods allow for flexible, reconfigurable, and virtual connections over a fixed set of wiring within the neuromorphic chips. (Young et al., 2019)

Routing

Neuromorphic hardware can employ two main routing methods, either source routing (packets are routed based on the source of the fire event) or destination routing (packets are routed based on the destination to which the fire event is traveling). While SpiNNaker uses source-based routing, Loihi applies destination-based routing to route SNN packets. Source-based routing bears the advantage of multicast routing that can easily be implemented by allowing the router to steer and duplicate a packet based on its own routing table, but needs a large off-chip memory for storing and external memory access is known to be comparatively slow. Routing packets by destination grants the connectivity information to be stored with the sending neurons and does not require a large off-chip memory.

Global communication

Global packet routing uses either mesh or tree routing schemes. Mesh routing (routers are connected to their neighbors) benefits from large channel bisection, with numerous network links that result in a high throughput of packets. SpiNNaker's ARM chip multiprocessors are connected to a two-dimensional toroidal mesh and emergency routing around a failed or congested link is supported by six connections to neighboring chips forming triangular facets. In contrast, Loihi connects all its cores and processors in a many-core mesh. Off-chip communication interfaces provided by the chip's edges permit Loihi to reach out to many other chips along the four planar directions.

Scalability

Neuromorphic systems bear great scaling potential to be either scaled up to biologically realistic sizes or based on the complexity of the application deployed. SpiNNaker is designed to scale to very large sizes. The chips are placed on a board in a 48-node hexagonal array. 24 boards are pieced together into a crate, with five crates stored in a single rack. Currently, the largest SpiNNaker1 system is the 106 machine including ten 19" rack cabinets and a total of 1,036,800 ARM processing cores. Loihi supports up to 4,096 on-chip cores as well as 16,384 chips. The design constraints can be traced back to the current mesh protocol and hierarchical addressing scheme. Intel's Loihi system “Pohoiki Beach” comprises 64 Loihi chips with over 8 million neurons and “Pohoiki Springs” contains 768 Loihi chips. The successor Loihi 2 scales larger size systems than its predecessor, but does not reach as great a size as SpiNNaker.

Efficiency

Just as in the brain “various feedback processes introduce synchronization and coherent information processing over different neurons and brain regions” (Davies et al., 2021), the implementation of adaptive self-modifying parallel computations by using an asynchronous SNN results in high efficiency. In a recent study comparing Loihi and a SpiNNaker2 prototype (Yan et al., 2021), the authors found that both chips were capable of performing low-latency keyword spotting and adaptive robotic control tasks, but that Loihi had an advantage in terms of energy efficiency. Another study demonstrated the use of a spiking central pattern generator implemented on both Loihi and SpiNNaker for controlling a simulated lamprey robot (Angelidis et al., 2021).

Synchronization

The brain is working asynchronously and biological spikes happen only as a response to some event. SpiNNaker is able to simulate these properties in real-time. An explicit synchronization procedure makes it possible to create a cycle-accurate, deterministic simulator of the neuromorphic hardware. Network synchronization can be achieved through fixed cycle times or cycles of variable length and the employment of other synchronization methods to then progress to the next cycle. Loihi uses variable length cycle time, which converts the timestamp of the network in algorithmic time, and is in turn unrelated to real-time. For this, a mesh-level barrier sync is applied to signify when packets have reached their destinations. Then, the timestep can be advanced to the next cycle, providing a substantial performance advantage.

Discussing the approaches of real-time and variable length cycle time

On the positive side, network activity becomes deterministic, needless idle time can be removed, and the network is able to run variably, even faster than real-time. The length of each cycle is set by the slowest component, which again represents a bottleneck for the system's performance. For instance, Loihi's maximum network speed is limited by the bandwidth of the on-chip router and the time that it takes to propagate the fire packets through the network. On the downside, variable length cycle times makes it harder to interface the network with real-time signals and perform real-time operations due to the separation of real-time and simulation time.

Which of these time simulations is the more suitable in terms of temporal resolution is open for debate. We consider real-time processing the approach to be more biologically plausible, even if performance could be improved with the alternatives. Markram argued that "detailed, biologically accurate models, based on first principles, are required to accurately model the cortex" (Markram, 2006, p. 153). Real-time processing may help ensure that a system is able to accurately respond to events as they occur since firing biological neurons as asynchronously events carry no other information than that they have happened. Thus, real-time computing helps to improve both the efficiency and reliability of a system by allowing it to respond to events or data as they occur, rather than having to wait for a batch of data to be processed or for a specific time period to elapse.

Conclusion

Both chips have impressive capabilities, especially for application in the domains of neuroscience and robotics. Due to their difference in size, a direct comparison of capabilities is biased towards the much larger SpiNNaker system. Nevertheless, it is still possible to compare the network architectures on their potential to accurately model the brain. SpiNNaker1 can already model 1% of the cortex, and the advances of SpiNNaker2 seem very promising. Loihi exhibits limitations concerning scalability, and additionally, the variable length cycle time employed by Loihi is biologically implausible. Therefore, SpiNNaker appears to be the more accurate and biologically realistic human brain replica.

In this essay, two state-of-the-art systems were presented, and their capabilities and potential to model the brain were compared. Particular emphasis was given to the communication of the different units. While capabilities were difficult to compare, SpiNNaker's approach holds more significant potential for modeling the brain. Still, both systems perform impressive feats, and Loihi, while not ideal for modeling the brain, bears great potential for technological advancement such as more powerful and energy efficient chips.

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