HARDWARE MANUAL

PMAC Mini PCI

Programmable Multi-Axis Controller

5xx-603712-xHxx

April 26, 2010

DELTA TAU
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REVISION HISTORY				
REV.	**DESCRIPTION**	**DATE**	**CHG**	**APPVD**
1	REVISIONS TO FLEX CPU BAUD RATE, PPS. 6 &21	05/09/06	CP	S. SATTARI
2	UPDATED ENCODER SETTING DESC., PPS. 6 & 20	01/30/09	CP	S. MILICI
3	CORRECTED JUMPER LAYOUT E85-E87-E88, P. 25	04/26/10	CP	S. MILICI

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INTRODUCTION

The PMAC Mini PCI is an inexpensive, compact 2-axis version of the PMAC family.

It can be used in a PC's PCI slot as a half-sized board (230 mm, 9" long) or it can be used as a standalone using serial communications for setup and/or application control.

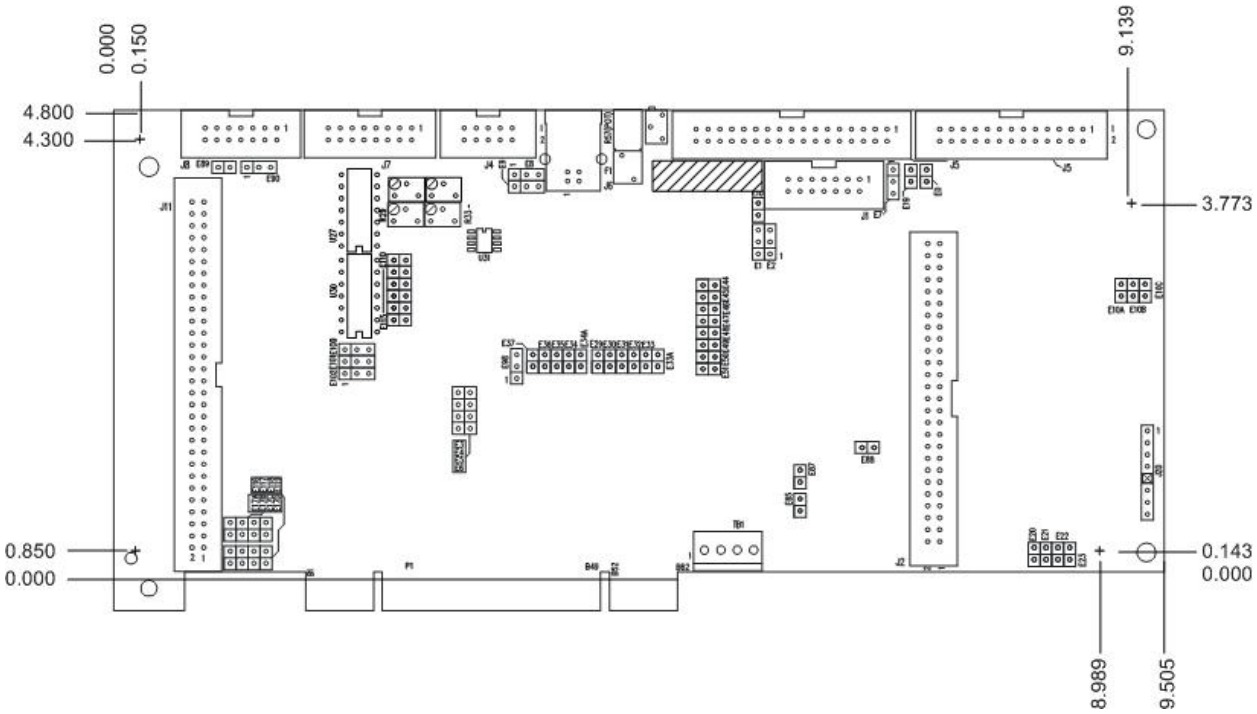
Programs for the PMAC Mini PCI, both motion and PLC, are 100% compatible with other versions of PMAC. However, there are several features unique to the PMAC Mini PCI:

1. There are only two output digital-to-analog converters: DAC1 and DAC2 (DAC3 and DAC4 do not exist). Both have differential outputs. The two analog outputs on the PMAC Mini PCI can be used as velocity or torque commands for separate axes, or as phase current commands for a single axis commutated by the card. However, there are four incremental encoder interfaces that can be used for feedback or master positions. Two of these may alternately be used to process analog voltages through optional on-board V/F converters.
2. There is no JPAN control panel port. There are no digital inputs dedicated to the functions of this port on other PMACs. To obtain equivalent functions, general-purpose inputs must be used along with a PLC program reading these inputs. Handwheel encoders may be brought in through the JMACH port. Wiper inputs may be brought in through the JAUX port if Option 15 is purchased.
3. The memory mapping of the general-purpose digital I/O is different from other versions of the PMAC. Different M-Variable definitions are required for these I/Os on the PMAC Mini PCI (see below).
4. The serial port is RS-232 only. There is no on-board or optional capability to use RS-422 format.
5. Dual-ported RAM (Option 2) is an on-board option that must be factory-installed. The PMAC Mini PCI cannot use the separate Option 2 DPRAM board.
6. The JTHW multiplexer port outputs are not as powerful as on other PMACs. There should be no more than one meter (three feet) of cable to any device on the port, instead of the three meters (ten feet) on other PMACs. Anything longer should use the Acc-35A driver board.
7. There are no jumpers to control the open-circuit voltage of the complementary inputs. Instead, there are removable socketed SIP resistor packs. At the factory, these are configured to tie the complementary lines to 2.5V. Removed, they will tie the complementary lines to 5V.
8. There is no JXIO connector to provide clock signals to mating connectors on Acc-24P or Acc-8D Option 8 boards. If either of these boards is used with the PMAC Mini PCI, a custom cable should be made to connect the DCLK signal on the PMAC Mini PCI J7 port to both the DCLK and SCLK inputs on the Acc-24P JXIO port, or the SCLK input on the Acc-8D Option 8 JXIO port.
9. The HMFLn, PLIMn, and MLIMn flag inputs on the PMAC Mini PCI can accept signals from both sourcing and sinking drivers. If the A+15V on JMACH is used to supply the flag isolators through E89 and E90, only sinking drivers can be used. But, if pin 13 on J8 (JAUX) is used to supply the isolators, a +12V to +24V supply can be used for sinking drivers, or a 0V supply can be used for sourcing drivers.
10. The PMAC Mini PCI has an interlock circuit that drops out the +/-15V supplies to the analog outputs through a fail-safe relay if any supply on PMAC is lost.
11. If Option 15 is purchased, the PMAC Mini PCI has the capability for two on-board voltage-to-frequency (V/F) converters. These may be used for two Wiper analog inputs, or to convert the two analog outputs to pulse trains for stepper-type drives. The V/F converters can each take an input of 0-10V referenced to AGND. The pulse trains can be tied into encoder channels 3 or 4 for counting. (It is also possible, but more expensive, to use the first two channels of the off-board Acc-8D Option 2 board.)

Features

- Motorola DSP 563xx Digital Signal Processor
- Two output digital-to-analog (DAC) converters
- Four full encoder channels
- 16 general purpose I/O, OPTO-22 compatible
- Multiplexer port for expanded I/O
- Overtravel limit, home, fault amplifier enable flags
- Display port for LCD and VFD displays
- Optional on-board dual-ported RAM
- Optional two on-board V to F converters
- Optional on-board stepper control
- PCI Bus and/or RS-232 control
- Stand-alone operation
- G-Code command processing for CNC
- Linear and circular interpolation
- 256 motion programs capacity
- Asynchronous PLC program capability
- Rotating buffer for large programs
- 36-bit position range (+/- 64 billion counts)
- 16-bit DAC output resolution
- S-curve acceleration and deceleration
- Cubic trajectory calculations, splines
- Electronic gearing

Dimensions



HARDWARE SETUP

The PMAC contains a number of jumpers (pairs of metal prongs) called E-points. These jumpers customize the hardware features of the board for a given application and must be set up appropriately. The following is an overview of the several PMAC jumpers grouped in appropriate categories. For a complete description of the jumper setup configuration, refer to the E-Point Descriptions section of this manual.

Board Configuration

Base Version

The base version of the PMAC Mini PCI provides a half sized board with:

- 40 MHz DSP563xx CPU
- 128k x 24 zero-wait-state flash-backed SRAM
- 512k x 8 flash memory for firmware and user backup
- Latest released firmware version
- RS232 serial interface, 33Mhz PCI bus interface
- Two channels axis interface circuitry, each including:
  - 16-bit +/-10V analog output
  - 3-channel (AB quad with index) differential/single-ended encoder input
  - Four input flags, two output flags
  - Interface to four external 16-bit serial ADC
- Display, muxed I/O, direct I/O interface ports
- Buffered expansion port
- Clock crystal with +/-100 ppm accuracy
- PID/notch/feedforward servo algorithms
- 1-year warranty from date of shipment
- One manuals CD per set of one to four PMACs in shipment (cables, mounting plates, mating connectors not included)

Option 2: Dual-Ported RAM

Dual-ported RAM provides a high-speed communications path for bus communications with the host computer through a bank of shared memory. DPRAM is advised if more than 100 data items per second are to be passed between the controller and the host computer in either direction.

- Option 2 provides an 8k x 16 bank of on-board dual-ported RAM. The key component on the board is U20 (located at the back of the board).

Part number: 302-603712-OPT

Option 5xF: CPU Speed Options

The base PMAC Mini PCI has a 40 MHz DSP563xx CPU. This is Option 5AF that is provided automatically if no CPU speed option is specified.

- Option 5AF: 40 MHz DSP563xx CPU (80 MHz 56002 equivalent). This is the default CPU speed.

  Part number: 5AF-603712-OPT
- Option 5CF: 80 MHz DSP563xx CPU (160 MHz 56002 equivalent)

  Part number: 5CF-603712-OPT
- Option 5EF: 160 MHz DSP563xx CPU (320 MHz 56002 equivalent)

  Part number: 5EF-603712-OPT

Option 6: Extended Servo Algorithm Firmware

- Option 6 provides an Extended (Pole-Placement) Servo Algorithm firmware instead of the regular servo algorithm firmware. This is required only in difficult-to-control systems (resonances, backlash, friction, disturbances, changing dynamics).

  Part number: 306-00PMAC-OPT

Option 6L: Special Lookahead Firmware

- Option 6L provides a special lookahead firmware for sophisticated acceleration and cornering profile execution. With the lookahead firmware, PMAC controls the speed along the path automatically (but without changing the path) to ensure that axis limits are not violated.

  Part number: 3L6-00PMAC-OPT

Option 8A: High-Accuracy Clock Crystal

The PMAC Mini PCI has a clock crystal of nominal frequency 19.6608 MHz (~20 MHz). The standard crystal's accuracy specification is +/-100 ppm.

- Option 8A provides a nominal 19.6608 MHz crystal with a +/-15 ppm accuracy specification.

  Part number: 3A8-603712-OPT

Option 10: Firmware Version Specification

Normally the PMAC Mini PCI is provided with the newest released firmware version. A label on the memory IC (U13) shows the firmware version loaded at the factory.

- Option 10 provides for a user-specified firmware version. (1.17 or newer)

  Part number: 310-00PMAC-OPT

Option 15: V-to-F Converter for Analog Input

The Mini PMAC PCI has an optional analog input called Wiper (because it is often tied to a potentiometer's wiper pin). Mini PMAC PCI can digitize this signal by passing it through an optional voltage-to-frequency converter. The key component on the board is U27 and U30.

- Option 15 provides a voltage-to-frequency converter that permits the use of the Wiper input on the auxiliary port J8 (JAUX).

Part number: 315-603712-OPT

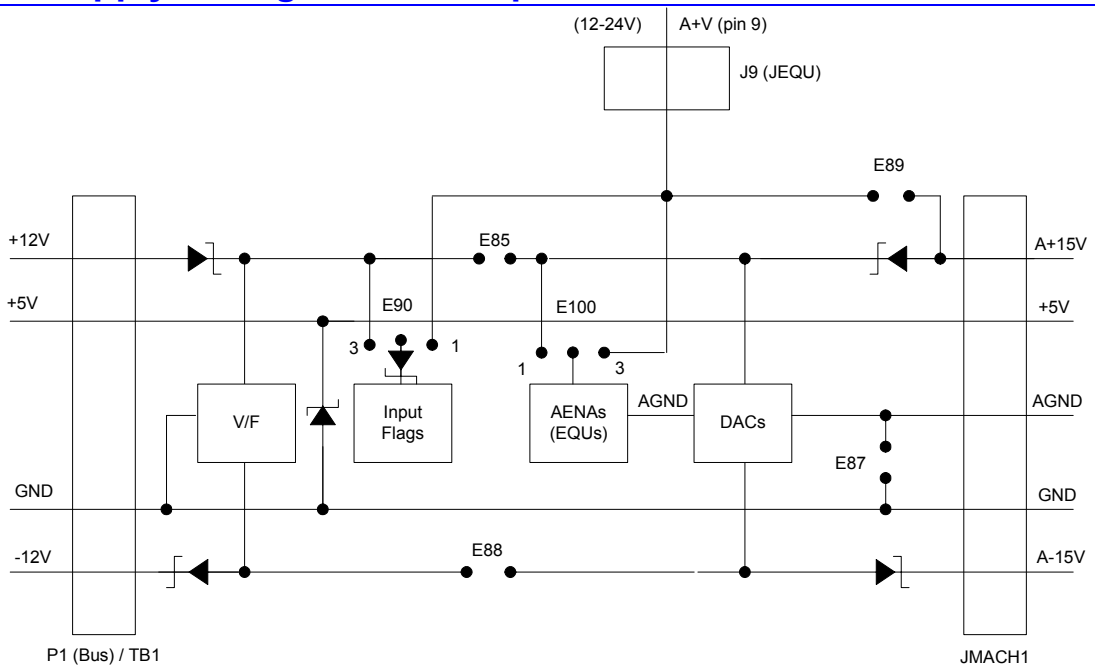
General Purpose Digital Inputs and Outputs (JOPTO Port)

PMAC Mini PCI's J5 or JOPTO connector provides eight general-purpose digital inputs and eight general-purpose digital outputs. Each input and each output has its own corresponding ground pin in the opposite row. The 34-pin connector was designed for easy interface to OPTO-22 or equivalent optically isolated I/O modules. Acc-21F is a six-foot cable for this purpose. Characteristics of the JOPTO port on the PMAC:

- 16 I/O points. 100mA per channel, up to 24V
- Hardware selectable between sinking and sourcing in groups of eight; default is all sinking (inputs can be changed simply by moving a jumper; sourcing outputs must be special-ordered or field-configured)
- Eight inputs, eight outputs only; no changes. Parallel (fast) communications to PMAC CPU
- Not opto-isolated; easily connected to Opto-22 (PB16) or similar modules through Acc-21F cable

Jumper E7 controls the configuration of the eight inputs. If it connects pins 1 and 2 (the default setting), the inputs are biased to +5V for the OFF state, and they must be pulled low for the ON state. If E7 connects pins 2 and 3, the inputs are biased to ground for the OFF state, and must be pulled high for the ON state. In either case, a high voltage is interpreted as a 0 by the PMAC software, and a low voltage is interpreted as a 1.

Power Supply Configuration Jumpers



E85, E87, E88: Analog Circuit Isolation Control – These jumpers control whether the analog circuitry on the PMAC is isolated from the digital circuitry, or electrically tied to it. In the default configuration, these jumpers are off, keeping the circuits isolated from each other (provided separate isolated supplies are used).

E89-E90: Input Flag Supply Control – If E90 connects pins 1 and 2 and E89 is on, the input flags (+LIMn, -LIMn, HMFLn, and FAULTn) are supplied from the analog A+15V supply, which can be isolated from the digital circuitry. If E90 connects pins 1 and 2 and E89 is off, the input flags are supplied from a separate A+V supply brought in on pin 13 of the J8 JAUX connector. This supply can be in the +12V to +24V range and can be kept isolated from the digital circuitry. If E90 connects pins 2 and 3, the input flags are supplied from the digital +12V supply and isolation from the digital circuitry is defeated.

E100: AENA/EQU Supply Control – If E100 connects pins 1 and 2, the circuits related to the AENAn, EQUn and FAULTn signals will be supplied from the analog A+15V supply which can be isolated from the digital circuitry. If E100 connects pins 2 and 3, the circuits will be supplied from a separate A+V supply brought in on pin 13 of the J8 JAUX connector. This supply can be in the +12V to +24V range and can be kept isolated from the digital circuitry.

Clock Configuration Jumpers

E3-E6: Servo Clock Frequency Control – The jumpers E3 – E6 determine the servo-clock frequency by controlling how many times it is divided down from the phase-frequency. The default setting of E3 and E4 off, E5 and E6 on divides the phase-clock frequency by 4, creating a 2.25 kHz servo-clock frequency. This setting is seldom changed.

E29-E33A: Phase Clock Frequency Control – Only one of the jumpers E29 – E33A which select the phase-clock frequency may be on in any configuration. The default setting of E31 on which selects a 9 kHz phase-clock frequency, is seldom changed.

E34A-E37: Encoder Sample Clock – Only one of the jumpers E34A – E37 which select the encoder sample clock frequency, may be on in any configuration. The frequency must be high enough to accept the maximum true count rate (no more than one count in any clock period), but a lower frequency can filter out longer noise spikes. The anti-noise digital delay filter can eliminate noise spikes up to one sample-clock cycle wide.

E98: DAC/ADC Clock Frequency Control – Leave E98 in its default setting of 1-2 which creates a 2.45 MHz DCLK signal, unless connecting an Acc-28 A/D-converter board. In this case, move the jumper to connect pins 2 and 3 which creates a 1.22 MHz DCLK signal.

Encoder Configuration Jumpers

Encoder Complementary Line Control – PMAC has differential line receivers for each encoder channel, but can accept either single-ended (one signal line per channel) or differential (two signal lines, main and complementary, per channel).

REV 102 and below: The selection of the type of encoder used, either single ended or differential, is made through resistor packs configurations and not through jumper configurations: RP13, RP14, RP20 and RP21.

REV 103 and above: The selection of the type of encoder used, either single ended or differential, is made through jumper configurations: E11, E12, E13 and E14.

Single-Ended Encoders

With the jumper for an encoder set for single-ended, the differential input lines for that encoder are tied to 2.5V; the single signal line for each channel is then compared to this reference as it changes between 0 and 5V.

When using single-ended TTL-level digital encoders, the differential line input should be left open, not grounded or tied high; this is required for The PMAC differential line receivers to work properly.

Differential Encoders

Differential encoder signals can enhance noise immunity by providing common-mode noise rejection. Modern design standards virtually mandate their use for industrial systems, especially in the presence of PWM power amplifiers, which generate a great deal of electromagnetic interference.

Connect pin 1 to 2 to tie differential line to +2.5V

- Tie to +2.5V when no connection
- Tie to +2.5V for single-ended encoders

Connect pin 2 to 3 to tie differential line to +5V

- Don't care for differential line driver encoders

Tie to +5V for complementary open-collector encoders (obsolete)

E117, E118: Wiper to Encoder Input Enable – Putting these jumpers on ties the output of the Option 10 voltage-to-frequency converter that can process the Wiper analog input on the JAUX port to the Channel 3 (E117) or 4 (E118) encoder circuitry. If the frequency signal is connected to one of these channels, no encoder should be connected through the JMACH1 connector.

Board Reset/Save Jumpers

E50: Flash-Save Enable/Disable Control – If E50 is on (default), the active software configuration of the PMAC can be stored to non-volatile flash memory with the **SAVE** command. If the jumper on E50 is removed, this **SAVE** function is disabled and the contents of the flash memory cannot be changed.

E51: Re-Initialization on Reset Control – If E51 is off (default), PMAC executes a normal reset, loading active memory from the last saved configuration in non-volatile flash memory. If E51 is on, PMAC re-initializes on reset, loading active memory with the factory default values.

Communication Jumpers

PCI Bus Base Address Control – The selection of the base address of the card in the I/O space of the host PC's expansion bus is assigned automatically by the operating system and it is not selected through a jumper configuration.

E44-E47: Serial Baud Rate Selection – The serial baud rate is determined by a combination of the setting of jumpers E44-E47 and the CPU frequency on a PMAC board. If the CPU's operational frequency has been determined by a non-zero setting of I46, the serial communications baud rate is determined at power-up/reset by variable I54 alone. Currently, the Flex CPU's serial baud rate is determined at power-up/reset by variable I54 alone.

E49: Serial Communications Parity Control – Jump pin 1 to 2 for no serial parity. Remove jumper for odd serial parity.

Reserved Configuration Jumpers

E0: Reserved for future use.

E48: Reserved for future use.

I/O Configuration Jumpers

Warning:

A wrong setting of these jumpers will damage the associated output IC.

E1-E2: Machine Output Supply Configure – With the default sinking output driver IC (ULN2803A or equivalent) in U55 for the J5 JOPTO port outputs, these jumpers must connect pins 1 and 2 to supply the IC correctly. If this IC is replaced with a sourcing output driver IC (UDN2981A or equivalent), these jumpers must be changed to connect pins 2 and 3 to supply the new IC correctly.

E7: Machine Input Source/Sink Control – With this jumper connecting pins 1 and 2 (default), the machine input lines on the J5 JOPTO port are pulled up to +5V or the externally provided supply voltage for the port. This configuration is suitable for sinking drivers. If the jumper is changed to connect pins 2 and 3, these lines are pulled down to GND. This configuration is suitable for sourcing drivers.

E17A - E17D: Motors 1-4 Amplifier-Enable Polarity Control – Jumpers E17A through E17D control the polarity of the amplifier enable signal for the corresponding motor 1 to 4. When the jumper is on (default), the amplifier-enable line for the corresponding motor is low true so the enable state is low-voltage output and sinking current and the disable state is not conducting current. With the default ULN2803A sinking driver used by the PMAC on U44, this is the fail-safe option, allowing the circuit to fail in the disable state. With this jumper off, the amplifier-enable line is high true so the enable state is not conducting current and the disable state is low-voltage output and sinking current. This setting is not recommended.

Warning:

A wrong setting of these jumpers will damage the associated output IC.

E101-E102: Motors 1-4 AENA/EQU Voltage Configure – The U37 driver IC controls the AENA and EQU signals of motors 1-4. With the default sinking output driver IC (ULN2803A or equivalent) in U44, these jumpers must connect pins 1 and 2 to supply the IC correctly. If this IC is replaced with a sourcing output driver IC (UDN2981A or equivalent), these jumpers must be changed to connect pins 2 and 3 to supply the new IC correctly.

Resistor Pack Configuration: Termination Resistors

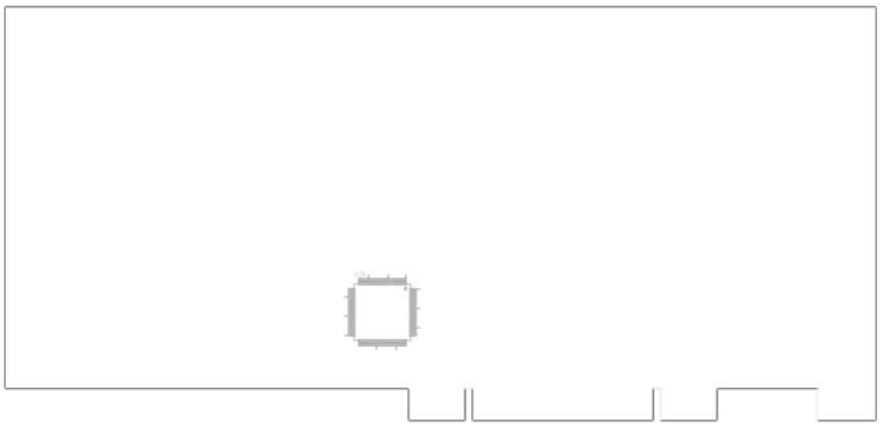
The PMAC provides sockets for termination resistors on differential input pairs coming into the board. If these signals are brought long distances into the PMAC board and ringing at signal transitions is a problem, SIP resistor packs may be mounted in these sockets to reduce or eliminate the ringing.

All termination resistor packs have independent resistors (no common connection) with each resistor using two adjacent pins. The following table shows which packs are used to terminate each input device:

Device	Resistor Pack	Pack Size
Encoder 1	RP15	6-pin
Encoder 2	RP18	6-pin
Encoder 3	RP23	6-pin
Encoder 4	RP25	6-pin

The Optional Dual-Ported RAM

When the PMAC Mini PCI Option 2 is ordered, U20 is installed on-board at the factory. The DPRAM is located on the back of the board.



See the PMAC User Manual for more information.

LED Indicators

The PMAC Mini PCI has two sets (front side and back) of three LED indicators.

D9 and D9A (green)	When the green LED is lit, this indicates that power is applied to the +5V input and it is good.
D10 and D10A (red)	When the red LED is lit, this indicates that the watchdog timer has tripped and shut down the PMAC.
D19 and D19A (yellow)	The PMAC Mini PCI has an interlock circuit that drops out the +/-15V supplies to the analog outputs through a fail-safe relay if any supply on PMAC is lost. In this case, the LED will be off.

Input and Output Mapping

Y:$FFC0 J1 (JDISP) Outputs

0	DB0	Display Data 0	(J1-8)
1	DB1	Display Data 1	(J1-7)
2	DB2	Display Data 2	(J1-10)
3	DB3	Display Data 3	(J1-9)
4	DB4	Display Data 4	(J1-12)
5	DB5	Display Data 5	(J1-11)
6	DB6	Display Data 6	(J1-14)
7	DB7	Display Data 7	(J1-13)

Y:$FFC1 J3 (JTHW) Inputs

0	DAT0	THW Data 0	(J3-3)
1	DAT1	THW Data 1	(J3-5)
2	DAT2	THW Data 2	(J3-7)
3	DAT3	THW Data 3	(J3-9)
4	DAT4	THW Data 4	(J3-11)
5	DAT5	THW Data 5	(J3-13)
6	DAT6	THW Data 6	(J3-15)
7	DAT7	THW Data 7	(J3-17)

Y:$FFC2 J3 (JTHW) Outputs

0	SEL0	THW Select 0	(J3-4)
1	SEL1	THW Select 1	(J3-6)
2	SEL2	THW Select 2	(J3-8)
3	SEL3	THW Select 3	(J3-10)
4	SEL4	THW Select 4	(J3-12)
5	SEL5	THW Select 5	(J3-14)
6	SEL6	THW Select 6	(J3 16)
7	SEL7	THW Select 7	(J3 18)

Y:$FFC3 J5 (JOPTO) Inputs

0	MI1	Machine Input 1	(J5-15)
1	MI2	Machine Input 2	(J5-13)
2	MI3	Machine Input 3	(J5-11)
3	MI4	Machine Input 4	(J5-9)
4	MI5	Machine Input 5	(J5-7)
5	MI6	Machine Input 6	(J5-5)
6	MI7	Machine Input 7	(J5-3)
7	MI8	Machine Input 8	(J5-1)

Y:$FFC4 J5 (JOPTO) Outputs

0	MO1	Machine Output 1	(J5-31)
1	MO2	Machine Output 2	(J5-29)
2	MO3	Machine Output 3	(J5-27)
3	MO4	Machine Output 4	(J5-25)
4	MO5	Machine Output 5	(J5-23)
5	MO6	Machine Output 6	(J5-21)
6	MO7	Machine Output 7	(J5-19)
7	MO8	Machine Output 8	(J5-17)

Y:$FFC5 Dedicated Use

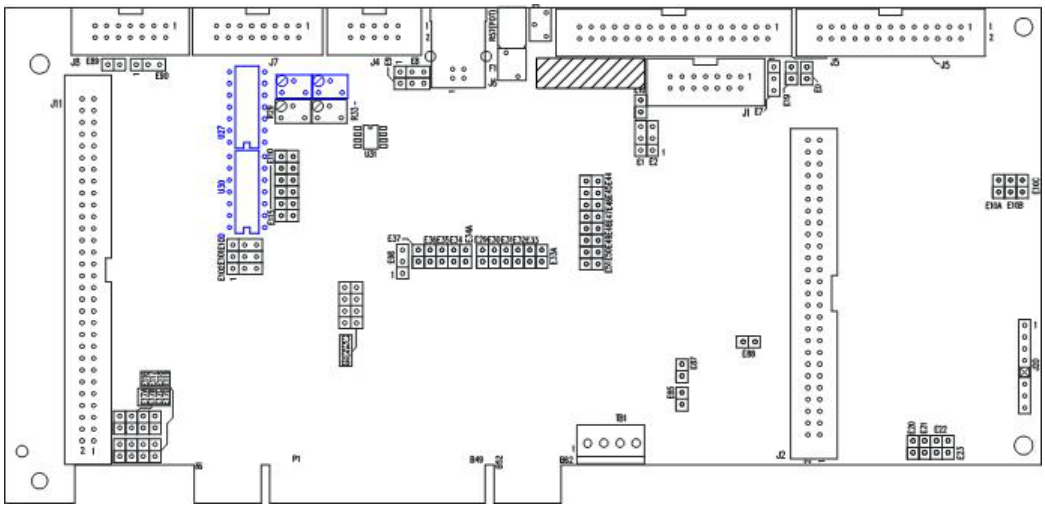
0	ENA422	Serial Enable
1	RS	Display Control
2	R/W	Display Control
3	E	Display Control
4	E44	Jumper E44
5	E45	Jumper E45
6	E46	Jumper E46
7	E47	Jumper E47

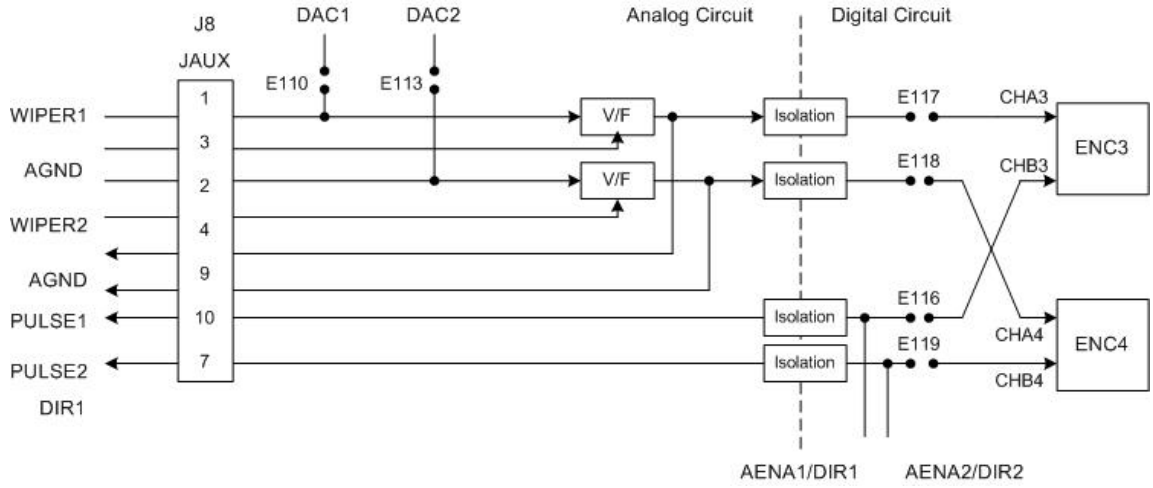
Y:$FFC6 Dedicated Use

0	E48	Jumper E48
1	E49	Jumper E49
2	E50	Jumper E50
3	E51	Jumper E51
4	PWR_GUD-	Power Supply Detect
5	(Reserved for future use)	
6	(Reserved for future use)	
7	(Reserved for future use)	

OPTION 15 — VOLTAGE TO FREQUENCY CONVERTER

When the PMAC Mini PCI Option 15 is ordered, the following components are installed on-board at the factory:





Configuration as Analog Input with a 0-100 kHz Frequency Range

Jumpers Setting									
Input 1					Input 2				
E110	E111	E112	E116	E117	E113	E114	E115	E118	E119
OFF	ON	ON	ON	ON	OFF	ON	ON	ON	ON

Software configuration to be typed in the terminal window:

```
WY$0724,$400722,1280          ;Timebase Encoder Conversion entry for Input #1
WY$0726,$400723,1280          ;Timebase Encoder Conversion entry for Input #2
I910=4                        ;Encoder channel 3 for pulse-and-direction decode
                              ;(Input #1)
I915=4                        ;Encoder channel 4 for pulse-and-direction decode
                              ;(Input #2)
M34->X:$0725,24               ;Result of the analog conversion. The range of
                              ;M34 is from 0 to the ;I10 value, proportional
                              ;to the 0-10V range on the analog input #1.
M35->X:$0727,24               ;Result of the analog conversion. The range of
                              ;M35 is from 0 to the I10 value, proportional to
                              ;the 0-10V range on the analog input #2.
```

Configuration as Analog Input with a 0-2 MHz Frequency Range

Jumpers Setting									
Input 1					Input 2				
E110	E111	E112	E116	E117	E113	E114	E115	E118	E119
OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	ON
E34 - E37: Encoder Sampling Clock Frequency Control									
E34A	E34	E35	E36	E37	SCLK Clock Frequency				
ON	OFF	OFF	OFF	OFF	19.6608 MHz				

Software configuration to be typed on the terminal window:

```
WY$0724,$40722,64            ;Timebase Encoder Conversion entry for Input #1
WY$0726,$40723,64            ;Timebase Encoder Conversion entry for Input #2
I911=1                       ;Encoder 3 digital delay filter disabled (bypassed)
I916=1                       ;Encoder 4 digital delay filter disabled (bypassed)
I910=4                       ;Encoder channel 3 for pulse-and-direction decode
                             ;(Input #1)
I915=4                       ;Encoder channel 4 for pulse-and-direction decode
                             ;(Input #2)
M34->X:$0725,24              ;Result of the analog conversion. The range of
                             ;M34 is from 0 to the I10 value, proportional
                             ;to the 0-10V range on the analog input #1.
M35->X:$0727,24              ;Result of the analog conversion. The range of
                             ;M35 is from 0 to the I10 value, proportional to
                             ;the 0-10V range on the analog input #2.
```

General Configuration for Step and Direction Outputs

- Set the appropriate jumpers as shown in the diagrams below.
- Wire the PULSEn and AENAn/DIRn open-collector outputs on the JAUX connector to the stepper drive inputs with AGND as the reference.
- Tie the DACn output to the WIPERn input by putting the jumper on.
- Select the desired frequency range with the two jumpers for the channel.
- If true open-loop operation is desired, tie the PULSEn output to the CHAm input with the jumper and tie the AENAn/DIRn output to the CHBm input; otherwise leave these jumpers off.
- If true open-loop operation is desired, set up the encoder channel for pulse-and-direction decode by setting I910 or I915 to 4; otherwise, use as normal for real encoder feedback.
- If true open-loop operation is desired and the 0-2 MHz frequency range is selected, set I911=1 or I916=1. This will disable the digital delay filter for Encoder 3 or Encoder 4, respectively.
- Put the PMAC output channel in magnitude-and-direction mode by setting bit 16 of Ix02 to 1 and bit 16 of Ix25 to 1
- Choose the appropriate simulated or real encoder for the motor's feedback loop by setting Ix03 and Ix04 to the address in the conversion table of the proper encoder channel. Assuming the default conversion table, the value is $0720 for ENC1, $0721 for ENC2, $0722 for ENC3, and $0723 for ENC4.
- If the simulated feedback is used, set Ix30 to 550,000 for 100 kHz max.; or Ix30 to 27,500 for 2 MHz max. Set Ix31 to 0, Ix32 to 1000, Ix33 to 0, and Ix35 to 0. If real feedback is used, tune the motor the same as for a velocity-mode amplifier.

0-100 kHz Frequency Range and Pseudo-Feedback (no External Encoder Connected)

Jumpers Setting									
Input 1					Input 2				
E110	E111	E112	E116	E117	E113	E114	E115	E118	E119
ON	ON	ON	ON	ON	ON	ON	ON	ON	ON

0-2 MHz Frequency Range and Pseudo-Feedback (no External Encoder Connected)

Jumpers Setting									
Input 1					Input 2				
E110	E111	E112	E116	E117	E113	E114	E115	E118	E119
ON	OFF	OFF	ON	ON	ON	OFF	OFF	ON	ON
E34 - E37: Encoder Sampling Clock Frequency Control									
E34A	E34	E35	E36	E37	SCLK Clock Frequency				
ON	OFF	OFF	OFF	OFF	19.6608 MHz				

0-100 kHz Frequency Range and Pseudo-Feedback (no External Encoder Connected)

Jumpers Setting									
Input 1					Input 2				
E110	E111	E112	E116	E117	E113	E114	E115	E118	E119
ON	ON	ON	OFF	OFF	ON	ON	ON	OFF	OFF

0-2 MHz Frequency Range and External Encoder Feedback Connected

Jumpers Setting									
Input 1					Input 2				
E110	E111	E112	E116	E117	E113	E114	E115	E118	E119
ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF

SUGGESTED I/O M-VARIABLE DEFINITIONS

General Purpose Inputs and Outputs

```
M1->Y:$FFC4,0,1                ; Machine Output 1
M2->Y:$FFC4,1,1                ; Machine Output 2
M3->Y:$FFC4,2,1                ; Machine Output 3
M4->Y:$FFC4,3,1                ; Machine Output 4
M5->Y:$FFC4,4,1                ; Machine Output 5
M6->Y:$FFC4,5,1                ; Machine Output 6
M7->Y:$FFC4,6,1                ; Machine Output 7
M8->Y:$FFC4,7,1                ; Machine Output 8
M9->Y:$FFC4,0,8,U              ; Machine Outputs 1-8 treated as byte
M11->Y:$FFC3,0,1               ; Machine Input 1
M12->Y:$FFC3,1,1               ; Machine Input 2
M13->Y:$FFC3,2,1               ; Machine Input 3
M14->Y:$FFC3,3,1               ; Machine Input 4
M15->Y:$FFC3,4,1               ; Machine Input 5
M16->Y:$FFC3,5,1               ; Machine Input 6
M17->Y:$FFC3,6,1               ; Machine Input 7
M18->Y:$FFC3,7,1               ; Machine Input 8
M19->Y:$FFC3,0,8,U             ; Machine Inputs 1-8 treated as byte
```

Thumbwheel Port Bits (Can be Used as General Purpose I/O)

(These definitions are valid for PMAC Mini PCI only)

```
M40->Y:$FFC2,0,1               ; SEL0 Output
M41->Y:$FFC2,1,1               ; SEL1 Output
M42->Y:$FFC2,2,1               ; SEL2 Output
M43->Y:$FFC2,3,1               ; SEL3 Output
M44->Y:$FFC2,4,1               ; SEL4 Output
M45->Y:$FFC2,5,1               ; SEL5 Output
M46->Y:$FFC2,6,1               ; SEL6 Output
M47->Y:$FFC2,7,1               ; SEL7 Output
M48->Y:$FFC2,0,8,U             ; SEL0-7 Outputs treated as a byte
M50->Y:$FFC1,0,1               ; DAT0 Input
M51->Y:$FFC1,1,1               ; DAT1 Input
M52->Y:$FFC1,2,1               ; DAT2 Input
M53->Y:$FFC1,3,1               ; DAT3 Input
M54->Y:$FFC1,4,1               ; DAT4 Input
M55->Y:$FFC1,5,1               ; DAT5 Input
M56->Y:$FFC1,6,1               ; DAT6 Input
M57->Y:$FFC1,7,1               ; DAT7 Input
M58->Y:$FFC1,0,8,U             ; DAT0-7 Inputs treated as a byte
```

E-POINT JUMPER DESCRIPTIONS

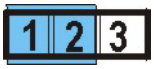
E0: Reserved for Future Use

E-Point and Physical Layout	Location	Description	Default
E0 	**F1**	Reserved for future use	No jumper installed

Warning:

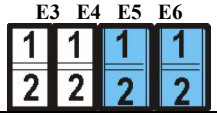
The jumper setting must match the type of driver IC, or damage to the IC will result.

E1 - E2: Machine Output Supply Voltage Configure

E-Point and Physical Layout	Location	Description	Default
E1 	**E1**	Jump pin 1 to 2 to apply +V (+5V to 24V) to pin 10 of U55 (should be ULN2803A for sink output configuration) JOPTO Machine outputs M01-M08. Jump pin 2 to 3 to apply GND to pin 10 of U55 (should be UDN2981A for source output configuration). Also see E2.	1-2 Jumper installed
E2 	**E1**	Jump pin 1 to 2 to apply GND to pin 9 of U55 (should be ULN2803A for sink output configuration). Jump pin 2 to 3 to apply +V (+5V to 24V) to pin 9 of "U55" (should be UDN2981A for source output configuration). Also see E1.	1-2 Jumper installed
Note: E1 and E2 must number in the same direction.			

E3 - E6: Servo Clock Frequency Control

The servo clock (which determines how often the servo loop is closed) is derived from the phase clock (see E29 - E33A and E98) through a divide-by-N counter. Jumpers E3 through E6 control this dividing function.

E3	E4	E5	E6	Servo Clock Frequency	Default and Physical Layout E3 E4 E5 E6 
ON	ON	ON	ON	= Phase Clock Divided by 1	
OFF	ON	ON	ON	= Phase Clock Divided by 2	
ON	OFF	ON	ON	= Phase Clock Divided by 3	
OFF	OFF	ON	ON	= Phase Clock Divided by 4	Only E5 and E6 On
ON	OFF	ON	ON	= Phase Clock Divided by 5	
OFF	ON	OFF	ON	= Phase Clock Divided by 6	
ON	OFF	OFF	ON	= Phase Clock Divided by 7	
OFF	OFF	OFF	ON	= Phase Clock Divided by 8	
ON	ON	ON	OFF	= Phase Clock Divided by 9	
OFF	ON	ON	OFF	= Phase Clock Divided by 10	
ON	OFF	ON	OFF	= Phase Clock Divided by 11	
OFF	OFF	ON	OFF	= Phase Clock Divided by 12	
ON	ON	OFF	OFF	= Phase Clock Divided by 13	
OFF	ON	OFF	OFF	= Phase Clock Divided by 14	
ON	OFF	OFF	OFF	= Phase Clock Divided by 15	
OFF	OFF	OFF	OFF	= Phase Clock Divided by 16	

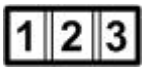
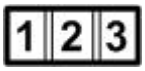
The setting of I-Variable I10 should be adjusted to match the servo interrupt cycle time set by E98, E3–E6, E29–E33 and the master clock frequency. I10 holds the length of a servo interrupt cycle, scaled so that 8,388,608 equals one millisecond. Since I10 has a maximum value of 8,388,607, the servo interrupt cycle time should always be less than a millisecond (unless the basic unit of time on PMAC should be something other than a millisecond. To have a servo sample time for a motor greater than one millisecond, the sampling may be slowed in software for that motor with variable Ix60.

Approximate servo frequency may be measured by typing successive **RX0** commands in a PMAC terminal window to read the servo cycle counter with the carriage return characters for the two commands hit exactly ten seconds apart. To obtain the servo frequency in kHz, take the difference of the two responses and divide by 10,000.

E7: Machine Input Sourcing/Sinking Control

E-Point and Physical Layout	Location	Description	Default
E7 	F1	Jump pin 1 to 2 to apply +5V to input reference resistor sip pack. This will bias MI1 to MI8 inputs to +5V for off state; input must then be grounded for on state. Jump pin 2 to 3 to apply GND to input reference resistor sip pack. This will bias MI1 to MI8 inputs to GND for off state; input must then be pulled up for on state (+5V to +24V)	1-2 Jumper installed

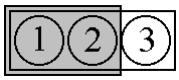
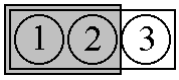
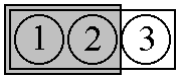
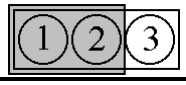
E8 – E10: Synchronizing PMAC

E-Point and Physical Layout	Location	Description	Default
E8 	**C1**	Jump pin 1-2 for NULL modem connection (DTR connects to DSR). Jump pin 2-3 for differential Phase signal (PHASE/).	No jumper installed
E9 	**C1**	Jump pin 1-2 for NULL modem connection (DTR connects to DSR). Jump pin 2-3 for differential Servo signal (SERVO/).	No jumper installed
E10 	**E1**	Jump pin 1-2 to select to receive external clocks CARD0.	No jumper installed
Note: Jumpers E8 and E9 must have the same settings.			

E10A - E10C: Flash Firmware Bank Select

E-Point and Physical Layout	Location	Description	Default
E10A 	**G2**	Flash firmware bank, select jumper 1.	No jumper installed
E10B 	**G2**	Flash firmware bank, select jumper 2.	No jumper installed
E10C 	**G2**	Flash firmware bank, select jumper 3.	No jumper installed

E11-E14: Encoder Single Ended/Differential Select (Note: REV-103 and above)

E Point and Physical Layout	Location	Description	Default
E11  **E12**  **E13**  **E14** 		Jump pin 2 to 3 to obtain differential encoder input mode. This will bias encoder negative inputs to VCC = 5V Jump pin 1 to 2 to obtain non-differential encoder input mode. This will bias encoder negative inputs to 1/2 VCC = 2.5V	1-2 Jumper installed

E17A - E17D: Amplifier-Enable/Direction Polarity Control

E-Point and Physical Layout	Location	Description	Default
E17A 	**A3**	Jump 1-2 for high TRUE AENA1. Remove jumper for low TRUE AENA1.	No jumper installed
E17B 	**A3**	Jump 1-2 for high TRUE AENA2. Remove jumper for low TRUE AENA2.	No jumper installed
E17C 	**A3**	Jump 1-2 for high TRUE AENA3. Remove jumper for low TRUE AENA3.	No jumper installed
E17D 	**A3**	Jump 1-2 for high TRUE AENA4. Remove jumper for low TRUE AENA4.	No jumper installed
Low-true enable is the fail-safe option with the default sinking (open-collector) ULN2803A output driver IC in U44. If U44 is replaced with a UDN2981A sourcing driver IC (and E101 and E102 are changed), high-true enable is the fail-safe option.			

E19: Watchdog Disable

E-Point and Physical Layout	Location	Description	Default
E19 	**F1**	Jump pin 1 to 2 to disable Watchdog timer (for test purposes only). Remove jumper to enable Watchdog timer.	No jumper installed

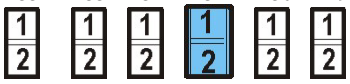
E20 - E22: Flash Firmware Bank Select

E-Point and Physical Layout	Location	Description	Default
E20 	**G3**	Power Up/Reset Load Source Jumper 1.	No jumper installed
E21 	**G3**	Power Up/Reset Load Source Jumper 2. Install to read flash IC on power-up/ reset.	Jumper installed
E22 	**G3**	Power Up/Reset Load Source Jumper 3. Install to read flash IC on power-up/ reset.	Jumper installed
Other combinations are for factory use only; the board will not operate in any other configuration			

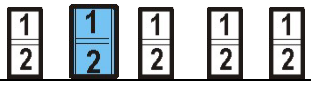
E23: Firmware Load

E-Point and Physical Layout	Location	Description	Default
E23 	**G3**	Remove jumper for normal operation. Jump pin 1 to 2 to reload firmware through serial or bus port.	No jumper installed

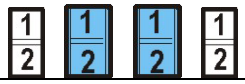
E29 - E33A: Phase Clock Frequency Control

E29	E30	E31	E32	E33	E33A	Phase Clock Freq. E98@1-2	Phase Clock Freq. E98@2-3	Default and Physical Layout E33A E33 E32 E31 E30 E29 
ON	OFF	OFF	OFF	OFF	OFF	2.26 kHz	1.13 kHz	
OFF	ON	OFF	OFF	OFF	OFF	4.52 kHz	2.26 kHz	
OFF	OFF	ON	OFF	OFF	OFF	9.04 kHz	4.52 kHz	E31 ON
OFF	OFF	OFF	ON	OFF	OFF	18.07 kHz	9.04 kHz	
OFF	OFF	OFF	OFF	ON	OFF	36.14 kHz	18.07 kHz	
OFF	OFF	OFF	OFF	OFF	ON	72.28 kHz	36.14 kHz	
Jumpers E29 through E33A control the speed of the phase clock, and, indirectly, the servo clock, which is divided down from the phase clock (see E3 - E6). No more than one of these six jumpers may be on at a time.								

E34A - E37: Encoder Sampling Clock Frequency Control

E34A	E34	E35	E36	E37	SCLK Clock Frequency 19.6608 MHz Master Clock	Default and Physical Layout E34A E34 E35 E36 E37 
ON	OFF	OFF	OFF	OFF	19.6608 MHz	
OFF	ON	OFF	OFF	OFF	9.8304 MHz	E34 On
OFF	OFF	ON	OFF	OFF	4.9152 MHz	
OFF	OFF	OFF	ON	OFF	2.4576 MHz	
OFF	OFF	OFF	OFF	ON	1.2288 MHz	
Jumpers E34 - E37 control the encoder-sampling clock (SCLK) used by the gate array ICs. No more than one of these five jumpers may be on at a time.						

E44 - E47: Communications Control

Baud Rate Control E Points				Baud Rate			Default and Physical Layout
E44	**E45**	**E46**	**E47**		**Standard CPU, 40 MHz Flash CPU (Opt 5A)**	**60 MHz Flash CPU (Opt 5B)**	**E44 E45 E46 E47** 
ON	ON	ON	ON		Disabled	Disabled	
OFF	ON	ON	ON		600	900	
ON	OFF	ON	ON		800*	1200	
OFF	OFF	ON	ON		1200	1800	
ON	ON	OFF	ON		1600*	2400	
OFF	ON	OFF	ON		2400	3600	
ON	OFF	OFF	ON		3200*	4800	
OFF	OFF	OFF	ON		4800	7200	
ON	ON	ON	OFF		6400*	9600	Opt 5B
OFF	ON	ON	OFF		9600	14400	Standard, Opt 5A
ON	OFF	ON	OFF		12800*	19200	
OFF	OFF	ON	OFF		19200	28800	
ON	ON	OFF	OFF		25600*	38400	
OFF	ON	OFF	OFF		38400	57600	
ON	OFF	OFF	OFF		51200*	76800	
OFF	OFF	OFF	OFF		76800	115200	

Jumpers E44 - E47 control what baud rate is used for serial communications. Any character received over the bus causes PMAC to use the bus for its standard communications. The serial port is disabled if E-points E44-E47 are all on.

These jumpers are read only at power-up/reset to set the baud rate at that time. Currently, Flex CPU's communication baud rate is determined at power-up/reset by variable I54.

* Non-standard baud rate

E48: Reserved for future use

E-Point and Physical Layout	Location	Description	Default
E48 	**E2**	Reserved for future use	No jumper installed

E49: Serial Communications Parity Control

E-Point and Physical Layout	Location	Description	Default
E49 	**E2**	Jump pin 1 to 2 for no serial parity; remove jumper for odd serial parity.	Jumper installed

E50: EAROM Save Enable/Disable

E-Point and Physical Layout	Location	Description	Default
E50 	**E2**	Jump pin 1 to 2 to enable save to EAROM or flash memory; remove jumper to disable save to EAROM or flash memory.	Jumper installed

E51: Normal/Re-Initializing Power-Up

E-Point and Physical Layout	Location	Description	Default
E51 	**E2**	Jump pin 1 to 2 to re-initialize on power-up/reset; remove jumper for normal power-up/reset.	No jumper installed

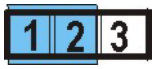
E85, E87, E88: Analog Power Source Configuration

E-Point and Physical Layout	Location	Description	Default
E85  E88 E87 **E85**	**E3**	Jump pin 1 to pin 2 to allow analog +V to come from digital side -- P1 or TB1 -- ties amplifier and PMAC Mini PCI power supply together, defeats opto-isolation. Remove jumper to keep analog +V separate from digital +12V. **Note:** If E85 is changed, E88 and E87 must also be changed Also see E90.	No jumper
E87  E88 **E87** E85	**E3**	Jump pin 1 to pin 2 to tie analog common AGND to digital common GND -- defeats opto-isolation. Remove jumper to keep AGND and GND separate. **Note:** If E87 is changed, E85 and E88 must also be changed Also see E90.	No jumper
E88  **E88** E87 E85	**E3**	Jump pin 1 to pin 2 to allow analog -V to come from digital side -- P1or TB1 – ties amplifier and PMAC Mini PCI power supply together, defeats opto-isolation. Remove jumper to keep analog -V separate from digital -12V. **Note:** If E88 is changed, E85 and E87 must also be changed Also see E90.	No jumper

E89: Amplifier-Supplied Switch Pull-Up Enable

E-Point and Physical Layout	Location	Description	Default
E89 	**A1**	Jump pin 1 to 2 to allow A+V on J8 (JAUX) pin 13, to tie to A+15V on J11 (JMACH1) pin 59. Remove jumper to permit separate voltage supply from A+V for input flags (+12V to +24V for sinking drivers, 0V for sourcing drivers). This jumper must be installed to allow A+15V to power the OPTO switch sensor inputs (including limits) from the same OPTO-power supply that powers the amplifier output stage. Also see E90.	Jumper installed

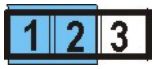
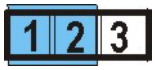
E90: Host-Supplied Switch Pull-Up Enable

E-Point and Physical Layout	Location	Description	Default
E90 	**A1**	Jump pin 1 to 2 to allow A+V/FRET on J8 pin 13 and/or J11 pin 59 (also see E89), to power OPTO switch sensor inputs (including limits). Jump pin 2 to 3 to allow +12V from DC bus connector P1-pin B09 to power "OPTO" switch sensor inputs (including limits). Optical isolation is then lost. Also see E85, E87, E88 and PMAC opto-isolation diagram.	1-2 Jumper installed

E98: DAC/ADC Clock Frequency Control

E-Point and Physical Layout	Location	Description	Default
E98 	**C2**	Jump 1-2 to provide a 2.45 MHz DCLK signal to DACs and ADCs. Jump 2-3 to provide a 1.23 MHz DCLK signal to DACs and ADCs. Important for high accuracy A/D conversion on Acc-28A boards. **Note:** This also divides the phase and servo clock freq. in half. See E29-E33, E3-E6	1-2 Jumper installed

E101 - E102: Amplifier Enable Output Configure

E-Point and Physical Layout	Location	Description	Default
E100 	**B2**	Jump pin 1 to 2 to apply A+15V from J11 pin 59 to pin 1 of E101, pin 3 of E102, and FAULT input flag return. This makes U44 AENA/ EQU / PULSE / DIR / FEFCO driver IC work from analog A+15V supply. Jump pin 2 to 3 to apply A+V (12-24V) from J8 pin 13 to pin 1 of E101, pin 3 of E102, and FAULT input flag return. This makes U44 AENA/EQU/PULSE/DIR/FEFCO driver IC work from separate A+V (12-24V) supply. (This cannot be used when A+V is brought from digital side through E85.)	1-2 Jumper installed
E101 	**B2**	Jump pin 1 to 2 to apply A+15V/A+V (as set by E100) to pin 11 of U44 AENAn and EQUn driver IC (should be ULN2803A for sink output configuration). Jump pin 2 to 3 to apply GND to pin 11 of U44 (should be UDN2981A for source output configuration).	1-2 Jumper installed
E102 	**B2**	Jump pin 1 to 2 to apply GND to pin 11 of U44 AENAn and EQUn (should be ULN2803A for sink output configuration). Jump pin 2 to 3 to apply A+15V/A+V (as set by E100) to pin 11 of U44 (should be UDN2981A for source output configuration).	1-2 Jumper installed
Note: E100, E101 and E102 must number in the same direction			

E110 - E115: V/F Converter Configuration

(Voltage-to-Frequency Converter Option [OPT 15] Required)

E-Point and Physical Layout	Location	Description	Default
E110 	**B1**	Jump pin 1 to 2 to tie DAC1 output to WIPER1 input (stepper drive). Remove jumper to keep lines separate.	No jumper installed
E111 	**B1**	Jump pin 1 to 2 to set 10kHz/V gain (100kHz max) on 1st V/F converter. Remove jumper to set 200kHz/V gain (2MHz max) on 1st V/F converter.	No jumper installed
E112 	**B1**	Jump pin 1 to 2 to set 10kHz/V gain (100kHz max) on 1st V/F converter. Remove jumper to set 200kHz/V gain (2MHz max) on 1st V/F converter.	No jumper installed
E113 	**B2**	Jump pin 1 to 2 to tie DAC2 output to WIPER2 input (stepper drive). Remove jumper to keep lines separate.	No jumper installed
E114 	**B2**	Jump pin 1 to 2 to set 10kHz/V gain (100kHz max) on 2nd V/F converter. Remove jumper to set 200kHz/V gain (2MHz max) on 2nd V/F converter.	No jumper installed
E115 	**B2**	Jump pin 1 to 2 to set 10kHz/V gain (100kHz max) on 2nd V/F converter. Remove jumper to set 200kHz/V gain (2MHz max) on 2nd V/F converter.	No jumper installed

E116 - E119: V/F Converter Configuration

(Voltage-to-Frequency Converter Option [OPT 15] Required)

E-Point and Physical Layout	Location	Description	Default
E116 	**A3**	Jump pin 1 to 2 to tie AENA1/DIR1 output to CHB3 input. Remove jumper to keep lines separate.	No jumper installed
E117 	**A3**	Jump pin 1 to 2 to tie PULSE1 output to CHA3 input. Remove jumper to keep lines separate.	No jumper installed
E118 	**A3**	Jump pin 1 to 2 to tie PULSE2 output to CHA4 input. Remove jumper to keep lines separate.	No jumper installed
E119 	**A3**	Jump pin 1 to 2 to tie AENA2/DIR2 output to CHB4 input. Remove jumper to keep lines separate.	No jumper installed
Note: For stepper Feedback install E116 and E119			

MATING CONNECTORS

This section lists several options for each connector. Choose an appropriate one for your application.

J1 (JDISP)/Display Port

1. Two 14-pin female flat cable connector Delta Tau P/N 014-R00F14-0K0 T&B Ansley P/N 609-1441
2. 171-14 T&B Ansley standard flat cable stranded 14-wire
3. Phoenix varioface modules type FLKM14 (male pins) P/N 22 81 02 1

J2 (JEXP)/Expansion

1. Two 50-pin female flat cable connector Delta Tau P/N 014-R00F50-0K0 T&B Ansley P/N 609-5041
2. 171-50 T&B Ansley standard flat cable stranded 50-wire
3. Phoenix varioface module type FLKM 50 (male pins) P/N 22 81 08 9 used for daisy chaining acc-14 I/0, -23 A and D connectors -24 expansion

J3 (JTHW)/Multiplexer Port

1. Two 26-pin female flat cable connector Delta Tau P/N 014-R00F26-0K0 T&B Ansley P/N 609-2641
2. 171-26 T&B Ansley standard flat cable stranded 26-wire
3. Phoenix varioface module type FLKM 26 (male pins) P/N 22 81 05 0

J4 (JRS232)/Serial Communications

1. Two 10-pin female flat cable connector Delta Tau P/N 014-R00F10-0K0 T&B Ansley P/N 609-1041
2. 171-10 T&B Ansley standard flat cable stranded 26-wire
3. Phoenix varioface module type FLKM 34 (male pins) P/N 22 81 06 3

J5 (JOPT)/OPTO I/O

1. Two 34-pin female flat cable connector Delta Tau P/N 014-R00F34-0K0 T&B Ansley P/N 609-3441
2. 171-34 T&B Ansley standard flat cable stranded 34 wire
3. Phoenix varioface module type FLKM 34 (male pins) P/N 22 81 06 3

J7 (JS1)/A-D Inputs 1-4

1. Two 16-pin female flat cable connector Delta Tau P/N 014-R00F16-0K0 T&B Ansley P/N 609-1641-16
2. 171-16 T&B Ansley standard flat cable stranded 16 wire
3. Phoenix varioface module type FLKM 16 (male pins) P/N 22 81 03 4

J8 (JAUX)/Auxiliary I/O

1. Two 14-pin female flat cable connector Delta Tau P/N 014-R00F14-0K0 T&B Ansley P/N 609-1641-14
2. 171-14 T&B Ansley standard flat cable stranded 14 wire
3. Phoenix varioface module type FLKM 14(male pins)

J11 (JMACH)/Machine Connector

1. Two 60-pin female flat cable connector Delta Tau P/N 014-R00F60-0K0 T&B Ansley P/N 609-6041 available as ACC 8P or 8D
2. 171-60 T&B Ansley standard flat cable stranded 60 wire
3. Phoenix varioface module type FLKM 60 (male pins) P/N 22 81 09 2

Note:

Normally, J11 is used with Acc-8P or 8D with Option P which provides complete terminal strip fan-out of all connections.

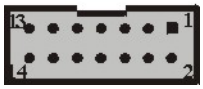
TB1 (JPWR)

1. 4-pin terminal block, Phoenix Connector, MKDS41-3.5

CONNECTOR PINOUTS

Headers

J1 JDISP (14-Pin Header)



Front View

Pin #	Symbol	Function	Description	Notes
1	Vdd	Output	+5V Power	Power Supply Out
2	Vss	Common	PMAC Common	
3	Rs	Output	Read Strobe	TTL Signal Out
4	Vee	Output	Contrast Adjust. VEE	0 to +5VDC *
5	E	Output	Display Enable	High is Enable
6	R/W	Output	Read or Write	TTL Signal Out
7	DB1	Output	Display Data 1	
8	DB0	Output	Display Data 0	
9	DB3	Output	Display Data 3	
10	DB2	Output	Display Data 2	
11	DB5	Output	Display Data 5	
12	DB4	Output	Display Data 4	
13	DB7	Output	Display Data 7	
14	DB6	Output	Display Data 6	

The JDISP connector is used to drive the 2-line x 24-character (Acc-12), 2 x 40 (Acc-12A) LCD, or the 2 x 40 vacuum fluorescent (ACC. 12C) display unit. The **DISPLAY** command may be used to send messages and values to the display.

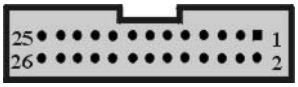
See Also:

Program Commands; **DISPLAY**
Accessories; Acc-12, ACC16D
Memory Map; Y:$0780 - $07D1

Note: There is no J2 (JPAN) control panel connector on PMAC Mini PCI.

* Controlled by potentiometer R57

J3 JTHW (26-Pin Header)



Front View

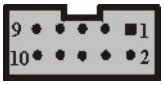
Pin #	Symbol	Function	Description	Notes
1	GND	Common	PMAC Common	
2	GND	Common	PMAC Common	
3	DAT0	Input	Data-0 Input	Data Input from Thumbwheel Switches
4	SEL0	Output	Select-0 Output	Scanner Output for reading TW Switches
5	DAT1	Input	Data-1 Input	Data Input from Thumbwheel Switches
6	SEL1	Output	Select-1 Output	Scanner Output for reading TW Switches
7	DAT2	Input	Data-2 Input	Data Input from Thumbwheel Switches
8	SEL2	Output	Select-2 Output	Scanner Output for reading TW Switches
9	DAT3	Input	Data-3 Input	Data Input from Thumbwheel Switches
10	SEL3	Output	Select-3 Output	Scanner Output for reading TW Switches
11	DAT4	Input	Data-4 Input	Data Input from Thumbwheel Switches
12	SEL4	Output	Select-4 Output	Scanner Output for reading TW Switches
13	DAT5	Input	Data-5 Input	Data Input from Thumbwheel Switches
14	SEL5	Output	Select-5 Output	Scanner Output for reading TW Switches
15	DAT6	Input	Data-6 Input	Data Input from Thumbwheel Switches
16	SEL6	Output	Select-6 Output	Scanner Output for reading TW Switches
17	DAT7	Input	Data-7 Input	Data Input from Thumbwheel Switches
18	SEL7	Output	Select-7 Output	Scanner Output for reading TW Switches
19	N.C.	N.C.	No Connection	
20	GND	Common	PMAC Common	
21	BFLD/	N.C.	No Connection	
22	GND	Common	PMAC Common	
23	IPLD/	N.C.	No Connection	
24	GND	Common	PMAC Common	
25	+5V	Output	+5VDC Supply	Power Supply Out
26	INIT/	Input	PMAC Reset	Low is Reset

The JTHW multiplexer port provides eight inputs and eight outputs at TTL levels. While these I/O can be used in un-multiplexed form for 16 discrete I/O points, most will utilize PMAC software and accessories to use this port in multiplexed form to multiply the number of I/O that can be accessed on this port. In multiplexed form, some of the SELn outputs are used to select which of the multiplexed I/O are to be accessed.

See also:

I/O and Memory Map Y:$FFC1, Y:$FFC2
Suggested M-variables M40 - M58
M-variable formats TWB, TWD, TWR, TWS
Acc-8D Opt 7, Acc-8D Opt 9, Acc-18, Acc-34x, NC Control Panel

J4 JRS232 (10-Pin Header)



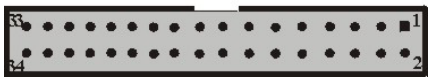
Front View

Pin #	Symbol	Function	Description	Notes
1	PHASE+	Bidirectional	Receive/Transmit Phase Clock. Check Jumpers E10, E8 and E9	
2	PHASE- or DTR	Bidirectional	Data Term Ready	Tied to DSR
3	TXD/	Input	Receive Data	Host Transmit Data
4	CTS	Input	Clear to Send	Host Ready Bit
5	RXD/	Output	Send Data	Host Receive Data
6	RTS	Output	Request to Send	PMAC Ready Bit
7	SERVO- or DSR	Bidirectional	Data set Ready	Tied to DTR
8	SERVO+	Bidirectional	Receive/Transmit Servo Clock. Check Jumpers E10, E8 and E9	
9	GND	Common	PMAC Common	
10	+5V	Output	+5VDC Supply	Power Supply Out

The JRS232 connector provides the PMAC Mini PCI with the ability to communicate serially with an RS232 port. This connector can be used for daisychain interconnection of multiple PMACs. Check E10.

See Also: Serial Communications

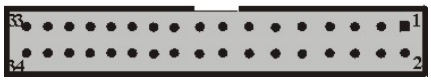
J5 JOPT (34-Pin Connector)



Front View

Pin #	Symbol	Function	Description	Notes
1	MI8	Input	Machine Input 8	Low is true
2	GND	Common	PMAC Common	
3	MI7	Input	Machine Input 7	Low is true
4	GND	Common	PMAC Common	
5	MI6	Input	Machine Input 6	Low is true
6	GND	Common	PMAC Common	
7	MI5	Input	Machine Input 5	Low is true
8	GND	Common	PMAC Common	
9	MI4	Input	Machine Input 4	Low is true
10	GND	Common	PMAC Common	
11	MI3	Input	Machine Input 3	Low is true
12	GND	Common	PMAC Common	
13	MI2	Input	Machine Input 2	Low is true
14	GND	Common	PMAC Common	
15	MI1	Input	Machine Input 1	Low is true
16	GND	Common	PMAC Common	
17	MO8	Output	Machine Output 8	If Sinking Out Low True; If Source Out High True
18	GND	Common	PMAC Common	
19	MO7	Output	Machine Output 7	If Sinking Out Low True; If Source Out High True
20	GND	Common	PMAC Common	
21	MO6	Output	Machine Output 6	If Sinking Out Low True; If Source Out High True
22	GND	Common	PMAC Common	
23	MO5	Output	Machine Output 5	If Sinking Out Low True; If Source Out High True
24	GND	Common	PMAC Common	
25	MO4	Output	Machine Output 4	If Sinking Out Low True; If Source Out High True
26	GND	Common	PMAC Common	

J5 JOPT (34-Pin Connector) Continued

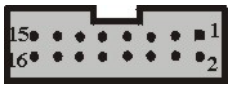


Front View

Pin #	Symbol	Function	Description	Notes
27	MO3	Output	Machine Output 3	If Sinking Out Low True; If Source Out High True
28	GND	Common	PMAC Common	
29	MO2	Output	Machine Output 2	If Sinking Out Low True; If Source Out High True
30	GND	Common	PMAC Common	
31	MO1	Output	Machine Output 1	If Sinking Out Low True; If Source Out High True
32	GND	Common	PMAC Common	
33	+V	I/O	+V Power I/O	+V = +5V TO +24V +5V Out from PMAC, +5 to +24V in from External Source, Diode Isolation from PMAC
34	GND	Common	PMAC Common	

This connector provides means for eight general-purpose inputs and eight general-purpose outputs. Inputs and outputs may be configured to accept or provide either +5V or +24V signals. Outputs can be made sourcing with an IC (U55 to UDN2981) and jumper (E1 and E2) change. E7 controls whether the inputs are pulled up or down internally. Outputs are rated to 100mA per line.

J7 JS1 (16- Pin Header)

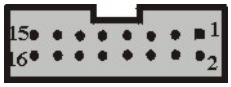


Front View

Pin #	Symbol	Function	Description	Notes
1	DCLK	Output	D to A, A to D Clock	DAC and ADC Clock for Chan. 1, 2, 3, 4
2	DATA+	Output	D to A Data	DAC Data for Chan. 1, 2, 3, 4
3	ASEL0/	Output	Chan. Select Bit 0	Select for Chan. 1, 2, 3, 4
4	ASEL1/	Output	Chan. Select Bit 1	Select for Chan. 1, 2, 3, 4
5	CNVRT	Output	A to D Convert	ADC Convert Sig. Chan. 1, 2, 3, 4
6	ADCIN	Input	A to D Data	ADC Data for Chan. 1, 2, 3, 4
7	OUT1/	Output	Amp. Enable/Dir.	Jumper-Set Polarity (E17A)
8	OUT2/	Output	Amp. Enable/Dir.	Jumper-Set Polarity (E17B)
9	OUT3/	Output	Amp. Enable/Dir.	Jumper-Set Polarity (E17C)
10	OUT4/	Output	Amp. Enable/Dir.	Jumper-Set Polarity (E17D)
11	AFLT1+	Input	Amp. Fault Input	Programmable Polarity (Ix25)
12	AFLT2+	Input	Amp. Fault Input	Programmable Polarity (Ix25)
13	AFLT3+	Input	Amp. Fault Input	Programmable Polarity (Ix25)
14	AFLT4+	Input	Amp. Fault Input	Programmable Polarity (Ix25)
15	+5V	Output	+5V Supply	Power Supply Out
16	GND	Common	PMAC Common	

This connector is used to communicate with an Acc-28 A/D converter board. It can be used also to build a digital amplifier interface. All signals are referenced to the digital common GND.

J8 JAUX (14-Pin Header)



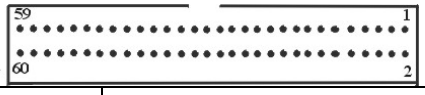
Front View

Pin #	Symbol	Function	Description	Notes
1	WIPER1	Input	0-10V Analog Input	1, 2
2	WIPER2	Input	0-10V Analog Input	1, 2
3	AGND	Common	Analog/Flag Common	
4	AGND	Common	Analog/Flag Common	
5	EQU1/	Output	Enc. 1 Position Compare	3
6	EQU2/	Output	Enc. 2 Position Compare	3
7	AENA1/ DIR1	Output	Amp. 1 Enable/Direction	3,4,5
8	AENA2/ DIR2	Output	Amp. 2 Enable/Direction	3,4,5
9	PULSE1	Output	Chan. 1 Pulse Command	1,3
10	PULSE2	Output	Chan. 2 Pulse Command	1,3
11	FEFCO/	Output	Watchdog Output	3
12	AGND	Common	Analog/Flag Common	
13	A+V/FRET	Input	Flag Supply Volt	6
14	A-15V	I/O	Analog Minus Supply	

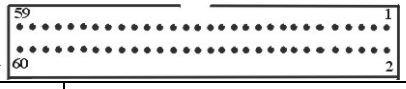
This connector provides auxiliary signals for the PMAC Mini PCI, including analog inputs, position compare outputs, pulse-and-direction outputs, and a flag supply/return voltage. All signals are referenced to AGND, isolated from the 5V digital circuitry.

Notes:

1. Requires Option 15 V/F Converters be installed to use.
2. WIPER1 is tied to DAC1 if jumper E110 is installed; WIPER2 is tied to DAC2 if jumper E113 is installed.
3. Open-collector sinking output in standard configuration (ULN2803A in U44); Can be replaced with sourcing driver (UDN2981A) in U44 socket; 100 mA per point sinking/sourcing capability.
4. Function of this signal determined by Ix02 and Ix25.
5. Can be tied to Encoder 3 or 4 feedback with jumpers (see E111, E112, E114, E115).
6. With jumper E89 ON, tied to A+15V from J11 pin 59; with E89 OFF and E90 at 1-2, can be separate +12V to +24V for input flags (HMFLn, PLIMn, MLIMn) with sinking drivers, or 0V for input flags with sourcing drivers.

J11 JMACH (60-Pin Header)			Top View 	
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	+5V	Output	+5V Power	For Encoders, 1
2	+5V	Output	+5V Power	For Encoders, 1
3	GND	Common	Digital Common	
4	GND	Common	Digital Common	
5	CHC3	Input	Encoder C Ch. Pos.	2
6	CHC4	Input	Encoder C Ch. Pos.	2
7	CHC3/	Input	Encoder C Ch. Neg.	2,3
8	CHC4/	Input	Encoder C Ch. Neg.	2,3
9	CHB3	Input	Encoder B Ch. Pos.	2
10	CHB4	Input	Encoder B Ch. Pos.	2
11	CHB3/	Input	Encoder B Ch. Neg.	2,3
12	CHB4/	Input	Encoder B Ch. Neg.	2,3
13	CHA3	Input	Encoder A Ch. Pos.	2
14	CHA4	Input	Encoder A Ch. Pos.	2
15	CHA3/	Input	Encoder A Ch. Neg.	2,3
16	CHA4/	Input	Encoder A Ch. Neg.	2,3
17	CHC1	Input	Encoder C Ch. Pos.	2
18	CHC2	Input	Encoder C Ch. Pos.	2
19	CHC1/	Input	Encoder C Ch. Neg.	2,3
20	CHC2/	Input	Encoder C Ch. Neg.	2,3
21	CHB1	Input	Encoder B Ch. Pos.	2
22	CHB2	Input	Encoder B Ch. Pos.	2
23	CHB1/	Input	Encoder B Ch. Neg.	2,3
24	CHB2/	Input	Encoder B Ch. Neg.	2,3
25	CHA1	Input	Encoder A Ch. Pos.	2
26	CHA2	Input	Encoder A Ch. Pos.	2
27	CHA1/	Input	Encoder A Ch. Neg.	2,3
28	CHA2/	Input	Encoder A Ch. Neg.	2,3
29	N.C.		No Connect	
30	N.C.		No Connect	
31	N.C.		No Connect	
32	N.C.		No Connect	
33	EQU1/	Output	Position Compare 1	6
34	EQU2/	Output	Position Compare 2	6
35	N.C.		No Connect	
36	N.C.		No Connect	
37	N.C.		No Connect	
38	N.C.		No Connect	
39	N.C.		No Connect	
40	N.C.		No Connect	
41	N.C.		No Connect	
42	N.C.		No Connect	
43	DAC1	Output	Ana. Out Pos. 1	4,11
44	DAC2	Output	Ana. Out Pos. 2	4,11

J11 JMACH (60-Pin Header) -Continued

Top View 

Pin #	Symbol	Function	Description	Notes
45	DAC1/	Output	Ana. Out Neg. 1	4,5
46	DAC2/	Output	Ana. Out Neg. 2	4,5
47	AENA1/DIR1	Output	Amp.-Ena/Dir. 1	6
48	AENA2/DIR2	Output	Amp.-Ena/Dir. 2	6
49	FAULT1	Input	Amp.-Fault 1	7
50	FAULT2	Input	Amp.-Fault 2	7
51	MLIM1	Input	Neg. End Limit 1	8,9
52	MLIM2	Input	Neg. End Limit 2	8,9
53	PLIM1	Input	Pos. End Limit 1	8,9
54	PLIM2	Input	Pos. End Limit 2	8,9
55	HMFL1	Input	Home-Flag 1	10
56	HMFL2	Input	Home-Flag 2	10
57	FEFCO/	Output	Watchdog Out	Indicator/Driver
58	AGND	Input	Analog Common	
59	A+15V/OPT+V	Input	Analog +15V Supply	
60	A-15V	Input	Analog -15V Supply	

The J11 connector is used to connect PMAC to the servo amps, flags, and encoders.

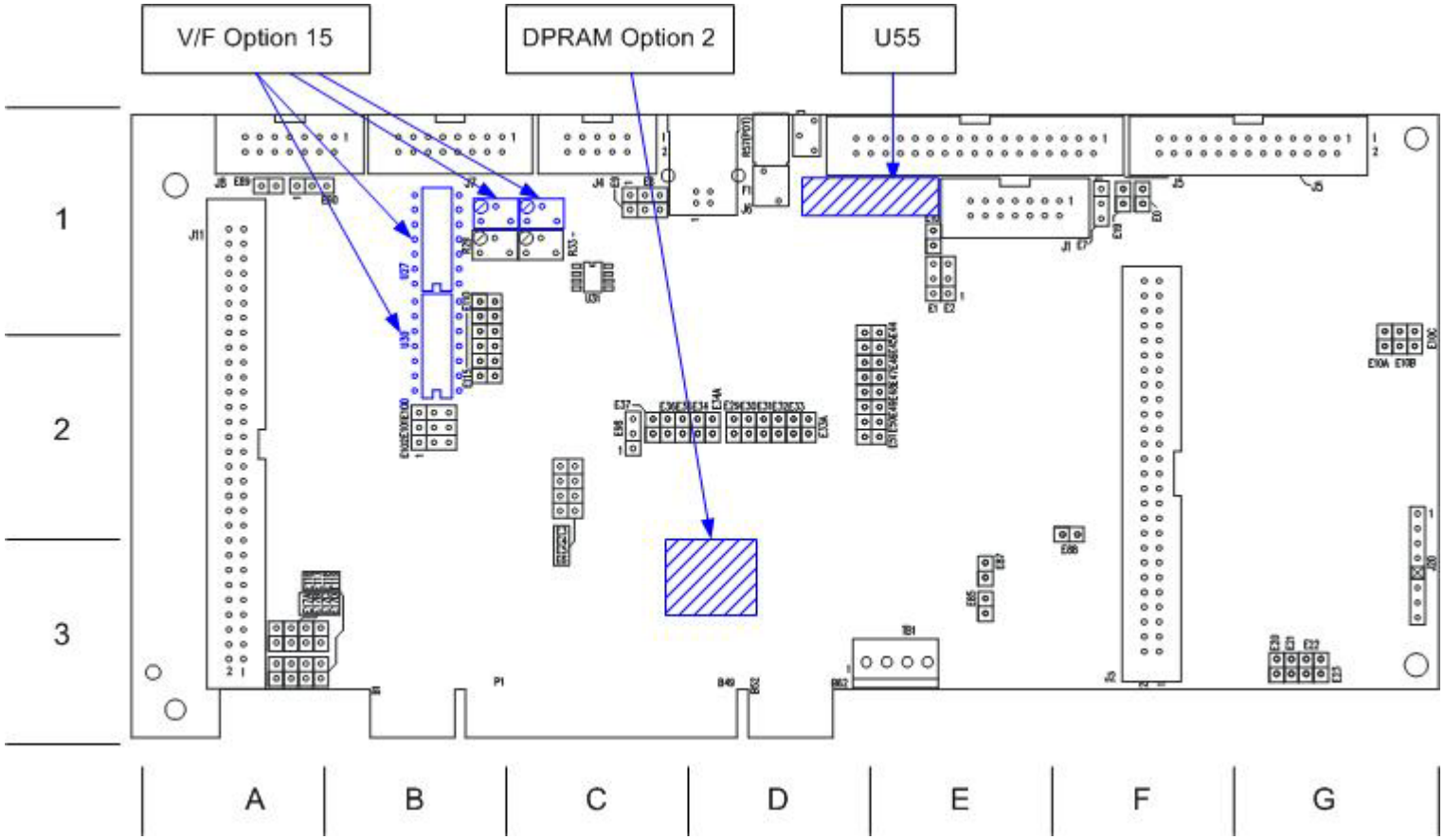
Notes:

1. In standalone applications, these lines can be used as +5V power supply inputs to power PMAC's digital circuitry. However, if a terminal block is available on the version of PMAC, bring the +5V power in through the terminal block.
2. Referenced to digital common (GND). Maximum of + 12V permitted between this signal and its complement.
3. If not used, leave this input floating (i.e. digital single-ended encoders).
4. + 10V, 10mA max, referenced to analog common (AGND).
5. Leave floating if not used; do not tie to AGND. In this case, AGND is the return line.
6. Functional polarity controlled by jumper E17. Sinking/sourcing nature of output control by IC type in U44 socket (default sinking) and E101/E102 configuration. Choice between AENA and DIR use controlled by Ix02 and Ix25.
7. Functional polarity controlled by variable Ix25. Must be conducting to AGND (sinking driver) to produce a 0 in PMAC software. Pull-up is to A+15V or A+V (12-24V) as determined by E100. Automatic fault function can be disabled with Ix25.
8. Pins marked PLIMn should be connected to switches at the positive end of travel. Pins marked MLIMn should be connected to switches at the negative end of travel.
9. Must be conducting to 0V (usually AGND) for PMAC to consider itself not into this limit. Automatic limit function can be disabled with Ix25.
10. Functional polarity for homing or other trigger use of HMFLn controlled by Encoder/Flag Variable 2 (I902, I907, etc.) HMFLn selected for trigger by Encoder/Flag Variable 3 (I903, I908, etc.). Must be conducting to 0V (usually AGND) to produce a 0 in PMAC software.
11. If DAC calibration is needed, R37 is for offset DAC1, and R41 is for offset DAC2.

Terminal Block

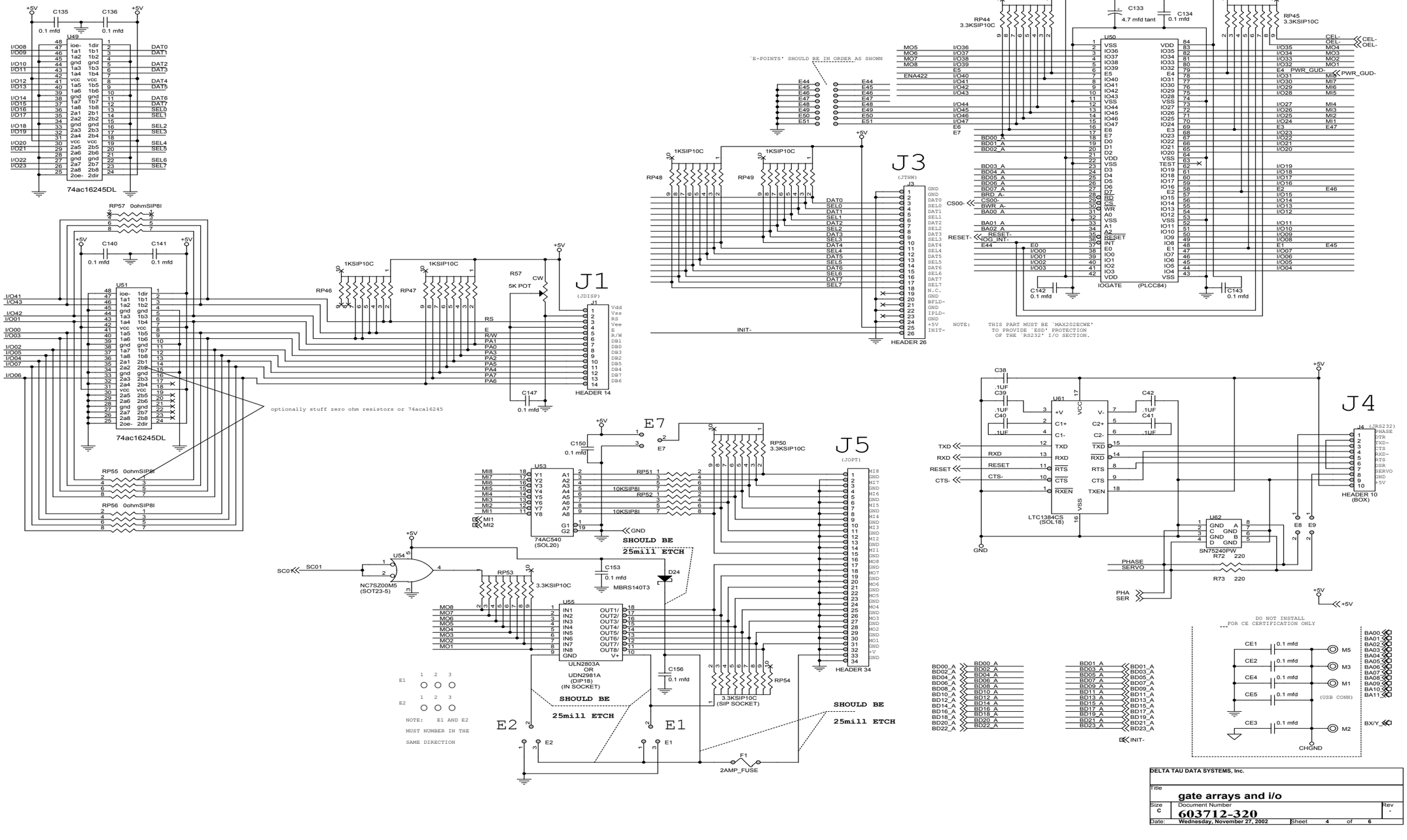
TB1 (JPWR) (4-Pin Terminal Block)				
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	GND	Common	Digital Ground	
2	+5V	Input	+5V Supply	Reference to digital ground
3	+12V	Input	+12V to +15V Supply	Reference to digital ground
4	-12V	Input	-12V to -15V Supply	Reference to digital ground
This terminal block may be used as an alternative power supply connector if PMAC Lite is not installed in a PC-bus. The +5V powers the digital electronics. If jumpers E85, E87, and E88 are installed, the +12V and -12V power the analog output stage (this defeats the optical isolation on PMAC). To keep the optical isolation between the digital and analog circuits on PMAC, provide analog power (+/-12V to +/-15V and AGND) through the JMACH connector, instead of the bus connector or this terminal block.				

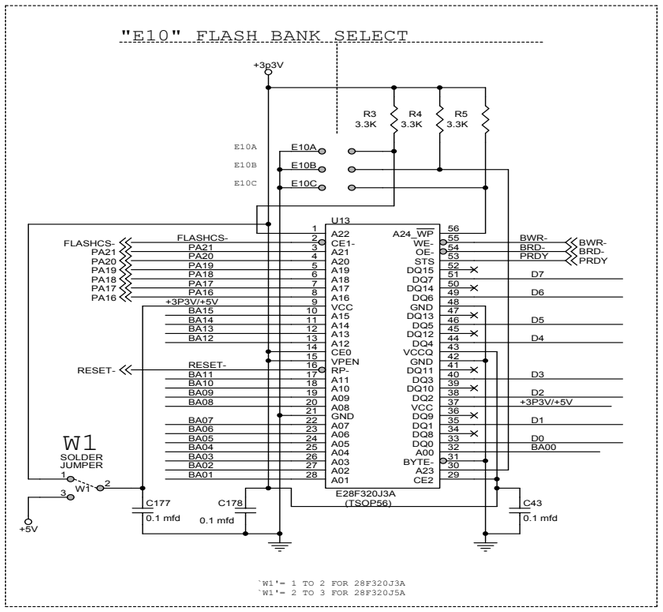
JUMPERS AND CONNECTORS LAYOUT

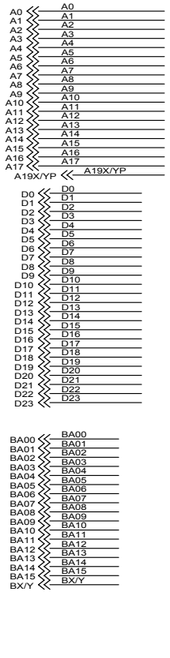


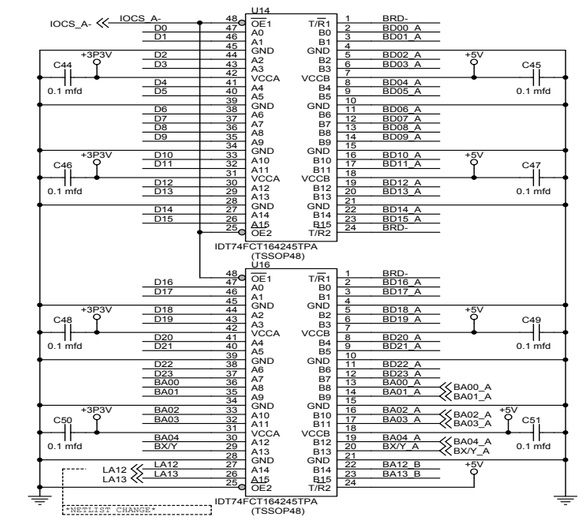
E1	D1	**E7**	D1	**E30**	E2	**E35**	D2	**E46**	C1	**E66**	E2	**E85**	F3	**E92**	E2	**E104**	A3	**E114**	E1
E2	D1	**E17A**	F2	**E31**	E2	**E36**	D2	**E47**	C1	**E67**	E2	**E87**	F3	**E98**	D2	**E105**	A3	**E115**	E1
E3	D3	**E17B**	F2	**E32**	E2	**E37**	D2	**E48**	C1	**E68**	E2	**E88**	G3	**E100**	G1	**E110**	F1	**E116**	G2
E4	D3	**E17C**	F2	**E33**	E2	**E39**	A3	**E49**	C1	**E69**	E2	**E89**	G1	**E101**	F1	**E111**	F1	**E117**	G2
E5	D3	**E17D**	F2	**E33A**	E2	**E44**	C1	**E50**	C1	**E70**	E2	**E90**	G1	**E102**	F1	**E112**	F1	**E118**	G2
E6	D3	**E29**	E2	**E34A**	D2	**E45**	C1	**E51**	C1	**E71**	E2	**E91**	E2	**E103**	A1	**E113**	E1	**E119**	G2
				E34	D2														

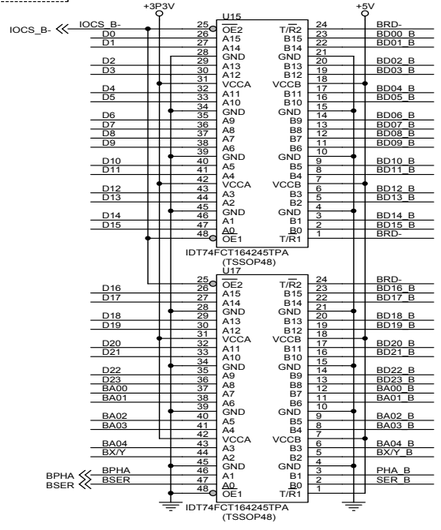
SCHEMATICS

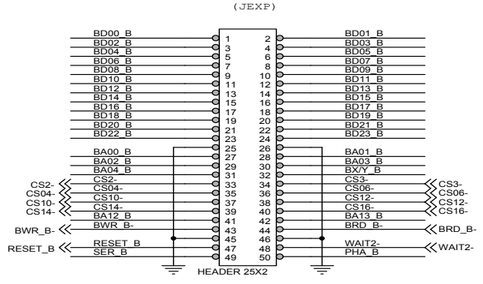

74ac16245DL
optionally stuff zero ohm resistors or 74aca16245
HEADER 14
HEADER 26
HEADER 34
HEADER 10 (BOX)
(PLCC84)
(SOL18)
(SOL20)
(SOT23-5)
(SIP SOCKET)
(IN SOCKET)
(USB CONN)
(JDISP)
(JTHW)
(JOPT)
(JRS232)
NOTE: THIS PART MUST BE `MAX202ECWE' TO PROVIDE `ESD' PROTECTION OF THE `RS232' I/O SECTION.
NOTE: E1 AND E2 MUST NUMBER IN THE SAME DIRECTION
`E-POINTS' SHOULD BE IN ORDER AS SHOWN
SHOULD BE 25mill ETCH
DO NOT INSTALL FOR CE CERTIFICATION ONLY
DELTA TAU DATA SYSTEMS, Inc.
gate arrays and i/o
603712-320
Wednesday, November 27, 2002
Sheet 4 of 6

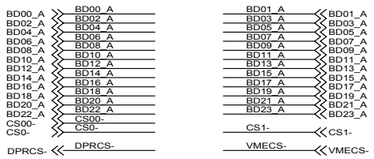




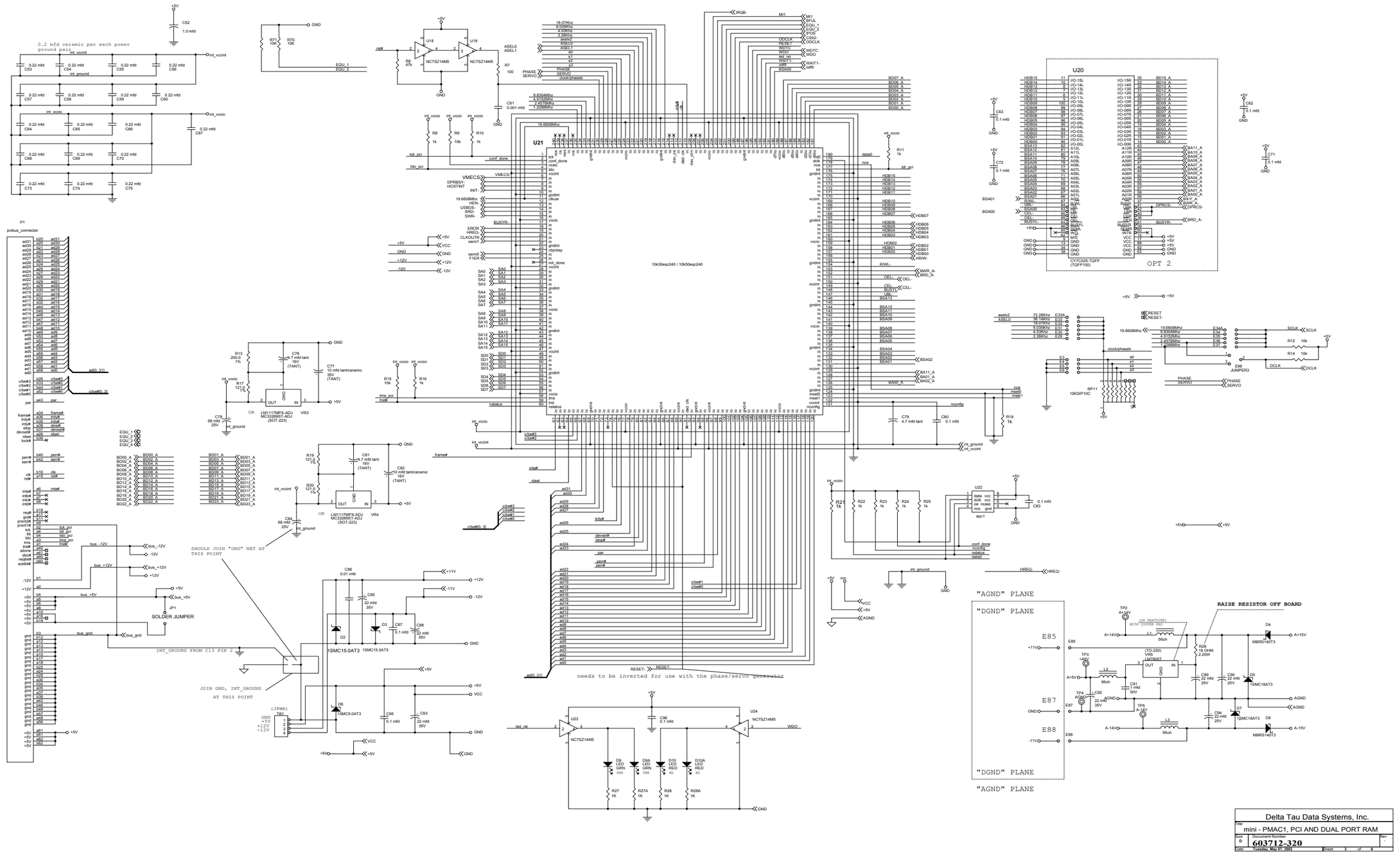








Delta Tau Data Systems, Inc.		
Title: mini - PMAC1 MEMORY,I/O		
Size: C	Document Number: 603712-320	Rev: -
Date: Tuesday, May 07, 2002	Sheet 2 of 6	


0.2 mfd ceramic per each power ground pair
int_vcoint
int_ground
int_vccio
int_vccio
P1
pcibus_connector
adi0_31
c/be#0_3
par
frame#
trdy#
irdy#
stop#
devsel#
idsel
perr#
serr#
clk
rst#
intab#
intcd#
req64#
ack64#
bus_-12V
bus_+12V
bus_+5V
bus_gnd
JP1
SOLDER JUMPER
INT_GROUND FROM C13 PIN 2
JOIN GND, INT_GROUND AT THIS POINT
SHOULD JOIN "GND" NET AT THIS POINT
OR
LM1117MPX-ADJ MC33269ST-ADJ (SOT-223)
VR3
VR4
1SMC15.0AT3
(JPWR)
TB1
U18
U19
NC7SZ14M5
ASEL0
ASEL1
PHASE
SERVO
clock/phaseb
9.8304Mhz
4.9152Mhz
2.4576Mhz
1.2288Mhz
19.6608Mhz
U21
10k30eqc240 / 10k50eqc240
VMECS-
DPRBSY-
HOSTINT
INIT-
HEN-
USBCE-
SRD-
SWR-
BUSYR-
ERQR
HREQ
CLKOUTN
serni0
F1ER
sernI0
conf_done
tck_pci
tdi_pci
tdo_pci
tms_pci
trst#
natatus
RESET-
RESET:
needs to be inverted for use with the phase/servo generator
IRQB-
MI1
WDTC
WDO
WAIT1-
odfit
BSA00
BSA01
BSA00
BWR_A-
BRD_A-
BUSYL-
CEL-
OEL-
BUSY-
BUSYR-
HREQ-
nconfig
msel0
msel1
U20
CYYC025-TQFP (TQFP100)
OPT 2
U22
epc1
RESET
RESET-
clock/phaseb
RP11
10KSIP10C
SCLK
DCLK
PHASE
SERVO
JUMPER3
"AGND" PLANE
"DGND" PLANE
RAISE RESISTOR OFF BOARD
LM7805ST
(TO-220)
MBRS140T3
U23
U24
NC7SZ14M5
led_rst
WDO
D9 LED GRN PWR
D9A LED GRN PWR
D10 LED RED RO
D10A LED RED RO
Delta Tau Data Systems, Inc.
mini - PMAC1, PCI AND DUAL PORT RAM
Size: D
Document Number: 603712-320
Rev: -
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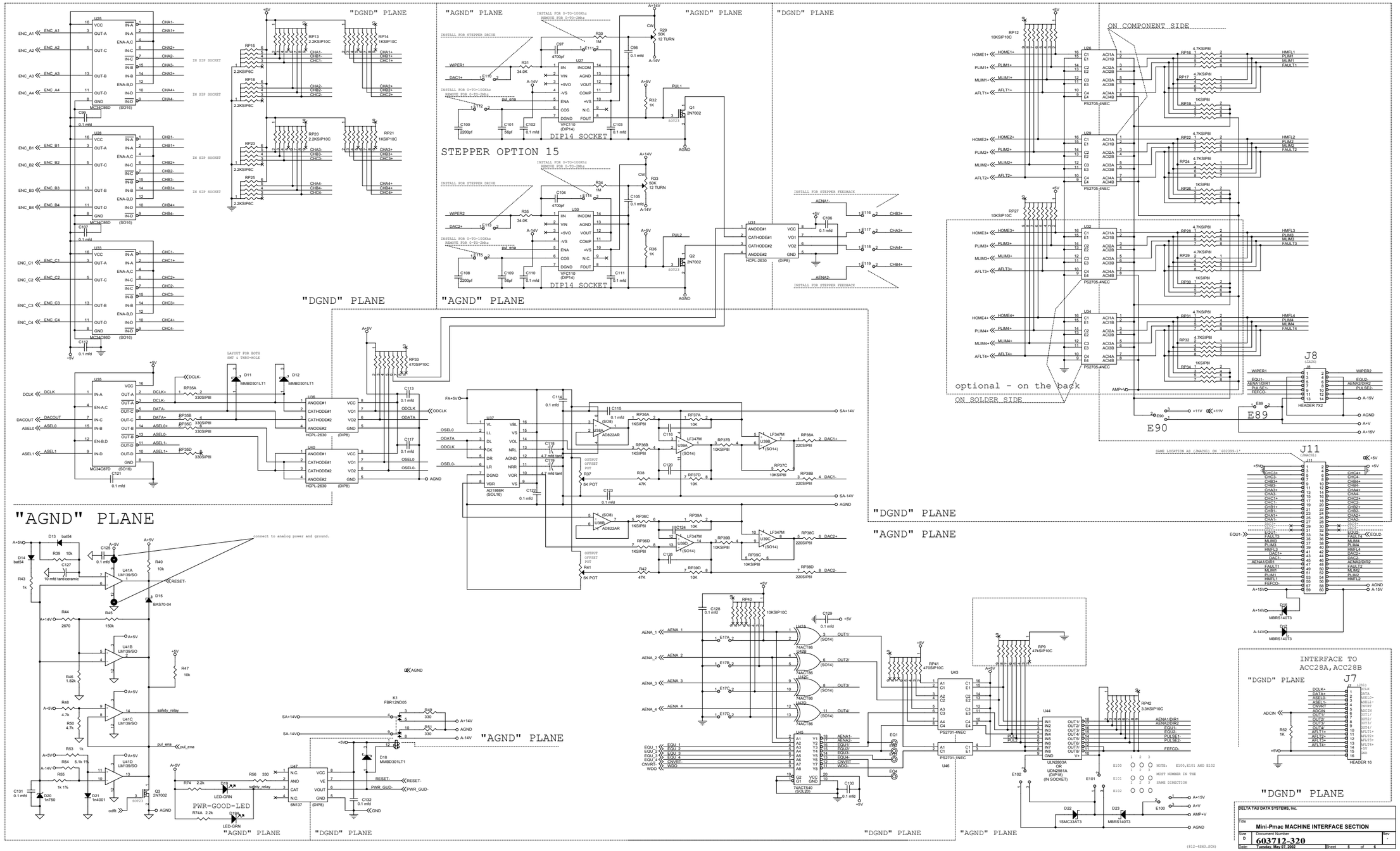
"DGND" PLANE
"AGND" PLANE
STEPPER OPTION 15
DIP14 SOCKET
ON COMPONENT SIDE
optional - on the back
ON SOLDER SIDE
INTERFACE TO ACC28A,ACC28B
PWR-GOOD-LED
DELTA TAU DATA SYSTEMS, Inc.
Mini-Pmac MACHINE INTERFACE SECTION
603712-320
Tuesday, May 07, 2002