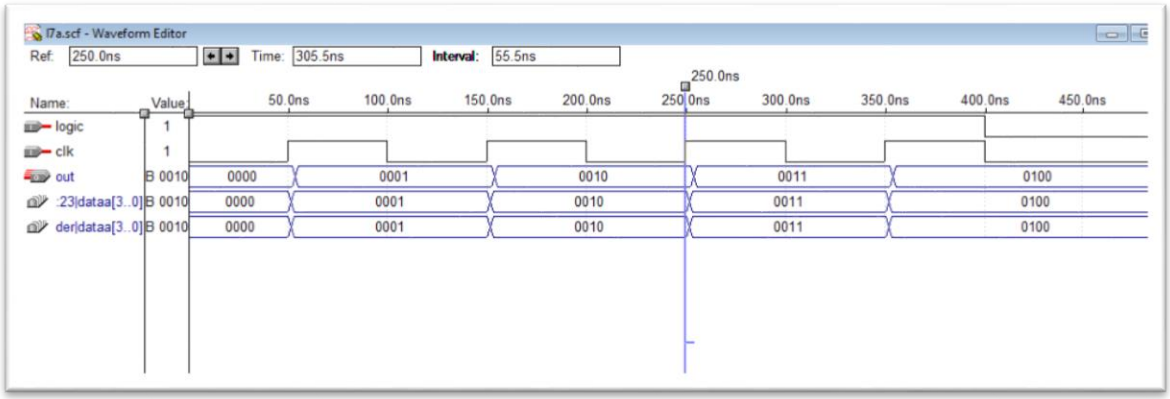
Week 7

1)

Part-A)

```
// four bit sync up counter
module l7a (clk,logic,out);
        input clk,logic;
        output [3:0]out;
        reg [3:0]out;
        always@(posedge clk)
        begin
                if(!logic)
                        out <= 0;
                else
                        out <= out + 1;
        end
endmodule
```



Part-B)

```
// three bit sync clocked up/down counter
module l7b (clock,updown,reset,c);
input clock,reset,updown;
output [2:0]c;
reg [2:0]c;
always@(posedge clock)
begin
        if(!reset)
                c <= 0;
        else
                begin
                        if(updown)
                                c <= c + 1;
                        else
                                c <= c - 1;
                end
end
endmodule
```