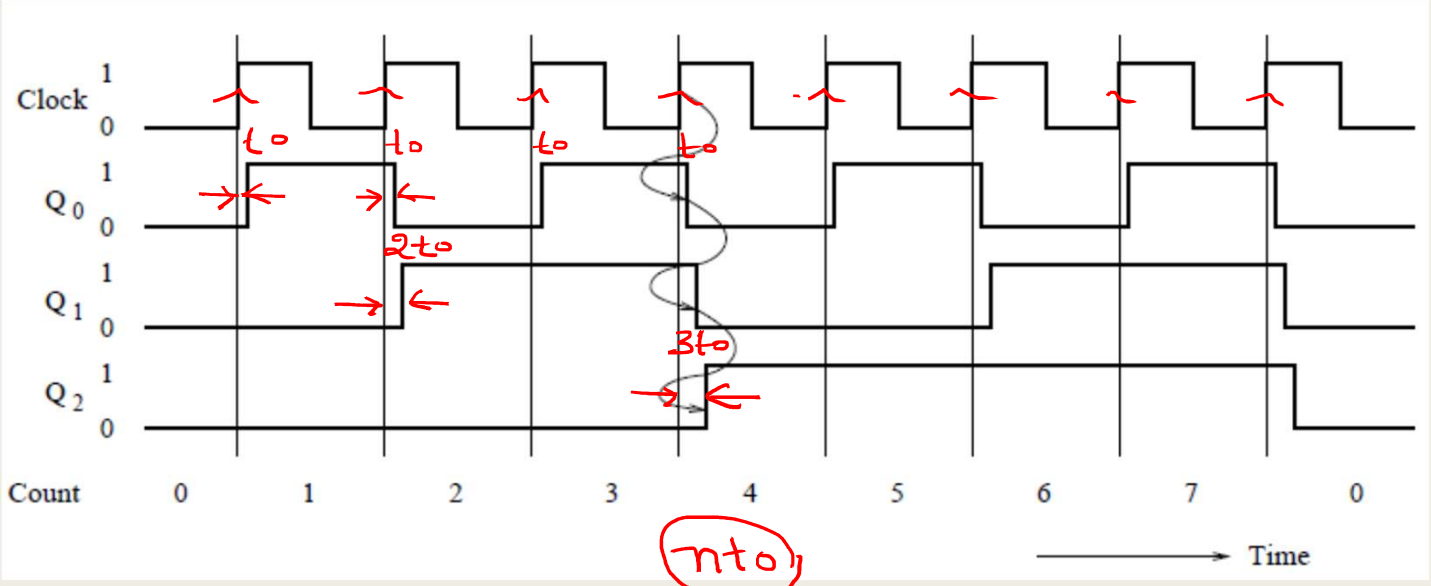
Synchronous counters

- Limitations of asynchronous counters
- Synchronous counter design
- Synchronous counter ICs

Limitation of asynchronous counters

RIPPLE ~~COUNTER~~ counters



Limitations: 1. Not suitable for high frequency applications

2. Not suitable for higher mod counters

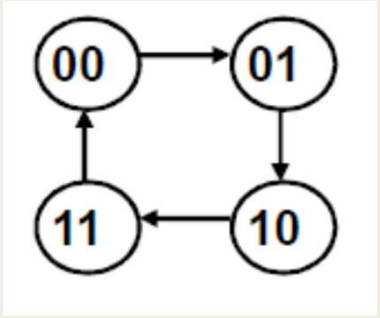
Synchronous counter design

- All the flip flops are clocked simultaneously using same clock.
- Suitable for high frequency applications
- Designed using sequential circuit design process which can be used for any synchronous circuit designs

1. Design 2-bit synchronous binary UP counter using T ffs

- Counter states: 00 → 01 →10 →11

State diagram

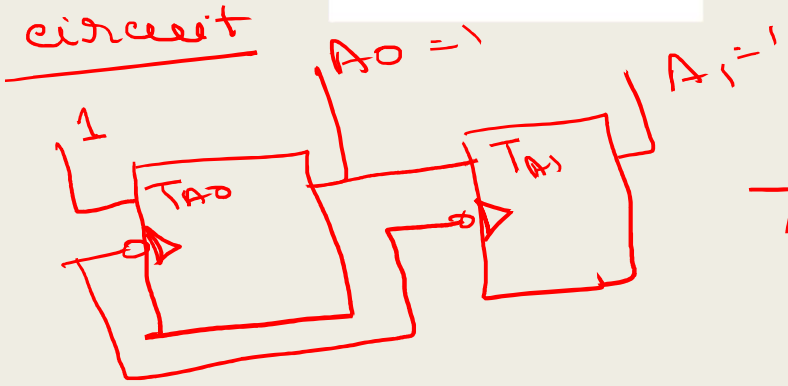


State table

Present state		Next state		Flip-flop inputs	
A_1	A_0	A_1^+	A_0^+	TA_1	TA_0
0	0	0	1	0	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	0	0	1	1

$TA_1 = A_0$

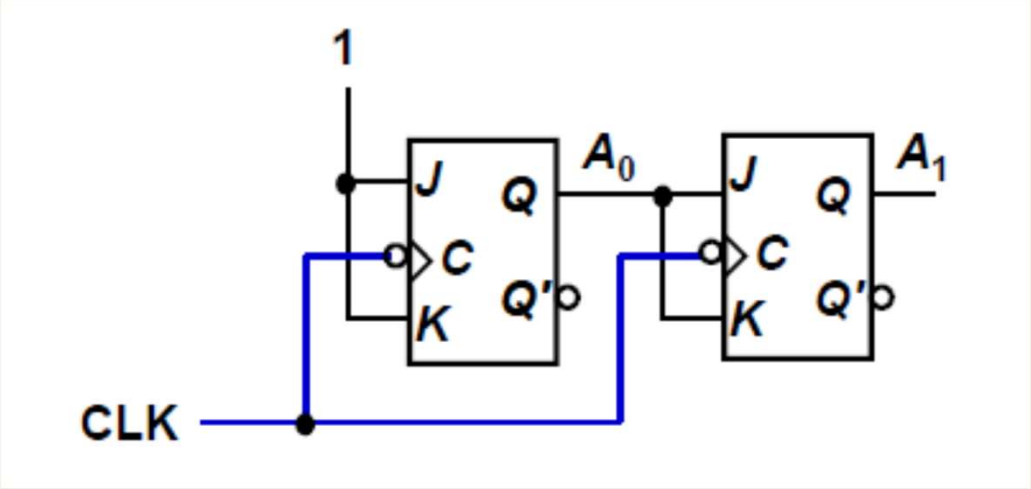
$TA_0 = 1$

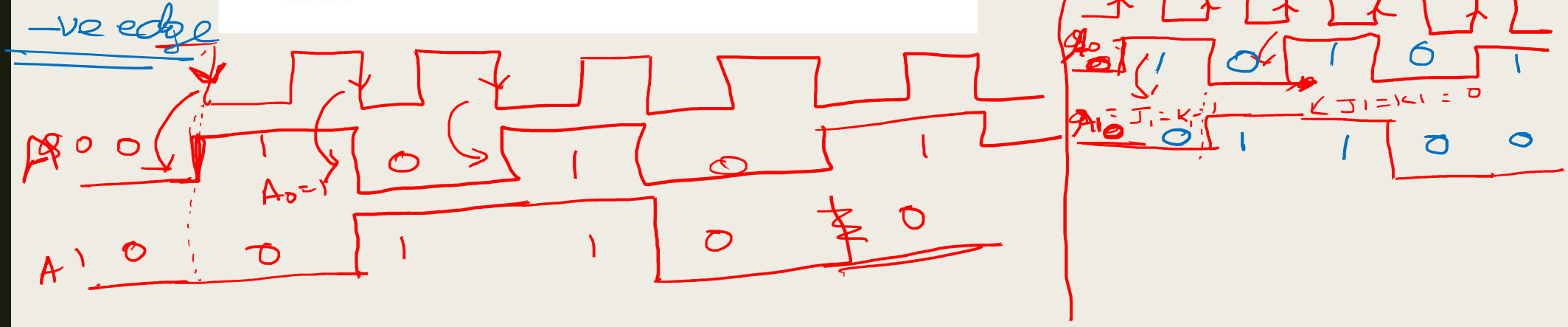


$TA_1(A_1, A_0) = A_0$

$TA_0 = 1$

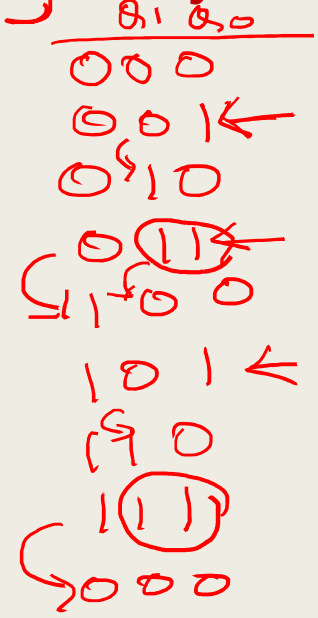
2-bit synchronous binary UP counter using JK ffs : circuit diagram





2. Design 2-bit synchronous binary UP counter using JK ffs

2-bit synchronous binary UP counter using JK ffs contd..



$J_0 = K_0 = 1$

$J_1 = K_1 = Q_0$

$J_2 = K_2 = Q_1 Q_0$

Solve & verify

3. Design 3-bit synchronous binary UP counter (MOD 8)using SR ffs

000 → 001 → 010 → 011 → 100 → 101 → 110 → 111

Present State $Q_2\ Q_1\ Q_0$	Next State $Q_2^+\ Q_1^+\ Q_0^+$	$Q_2 \times Q_2^+$ $S_2\ R_2$	$Q_1 \times Q_1^+$ $S_1\ R_1$	$S_0\ R_0$
0 0 0	0 0 1	0 ϕ	0 ϕ	1 0
0 0 1	0 1 0	0 ϕ	1 0	0 1
0 1 0	0 1 1	0 ϕ	ϕ 0	1 0
0 1 1	1 0 0	1 0	0 1	0 1
1 0 0	1 0 1	ϕ 0	0 ϕ	1 0
1 0 1	1 1 0	ϕ 0	1 0	0 1
1 1 0	1 1 1	ϕ 0	ϕ 0	1 0
1 1 1	0 0 0	0 1	0 1	0 1

$S_2 = \overline{Q_2} Q_1 Q_0$

$R_2 = Q_2 Q_1 Q_0$

$S_1 = \overline{Q_1} Q_0$

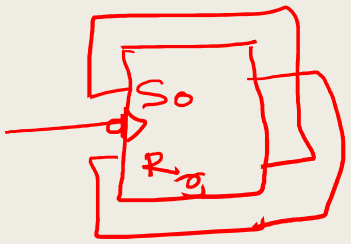
$R_1 = Q_1 Q_0$

$S_0 = \overline{Q_0}$

$R_0 = Q_0$

$S_1 = Q_0$

Q_2 \ $Q_1 Q_0$	01	11	10	00
0	1	0	ϕ	
0	1	0	ϕ	



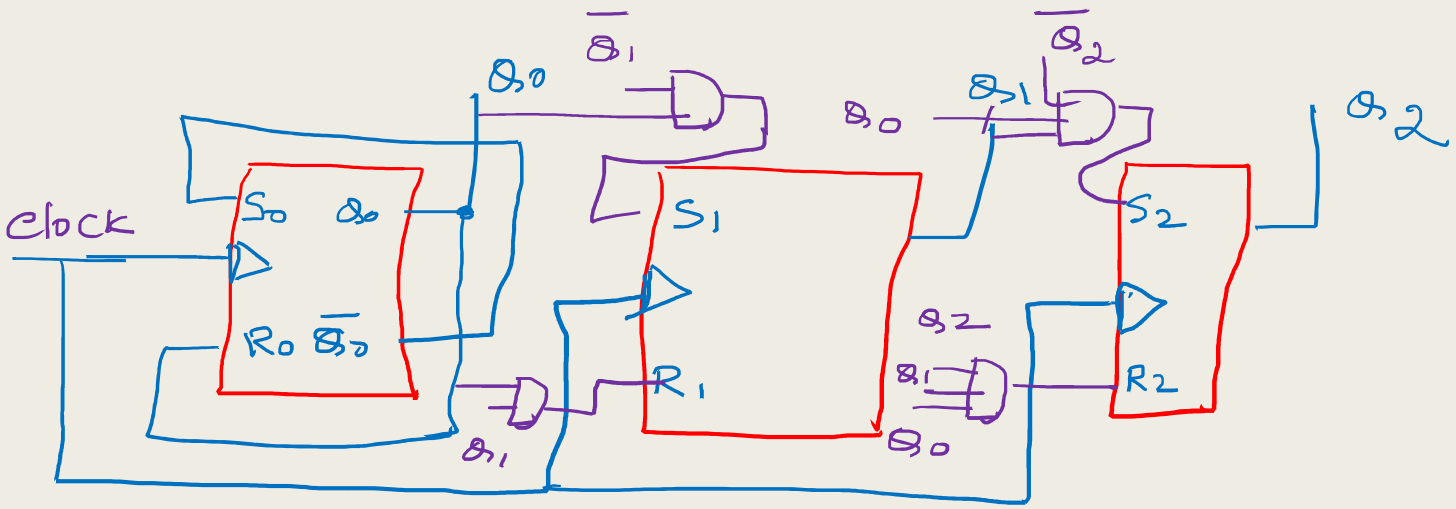
?

$Q_2 Q_2^+$	S	R
0 0	0	ϕ
0 1	1	0
1 0	0	1
ϕ ϕ	ϕ	0

S=0 R=1 / S=0 R=0 → Reset / No change

S=1 R=0 / S=0 R=0 → Set / No change

3-bit synchronous binary UP counter (MOD 8)using SR ffs



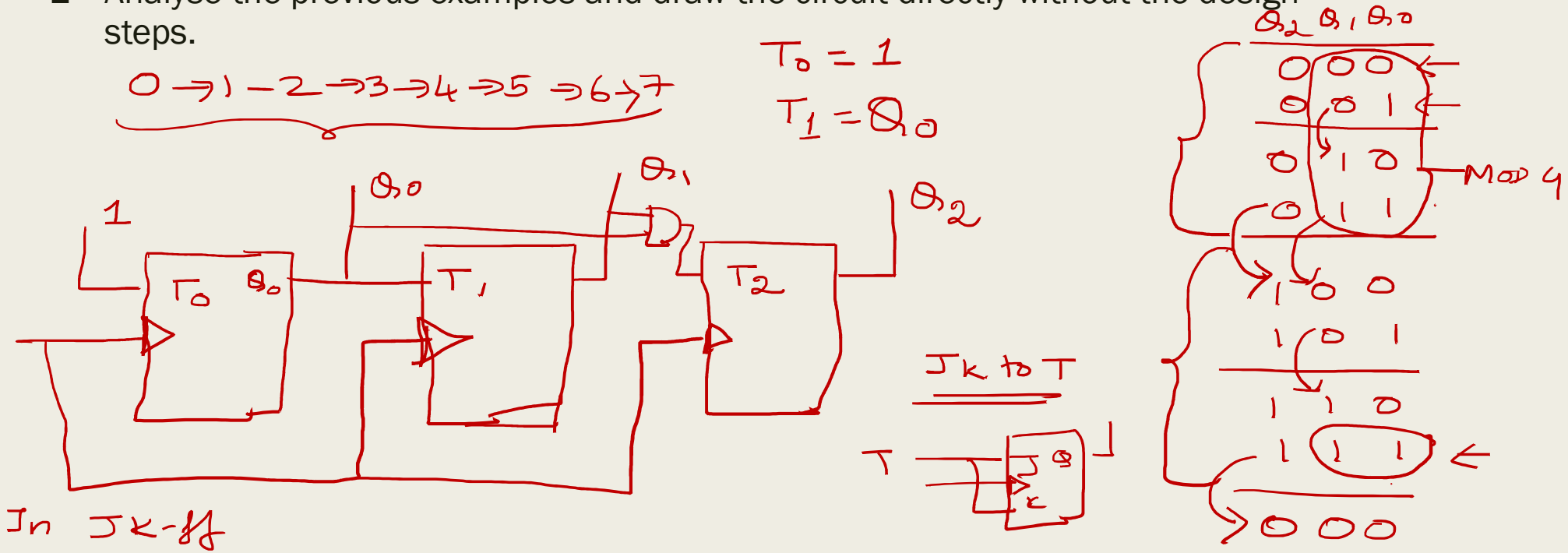
$S_0 = \overline{Q_0}$ $R_0 = Q_0$

$S_1 = \overline{Q_1} Q_0$ $R_1 = Q_1 Q_0$

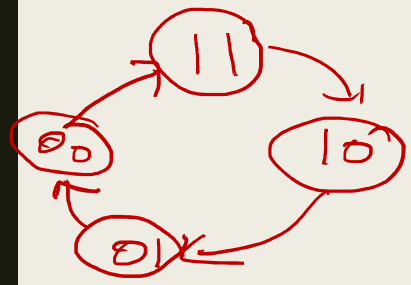
$S_2 = \overline{Q_2} Q_1 Q_0$ $R_2 = Q_2 Q_1 Q_0$

4. Draw the circuit of 3-bit synchronous binary up counter (MOD 8) using T ffs

- Analyse the previous examples and draw the circuit directly without the design steps.



5. Design 2-bit synchronous binary down counter (MOD 4) using D ffs



State diagram

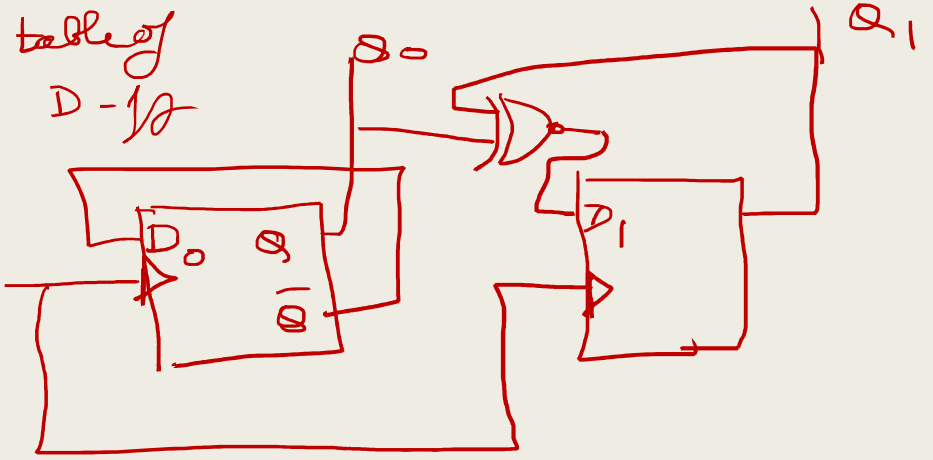
$D_1(Q_1, Q_0) = \overline{(Q_1 + Q_0)}$

$D_0(Q_1, Q_0) = \overline{Q_0}$

$Q_1Q_0 = 10 \Rightarrow 01$

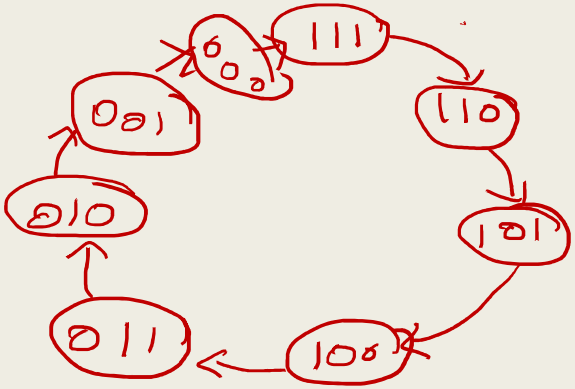
State table

Present state $Q_1\ Q_0$	Next state $Q_1^+\ Q_0^+$	Excitation table of D-ff $D_1\ D_0$
0 0	1 1	1 1
0 1	0 0	0 0
1 0	0 1	0 1
1 1	1 0	1 0



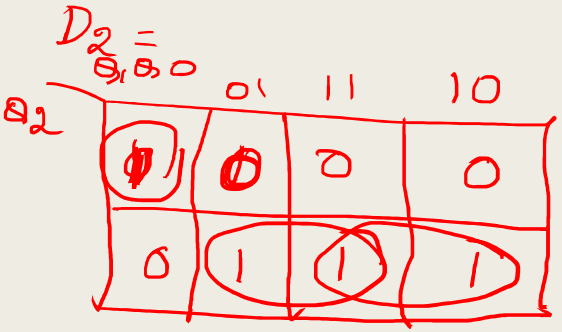
2-bit synchronous binary down counter (MOD 4) using D ffs

6. Design 3-bit synchronous binary down counter (MOD 8) using D ffs



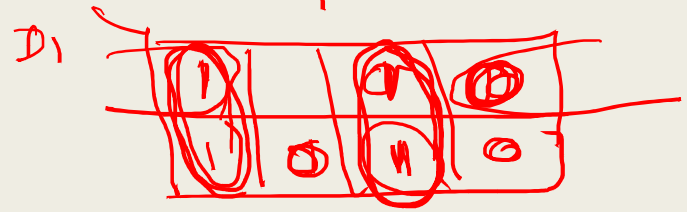
Present state			Next state			D_2	D_1	D_0
Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+			
0	0	0	1	1	1	1	1	1
0	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	1
0	1	1	0	1	0	0	1	0
1	0	0	0	1	1	0	1	1
1	0	1	1	0	0	1	0	0
1	1	0	1	0	1	1	0	1
1	1	1	1	1	0	1	1	0

$D_2 =$



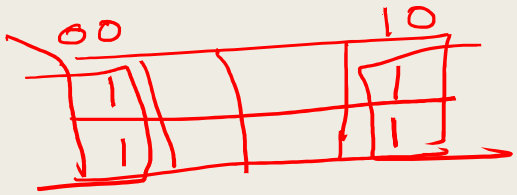
$= \bar{Q}_2\bar{Q}_1\bar{Q}_0 + Q_2Q_0 + Q_2Q_1$

D_1



$D_1 = \bar{Q}_1\bar{Q}_0 + Q_1Q_0$

$= Q_1 \odot Q_0$



$D_0 = \overline{Q_0}$

7. Design decade (BCD) synchronous up counter (MOD 10)using T ffs → 4 ffs

- (0→1→2→3→4→5→6→7→8→9→0)

16 states → 10 states (1001)

10 to 15 → Not required, unused

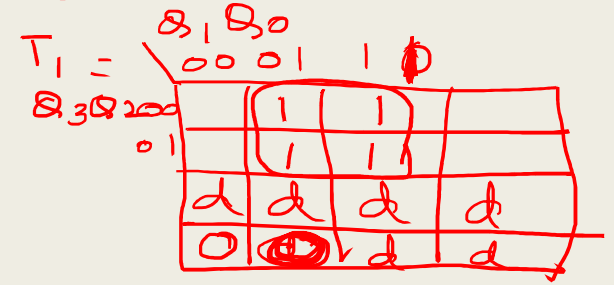
Decade (BCD) synchronous up counter contd..

Present state $Q_3\ Q_2\ Q_1\ Q_0$	Next-state $Q_3^+\ Q_2^+\ Q_1^+\ Q_0^+$	T_3	T_2	T_1	T_0
0 0 0 0	0 0 0 1	0	0	0	1
0 0 0 1	0 0 1 0	0	0	1	1
0 0 1 0	0 0 1 1	0	0	0	1
0 0 1 1	0 1 0 0	0	1	1	1
0 1 0 0	0 1 0 1	0	0	0	1
0 1 0 1	0 1 1 0	0	0	1	1
0 1 1 0	0 1 1 1	0	0	0	1
0 1 1 1	1 0 0 0	1	1	1	1
1 0 0 0	1 0 0 1	0	0	0	1
1 0 0 1	0 0 0 0	1	0	0	1
1 0 1 0	x x x x	x	x	x	x
1 0 1 1	x x x x	x	x	x	x
1 1 0 0	x x x x	x	x	x	x
1 1 0 1	x x x x	x	x	x	x
1 1 1 0	x x x x	x	x	x	x
1 1 1 1	x x x x	x	x	x	x

Q_t	Q_t^+	T
0	0	0
0	1	1
1	0	1
1	1	0

$T_0 = 1$

T_1 =



$T_1 = \sum m(1,3,5,7) + d(10,11,12,13,14,15)$

$= \bar{Q}_3 Q_0$

$T_2 = Q_1 Q_0 \Rightarrow (3, 7, \underbrace{11, 15}_{d})$

$T_3 = \underbrace{Q_0 Q_1 Q_2}_{(7,15)} + \underbrace{Q_0 \bar{Q}_2 Q_3}_{(9,13) \text{ or } (9,11)}$

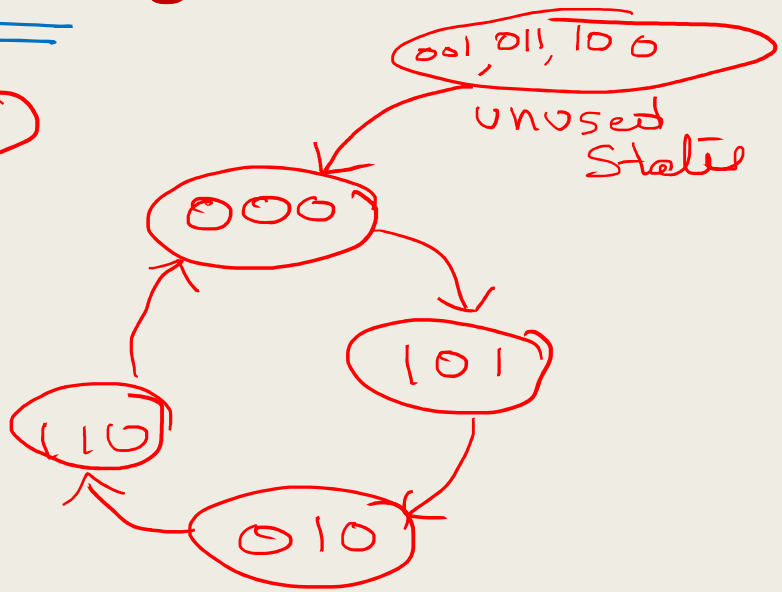
1001

1101

Design 3-bit synchronous counter to count according to the given sequence using D ffs. All the undefined (unused) states should go to state 0.---Self correcting counters.

- 0→5→2→6→7→0

(1)



(2)

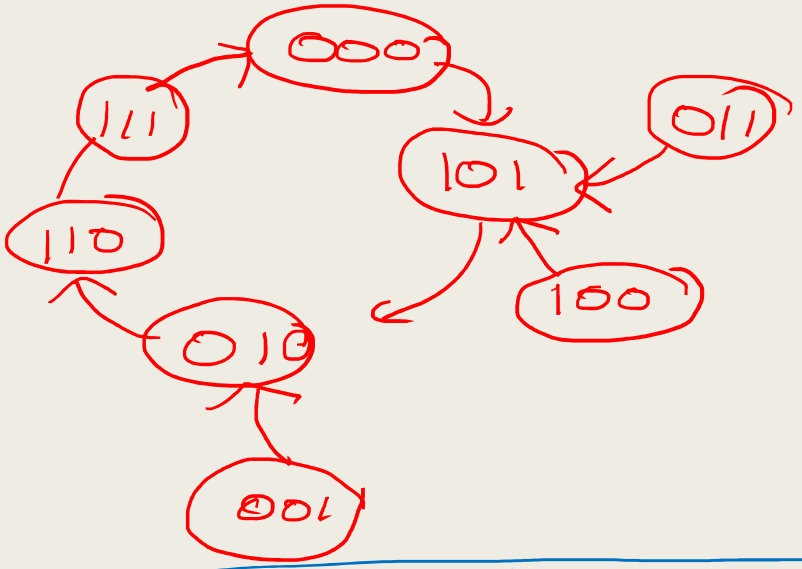
Present States $Q_2Q_1Q_0$	Next States $Q_2^+Q_1^+Q_0^+$	$D_2D_1D_0$
0 0 0 →	1 0 1	1 0 1
0 0 1 →	0 0 0	0 0 0
0 1 0 →	1 1 0	1 1 0
0 1 1 →	0 0 0	0 0 0
1 0 0 —	0 0 0	0 0 0
1 0 1 —	0 0 0	0 1 0
1 1 0 →	1 1 1	1 1 1
1 1 1 →	0 0 0	0 0 0

(3) Simplified expressions for $D_2D_1D_0$

(4) Circuit diagram

Design 3-bit synchronous counter to count according to the given sequence using D ffs. All the undefined states should go to next valid/defined state.

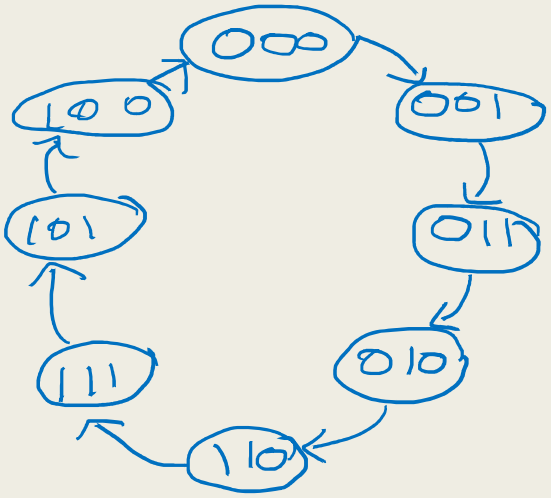
- 0→5→2→6→7→0



Complete simplification & Circuit

Present state $Q_2\ Q_1\ Q_0$	Next state $Q_2^+\ Q_1^+\ Q_0^+$	$D_2\ D_1\ D_0$
0 0 0	1 0 1	1 0 1
0 0 1	0 1 0	0 1 0
0 1 0	1 1 0	1 1 0
0 1 1	1 0 1	1 0 1
1 0 0	1 0 1	1 0 1
1 0 1	0 1 0	0 1 0
1 1 0	1 1 1	1 1 1
1 1 1	0 0 0	0 0 0

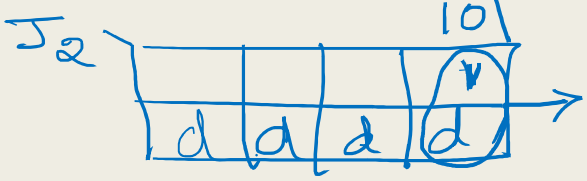
8. Design 3-bit gray code counter using JK ffs



Present st. $Q_2Q_1Q_0$	Next state $Q_2^+Q_1^+Q_0^+$	J_2 K_2	J_1 K_1	J_0 K_0
000	001	0 d	0 d	1 d
001	011	0 d	1 d	d 0
011	010	1 d	d 0	0 d
010	110	0 d	d 0	d 1
110	111	d 1	0 d	0 d
111	101	d 0	d 1	d 1
101	100	d 0	d 1	d 0
100	000			

Q	Q_+	J	K
0	0	0	d
0	1	1	d
1	0	d	1
1	1	d	0

Set/toggle



$J_2 = Q_1\bar{Q}_0$ $K_2 = \bar{Q}_1\bar{Q}_0 \rightarrow Q_2 \odot Q_1$

$J_1 = \bar{Q}_2 Q_0$ (1, d 3)

$K_1 = Q_2 Q_0$ (5, 7)

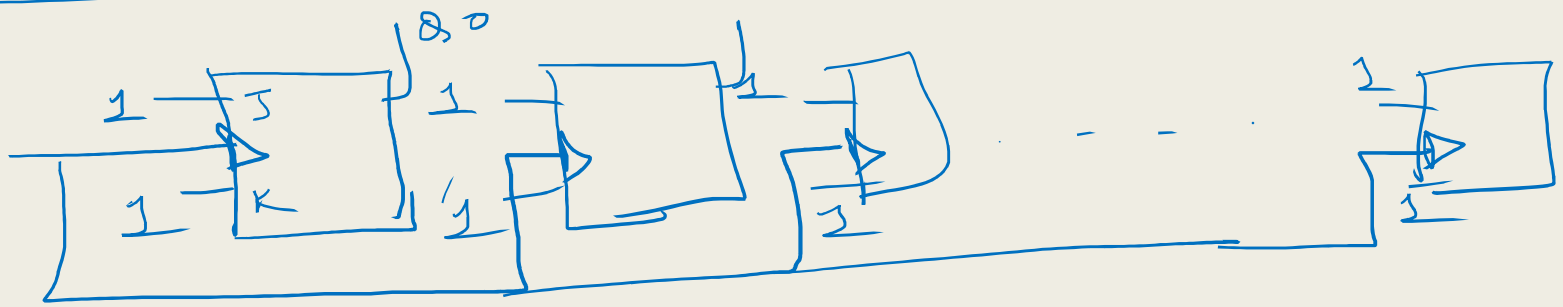
$J_0 = \bar{Q}_2\bar{Q}_1 + Q_2Q_1$

$K_0 =$

$Q_1 \oplus Q_2$ = ___ + ___

~~3-bit gray code counter using JK ffs~~

Ques of prev class

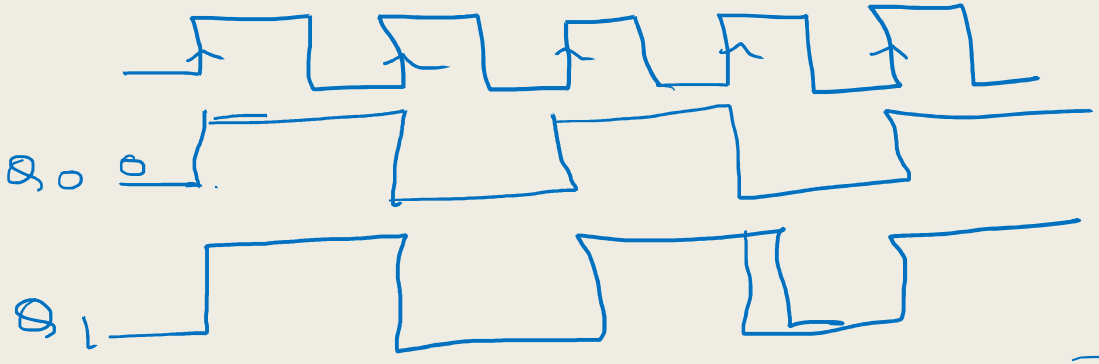


→ 00 - - - 0

→ 111 - - - 1

000 - - -

111 - - -



2 Q_2 MOD 12 ⇒ MOD M x MOD N

0 — 0000
1 0001
2 0010
3 0011
4 0100
0101

6
1000 — 8
1001 — 9
1010 — 10
1011 — 11
1100 — 12
1101 — 13

2

6 7

14, 15