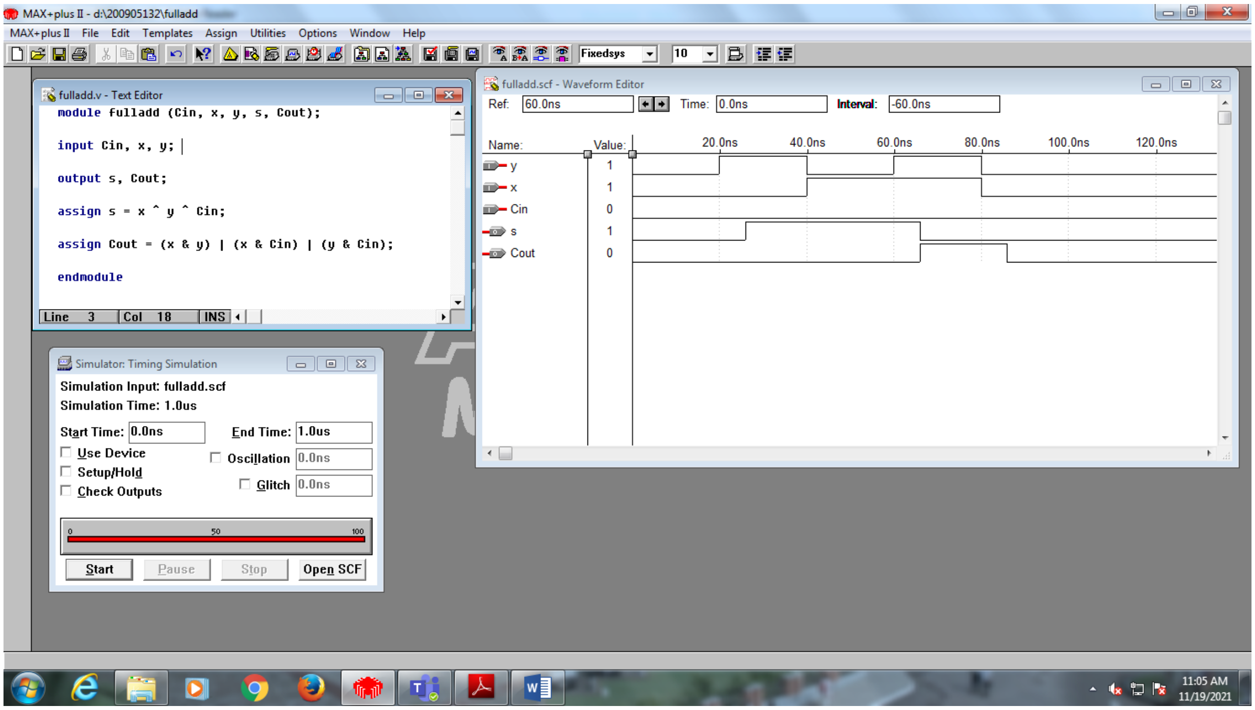
DSD LAB 2

Write behavioral Verilog code to implement the following and simulate

1. Full adder

```
module fulladd (Cin, x, y, s, Cout);
input Cin, x, y;
output s, Cout;
assign s = x ^ y ^ Cin;
assign Cout = (x & y) | (x & Cin) | (y & Cin);
endmodule
```



```
module fulladd (Cin, x, y, s, Cout);

input Cin, x, y;

output s, Cout;

assign s = x ^ y ^ Cin;

assign Cout = (x & y) | (x & Cin) | (y & Cin);

endmodule
```

Ref: 60.0ns Time: 0.0ns Interval: -60.0ns

Name:	Value:
y	1
x	1
Cin	0
s	1
Cout	0

Simulation Input: fulladd.scf

Simulation Time: 1.0us

Start Time: 0.0ns End Time: 1.0us

☐ Use Device ☐ Oscillation 0.0ns

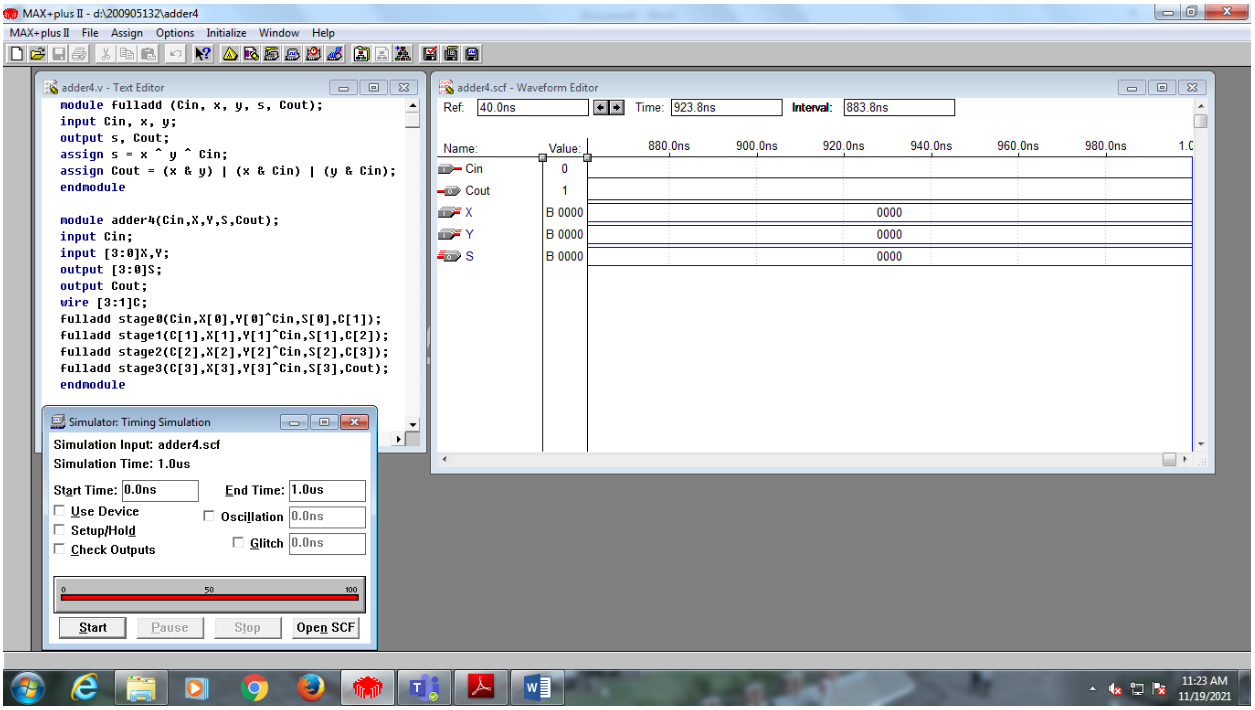
☐ Setup/Hold ☐ Glitch 0.0ns

☐ Check Outputs

2. Four-bit adder/ subtractor

```
module fulladd (Cin, x, y, s, Cout);
input Cin, x, y;
output s, Cout;
assign s = x ∧ y ∧ Cin;
assign Cout = (x & y) | (x & Cin) | (y & Cin);
endmodule
```

```
module adder4(Cin,X,Y,S,Cout);

input Cin;

input [3:0]X,Y;

output [3:0]S;

output Cout;

wire [3:1]C;

fulladd stage0(Cin,X[0],Y[0]^Cin,S[0],C[1]);

fulladd stage1(C[1],X[1],Y[1]^Cin,S[1],C[2]);

fulladd stage2(C[2],X[2],Y[2]^Cin,S[2],C[3]);

fulladd stage3(C[3],X[3],Y[3]^Cin,S[3],Cout);

endmodule
```



MAX+plus II - d:\200905132\adder4
MAX+plus II File Assign Options Initialize Window Help
adder4.v - Text Editor

```
module fulladd (Cin, x, y, s, Cout);
input Cin, x, y;
output s, Cout;
assign s = x ^ y ^ Cin;
assign Cout = (x & y) | (x & Cin) | (y & Cin);
endmodule

module adder4(Cin,X,Y,S,Cout);
input Cin;
input [3:0]X,Y;
output [3:0]S;
output Cout;
wire [3:1]C;
fulladd stage0(Cin,X[0],Y[0]^Cin,S[0],C[1]);
fulladd stage1(C[1],X[1],Y[1]^Cin,S[1],C[2]);
fulladd stage2(C[2],X[2],Y[2]^Cin,S[2],C[3]);
fulladd stage3(C[3],X[3],Y[3]^Cin,S[3],Cout);
endmodule
```

Simulator: Timing Simulation

Simulation Input: adder4.scf

Simulation Time: 1.0us

Start Time: 0.0ns End Time: 1.0us

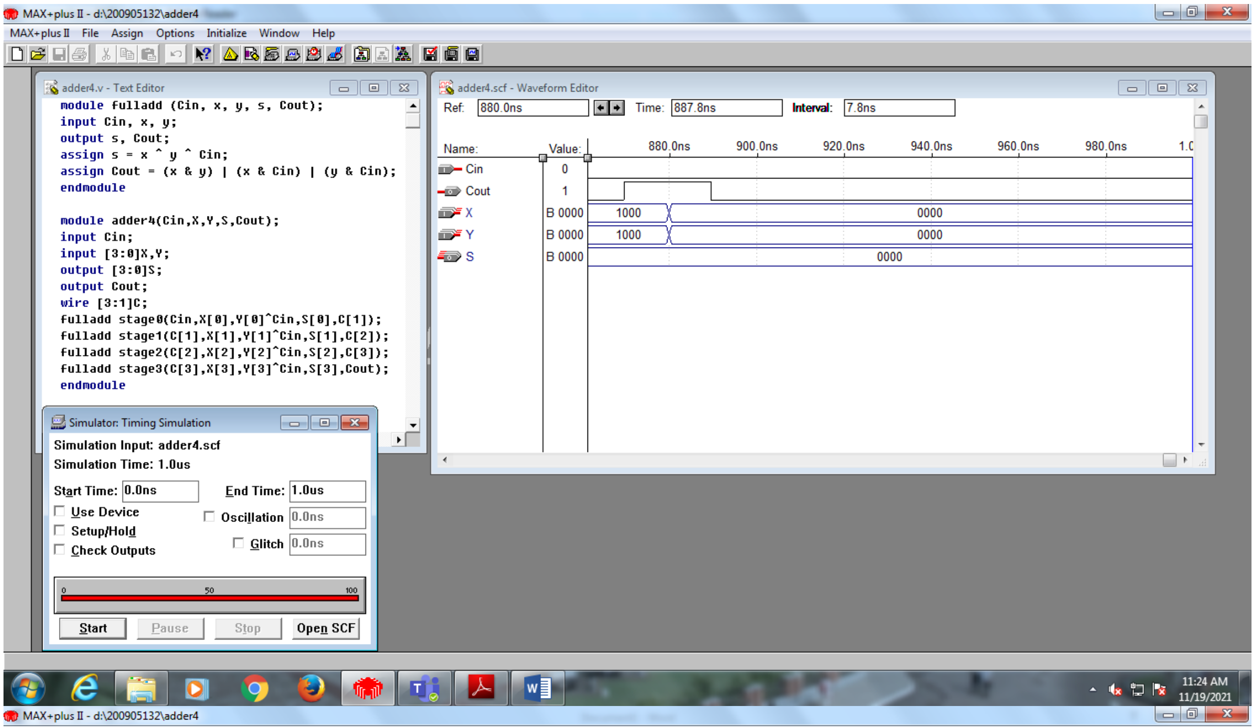
□ Use Device □ Oscillation 0.0ns

□ Setup/Hold □ Glitch 0.0ns

□ Check Outputs

Ref: 40.0ns Time: 923.8ns Interval: 883.8ns

Name:	Value:	
Cin	0	
Cout	1	
X	B 0000	0000
Y	B 0000	0000
S	B 0000	0000


MAX+plus II - d:\200905132\adder4
MAX+plus II File Assign Options Initialize Window Help
adder4.v - Text Editor
adder4.scf - Waveform Editor
Simulator: Timing Simulation
Start
Pause
Stop
Open SCF
11:24 AM
11/19/2021

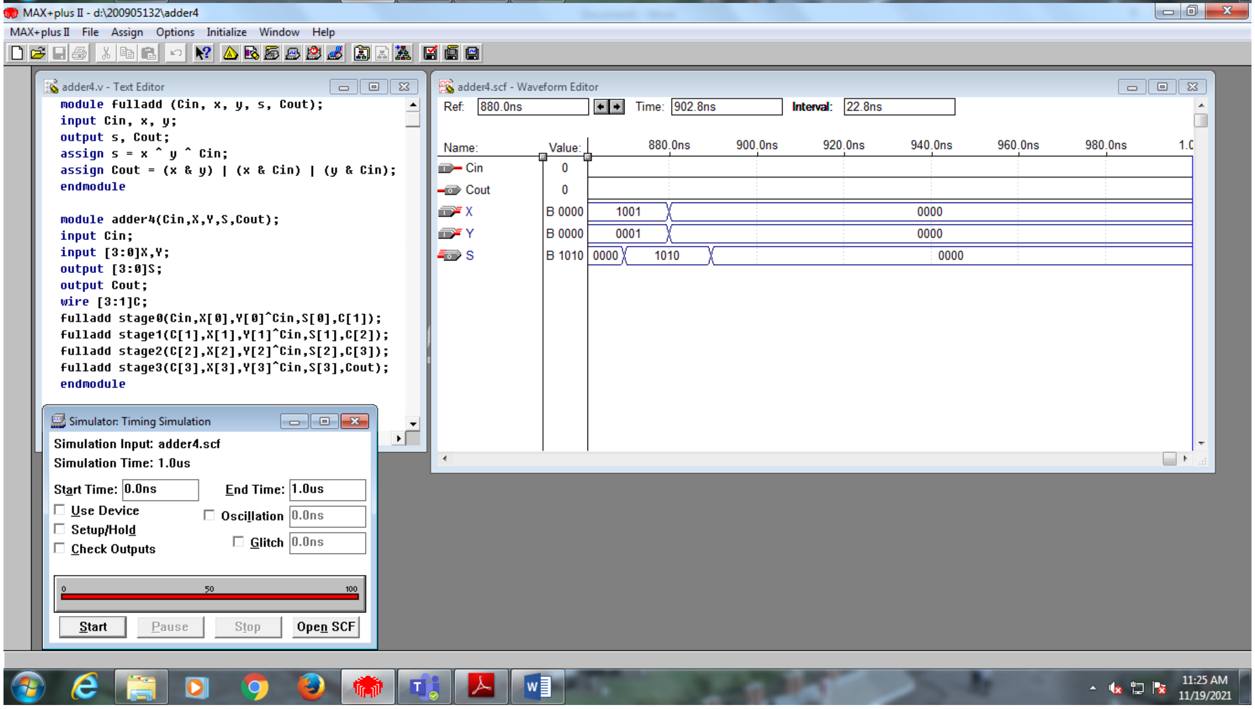
```
module fulladd (Cin, x, y, s, Cout);
input Cin, x, y;
output s, Cout;
assign s = x ^ y ^ Cin;
assign Cout = (x & y) | (x & Cin) | (y & Cin);
endmodule

module adder4(Cin,X,Y,S,Cout);
input Cin;
input [3:0]X,Y;
output [3:0]S;
output Cout;
wire [3:1]C;
fulladd stage0(Cin,X[0],Y[0]^Cin,S[0],C[1]);
fulladd stage1(C[1],X[1],Y[1]^Cin,S[1],C[2]);
fulladd stage2(C[2],X[2],Y[2]^Cin,S[2],C[3]);
fulladd stage3(C[3],X[3],Y[3]^Cin,S[3],Cout);
endmodule
```

Ref: 880.0ns Time: 887.8ns Interval: 7.8ns

Name:	Value:	880.0ns	900.0ns	920.0ns	940.0ns	960.0ns	980.0ns
Cin	0						
Cout	1						
X	B 0000	1000		0000			
Y	B 0000	1000		0000			
S	B 0000			0000			

Simulation Input: adder4.scf
Simulation Time: 1.0us

Start Time: 0.0ns End Time: 1.0us
□ Use Device □ Oscillation 0.0ns
□ Setup/Hold □ Glitch 0.0ns
□ Check Outputs


MAX+plus II - d:\200905132\adder4
MAX+plus II File Assign Options Initialize Window Help
adder4.v - Text Editor
adder4.scf - Waveform Editor
Simulator: Timing Simulation
Start
Pause
Stop
Open SCF
11:25 AM
11/19/2021

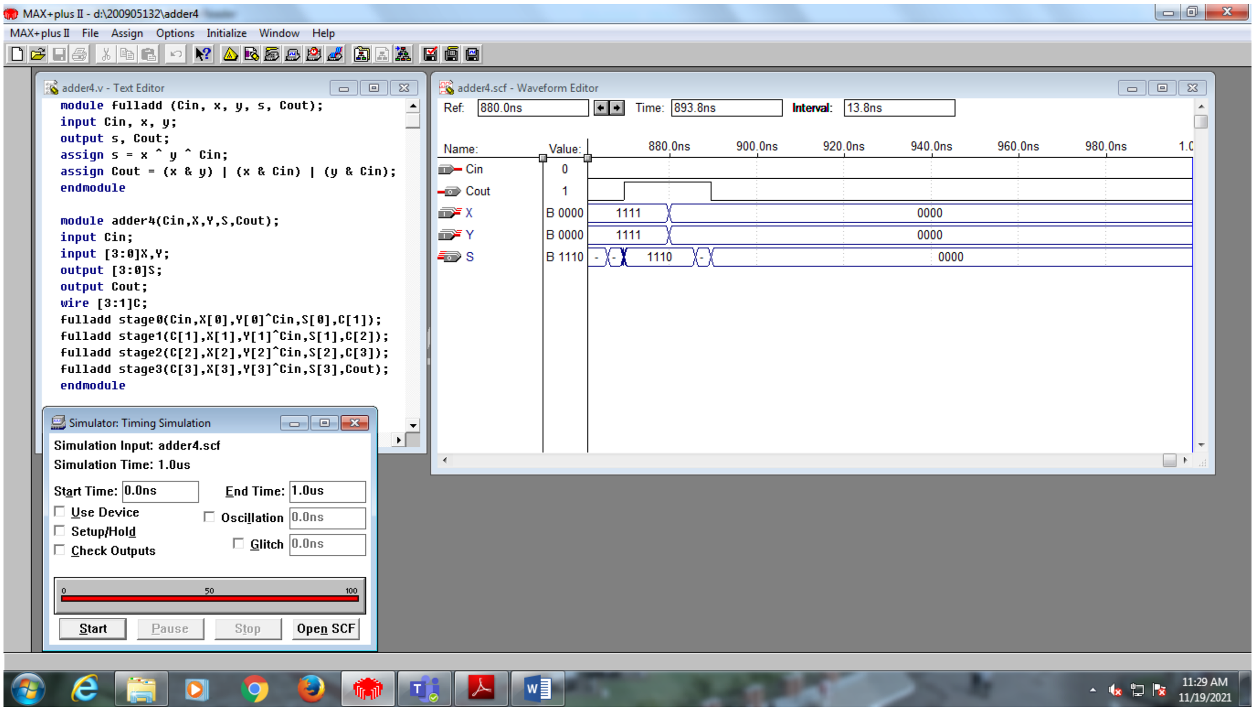
```
module fulladd (Cin, x, y, s, Cout);
input Cin, x, y;
output s, Cout;
assign s = x ^ y ^ Cin;
assign Cout = (x & y) | (x & Cin) | (y & Cin);
endmodule

module adder4(Cin,X,Y,S,Cout);
input Cin;
input [3:0]X,Y;
output [3:0]S;
output Cout;
wire [3:1]C;
fulladd stage0(Cin,X[0],Y[0]^Cin,S[0],C[1]);
fulladd stage1(C[1],X[1],Y[1]^Cin,S[1],C[2]);
fulladd stage2(C[2],X[2],Y[2]^Cin,S[2],C[3]);
fulladd stage3(C[3],X[3],Y[3]^Cin,S[3],Cout);
endmodule
```

Ref: 880.0ns Time: 902.8ns Interval: 22.8ns

Name:	Value:	880.0ns	900.0ns	920.0ns	940.0ns	960.0ns	980.0ns
Cin	0						
Cout	0						
X	B 0000	1001		0000			
Y	B 0000	0001		0000			
S	B 1010	0000 1010		0000			

Simulation Input: adder4.scf
Simulation Time: 1.0us

Start Time: 0.0ns End Time: 1.0us
□ Use Device □ Oscillation 0.0ns
□ Setup/Hold □ Glitch 0.0ns
□ Check Outputs



```
module fulladd (Cin, x, y, s, Cout);
input Cin, x, y;
output s, Cout;
assign s = x ^ y ^ Cin;
assign Cout = (x & y) | (x & Cin) | (y & Cin);
endmodule

module adder4(Cin,X,Y,S,Cout);
input Cin;
input [3:0]X,Y;
output [3:0]S;
output Cout;
wire [3:1]C;
fulladd stage0(Cin,X[0],Y[0]^Cin,S[0],C[1]);
fulladd stage1(C[1],X[1],Y[1]^Cin,S[1],C[2]);
fulladd stage2(C[2],X[2],Y[2]^Cin,S[2],C[3]);
fulladd stage3(C[3],X[3],Y[3]^Cin,S[3],Cout);
endmodule
```

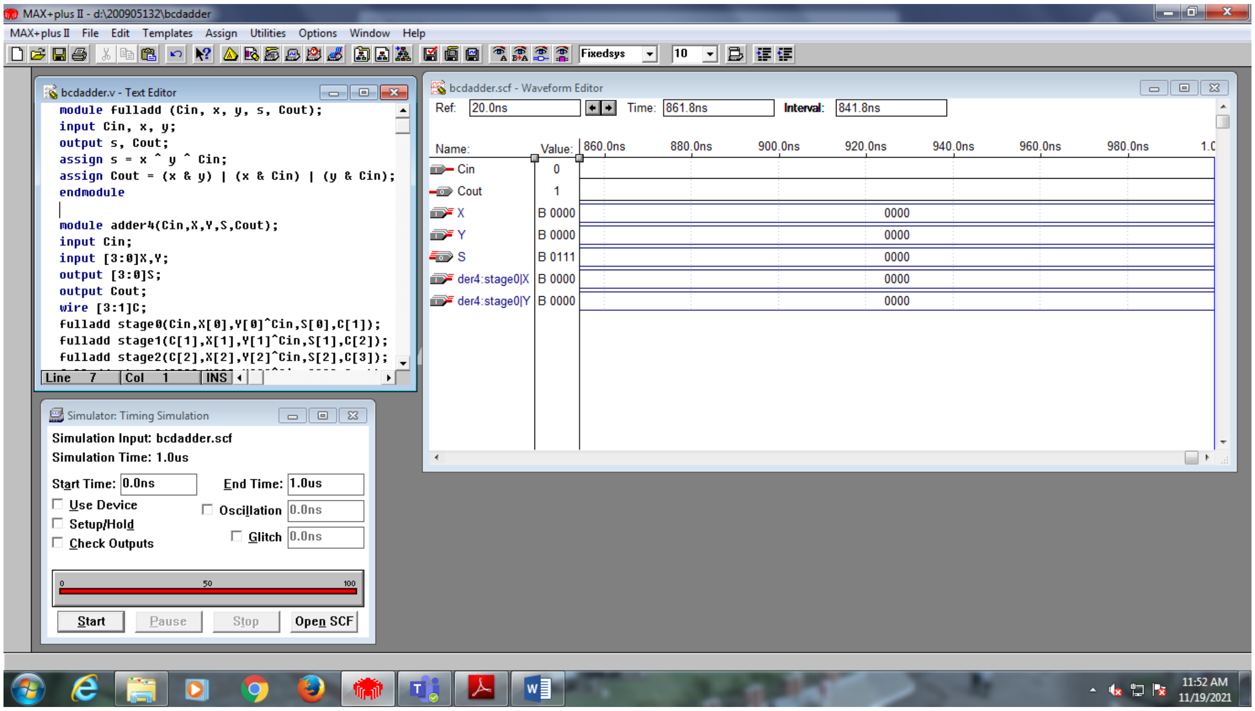
Ref: 880.0ns Time: 893.8ns Interval: 13.8ns

Simulation Input: adder4.scf
Simulation Time: 1.0us

Start Time: 0.0ns End Time: 1.0us
□ Use Device
□ Setup/Hold
□ Check Outputs
□ Oscillation 0.0ns
□ Glitch 0.0ns

3. Single-digit BCD adder using a four-bit adder(s).

```
module fulladd (Cin, x, y, s, Cout);

input Cin, x, y;

output s, Cout;

assign s = x ^ y ^ Cin;

assign Cout = (x & y) | (x & Cin) | (y & Cin);

endmodule


module adder4(Cin,X,Y,S,Cout);

input Cin;

input [3:0]X,Y;

output [3:0]S;
output Cout;
wire [3:1]C;
fulladd stage0(Cin,X[0],Y[0]^Cin,S[0],C[1]);
fulladd stage1(C[1],X[1],Y[1]^Cin,S[1],C[2]);
fulladd stage2(C[2],X[2],Y[2]^Cin,S[2],C[3]);
fulladd stage3(C[3],X[3],Y[3]^Cin,S[3],Cout);
endmodule

module bcdadder(Cin,X,Y,S,Cout);
input Cin;
input [3:0]X,Y;
output [3:0]S;
output Cout;
wire m,a,b,c;
wire [3:0]Z;
adder4 stage0(Cin,X,Y,Z,m);
assign a=Z[3]&Z[1];
assign b=Z[3]&Z[2];
assign Cout=a|b|m;
adder4 stage1(Cin,{1'b0,Cout,Cout,1'b0},Z,S,c);
endmodule
```


MAX+plus II - d:\200905132\bcdadder
MAX+plus II File Edit Templates Assign Utilities Options Window Help
Fixedsys
10
bcdadder.v - Text Editor
bcdadder.scf - Waveform Editor
Simulator: Timing Simulation
Start
Pause
Stop
Open SCF
11:52 AM
11/19/2021

```
module fulladd (Cin, x, y, s, Cout);
input Cin, x, y;
output s, Cout;
assign s = x ^ y ^ Cin;
assign Cout = (x & y) | (x & Cin) | (y & Cin);
endmodule

module adder4(Cin,X,Y,S,Cout);
input Cin;
input [3:0]X,Y;
output [3:0]S;
output Cout;
wire [3:1]C;
fulladd stage0(Cin,X[0],Y[0]^Cin,S[0],C[1]);
fulladd stage1(C[1],X[1],Y[1]^Cin,S[1],C[2]);
fulladd stage2(C[2],X[2],Y[2]^Cin,S[2],C[3]);
```

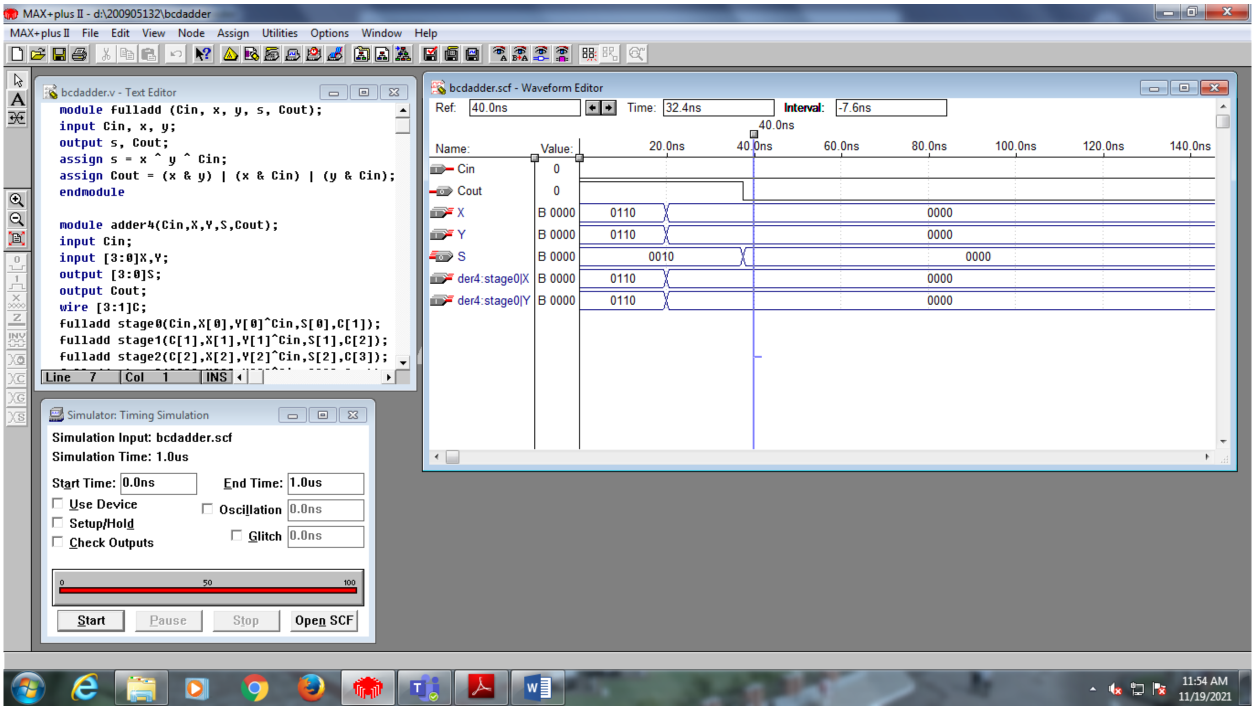
Line 7 Col 1 INS

Simulation Input: bcdadder.scf
Simulation Time: 1.0us

Start Time: 0.0ns   End Time: 1.0us
□ Use Device   □ Oscillation 0.0ns
□ Setup/Hold   □ Glitch 0.0ns
□ Check Outputs

Ref: 20.0ns Time: 861.8ns Interval: 841.8ns

```
Name:            Value:   860.0ns  880.0ns  900.0ns  920.0ns  940.0ns  960.0ns  980.0ns  1.0
Cin              0
Cout             1
X                B 0000                     0000
Y                B 0000                     0000
S                B 0111                     0000
der4:stage0|X    B 0000                     0000
der4:stage0|Y    B 0000                     0000
```


MAX+plus II - d:\200905132\bcdadder
MAX+plus II File Edit View Node Assign Utilities Options Window Help
bcdadder.v - Text Editor
bcdadder.scf - Waveform Editor
Simulator: Timing Simulation
Start
Pause
Stop
Open SCF
11:54 AM
11/19/2021

```
module fulladd (Cin, x, y, s, Cout);
input Cin, x, y;
output s, Cout;
assign s = x ^ y ^ Cin;
assign Cout = (x & y) | (x & Cin) | (y & Cin);
endmodule

module adder4(Cin,X,Y,S,Cout);
input Cin;
input [3:0]X,Y;
output [3:0]S;
output Cout;
wire [3:1]C;
fulladd stage0(Cin,X[0],Y[0]^Cin,S[0],C[1]);
fulladd stage1(C[1],X[1],Y[1]^Cin,S[1],C[2]);
fulladd stage2(C[2],X[2],Y[2]^Cin,S[2],C[3]);
```

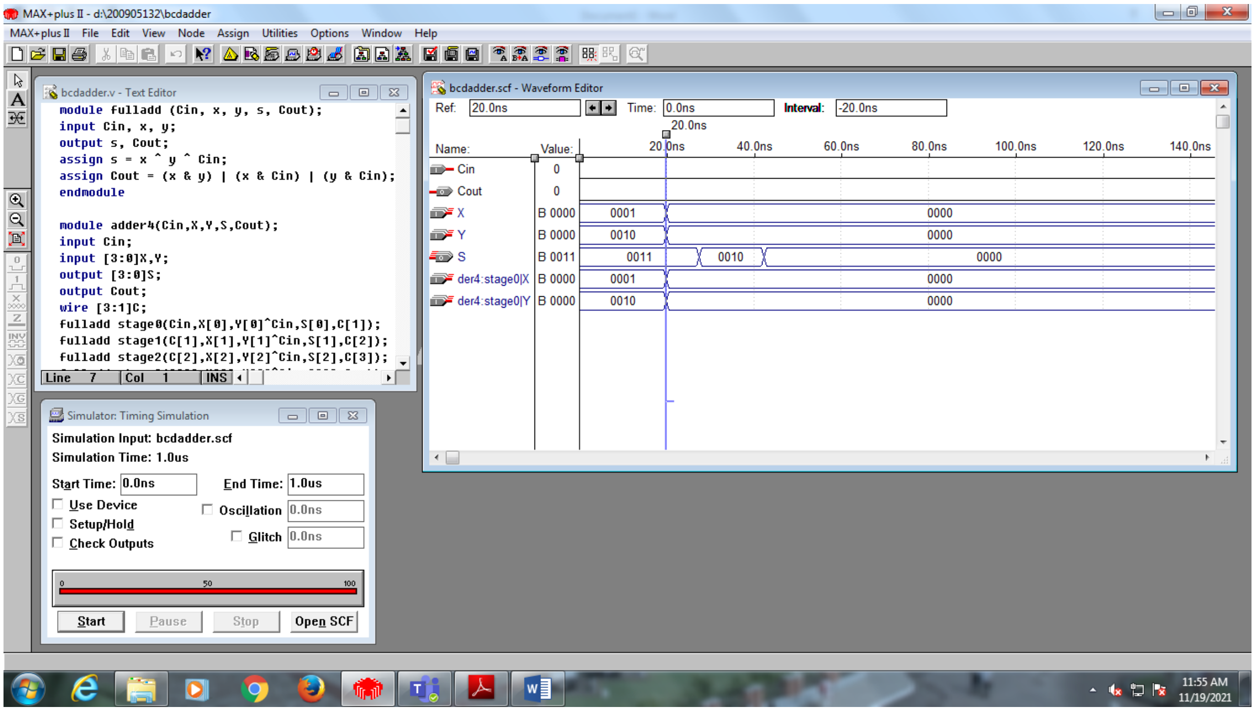
Line 7 Col 1 INS

Simulation Input: bcdadder.scf
Simulation Time: 1.0us

Start Time: 0.0ns   End Time: 1.0us
□ Use Device   □ Oscillation 0.0ns
□ Setup/Hold   □ Glitch 0.0ns
□ Check Outputs

Ref: 40.0ns Time: 32.4ns Interval: -7.6ns

```
                                    40.0ns
Name:            Value:      20.0ns   40.0ns   60.0ns   80.0ns   100.0ns  120.0ns  140.0ns
Cin              0
Cout             0
X                B 0000   0110              0000
Y                B 0000   0110              0000
S                B 0000        0010                  0000
der4:stage0|X    B 0000   0110              0000
der4:stage0|Y    B 0000   0110              0000
```



```
module fulladd (Cin, x, y, s, Cout);
input Cin, x, y;
output s, Cout;
assign s = x ^ y ^ Cin;
assign Cout = (x & y) | (x & Cin) | (y & Cin);
endmodule

module adder4(Cin,X,Y,S,Cout);
input Cin;
input [3:0]X,Y;
output [3:0]S;
output Cout;
wire [3:1]C;
fulladd stage0(Cin,X[0],Y[0]^Cin,S[0],C[1]);
fulladd stage1(C[1],X[1],Y[1]^Cin,S[1],C[2]);
fulladd stage2(C[2],X[2],Y[2]^Cin,S[2],C[3]);
```

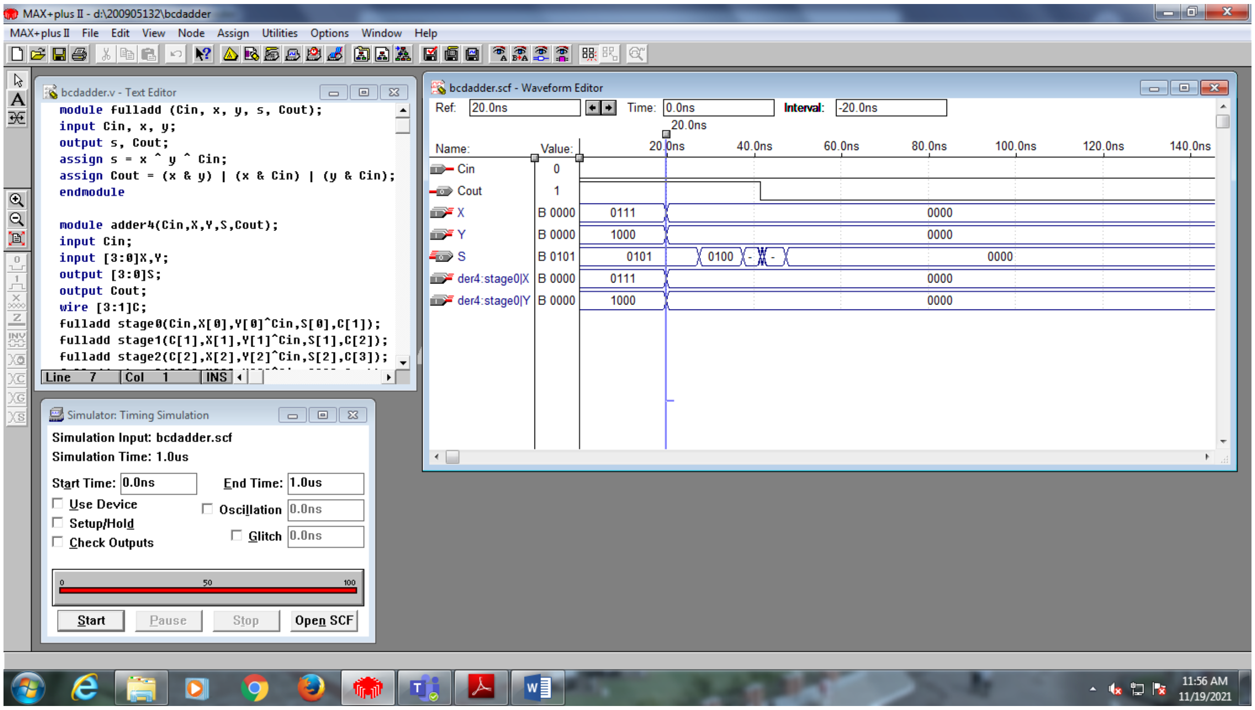
Simulation Input: bcdadder.scf
Simulation Time: 1.0us

Start Time: 0.0ns End Time: 1.0us

□ Use Device □ Oscillation 0.0ns

□ Setup/Hold □ Glitch 0.0ns

□ Check Outputs


MAX+plus II - d:\200905132\bcdadder
MAX+plus II File Edit View Node Assign Utilities Options Window Help
bcdadder.v - Text Editor
Line 7 Col 1 INS
bcdadder.scf - Waveform Editor
Ref: 20.0ns
Time: 0.0ns
Interval: -20.0ns
20.0ns
Name:
Value:
20.0ns
40.0ns
60.0ns
80.0ns
100.0ns
120.0ns
140.0ns
Cin 0
Cout 1
X B 0000 0111 0000
Y B 0000 1000 0000
S B 0101 0101 0100 - - 0000
der4:stage0|X B 0000 0111 0000
der4:stage0|Y B 0000 1000 0000
Simulator: Timing Simulation
0
50
100
Start
Pause
Stop
Open SCF
11:56 AM
11/19/2021

```
module fulladd (Cin, x, y, s, Cout);
input Cin, x, y;
output s, Cout;
assign s = x ^ y ^ Cin;
assign Cout = (x & y) | (x & Cin) | (y & Cin);
endmodule

module adder4(Cin,X,Y,S,Cout);
input Cin;
input [3:0]X,Y;
output [3:0]S;
output Cout;
wire [3:1]C;
fulladd stage0(Cin,X[0],Y[0]^Cin,S[0],C[1]);
fulladd stage1(C[1],X[1],Y[1]^Cin,S[1],C[2]);
fulladd stage2(C[2],X[2],Y[2]^Cin,S[2],C[3]);
```

Simulation Input: bcdadder.scf
Simulation Time: 1.0us

Start Time: 0.0ns End Time: 1.0us

□ Use Device □ Oscillation 0.0ns

□ Setup/Hold □ Glitch 0.0ns

□ Check Outputs