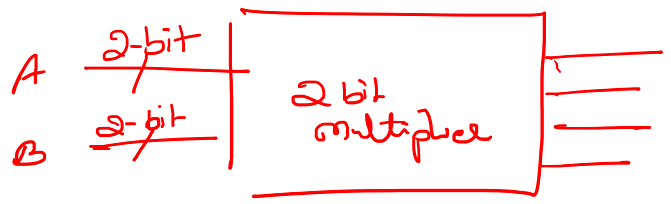
Multipliers and Magnitude comparators

Binary Multiplier



- 2 bit × 2 bit binary multiplier using adders and external gates.

$$B_1B_0 \times A_1A_0$$

		A_0B_1	A_0B_0
	A_1B_1	A_1B_0	
P_3	P_2	P_1	P_0

C_2, $C_1 + A_1B_1$, (MSB), (LSB), C_1, S_1

$P_3 = C_2$

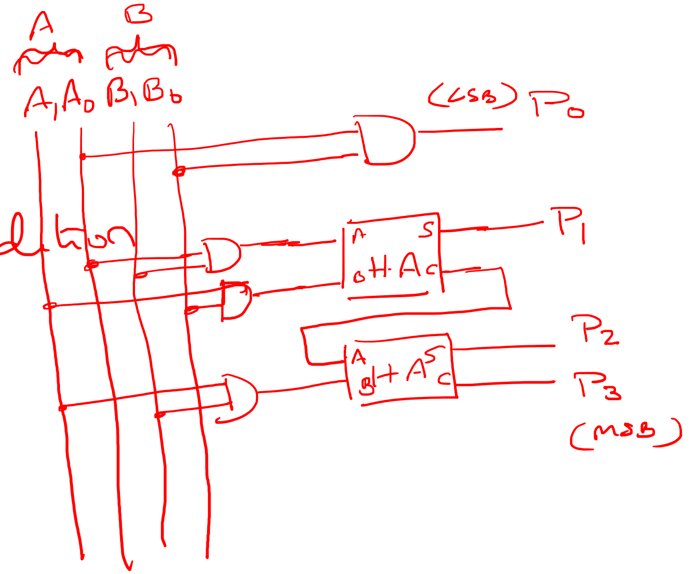
$P_2 = C_1 + A_1B_1$ Half Adder

$A_0B_1 + A_1B_0$ Half Adder → Arithmatic addition

Ex: $b_1 b_0 \times a_1 a_0$: 10×11

$b_1 \times a_0$: 1×1, $b_0 \times a_0$: 0×1

$b_1 \times a_1$: 1×1, $b_0 \times a_1$: 0×1



Bit by Bit multiplication

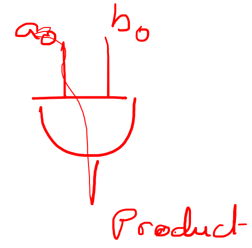
logical

a_0	b_0	Product
0	0	0
0	1	0
1	0	0
1	1	1

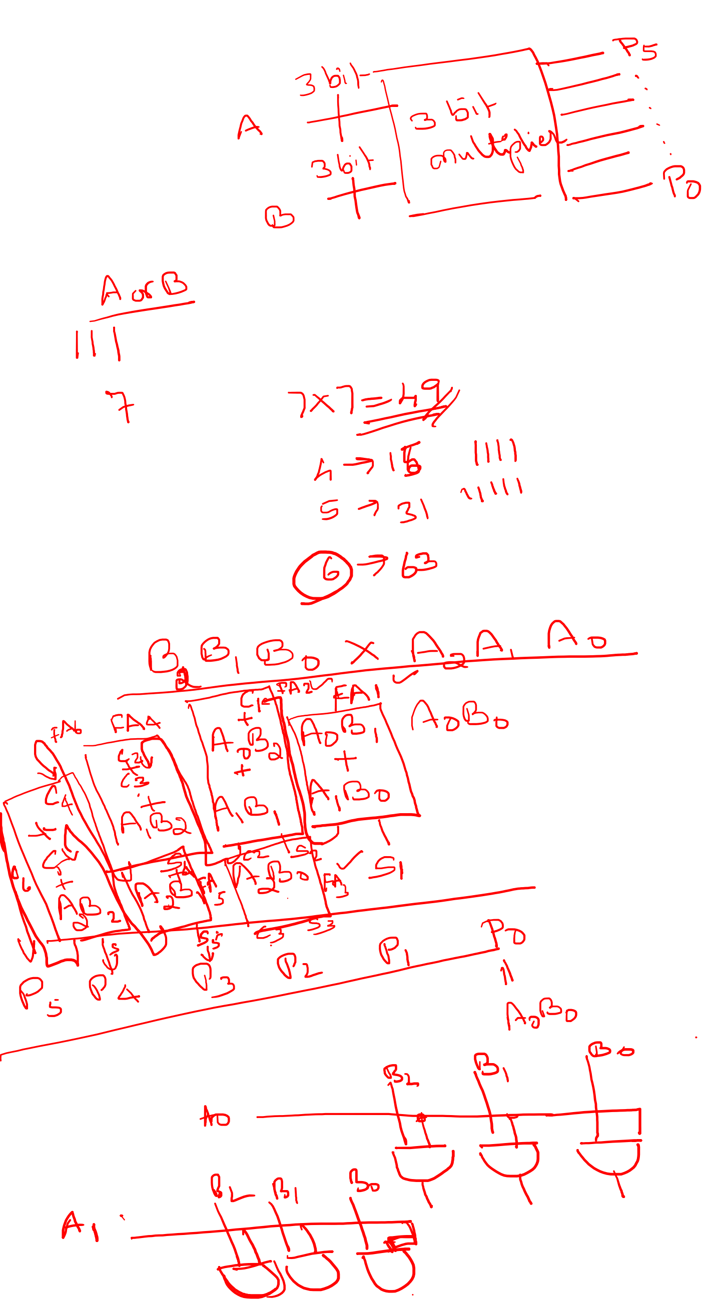
$a_0 \times b_0$

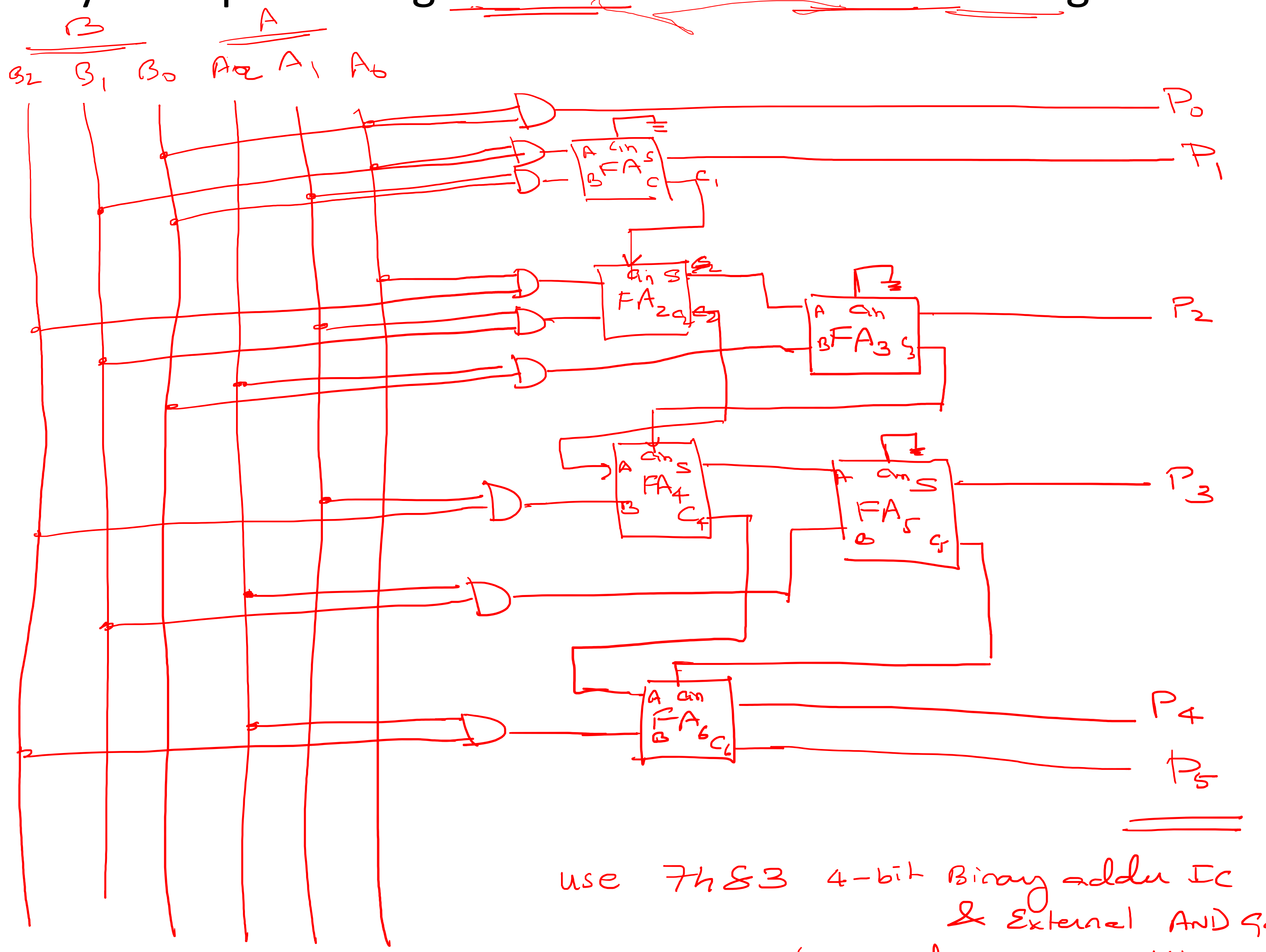
Arithmatic → logic

Bit by Bit multiplication } resembles AND operation



- Design a 3 bit × 3 bit binary multiplier using Full adders and external AND gates.



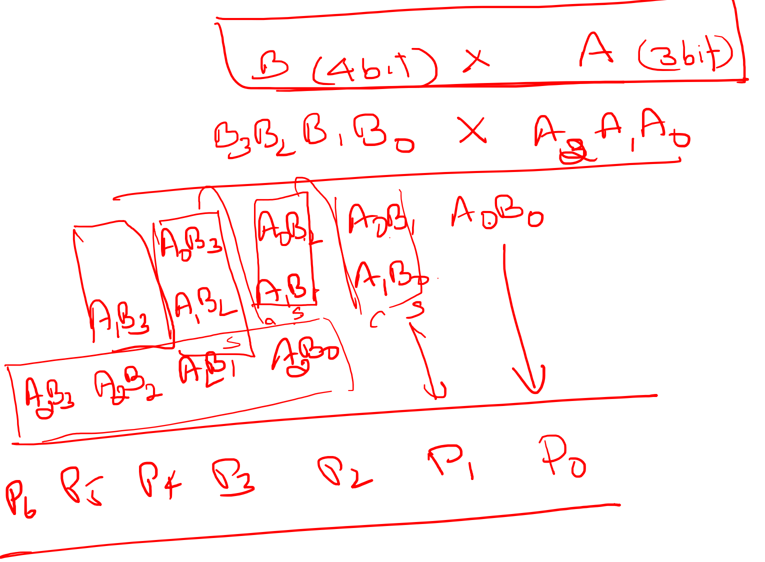


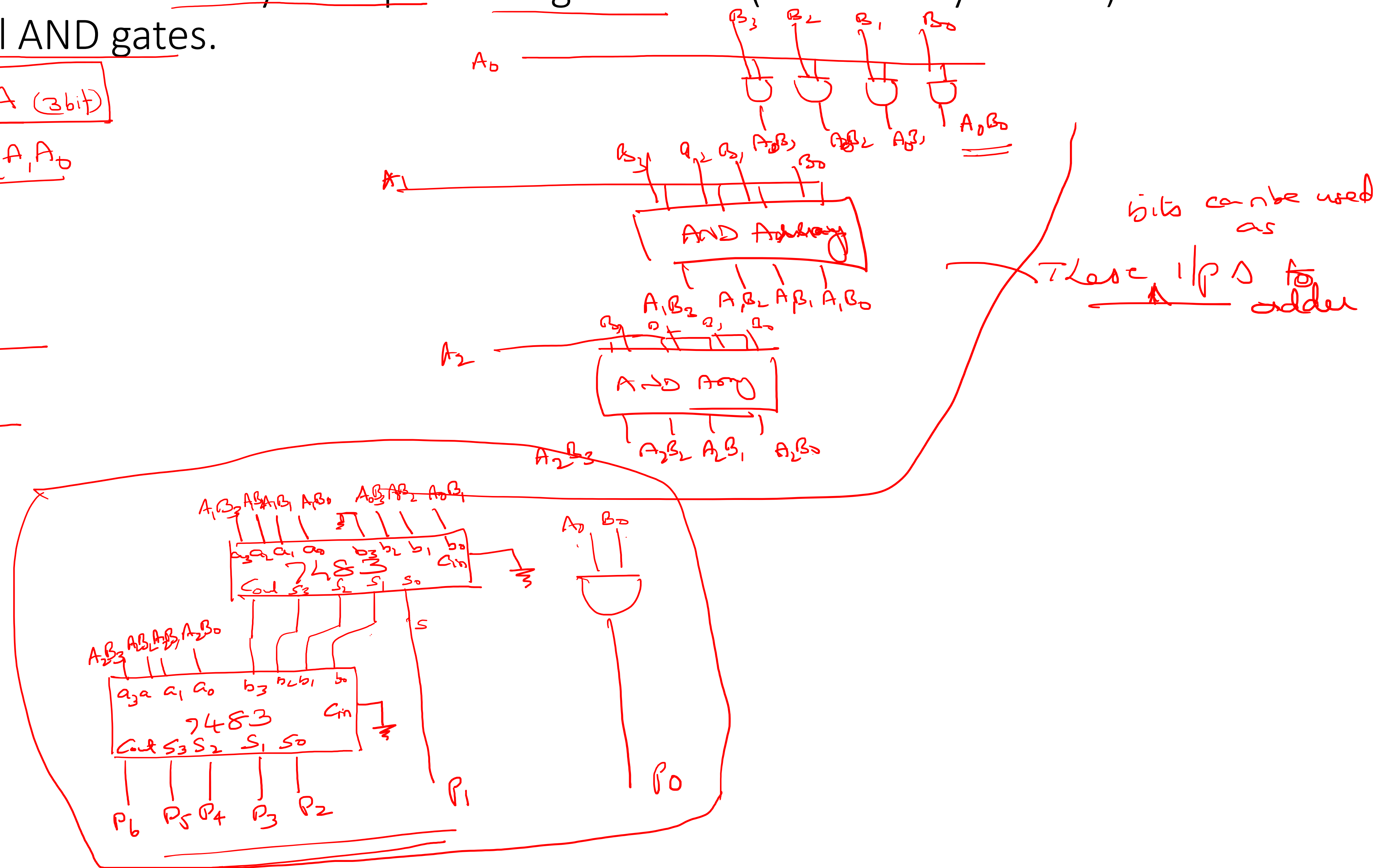
use 74 83 4-bit Binary adder IC & External AND gates to realize 3×3 bit multiplication.

$15 \times 7 = 105$ minimum 7 bits

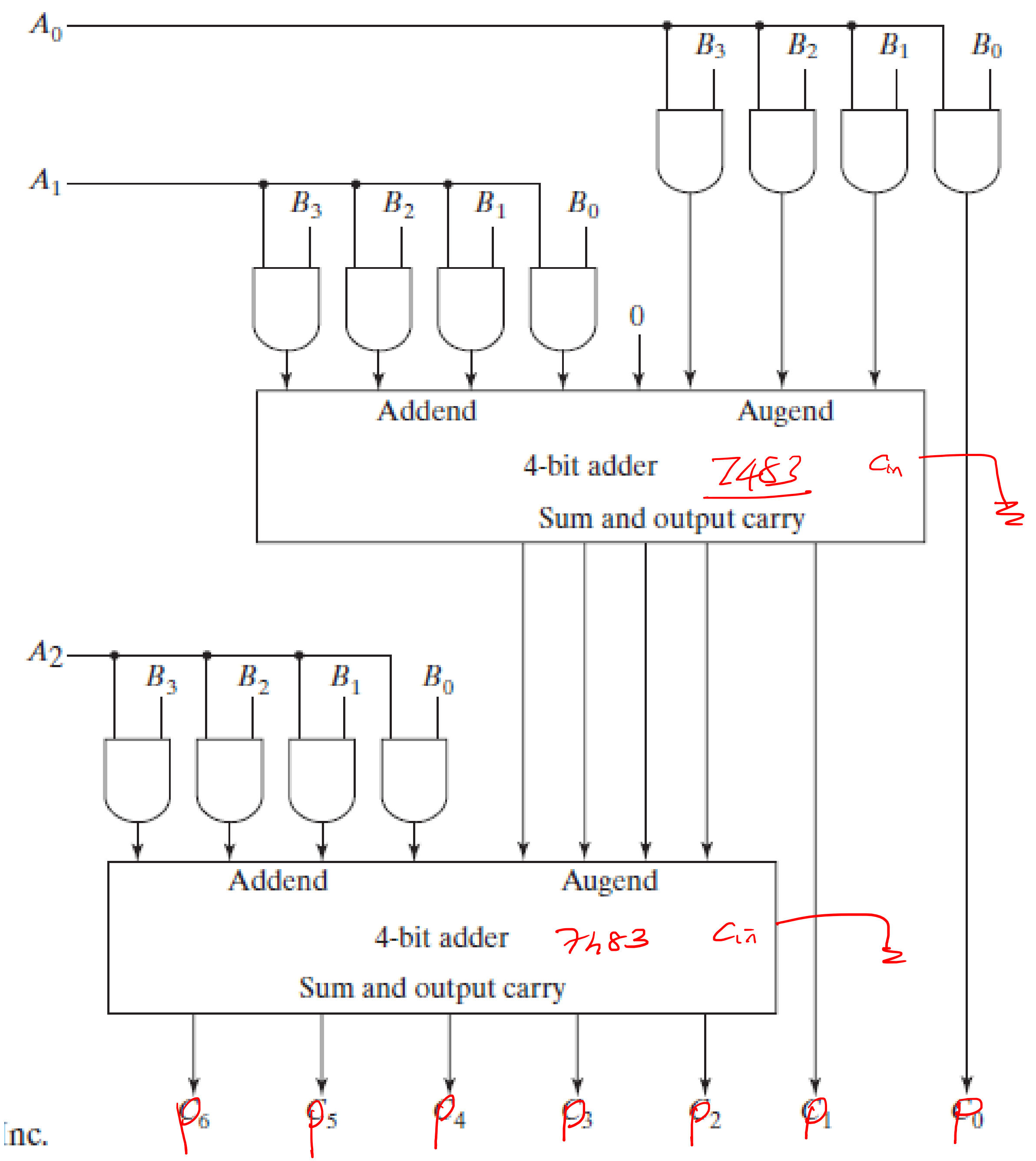
1111×111

Design a 4 bit × 3 bit binary multiplier using 7483 ICs (4 bit binary adders) and external AND gates.





4-bit by 3-bit binary multiplier



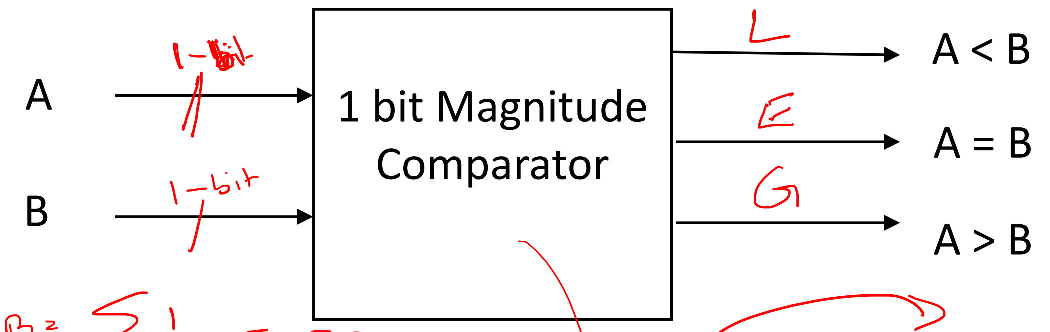
Magnitude Comparator

- 1 bit Magnitude comparator

Truth table

	Input		Output		
	A	B	A<B	A=B	A>B
m_0	0	0	0	1	0
m_1	0	1	1	0	0
m_2	1	0	0	0	1
m_3	1	1	0	1	0

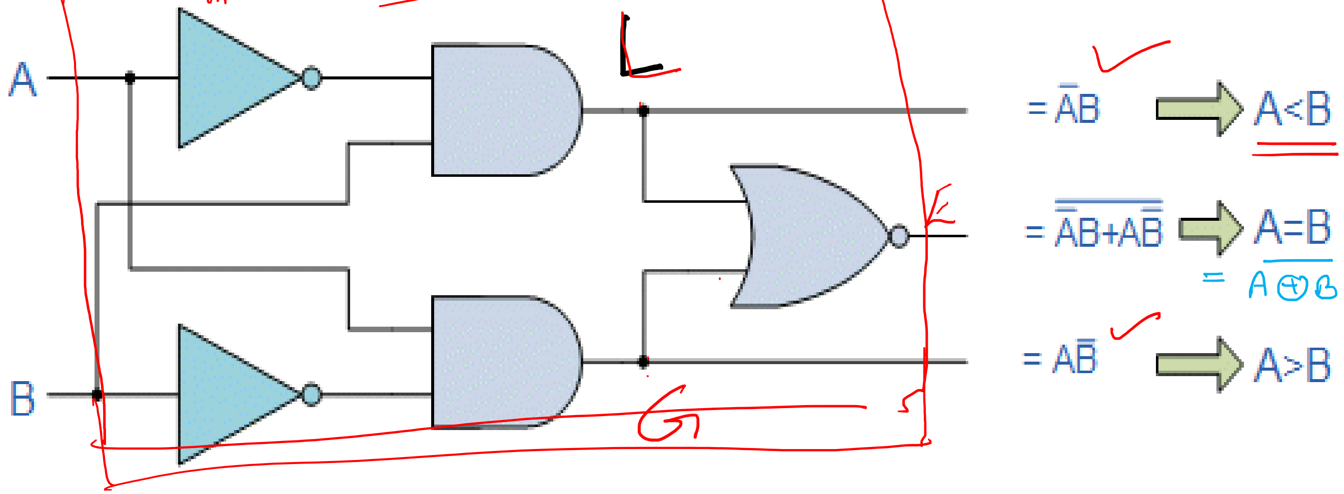
In 1-bit



$A<B = \sum_m 1 = \bar{A}B$

$A=B = \sum_m 0,3 = \cancel{\bar{A}\bar{B}+AB} = \overline{A \oplus B} = \bar{A}\bar{B}+AB = \overline{\bar{A}B+A\bar{B}}$

$A>B = \sum_m 2 = A\bar{B}$



for Example

if to compare A & B ⇒ whether A>B, A=B, A<B

① Draw i/p & o/p relation using combinational logic

② subtraction A − B

$$\begin{array}{r} A \\ -\,B \\ \hline \text{ANS} \end{array}$$

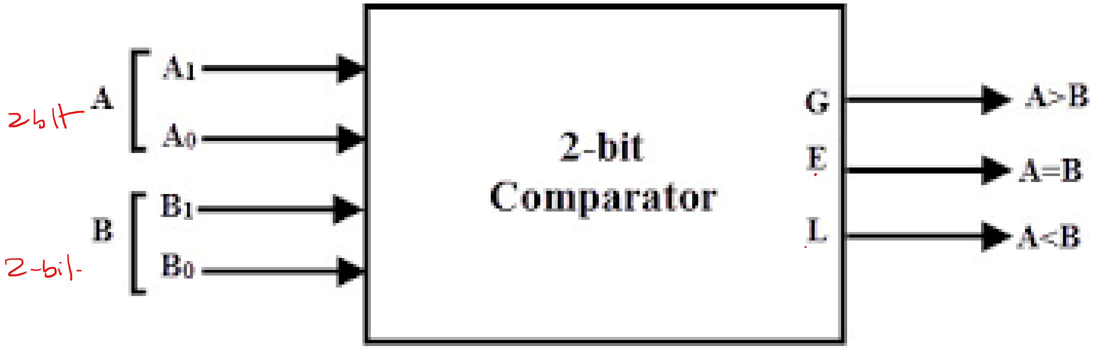
≠ 0 & +ve — A>B

≠ 0 & −ve — A<B

= 0 — A=B

• 2 bit magnitude comparator

	Inputs				Outputs		
	A_1	A_0	B_1	B_0	A>B (G)	A=B (E)	A<B (L)
m_0	0	0	0	0	0	1	0
m_1	0	0	0	1	0	0	1
m_2	0	0	1	0	0	0	1
m_3	0	0	1	1	0	0	1
m_4	0	1	0	0	1	0	0
m_5	0	1	0	1	0	1	0
m_6	0	1	1	0	0	0	1
m_7	0	1	1	1	0	0	1
m_8	1	0	0	0	1	0	0
m_9	1	0	0	1	1	0	0
m_{10}	1	0	1	0	0	1	0
m_{11}	1	0	1	1	0	0	1
m_{12}	1	1	0	0	1	0	0
m_{13}	1	1	0	1	1	0	0
m_{14}	1	1	1	0	1	0	0
m_{15}	1	1	1	1	0	1	0



$G = A>B = \sum_m 4, 8, 9, 12, 13, 14$

$E = A=B = \sum_m 0, 5, 10, 15$

$L = A<B = \sum_m 1, 2, 3, 6, 7, 11$

G:

$A_1A_0 \backslash B_1B_0$	00	01	11	10
00	0	0	0	0
01	1	0	0	0
11	1	1	0	1
10	1	1	0	0

A: $A_1 A_0$ B: $B_1 B_0$

48 A

43 B

$G = \sum_m 4, 8, 9, 12, 13, 14$

$G = A_1\bar{B}_1 + A_0\bar{B}_1\bar{B}_0 + A_1A_0\bar{B}_0$

$G = A_1\bar{B}_1 + A_0\bar{B}_0[A_1 + \bar{B}_1]$

$G = A_1\bar{B}_1 + \bar{A}_1A_0\bar{B}_1\bar{B}_0 + A_1A_0B_1\bar{B}_0$

$= A_1\bar{B}_1 + A_0\bar{B}_0(\bar{A}_1\bar{B}_1 + A_1B_1)$

$= A_1\bar{B}_1 + A_0\bar{B}_0(A_1 \odot B_1)$

$A>B = (A_1>B_1) + (A_1=B_1)(A_0>B_0)$

$A_1\bar{B}_1 + (A_1 \odot B_1)(A_0\bar{B}_0)$

E

2-bit magnitude comparator

$A_1 A_0$

$B_1 B_0$

$\overline{A_1 \oplus B_1} = \overline{\overline{A_1} B_1 + A_1 \overline{B_1}}$

$A = B \Rightarrow E = (A_1 = B_1).(A_0 = B_0) = (\overline{A_1 \oplus B_1}).(\overline{A_0 \oplus B_0})$

$E_1 . E_0$

$A < B \Rightarrow L = (A_1 < B_1) + (A_1 = B_1).(A_0 < B_0)$

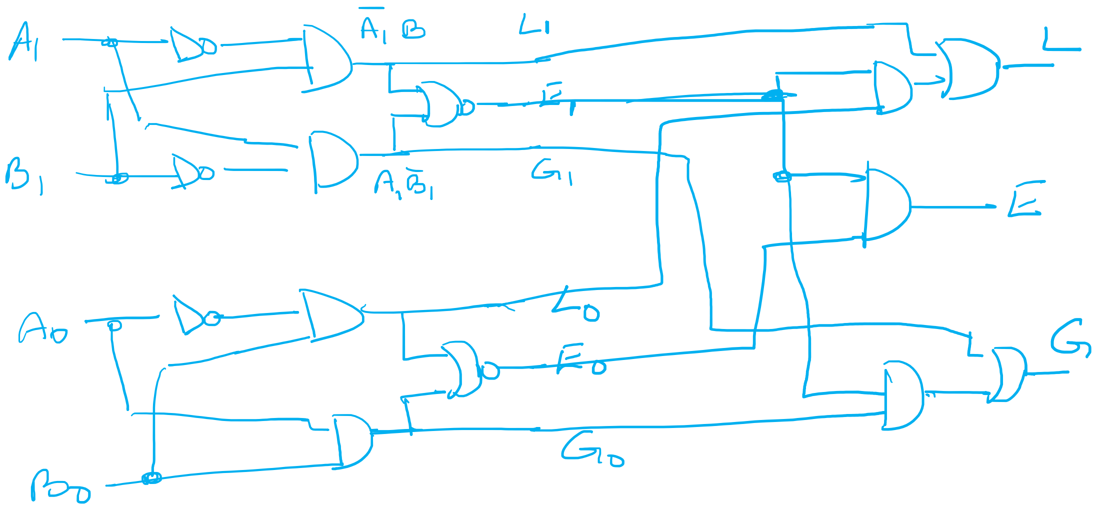
$$\boxed{L = (\overline{A_1} B_1) + (\overline{A_1 \oplus B_1}).(\overline{A_0} B_0)}$$

$L_1 + E_1 . L_0$

$A > B = G = (A_1 > B_1) + (A_1 = B_1)(A_0 > B_0)$

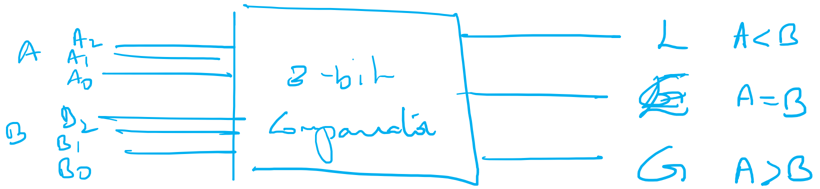
$$\boxed{G = A_1 \overline{B_1} + (\overline{A_1 \oplus B_1}).(A_0 \overline{B_0})}$$

$G_1 + E_1 . G_0$



Two-bit magnitude comparator using 1-bit magnitude comparators

- 3 bit magnitude comparator using 1-bit magnitude comparator block



$A_2 \; A_1 \; A_0$

$B_2 \; B_1 \; B_0$

A_i's, B_i's are 0 or 1

000
001
010
011
100
101
110
111

1 1 1

0 0 0

0 0 0

0 0 1

$$G \text{ or } A>B = G_2 + E_2 G_1 + E_2 E_1 G_0 = A_2\bar{B}_2 + \overline{(A_2 \oplus B_2)} \cdot A_1 \bar{B}_1 + \overline{(A_2 \oplus B_2)}\,\overline{(A_1 \oplus B_1)}\, A_0 \bar{B}_0$$

$$(A_2>B_2) + (A_2=B_2)(A_1>B_1) + (A_2=B_2)(A_1=B_1)(A_0>B_0)$$

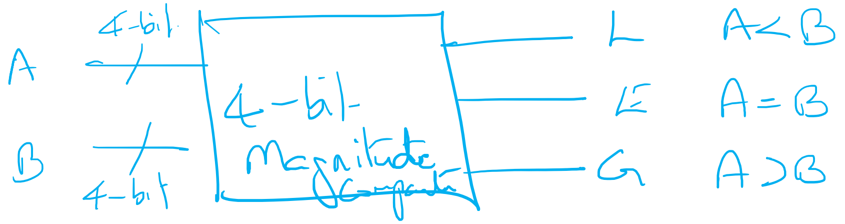
$$E \text{ or } A=B = E_2 \cdot E_1 \cdot E_0 = \overline{(A_2 \oplus B_2)} \cdot \overline{(A_1 \oplus B_1)} \cdot \overline{(A_0 \oplus B_0)}$$

$$(A_2=B_2)\cdot(A_1=B_1)\cdot(A_0=B_0)$$

$$L \text{ or } A<B = L_2 + E_2 L_1 + E_2 E_1 L_0 = \bar{A}_2 B_2 + \overline{(A_2 \oplus B_2)} \cdot \bar{A}_1 B_1 + \overline{(A_2 \oplus B_2)} \cdot \overline{(A_1 \oplus B_1)} \cdot \bar{A}_0 B_0$$

$$(A_2<B_2) + (A_2=B_2)(A_1<B_1) + (A_2=B_2)(A_1=B_1)(A_0<B_0)$$

- 4 bit magnitude comparator



$A_3 A_2 A_1 A_0$

$B_3 B_2 B_1 B_0$

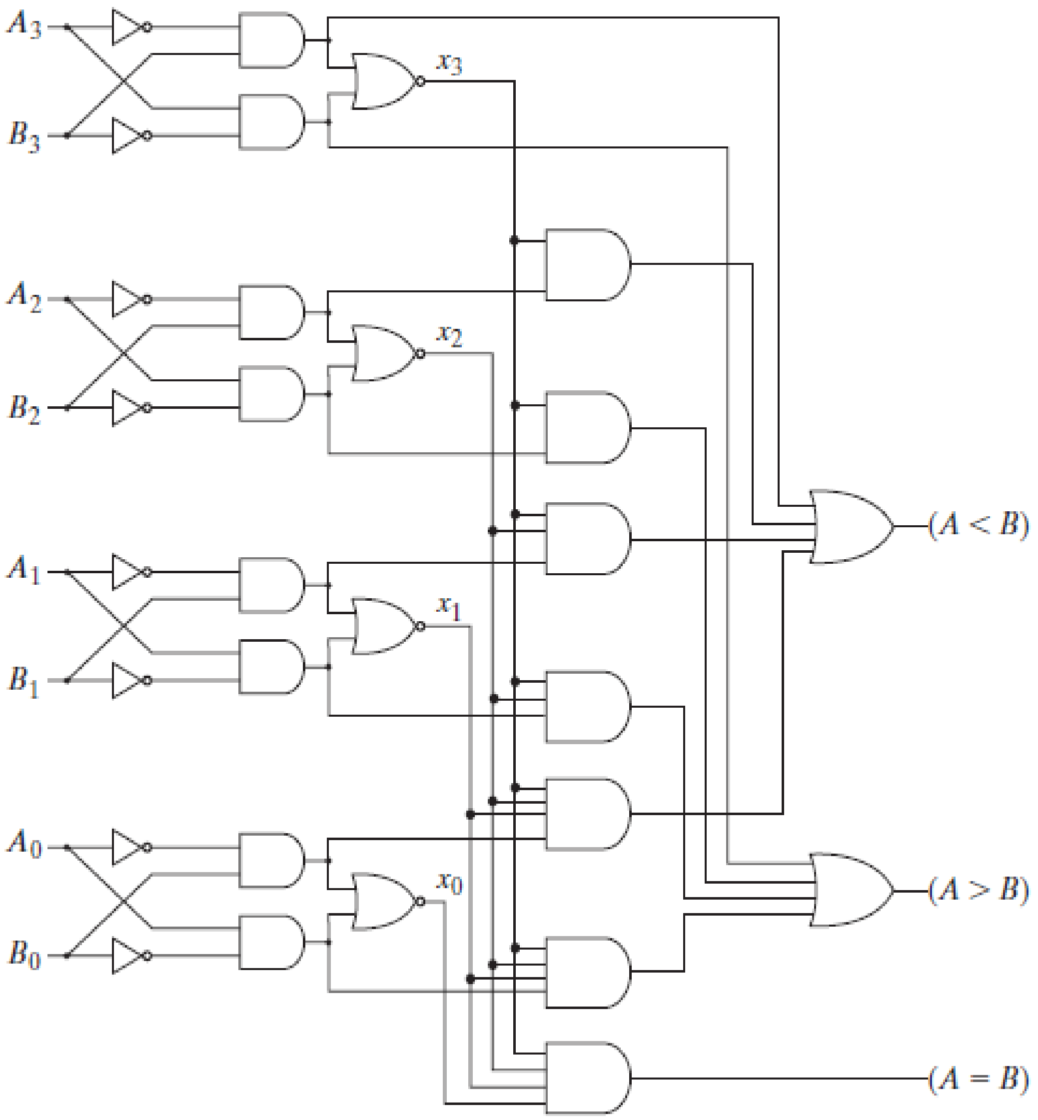
$$G = A > B = G_3 + E_3 G_2 + E_3 E_2 G_1 + E_3 E_2 E_1 G_0$$

$$A_3 \bar{B}_3 + (\overline{A_3 \oplus B_3}) A_2 \bar{B}_2 + \ldots$$

$$E = A = B \Rightarrow E_3 \cdot E_2 \cdot E_1 \cdot E_0$$

$$L = A < B \Rightarrow L_3 + E_3 L_2 + E_3 E_2 L_1 + E_3 E_2 E_1 L_0$$

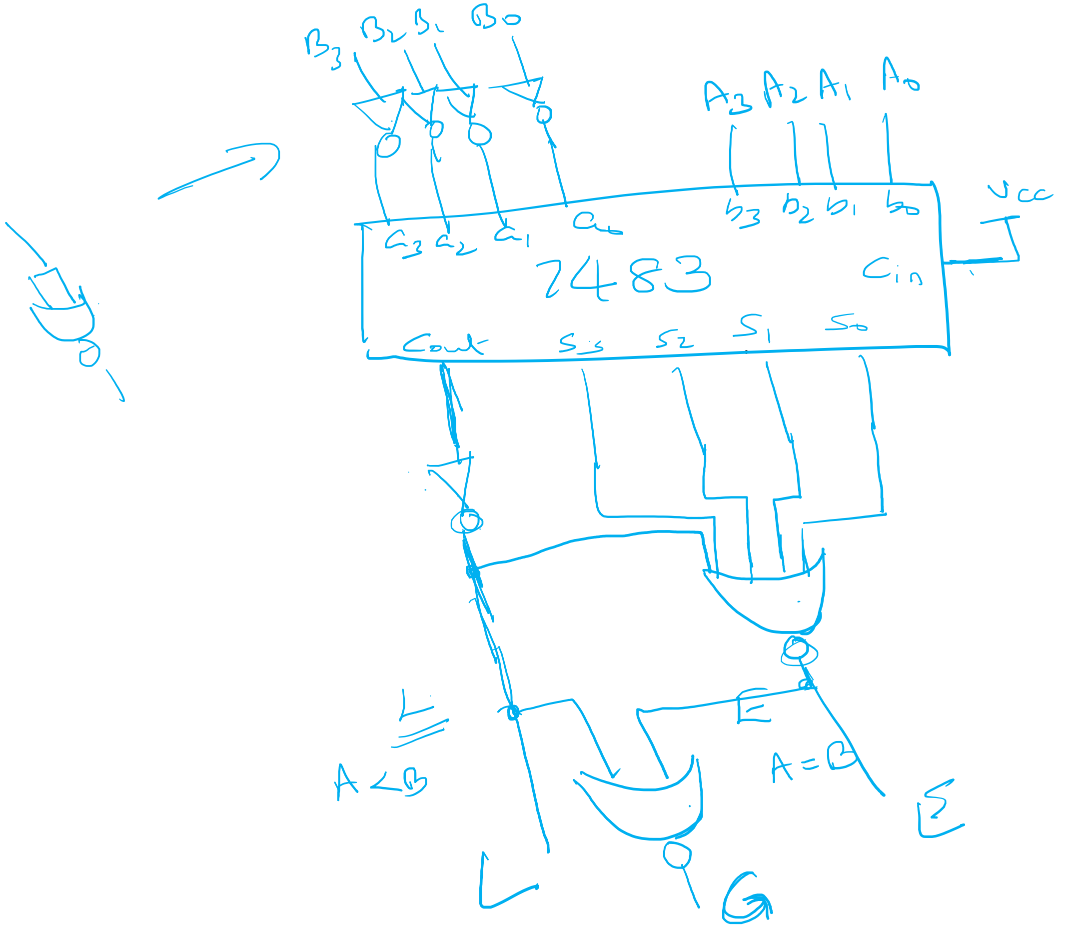
4-bit magnitude comparator



only NOR

Design a 4-bit magnitude comparator using 7483 IC and external gates

What is 7483 IC? → it is 4-bit Binary Adder



A − B → A + 2's comp B

6 → 0110 A
−4 → 1011 B } 2's complement
+1
−0100 → [1] 0010

EQUAL?

4 → 0100
−4 → 1011 } 2's cmp of 4
1
E [1] 0000 ANS

4
−6 −0110

Carry → +ve

No Carry → −ve

0100
1001
1
[0] 1110 Ans − 2's cmp

G = ?

$G = \overline{L} \cdot \overline{E}$

$L + E = \overline{\overline{L} \cdot \overline{E}}$