

**Department of Information & Communication Technology**  
**MIT, Manipal**

**III Sem B. Tech (IT/CCE),**  
**ICT 2154 Digital Systems / ICT 2171 Digital Systems and Computer Organization**  
**In-sem Examination**

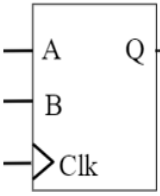
**Date: 15/12/2021**

**Max. Marks: 20**

**Write-up Time: 10.30 to 11.50am**

**Upload time: 11.50am to 12.00pm**

**Note to Students: Answer ALL Questions**

<b>Q1.</b>	Design the following combinational circuit using minimum number of 7483 ICs and half adder blocks.  If $A < B$ , $F = 2A + 4B$  Else $F = 4A + 2B$  Where A and B are 2-bit binary numbers.	<b>3 Marks</b>															
<b>Q2.</b>	Construct a mod-42 decimal up counting circuit using only asynchronous ICs. Draw the logic diagram.	<b>3 Marks</b>															
<b>Q3.</b>	Design a 2-bit x 2-bit binary multiplier using 74151 ICs and minimum external gates.	<b>3 Marks</b>															
<b>Q4.</b>	Function table defines the working of a fictitious AB flip flop. Design the AB flip flop using D flip flop and external gates.	<table border="1"> <thead> <tr> <th>A</th><th>B</th><th>Q(t+1)</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>0</td></tr> <tr> <td>0</td><td>1</td><td>1</td></tr> <tr> <td>1</td><td>0</td><td>Q</td></tr> <tr> <td>1</td><td>1</td><td>Q'</td></tr> </tbody> </table> 	A	B	Q(t+1)	0	0	0	0	1	1	1	0	Q	1	1	Q'
A	B	Q(t+1)															
0	0	0															
0	1	1															
1	0	Q															
1	1	Q'															
<b>Q5.</b>	Design a T flip flop using a basic NOR latch and external gates.	<b>4 Marks</b>															
<b>Q6.</b>	Design a code converter to convert a decimal digit represented in excess-3 code to a decimal digit represented in self-complementary 5 2 1 1 code using minimum number of 3 to 8 decoders with active low output and active high enable input, and external gates.	<b>4 Marks</b>															