COURSE PLAN

Department: INFORMATION & COMMUNICATION TECHNOLOGY

Computer Organisation & Microprocessor Systems &

Course Name & code : ICT 2256

Semester & branch : IV sme & B.Tech (IT)

Name of the faculty : Dr. Santhosha Rao, Mr. Raviraja Holla M

No of contact hours/week:

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Course Outcomes (COs)

	At the end of this course, the student should be able to:	No. of Contact Hours	Marks
CO1:	Recall 8086 architecture	4	12
CO2:	Write assembly language programs using development tools	14	38
CO3:	Understand the interfacing of programmable devices to 8086 microprocessor	3	08
CO4:	Understand the organization of various parts in computer system	8	22
CO5:	Design building blocks of computer system	7	20
	Total	36	100

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Assessment Plan

Components	Assignments	Sessional Tests	End Semester/
Duration	20 to 30 minutes	60 minutes	Make-up Examination 180 minutes
Weightage	20 % (4 X 5 marks)	30 % (2 X 15 Marks)	50 % (1 X 50 Marks)
Typology of Questions	Understanding/ Comprehension; Application; Analysis; Synthesis; Evaluation	Knowledge/ Recall; Understanding/ Comprehension; Application	Understanding/ Comprehension; Application; Analysis; Synthesis; Evaluation
Pattern	Answer one randomly selected question from the problem sheet (Students can refer their class notes)	MCQ: 10 questions (0.5 marks) Short Answers: 5 questions (2 marks)	Answer all 5 full questions of 10 marks each. Each question may have 2 to 3 parts of 3/4/5/6/7 marks
Schedule	4, 7, 10, and 13 th week of academic calendar	Calendared activity	Calendared activity
Topics Covered	Quiz 1 (L 1-9 & T _{y1-y2}) (CO1,CO2) Quiz 2 (L 10-18 & T _{y3-y4}) (CO2) Quiz 3 (L 19-26 & T _{y5-y6}) (CO3,CO4,CO5) Quiz 4 (L 27-34 & T _{y7-y8}) (CO4,CO5)	Test 1 (L 1-15 & T _{b1-b2}) (CO1,CO2) Test 2 (L 16-27 & T _{b3-b4}) (CO2,CO3,CO4,CO5)	Comprehensive examination covering full syllabus. Students are expected to answer all questions (CO1-5)

Lesson Plan

L. No./ T. No.	Topics	Course Outcome Addressed
LO	Objectives of the course, relevance, course plan, evaluation, references,	CO1
	Introduction to microprocessor	
L1	8086 internal architecture-Bus Interface Unit, Execution Unit	CO1
L2	Functional pin diagram	CO1
L3	Segmentation & memory addressing	CO1
L4	Modes operation	CO1
L5	Addressing modes	CO2
L6	Assembler Directives	CO2
L7	Data movement instructions	CO2
L8	Arithmetic and logical instructions	CO2
L9	Process control instructions	CO2

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L11 Br L12 As L13 As L14 M L15 Pr L16 BI L17 Pr L18 Pr L19 82 L20 82 L21 82	tring instructions tranch instructions assembly language programs assembly language development tools, stacks and subroutine Macro and procedure trograms using macro and procedure trograms using interrupts trograms using interrupts trograms using interrupts contd. 255 Programmable Peripheral Interface	CO2
L12 As L13 As L14 M L15 Pr L16 BI L17 Pr L18 Pr L19 82 L20 82 L21 82	Assembly language programs Assembly language development tools, stacks and subroutine Macro and procedure Programs using macro and procedure Programs using interrupts Programs using interrupts Programs using interrupts Programs using interrupts contd.	CO2 CO2 CO2 CO2 CO2 CO2 CO2
L13 As L14 M L15 Pr L16 BI L17 Pr L18 Pr L19 82 L20 82 L21 82	Assembly language development tools, stacks and subroutine Acro and procedure Programs using macro and procedure Programs using interrupts Programs using interrupts Programs using interrupts contd.	CO2 CO2 CO2 CO2 CO2
L14 M L15 Pr L16 BI L17 Pr L18 Pr L19 82 L20 82 L21 82	Macro and procedure Programs using macro and procedure Programs using interrupts Programs using interrupts Programs using interrupts Programs using interrupts contd. Programs using interrupts contd.	CO2 CO2 CO2 CO2
L15 Pr L16 BI L17 Pr L18 Pr L19 82 L20 82 L21 82	Programs using macro and procedure BIOS and DOS interrupts Programs using interrupts Programs using interrupts contd. Programs using interrupts contd.	CO2 CO2 CO2
L16 BI L17 Pr L18 Pr L19 82 L20 82 L21 82	Programs using interrupts Programs using interrupts contd. Programmable Peripheral Interface	CO2 CO2
L17 Pr L18 Pr L19 82 L20 82 L21 82	rograms using interrupts rograms using interrupts contd. 255 Programmable Peripheral Interface	CO2
L18 Pr L19 82 L20 82 L21 82	Programs using interrupts contd. 255 Programmable Peripheral Interface	CO2
L19 82 L20 82 L21 82	255 Programmable Peripheral Interface	
L20 82	·	CO3
L21 82	254 Programmable Interval Timer	
	20.1.1.08.4	CO3
122 E	259 Programmable Interrupt Controller	CO3
	Evolution of computers, Von- Neumann architecture	CO4
	Computer structures: General register machine, Accumulator based machine, stack nachines.	CO4
	Combinational shifter design	CO5
L25 A	Adders. Arithmetic and Logic Unit Design	CO5
L26 M	Aultiplication algorithms	CO5
L27 Di	Division algorithms	CO5
L28 Co	Control unit basic concepts	CO4
L29 Co	Control Unit design using Hardwired approach	CO5
L30 Co	Control Unit design using Microprogramming approach	CO5
L31 Co	Control Unit design using Microprogramming approach contd.	CO5
L32 Ty	Types of memory and characteristics, memory hierarchy	CO4
L33 M	Main memory design, Cache memory	CO4
L34 Ca	Cache mapping techniques, Virtual Memory	CO4
L35 Pr	Programmed I/O, Interrupt I/O	CO4
L36 D:	Direct memory access, I/O bus standards	CO4

Refe	erences:						
1.	Douglas V	/. Hall, Mid	croprocessors and Ir	nterfacing: Pro	ogramming and Hardware, revis	sed 2nd Edi-tion	
	,Tata McG	Graw Hill, 2	2006				
2.	Barry B. Brey, The Intel Microprocessors: 8086 to Pentium Pro - Architecture, Programming and Interfacing (8e), Prentice Hall of India, 2012						
3.	K. Udaykumar and B. S Umashankar, Advanced microprocessors and IBM –PC assembly language programming, McGraw Hill Education, 2017.						
4.	Mohamed Pvt. Ltd, 2		aman and Rajan Cha	andra, Moder	n computer Architecture, Galgo	tia Publications	
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