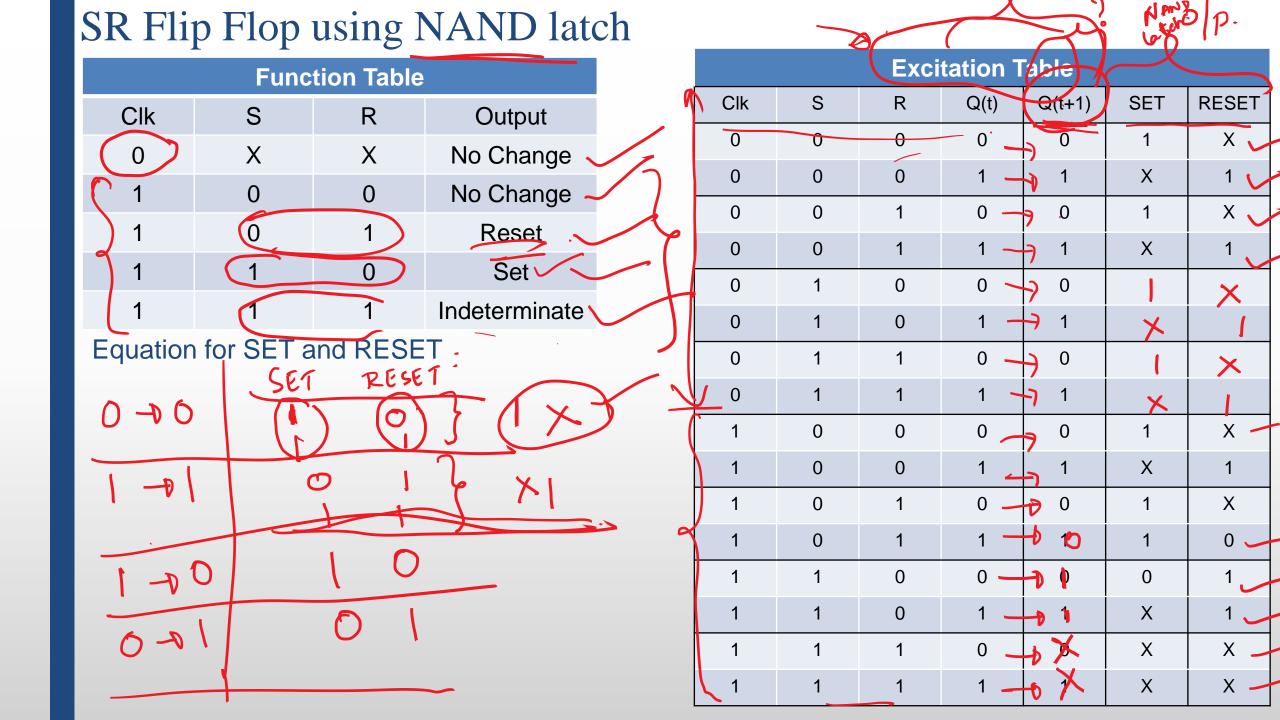
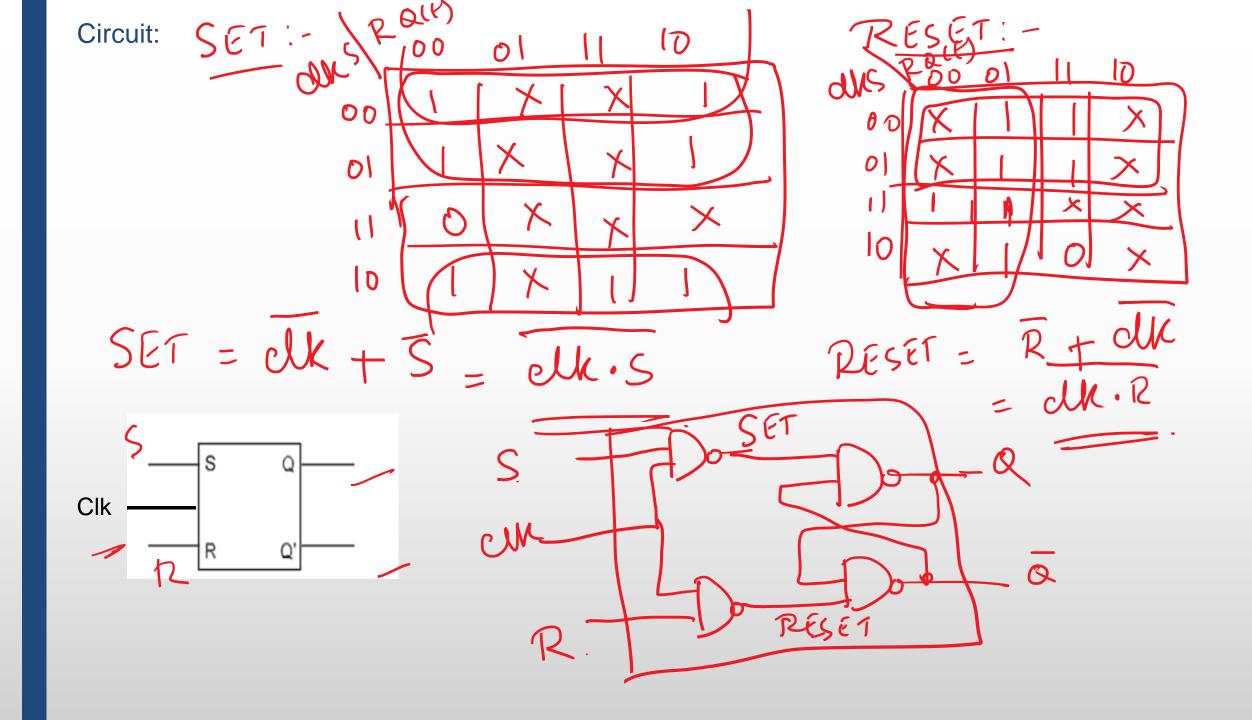
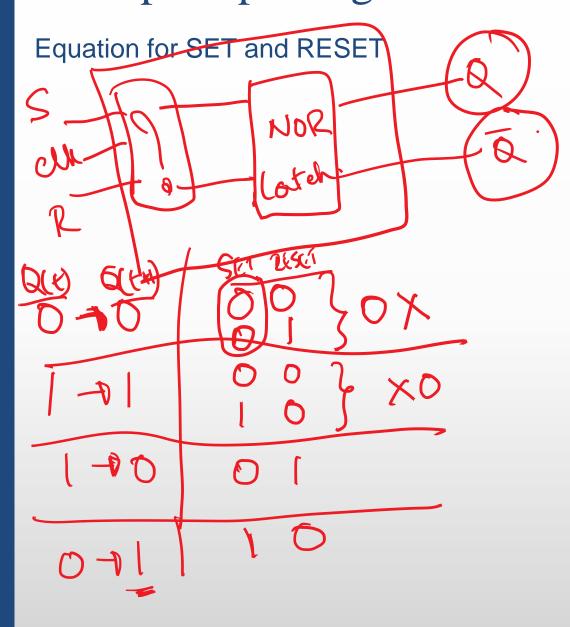
SEQUENTIAL CIRCUITS

- NAND Latch
- NOR Latch
- SR, D, JK, T flip flop



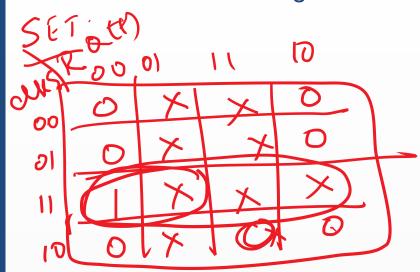


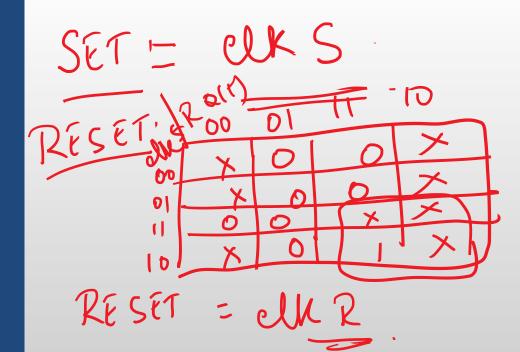
SR Flip Flop using NOR latch

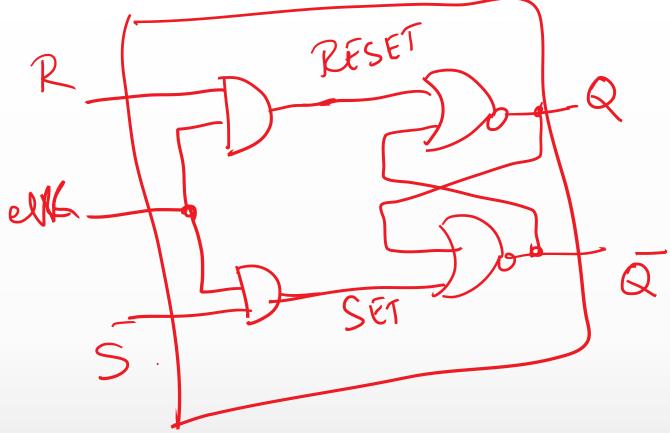


		~	م ال	} / /	\ \\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	of bid
			EXCI	tation Table		1
•	Clk	S	R	Q(t) Q(t+1)	SET	RESET
	0	0	0	0 () 0	Q	×
	0	0	0	1)	×	0
	0	0	1	0 0	0	×
X	0	0	1	1 -> 1	X	× 0
	0	1	0	0 -> 0	0	×
	0	1	0	1 -> 1	X	0
	0	1	1	0 -> 0	0	×
	0	1	1	1 -0 1	O ×	0
	1	0	0	0 -> 0	0	×
	1	0	0	1 ->1	X	D
	1	0	1	0 -> 0	0	×
C	1	0	1	1 6	0	1
	1	1	0	0		0
	1	1	0	1	K	0
	1	1	1	0 -> +	*	×
	1	1	1	1, 1, 1	× ×	×
			V			

Circuit and Block Diagram



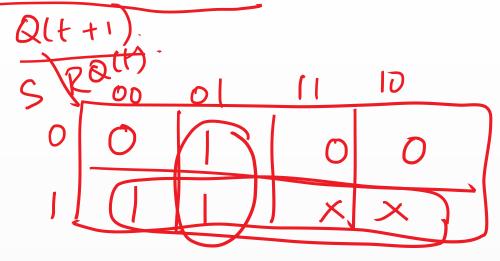




SR-PF.

Characteristic Table									
S	R	Q(t)	Q(t+1)						
0	0	0	O						
0	0	1							
0	1	0	6						
0	1	1	0						
1	0	0							
1	0	1							
1	1	0	X						
1	1	1	X						

Characteristic equation:



$$Q(t+1) = S + RQ(t)$$

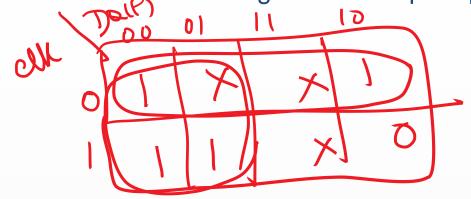
9 When S=R=I does not occur

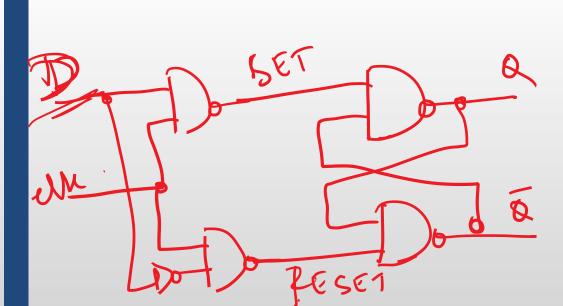
D Flip Flop using NAND latch

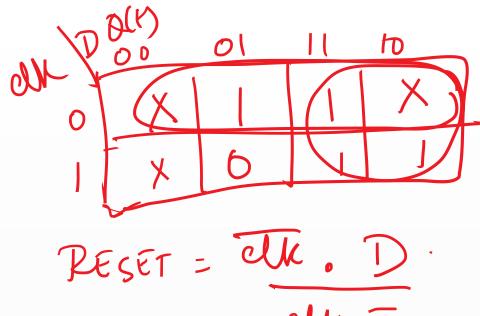


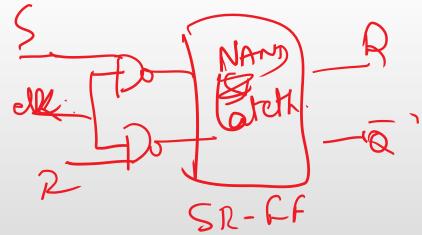
Difficultification and the contraction of the contr									
	Function Table					Excitation	on Table	~	4
Clk	D	Output	ll .	Clk	D	Q(t)	Q(t+1)	SET	RESET
0	x 0 · 7	No change		0	0	04	-D O	1	X
1	1	Set 1	•	0	0	1 4	1 (X	1
Equation for SE	ET and RESET	SET ZESE	1	0	1	0 _	VO		X
0-00	Seria	1 2 1 X		0	1	1	0	X	1
	,	0		1	0	0	70		×
		T X I		1	0	1 _	00	- 1	O
		_	1	1	0	Ð	0		
		5		1	1	1	7	X	
1-06									·

Circuit and block diagram of D Flip Flop



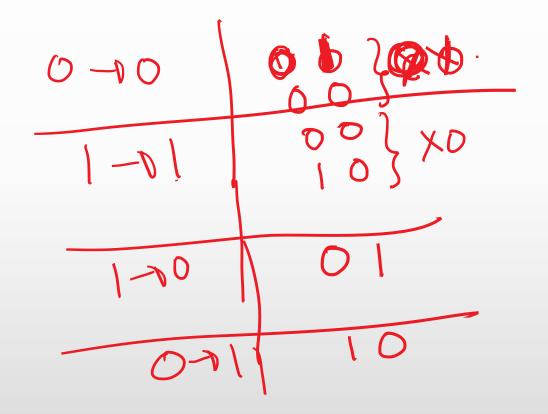




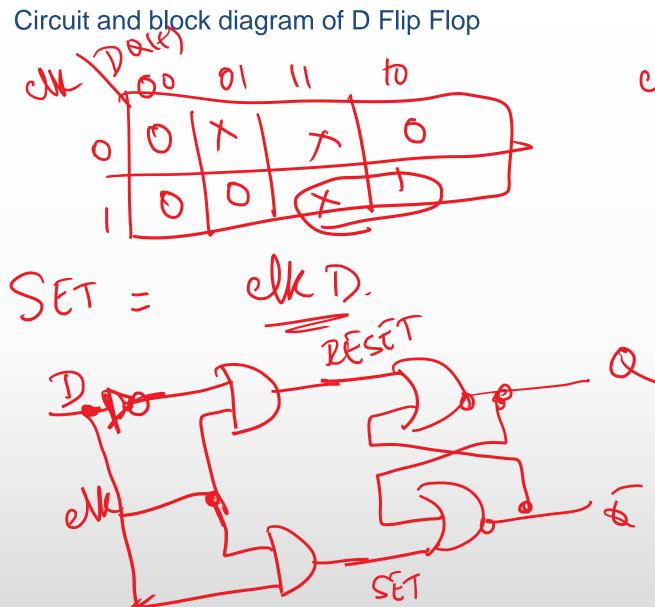


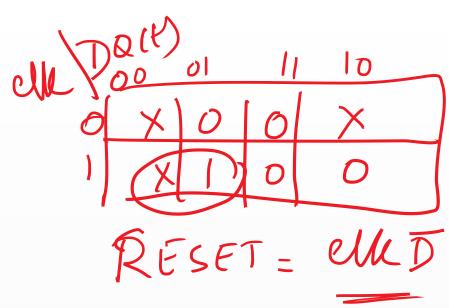
D Flip Flop using NOR Latch

Equation for SET and RESET

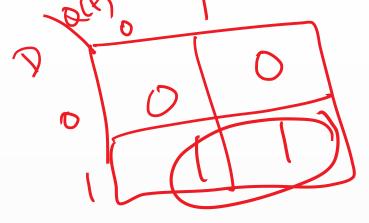


Excitation Table								
Clk	D	Q(t)	Q(t+1)	SET	RESET			
0	0	0 _) 0	\bigcirc	×			
0	0	1 —	D 1	X	0			
0	1	0 —	1 0	0	×			
0	1	1 -	1 1	X	0			
1	0	0 -	1 0	0	×			
1	0	1 _	0	0				
1	1	0	3 1	1	0			
1	1	1 _) 1	X	0			

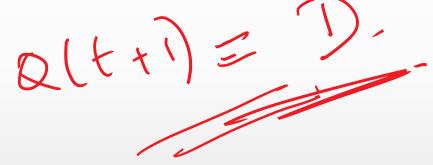


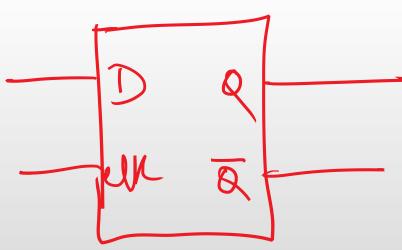


Characteristic equation:

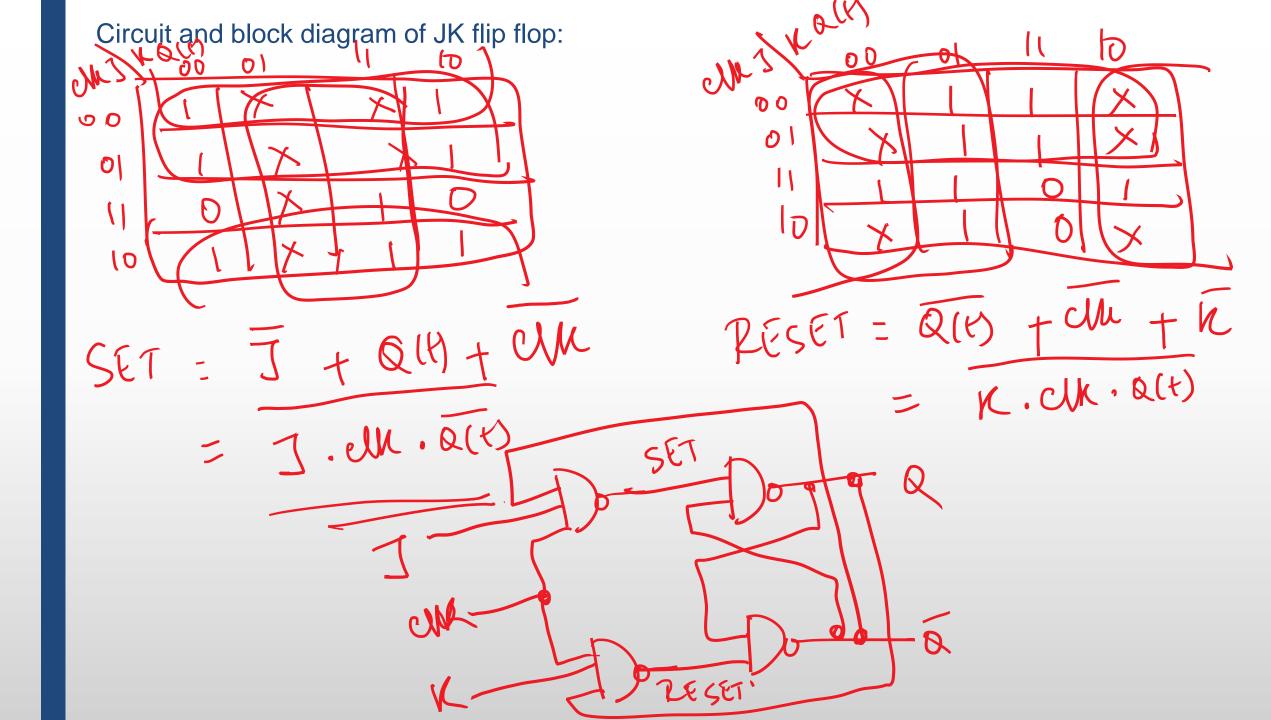


Characteristic Table								
D	Q(t)	Q(t+1)						
0	0	0						
0	1	0						
1	0							
1	1	1						





JK Flij	JK Flip Flop using NAND latch									NR	17) (40)
	Fun	ction Table	Q(K4)	ļ			Exci	tation 1	able		
Clk	J	K	Output		Clk	J	K	Q(t)	Q(t+1)	SET	RESET
0	X	X	No Change		0	0	0	0 —	10	(×
1	0	0	No Change ~	7	0	0	0	1 _	-61	X	1
1	0	1	Reset \checkmark	1	0	0	1	0	0		X
$\sqrt{1}$	1	0	Set ~		0	0	1	1	l	×	1
1	1	_	QUYoggle _		0	1	0	0	0		×
Fountion	for SET	and RESE			0	1	0	1	1	X	ſ
Equation			_	:	0	1	1	0	0	1	×
0 -	· FS	SET RESET	Set ices		0	1	1	1	- 1	X	1
0-6	U		\sim	· (1	0	0	0	0	l	×
		10) <u>[</u>		1	0	0	1		<u> </u>	1
1-01			1 × 1		1	0	1	0 —			X
		DI	S		1	0	1	1	D		0
					1	1	0	0 -	0 1	0	
(-)	5	1 0		<u> </u>	1	1	0	1 _	D I	X	
		a I			1	1	1	0 —	7	0	İ
0 -	16	U (1	Ţ	1	1	1	1 –	70	t	o



JK Flip Flop using NOR latch

Equation for SET and RESET

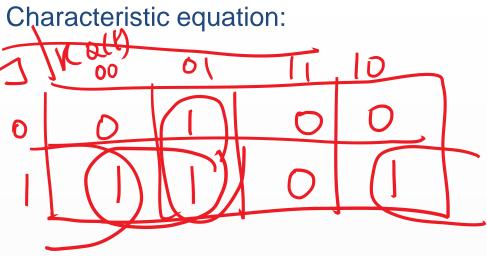


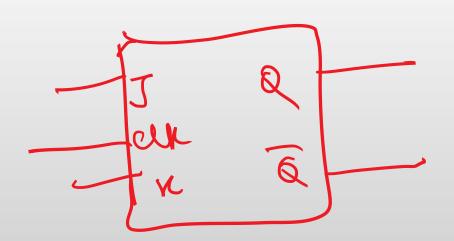
Excitation Table										
Clk	J	K	Q(t)	Q(t+1)	SET	RESET				
0	0	0	0							
0	0	0	1							
0	0	1	0							
0	0	1	1							
0	1	0	0							
0	1	0	1							
0	1	1	0							
0	1	1	1							
1	0	0	0							
1	0	0	1							
1	0	1	0							
1	0	1	1							
1	1	0	0							
1	1	0	1							
1	1	1	0							
1	1	1	1							

Circuit and Block Diagram

5612 Jus

	Characteristic Table								
	J	K	Q(t)	Q(t+1)					
(0	0	0	٥					
,	0	0	1	1					
	0	1	0	Ó					
	0	1	1	D					
	1	0	0						
	1	0	1						
	1	1	0	1					
\	1	1	1	D					





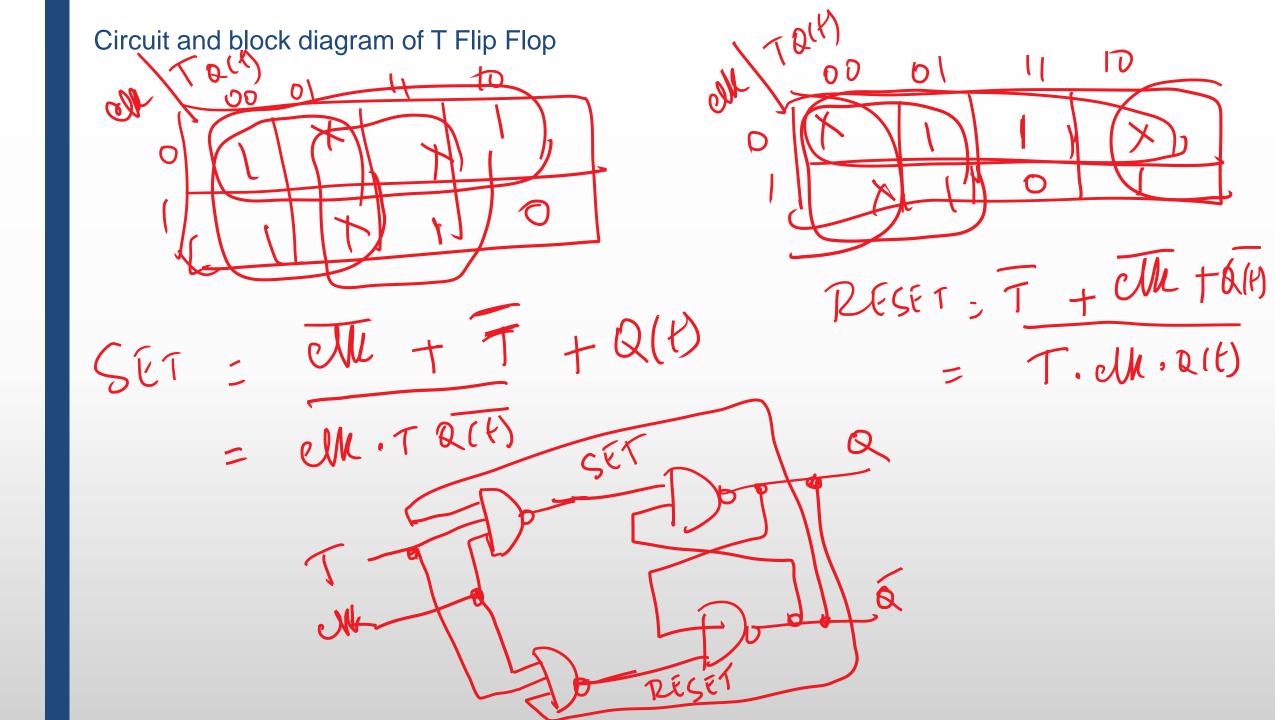
T Flip Flop using NAND latch

NAN	D	Catch

		Function Table	Q(K+1)
	Clk	Т	Output
	0	X	No change
5	1	0	No Change 📞
	1	1	Toggle 🔾

Equation for SET	SET RESET	
0-00		XIF
)
1-01		4 1
0-71	0 1	1
1-20	10	

Excitation Table									
Clk	Т	Q(t)	Q(t+1)	SET	RESET				
0	0	0 _	-D O	L	×				
0	0	1 -	7	X	1				
0	1	0 _	-DO	l	×				
0	1	1 —	D 1	×	1				
1	0	0 _	10	1	×				
1	0	1 —	1 0	X	1				
1	1	0 _	- 0)	0					
1	1	1 _	70		O				



T Flip Flop using NOR Latch

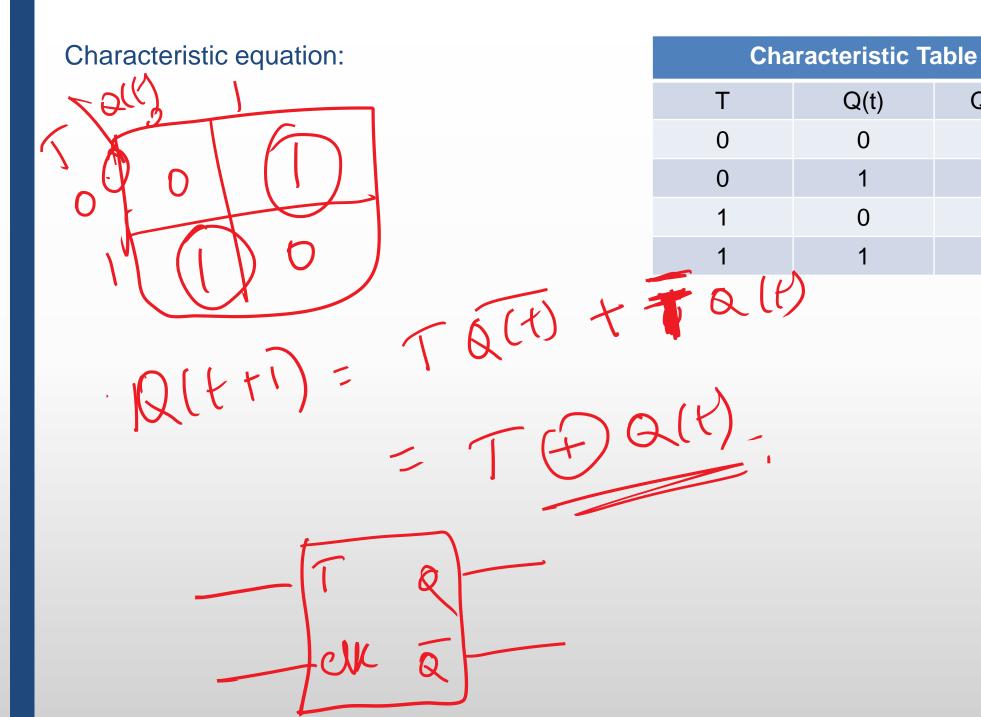
Equation for SET and RESET



Excitation Table					
Clk	Т	Q(t)	Q(t+1)	SET	RESET
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

Circuit and block diagram of T Flip Flop





Q(t+1)

Q(t)

0

0