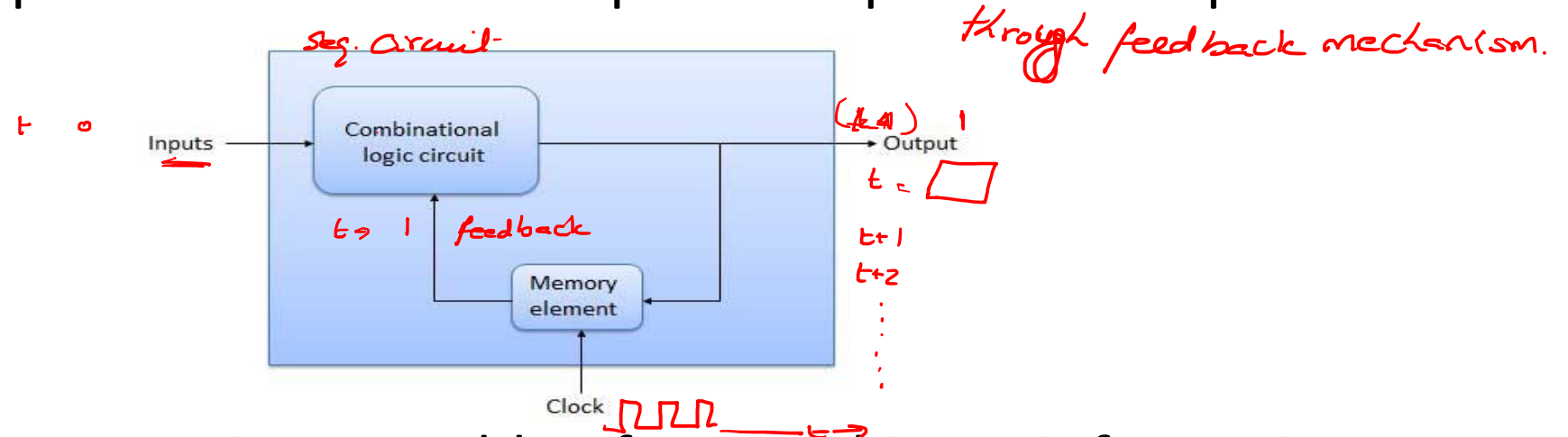


Sequential circuits

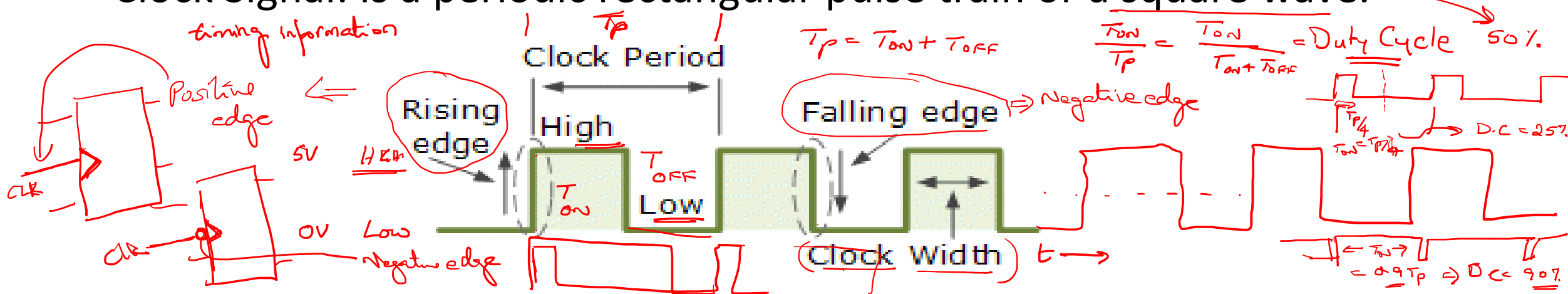
- NAND Latch
- NOR Latch
- SR, D, JK, T flip flop

Sequential circuits:

- Outputs are dependent on current inputs and previous outputs.



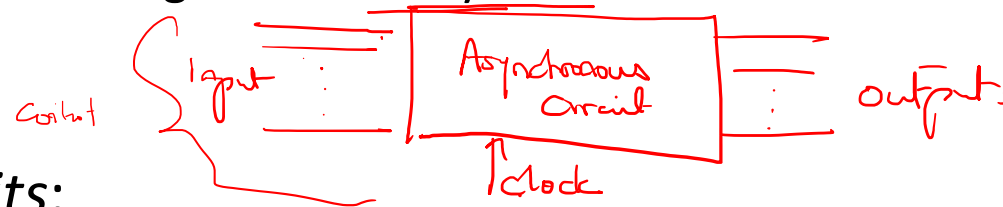
- Storage elements : Devices capable of storing binary information *in terms of bits*
- Clock Signal: Is a periodic rectangular pulse train or a square wave.



- Two types of sequential circuits:

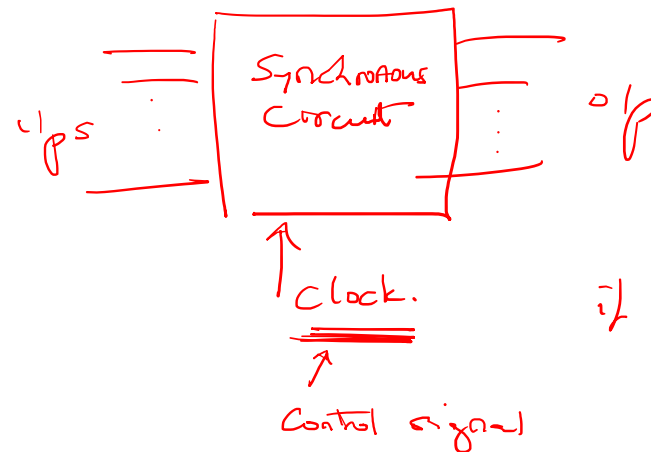
- Asynchronous sequential circuits:*

The output of the logic circuits can change state at any time when one or more of the inputs change.



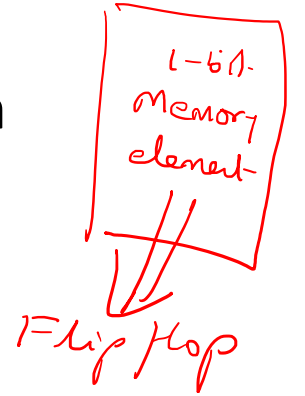
- Synchronous sequential circuits:*

The exact times at which any output can change states are determined by a signal called the clock.



if clock change \rightarrow o/p change

- Flip Flop:
 - Is a binary storage element capable of storing one bit of information
- Latch: *basic circuit within flip flop*
 - Basic type of flip flop is referred as Latch



(Latch + control) = flip flop

In latches : circuit is built using NAND or NOR gates.

NAND Latch (Active Low latch)

Characteristic Table

Present state

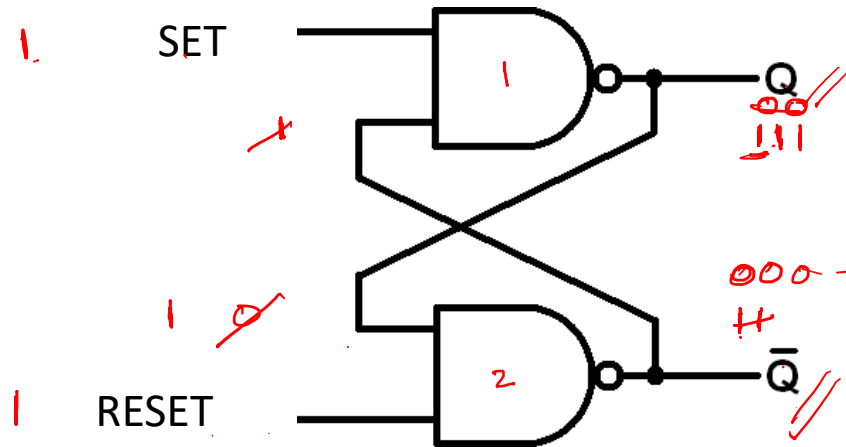
Next state

$Q = \bar{Q}$

Step → time count

Previous state

Present state



Set 1 R=0 $Q(t+1) = Q(t)$

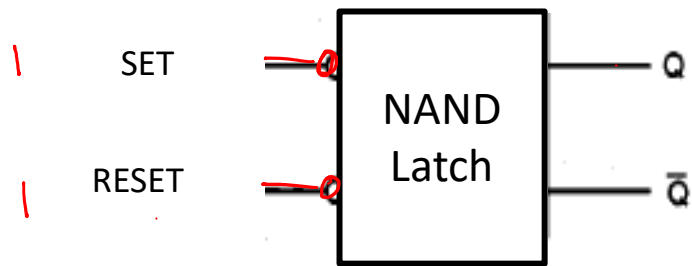
Set 1 R=0 $Q(t+1) = 0$

SET	RESET	Q(t)	Q(t+1)	Q'(t+1)
0	0	0	1	1
0	0	1	1	1
0	1	0	1	0
0	1	1	1	0
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

INVALID or Indeterminate state OR

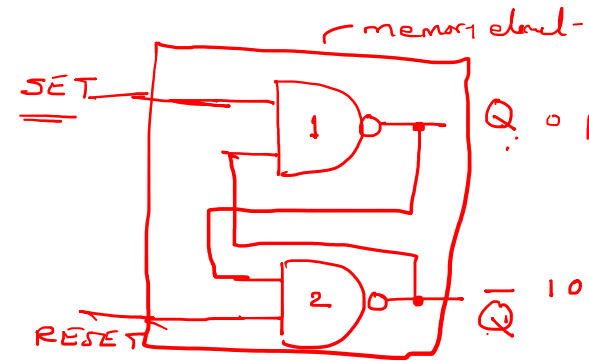
Q(t-1)	Q(t)	Q'(t)
0	1	1
1	1	1
0	1	0
1	1	0
0	0	1
1	0	1
0	0	1
1	1	0

Retained / No change



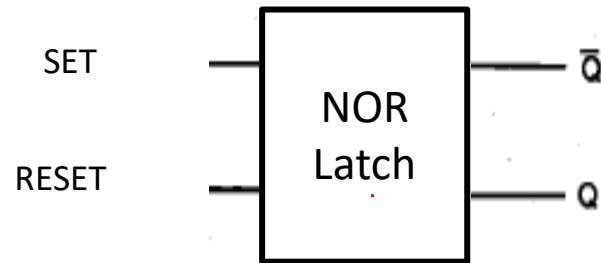
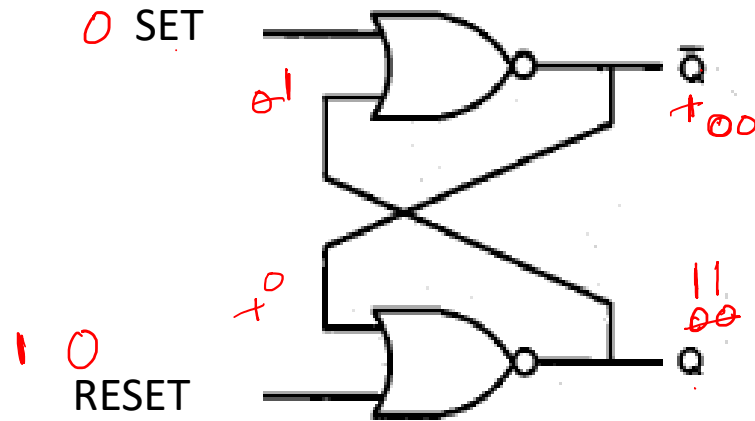
$Q(t+1) = 1$
 $Q(t+1) = 0$
 $Q(t+1) = Q(t)$

Function table		
SET	RESET	Output
0	0	Invalid state Indeterminate state
0	1	Set $Q=1$
1	0	Reset $Q=0$
1	1	No Change



If $Q=1$ we say Latch is in set condition
 If $Q=0$ we say Latch is in reset condition

NOR Latch (Active high Latch)



$Q(t-1)$ $Q(t)$ $Q'(t)$

SET	RESET	$Q(t)$	$Q(t+1)$	$Q'(t+1)$
0	0	0	0	1
0	0	1	1	0
0	1	0	0	1
0	1	1	0	1
1	0	0	1	0
1	0	1	1	0
1	1	0	0	0
1	1	1	0	0

Handwritten notes on the table: 'Retains previous output' for (0,0) to (0,1); 'Reset' for (0,1) to (1,0); 'Sets' for (1,0) to (1,1); 'Don't use this' for (1,1).

Same table

$Q(t-1)$	$Q(t)$	$Q'(t)$
0	0	1
1	1	0
0	0	1
1	0	1
0	1	0
1	1	0
0	0	0
1	0	0

Function table		
SET	RESET	Output
0	0	No Change <i>in state</i>
0	<u>1</u>	Reset <i>Resets</i>
<u>1</u>	0	Set <i>→ 1</i>
1	1	Indeterminate <i>Invalid state</i>

$$Q(t+1) = Q(t)$$

$$\rightarrow 0 \quad Q(t+1) = 0$$

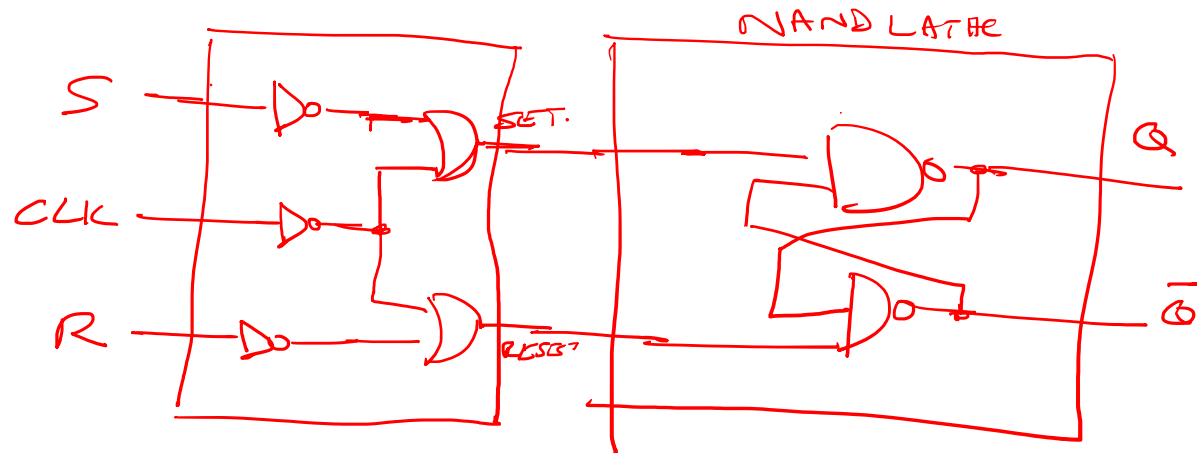
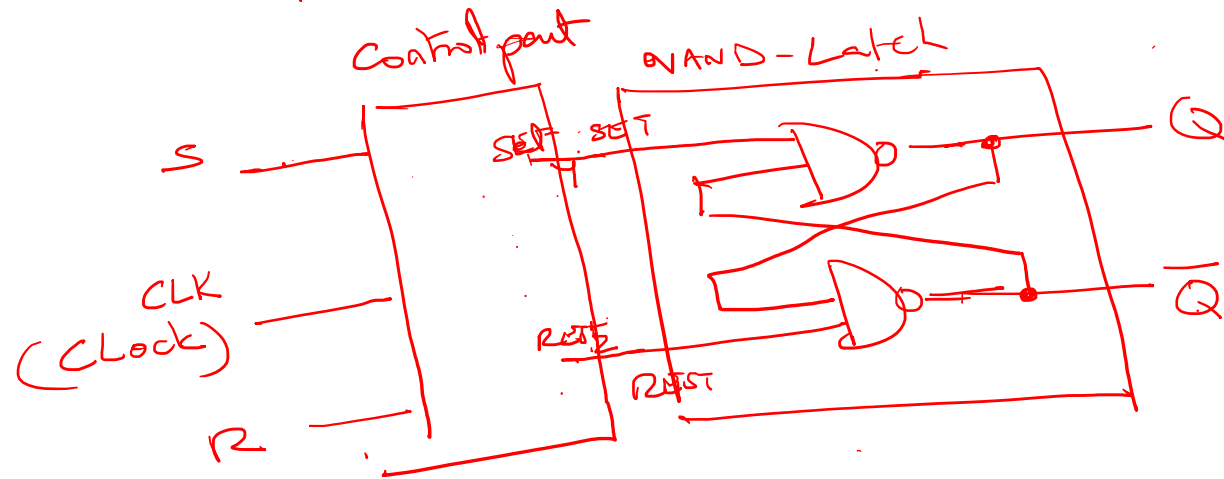
$$\rightarrow 1 \quad Q(t+1) = 1$$

$$\text{Invalid state } Q(t+1) = \text{X} \quad \text{Don't use}$$

SR Flip Flop using NAND latch

Flip-Flop is a 1-bit storing circuit employs a basic latch and a control input-clk.

Active High Flip-Flop

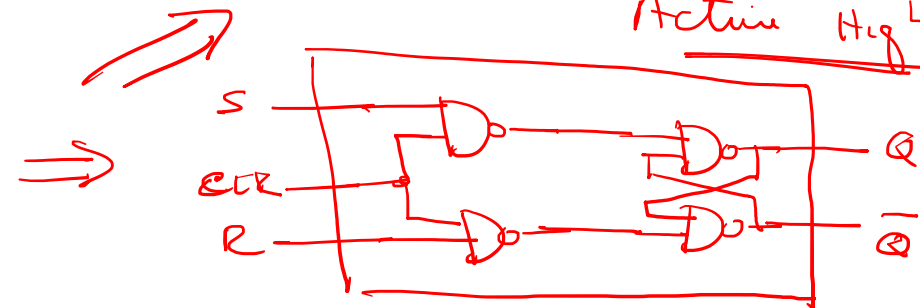


Requirements for SR flipflop

Clk	S	R	Output	$Q(t+1)$ $\bar{Q}(t+1)$
0	x	x	No change	$Q(t+1) = Q(t)$
1	0	0	No change	$Q(t+1) = Q(t)$
1	0	1	<u>Reset</u>	$Q(t+1) = 0$
1	1	0	Set	$Q(t+1) = 1$
1	1	1	Indeterminate	X X

level trigger

Active High latch



SR Flip Flop using NAND latch

Function Table <i>for SR flip flop</i>			
Clk	S	R	Output
0	X	X	No Change
1	0	0	No Change
1	0	1	Reset
1	1	0	Set
1	1	1	Indeterminate

clk →

0 →

0

0

0

1

1

1

1

Excitation Table

Clk	S	R	Q(t)	Q(t+1)	SET	RESET
0	0	0	0 → 0	0	1	X
0	0	0	1 → 1	1	X	1
0	0	1	0 → 0	0	1	X
0	0	1	1 → 1	1	X	1
0	1	0	0 → 0	0	1	X
0	1	0	1 → 1	1	X	1
0	1	1	0 → 0	0	1	X
0	1	1	1 → 1	1	X	1
1	0	0	0 → 0	0	1	X
1	0	0	1 → 1	1	X	1
1	0	1	0 → 0	0	1	X
1	0	1	1 → 0	0	1	0
1	1	0	0 → 1	1	0	1
1	1	0	1 → 1	1	X	1
1	1	1	0 → X	X	X	X
1	1	1	1 → X	X	X	X

Equation for SET and RESET

SET

Q	S	R	Q
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

$CLK + \bar{S} = SET = CLK \cdot S$

$RESET = CLK + \bar{R} = CLK \cdot R$

RESET

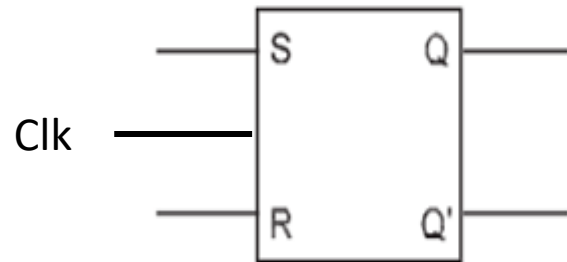
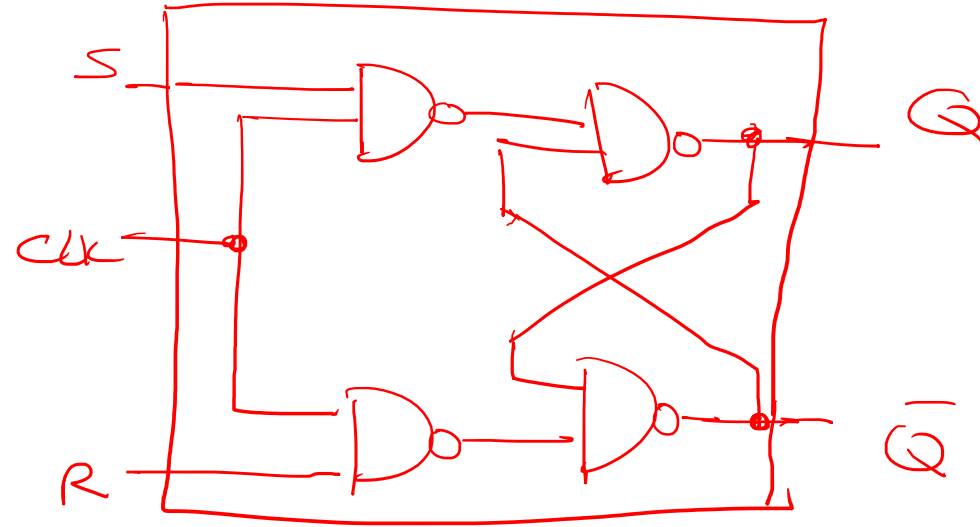
Q	S	R	Q
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

$SET = CLK + \bar{S} = CLK \cdot S$

$RESET = CLK + \bar{R} = CLK \cdot R$

Circuit:

clk	S	R	$Q(t+1)$	$\bar{Q}(t+1)$
0	X	X	No change	
1	0	0	No change $Q(t)$ $\bar{Q}(t)$	
1	0	1	0	1
1	1	0	1	0
1	1	1	Indeterminate	



Active high SR flipflop