



# MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

## COURSE PLAN

Department	:	Information and Communication Technology			
Course Name & code	:	Digital Systems and Computer Organization & ICT 2171			
Semester & branch	:	III & CCE			
Name of the faculty	:	Mrs. Divya S.			
No of contact hours/week:		L	T	P	C
		3	1	0	4

## Course Outcomes (COs)

*At the end of this course, the student should be able to:*

		No. of Contact Hours	Marks
C01:	Identify the applications of various elements of digital system abstractions.	5	10
C02:	Design MSI combinational logic circuits using typical TTL integrated circuit components.	17	36
C03:	Device applications employing sequential logic circuits.	10	21
C04:	Distinguish operations of control unit, execution unit and I/O in computer organization.	16	33
C05:			
Total		48	100



### Assessment Plan

Components	Assignments	Sessional Tests	End Semester/ Make-up Examination
Duration	20 to 30 minutes	60 minutes	180 minutes
Weightage	20 % (4 X 5 marks)	30 % (2 X 15 Marks)	50 % (1 X 50 Marks)
Typology of Questions	Understanding/ Comprehension; Application; Analysis; Synthesis; Evaluation	Knowledge/ Recall; Understanding/ Comprehension; Application	Understanding/ Comprehension; Application; Analysis; Synthesis; Evaluation
Pattern	Answer one randomly selected question from the problem sheet (Students can refer their class notes)	MCQ: 10 questions (0.5 marks) Short Answers: 5 questions (2 marks)	Answer all 5 full questions of 10 marks each. Each question may have 2 to 3 parts of 3/4/5/6/7 marks
Schedule	4, 7, 10, and 13 <sup>th</sup> week of academic calendar	Calendared activity	Calendared activity
Topics Covered	Quiz 1 (L 1-8 & T 1-2 ) (CO1,2)	Test 1 (L 1-15 & T 1-5 ) (CO1,2)	Comprehensive examination covering full syllabus. Students are expected to answer all questions (CO1-4)
	Quiz 2 (L 9-16 & T 3-5 ) (CO2)		
	Quiz 3 (L 17-24 & T 6-8 ) (CO2,3)	Test 2 (L 16-30 & T 6-10 ) (CO2,3,4)	
	Quiz 4 (L 25-32 & T 9-10 ) (CO3,4)		

### Lesson Plan

L. No.	Topics	Course Outcome Addressed
L0	Introduction to the course Introduction to digital systems, Basic theorems and properties, truth table, Boolean functions, canonical and standard forms	CO1
L1	Introduction to digital systems, Basic theorems and properties, truth table, Boolean functions, canonical and standard forms	CO1
L2	The map method: 2 variables, 3 variables, 4 variables.	CO1
L3	Simplification into POS and SOP expressions using K-map, and implementation using NAND and NOR gates( upto 4 variables).	CO1
T1	Simplification into POS and SOP expressions using K-map, and implementation using NAND and NOR gates ( upto 4 variables).	CO1
L4	Simplification into POS and SOP expressions using K-map for Don't care conditions, and implementation using NAND and NOR gates( upto 4 variables).	CO1
L5	Design of Half adder, Full adder, Parallel Adder(7483).	CO2
L6	Design of half subtractor, full subtractor, Parallel subtractor (using 7483), Parallel Adder/ Subtractor.	CO2
T2	Design of one digit and two digit BCD adder	CO2
L7	Design of 4 bit Carry Look Ahead Adder	CO2



<b>L8</b>	Design of 4 bit Carry Save Adder	CO2
<b>L9</b>	Design of Code converters and implementation using NAND and NOR gates.	CO2
<b>T3</b>	Design questions on combinational Circuits using IC 7483, IC 74283	CO2
<b>L10</b>	Design of binary multipliers using half adder and full adders, Design of multiplier using 74283 IC.	CO2
<b>L11</b>	Design of magnitude comparators	CO2
<b>L12</b>	Design of Decoders with and without enable i/p. Design of high order decoders using low order decoders.	CO2
<b>T4</b>	Combinational Circuit design using decoder IC74138	CO2
<b>L13</b>	Design of encoders, priority encoders.	CO2
<b>L14</b>	Design of cascading magnitude comparators, IC 7485 applications.	CO2
<b>L15</b>	Design of multiplexers with and without enable i/p. Higher order mux using lower order mux.	CO2
<b>T5</b>	Design of combinational circuits using MUX.	CO2
<b>L16</b>	Design of combinational circuits using 74151 IC and 74153 IC, 74157 IC's.	CO2
<b>L17</b>	Combinational shifter design using MUX. Design of De Multiplexers.	CO2
<b>L18</b>	NAND latch, NOR latch, SR flip flop, D FF. Excitation and characteristic equation of every FF.	CO3
<b>T6</b>	SR flip flop, D FF. Excitation and characteristic equation of every FF, JK FF AND T FF	CO3
<b>L19</b>	Flip Flop Conversion, Race around condition and solution.	CO3
<b>L20</b>	Asynchronous counter design	CO3
<b>L21</b>	Asynchronous counter design using IC 7490 and IC 7493	CO3
<b>T7</b>	Synchronous counter design	CO3
<b>L22</b>	Synchronous counter design using 74193 IC	CO3
<b>L23</b>	Synchronous counter design	CO3
<b>L24</b>	Shift registers, sequence generators.	CO3
<b>T8</b>	Applications of sequential circuit ex: Sequence detectors.	CO3
<b>L25</b>	Introduction to computer organization, Von – Neumann architecture.	CO4
<b>L26</b>	Arithmetic and logic unit design.	CO4
<b>L27</b>	Multiplication algorithms.	CO4
<b>T9</b>	Related Problems	CO4
<b>L28</b>	Division algorithms.	CO4



<b>L29</b>	Related Problems.	CO4
<b>L30</b>	Control Unit: Introduction, basic concepts	CO4
<b>T10</b>	Design methods: Hardwired approach.	CO4
<b>L31</b>	Hardwired approach	CO4
<b>L32</b>	Micro- programming	CO4
<b>L33</b>	Micro – programming	CO4
<b>T11</b>	Memory Unit: Types of memory and characteristics, memory hierarchy.	CO4
<b>L34</b>	Cache memory mapping	CO4
<b>L35</b>	Input and Output: I/O subsystem	CO4
<b>L36</b>	Programmed I/O, Interrupt I/O	CO4
<b>T12</b>	Direct memory access, I/O bus standards	CO4

#### References:

1. M. Morris Mano: "Digital Design", Prentice Hall India, 3rd edition, 2002.
2. Ronald J. Tocci, Neal S. Widmer and Gregory L. Moss: "Digital Systems: Principles and Applications", Pearson Education India, 12th Edition, 2017.
3. Mohamed Rafiquzzaman and Rajan Chandra, "Modern Computer Architecture", Galgotia publications Pvt Ltd, 3rd edition, 2015
- 4.
- 5.
- 6.
- 7.

Submitted by: **MRS. DIVYA S.**



(Signature of the faculty)

Date:

26/7/2019

Approved by: DR. BALACHANDRA

(Signature of HOD)

Date:

27/7/19

Dr. Balachandra  
Professor & Head  
Dept. of Information &  
Communication Technology  
M.I.T., Manipal - 576 104

FACULTY MEMBERS TEACHING THE COURSE (IF MULTIPLE SECTIONS EXIST):

FACULTY	SECTION	FACULTY	SECTION
Mrs. Rashmi N.R.	A	Mrs. Divya S.	B

\*\*\*\*\*



Handwritten signature or name

Handwritten text, possibly a date or initials