III SEMESTER B.TECH. INTERNAL EXAMINATIONS OCTOBER 2020

MID TERM TEST

SUBJECT: COMPUTER ORGANIZATION AND ARCHITECTURE [CSE 2151]

Date of Exam: **20/10/2020** Time of Exam: **8 AM – 9.45 AM** Max. Marks: 20

Instructions to Candidates:

1) Answer ALL the questions.
2) Students have to write their answers in their own handwriting on white sheets.
*3) **On the top of answer sheet, mandatorily student should write name, sem, Reg no., Course name, and student signature.***
4) Pages scanned should be included in a single file before uploading.

1. A system with a word length of 32-bit and byte-addressable memory has ten consecutive 32-bit signed numbers stored starting from memory location NUM. Write a RISC-style program to count the number of positive numbers in it and store the count in location COUNT. **2M**

2. Tabulate the 2s complement representations for all negative integers representable using 5 bits. **2M**

3. Write two features of horizontal and vertical microinstruction. Show how seven control signals C0, C1, ….C6 can be specified in **2M**
i) Unencoded format
ii) Fully encoded format

4. Consider a 12-bit, floating-point number in a format similar to IEEE format with a 5-bit exponent and a 6-bit mantissa fraction. The base of the scale factor is 2 and the exponent is the biased exponent. Consider the two floating point numbers represented in this format as shown below. **3M**

A = 0 10001 011100
B = 0 01111 100000

i) Convert them to binary numbers to multiply them.
ii) Normalize the product and represent it in the above format.
iii) Round the final result obtained from 6 bits to 4 bits in the fraction part using
a. Van Neumann rounding
b.. Rounding Procedure

5. i) Represent the following numbers in IEEE single precision floating point format: a) -0 b) $+\infty$ **1M**
ii) Perform the following arithmetic operation using the rules for arithmetic operations in IEEE single precision format: **2M**
-116.5 – (+211.75)

6. Consider the register transfer description algorithm given below. **4M**

```
Declare registers A[4], M[4], Q[4], L[3], C[1]
Declare buses inbus[4], outbus[4]
Start:  A←0, C←0, M←inbus, L←4;
        Q←inbus
Loop:   if Q[0]= 1, then go to ADD
        Go to Rshift;
ADD:    A←A+M;
Rshift: LSR(C$A$Q)
        L←L-1;
        if L>0, then go to Loop
        outbus ←A;
        outbus←Q ;
Halt:   Go to Halt
```

Draw the complete processing section diagram for implementing the given algorithm, indicating all the control points, inputs and outputs. List out the control points and the operation performed

7. Consider the following decimal numbers A=28 and B=11 **4M**

i) Represent the two numbers in binary using minimum number of bits required for implementing the restoring division technique.
ii) Perform the division of A by B using restoring division technique. Show the sequence of steps.
iii) Write the result in binary and decimal notation.
iv) What would be the quotient and the remainder in decimal notation if A = 28 and B = -11 , if A = -28 and B = -11