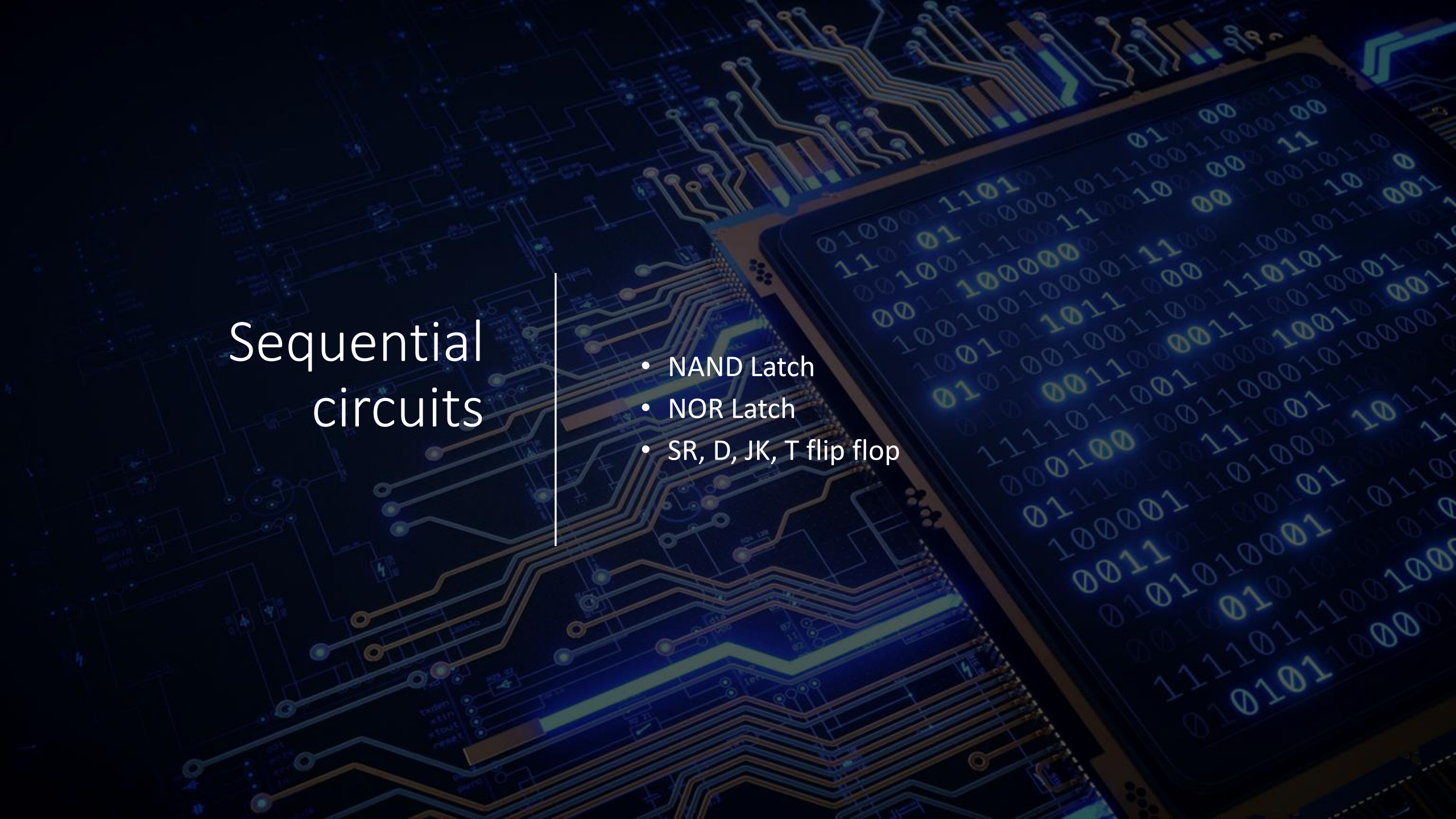
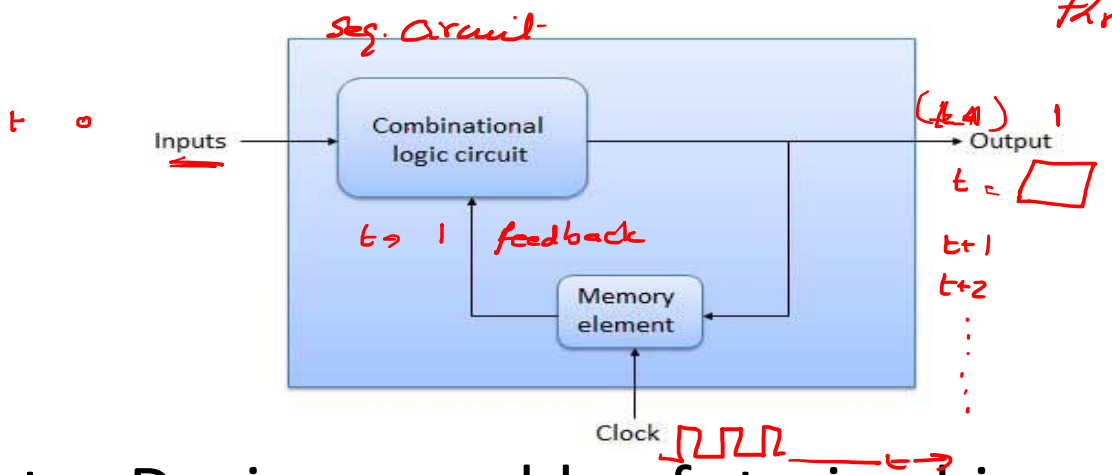


Sequential circuits

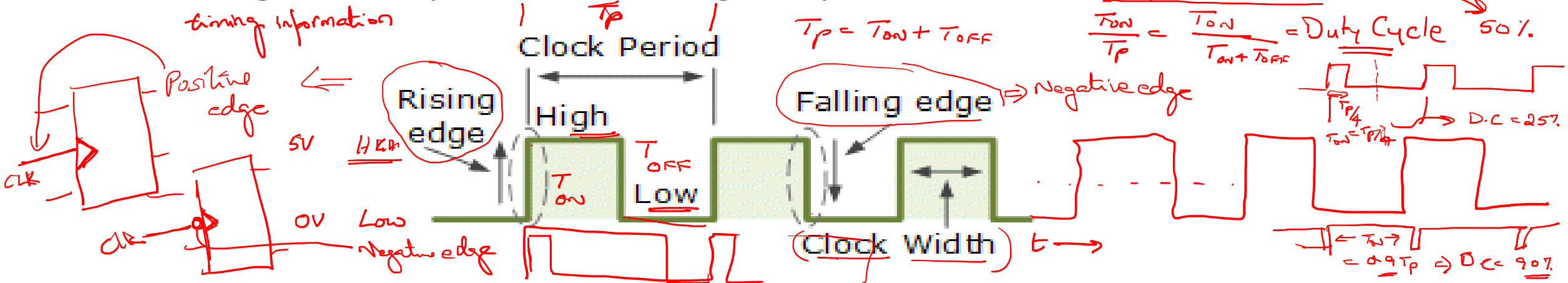
- NAND Latch
- NOR Latch
- SR, D, JK, T flip flop

Sequential circuits:

- Outputs are dependent on current inputs and previous outputs.

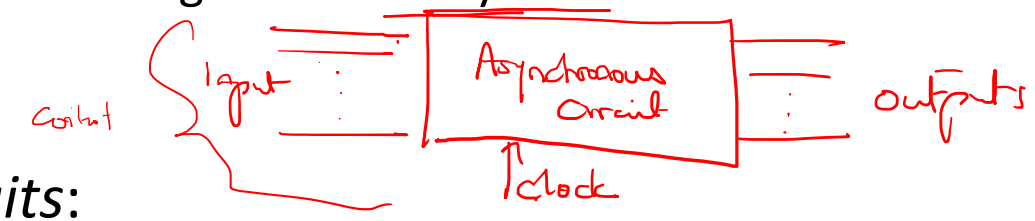


- Storage elements : Devices capable of storing binary information
- Clock Signal: Is a periodic rectangular pulse train or a square wave.



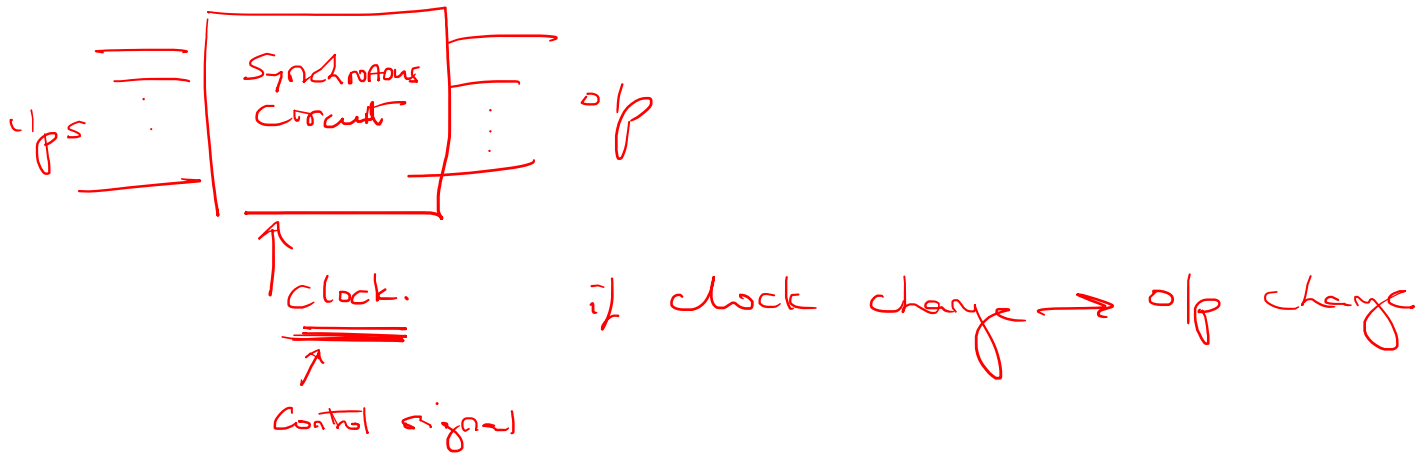
- Two types of sequential circuits:
  - *Asynchronous sequential circuits*:

    The output of the logic circuits can change state at any time when one or more of the inputs change.

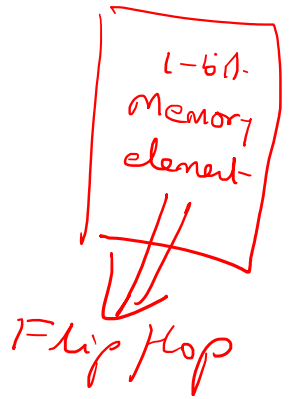


  - *Synchronous sequential circuits*:

    The exact times at which any output can change states are determined by a signal called the clock.



- Flip Flop:
  - Is a binary storage element capable of storing one bit of information

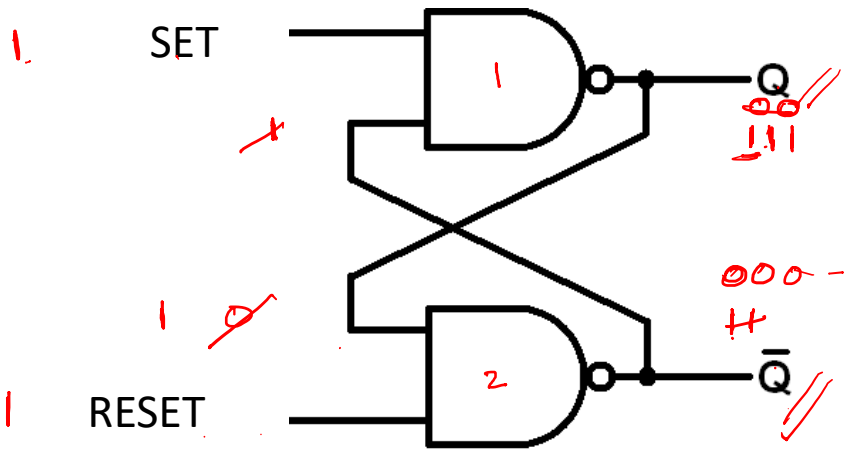


- Latch: basic circuit within flip flop
  - Basic type of flip flop is referred as Latch

(Latch + control) = flip flop

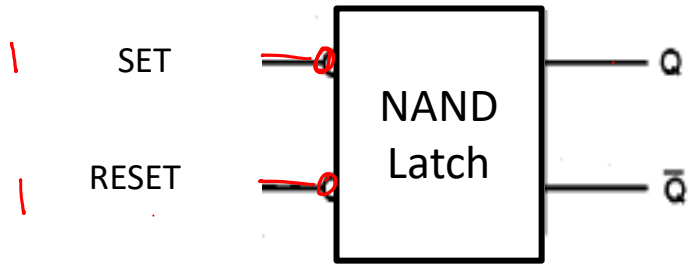
In latches : circuit is built using NAND or NOR gates.

NAND Latch (Active Low latch)

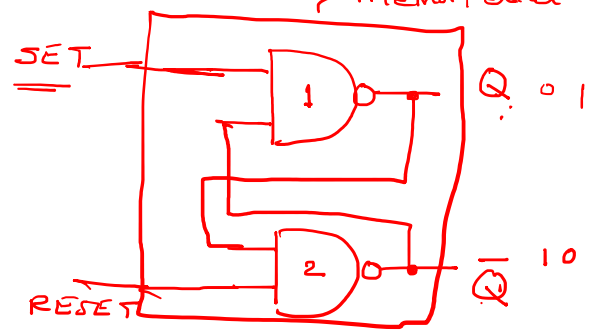


SET	RESET	Q(t)	Q(t+1)	Q'(t+1)
0	0	0	1	1
0	0	1	1	1
0	1	0	1	0
0	1	1	1	0
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

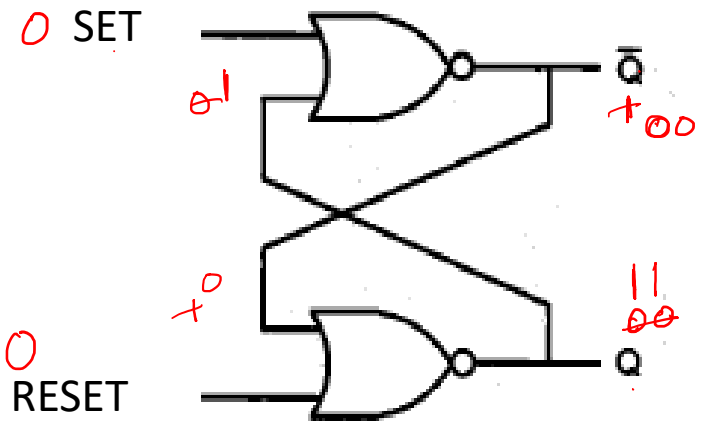
Q(t-1)	Q(t)	Q'(t)
0	1	1
1	1	1
0	1	0
1	1	0
0	0	1
1	0	1
0	0	1
1	1	0

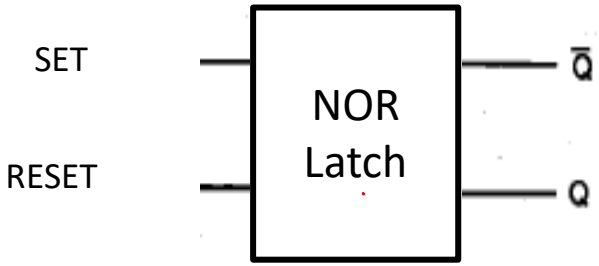


Function table		
SET	RESET	Output
0	0	Indeterminate state
0	1	Set
1	0	Reset
1	1	No Change



NOR Latch (Active high Latch)





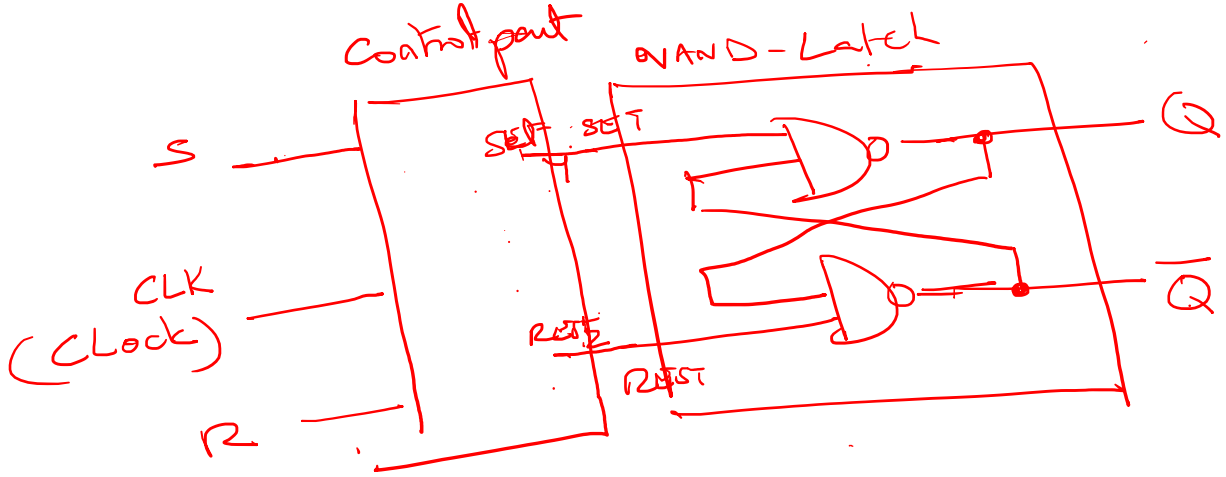
SET	RESET	Q(t)	Q(t+1)	Q'(t+1)
0	0	0	0	1
0	0	1	1	0
0	1	0	0	1
0	1	1	0	1
1	0	0	1	0
1	0	1	1	0
1	1	0	0	0
1	1	1	0	0

Q(t-1)	Q(t)	Q'(t)
0	0	1
1	1	0
0	0	1
1	0	1
0	1	0
1	1	0
0	0	0
1	0	0

Function table		
SET	RESET	Output
0	0	No Change
0	1	Reset
1	0	Set
1	1	Indeterminate

SR Flip Flop using NAND latch

Flip-Flop is a 1-bit storing circuit employs a basic latch and a control input ckt.

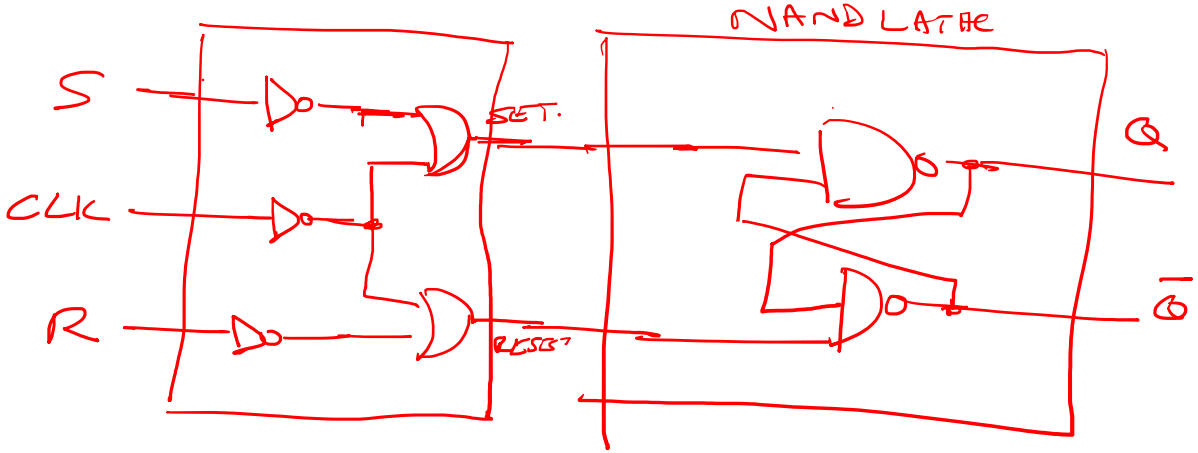


Active High Flip-flop

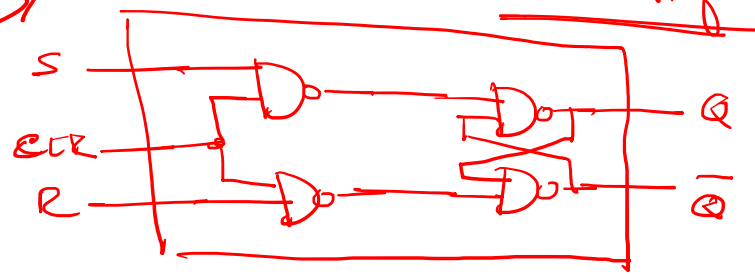
Requirements for SR flipflop

Clk	S	R	output	$Q_{(t+1)}$ $\bar{Q}_{(t+1)}$
0	x	x	No change	$Q_{(t+1)} = Q_{(t)}$
1	0	0	No change	$Q_{(t+1)} = Q_{(t)}$
1	0	1	Reset	$Q_{(t+1)} = 0$
1	1	0	Set	$Q_{(t+1)} = 1$
1	1	1	Indeterminate	X X

level trigger



Active High level latch

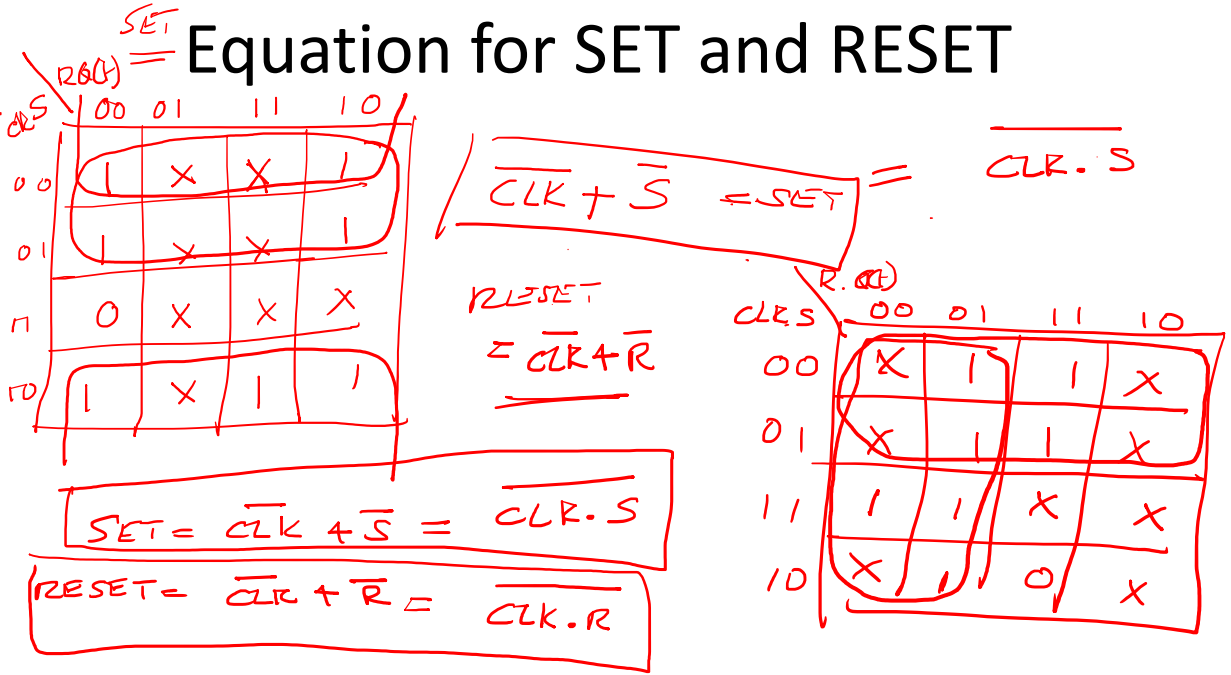


SR Flip Flop using NAND latch

Function Table for SR flip flop			
Clk	S	R	Output
0	X	X	No Change
1	0	0	No Change
1	0	1	Reset
1	1	0	Set
1	1	1	Indeterminate

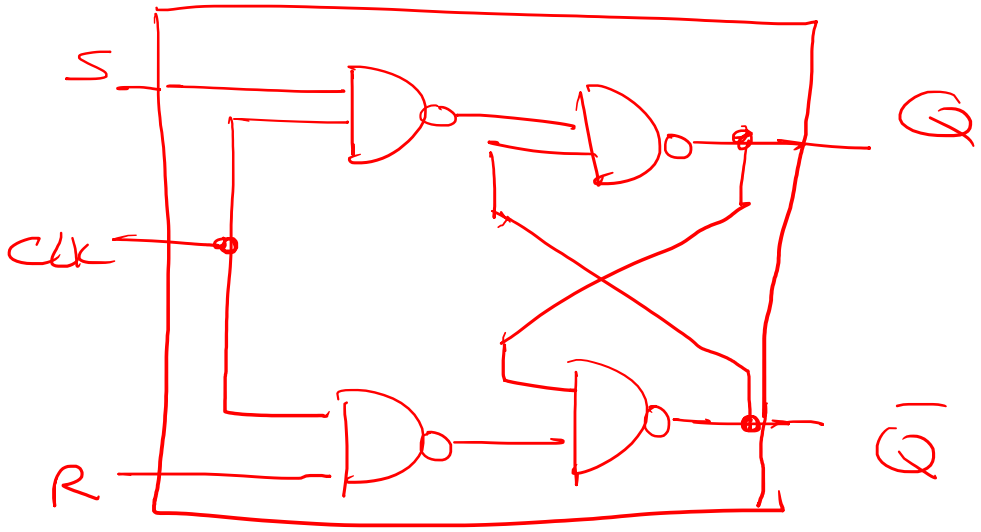
Excitation Table						
Clk	S	R	Q(t)	Q(t+1)	SET	RESET
0	0	0	0	0	1	X
0	0	0	1	1	X	1
0	0	1	0	0	1	X
0	0	1	1	1	X	1
0	1	0	0	0	1	X
0	1	0	1	1	X	1
0	1	1	0	0	1	X
0	1	1	1	1	X	1
1	0	0	0	0	1	X
1	0	0	1	1	X	1
1	0	1	0	0	1	X
1	0	1	1	0	1	0
1	1	0	0	1	0	1
1	1	0	1	1	X	1
1	1	1	0	X	X	X
1	1	1	1	X	X	X

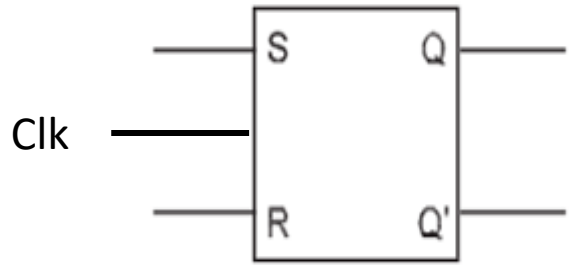
Equation for SET and RESET



Circuit:

Clk	S	R	Q(t+1)	$\bar{Q}(t+1)$
0	X	X	No change	
1	0	0	No change Q(t)	$\bar{Q}(t)$
1	0	1	0	1
1	1	0	1	0
1	1	1	Indeterminate	





Active high SR flipflop