DECODERS AND ENCODERS CONTD

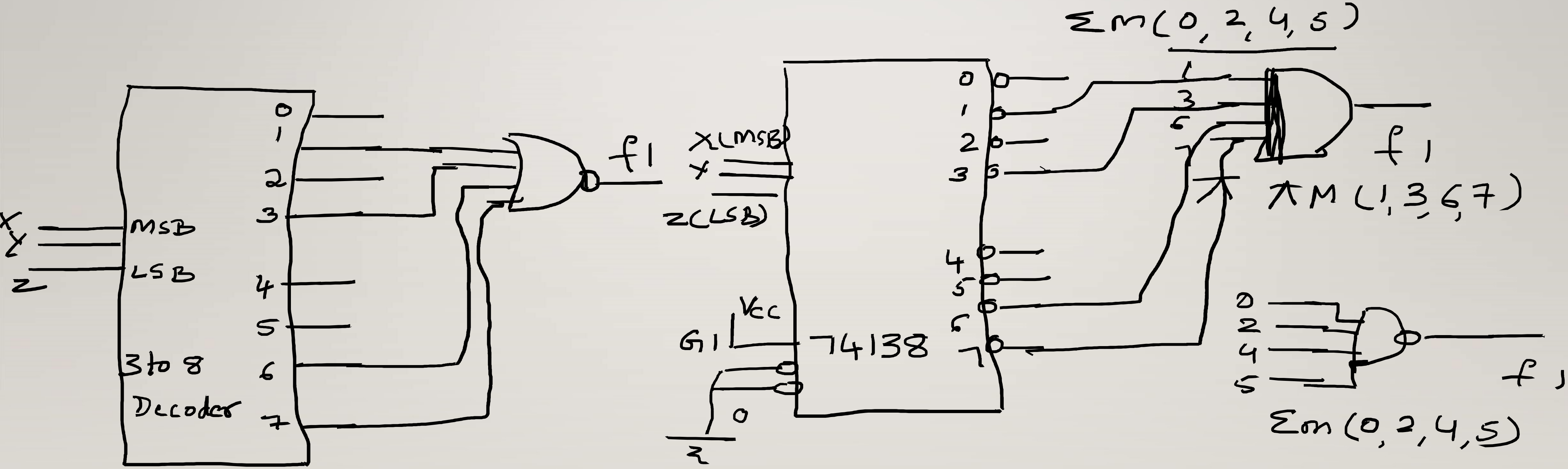
STUDENTS ARE ADVISED TO WRITE DOWN THE NOTES FOR EVERY LECTURE

NOV. 2ND 2021(10.30 AM TO 12.30 PM)

Realize f1(x,y,z) = ΠM(1,3,6,7) using $= \Sigma m(0,2,4,5) \Rightarrow OR$

a. 3-to-8 line decoder with active high output and suitable gates

b. 74138 decoder and suitable gates


x
y
z
MSB
LSB
3to 8
Decoder
0
1
2
3
4
5
6
7
f1
X(MSB)
Y
Z(LSB)
Vcc
G1
0
Z
74138
0
1
2
3
4
5
6
7
Σm(0, 2, 4, 5)
1
3
6
7
f1
ΠM (1,3,6,7)
0
2
4
5
f1
Σm (0,2,4,5)

Design a code converter to convert a decimal digit represented in 84-2-1 code to a decimal digit represented in excess-3 code using 74138 decoder and external gates..

→ complete the truthtable

84-2-1					Excess-3			
A	B	C	D		e3	e2	e1	e0
0	0	0	0	0	0	0	1	1
0	1	1	1	7	0	1	0	0
0	1	1	0	6	0	1	0	1
0	1	0	1	5	0	1	1	0
0	1	0	0	4	0	1	1	1
1	0	1	1	11	1	0	0	0
1	0	1	0	10	1	0	0	1
1	0	0	1	9	1	0	1	0
1	0	0	0	8	1	0	1	1
1	1	1	1	15	1	1	0	0

$e_3 = A$

$e_3 = \Sigma m(\overset{8,9,10,11,15}{\cancel{0,1,2,3,4}}) = \pi M(\quad 5 \text{ terms})$

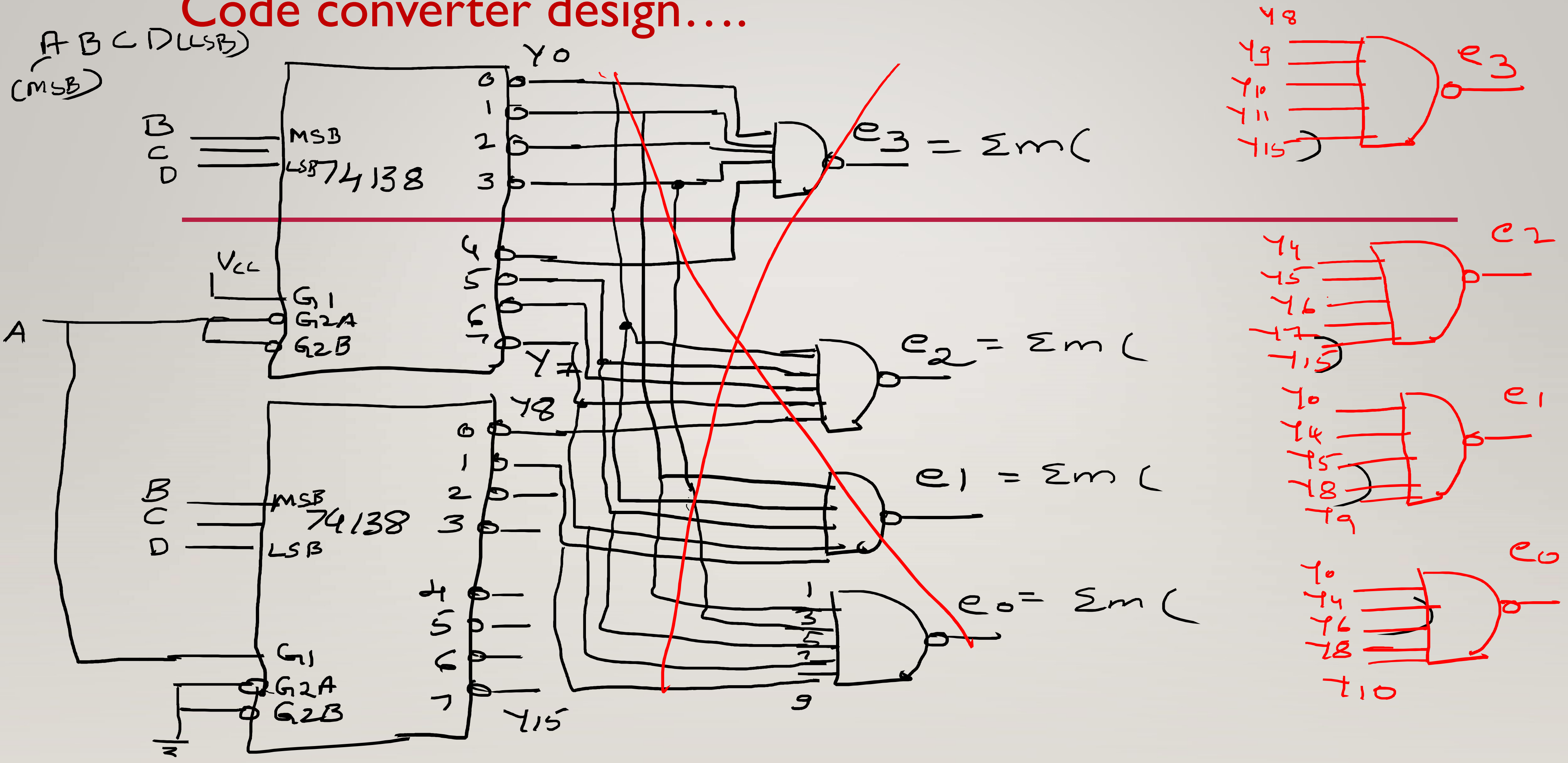
$e_2 = \Sigma m(\overset{4,5,6,7,15}{\cancel{0,5,6,7,8}}) = B$

$e_1 = \Sigma m(\overset{0,4,5,8,9}{\cancel{1,2,5,6,9}}) = \overline{C}$

$e_0 = \Sigma m(\underset{0,4,6,8,10}{\cancel{1,3,5,7,9}}) = \overline{D}$

$e_3(A, B, C, D)$

Code converter design….


A B C D(LSB)
(MSB)
B
C
D
MSB
LSB
74138
Y0
0
1
2
3
4
5
6
7
Y7
Vcc
G1
G2A
G2B
A
B
C
D
MSB
74138
LSB
Y8
0
1
2
3
4
5
6
7
Y15
G1
G2A
G2B
e3 = Σm(
e2 = Σm(
e1 = Σm(
e0 = Σm(
1
3
5
7
9
Y8
Y9
Y10
Y11
Y15
e3
Y4
Y5
Y6
Y7
Y15
e2
Y0
Y4
Y5
Y8
Y9
e1
Y0
Y4
Y6
Y8
Y10
e0

Code converter design…

Design f(x,y,z) = x' +y'z using 3-to-8 line decoder and external gates.

$f(\overset{\text{MSB}}{x},y,z) =$

assumed as active high o/p

Minterms for x' ($x=0$, $y=z=$ don't care) $= \Sigma m(0,1,2,3)$

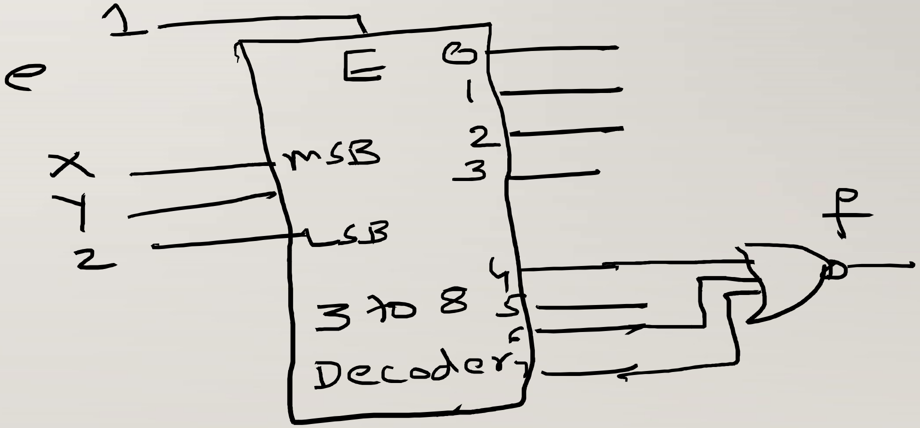
x	y	z
0	0	0
0	0	1
0	1	0
0	1	1

$\bar{y}z$ ($x=0$ or 1, $y=0$ & $z=1$) $= 1, 5$

001, 101

$f(x,y,z) = \bar{x} + \bar{y}z = \Sigma m(0,1,2,3,5) = \Pi M(4,6,7)$

Can also be written from truth table



1
E
x
y
z
MSB
LSB
0
1
2
3
4
5
6
7
3 to 8 Decoder
f

ENCODER:

- Combinational circuit that performs inverse operation of a decoder.
- Encoder has 2^n (or fewer) input lines and n output lines. Ex: 4-to-2 line, 8-to-3 line…etc
- 4-to-2 encoder is given below:

2^2 to 2

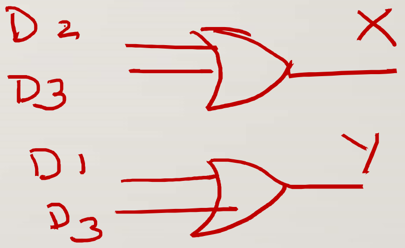
Truth table

Inputs				Outputs	
D_0	D_1	D_2	D_3	x	y
→ 1	0	0	0	0	0
0	1	0	0	0	1 ✓
0	0	1	0	1	0 ✓
0	0	0	1	1	1 ✓

$X = D_2 + D_3$

$Y = D_1 + D_3$

Circuit



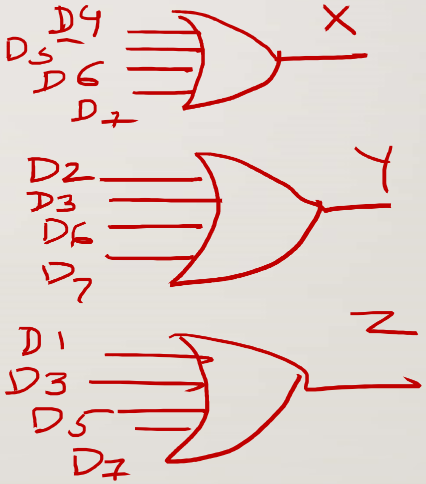
Write the truth table and circuit for 8-to-3 line encoder

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	X	Y	Z
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

$X = D_4 + D_5 + D_6 + D_7$

$Y = D_2 + D_3 + D_6 + D_7$

$Z = D_1 + D_3 + D_5 + D_7$


D4
D5
D6
D7
X
D2
D3
D6
D7
Y
D1
D3
D5
D7
Z

Design a 4 –to-2 line priority encoder

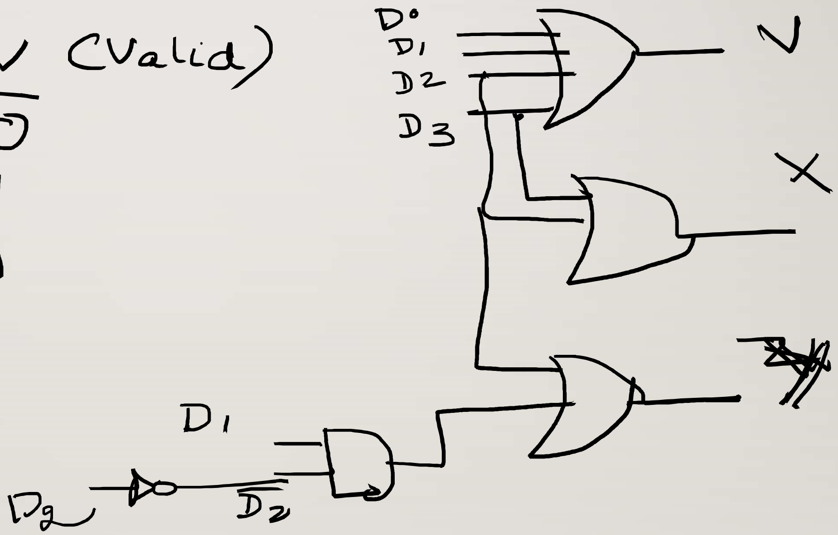
$D_0 < D_1 < D_2 < D_3$

D_0	D_1	D_2	D_3	X	Y	V (Valid)
0	0	0	0	⊗	⊗	0
1	0	0	0	0	0	1
✓ ϕ	1	0	0	0	1	1
✓ ϕ	ϕ	1	0	1	0	1
ϕ	ϕ	ϕ	1	1	1	1

$V = D_0 + D_1 + D_2 + D_3$

$X = D_3 + D_2\overline{D_3} = D_2 + D_3$

$Y = D_1\overline{D_2}\,\overline{D_3} + D_3 = D_3 + D_1\overline{D_2}$



D_0
D_1
D_2
D_3
V
X
Y
D_1
D_2
$\overline{D_2}$

4-to-2 line priority encoder contd…

- Any questions?