MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

III SEMESTER B.TECH. (CSE)

IN SEMESTER EXAMINATION

SUBJECT: COMPUTER ORGANIZATION AND ARCHITECTURE (CSE 2151)

Time:10.30AM- 12.00 NOON Date: 15/12/2021 MAX.MARKS: 20

Scheme of Evaluation Set3

1 Divide 125.125 by 16.25 by representing in IEEE 32-bit format. Show all the steps clearly and represent the final in both IEEE 32-bit format and decimal representation. 4

Step i: Convert 125.125 to binary representation **(0.5)**

1111101.001 →After normalizing 1.111101001×2^6

E'= 6+127=133 =10000101

In IEEE 32-bit format: A= 0 10000101 1111010010……

Step ii: Convert 16.25 to binary representation **(0.5)**

10000.01 →After normalizing $1.0000011 \text{ X } 2^4$

E'= 4+127=131 = 10000011

In IEEE 32-bit format: B= 0 10000011 00000110……

Step 1: subtract exponents and add 127 **(0.5)**

133-131+127=129 →10000001 (unsigned representation)

Step 2: Divide the mantissa **(1)**

```
                1.1 1 1 1_____________
1.000001 | 1.1 1 1 1 0 1 0 0 1
           1.0 0 0 0 0 1
             1 1 1 1 0 0 0
             1 0 0 0 0 0 1
               1 1 0 1 1 1 0
               1 0 0 0 0 0 1
                 1 0 1 1 0 1 1
                 1 0 0 0 0 0 1
                     1 1 0 1 0
```

1.111101001 ÷ 1.0000011 = 1.111 **(0.5)**

The result is already normalized.

The result in IEEE 32-bit format: 0 10000001 11100000000……. **(0.5)**

Decimal format: 7 **(0.5)**

Step i: Convert 125.125 to binary representation **(0.5)**

1111101.001 →After normalizing 1.111101001×2^6

E'= 6+127=133 =10000101

In IEEE 32-bit format: A= 0 10000101 1111010010……

Step ii: Convert 16.25 to binary representation **(0.5)**

10000.01 →After normalizing 1.0000011 X 2^4

E'= 4+127=131 = 10000011

In IEEE 32-bit format: B= 0 10000011 00000110……

Step 1: subtract exponents and add 127 **(0.5)**

133-131+127=129 →10000001 (unsigned representation)

Step 2: Divide the mantissa **(1)**

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          1 0 0 0 0 0 1
            1 1 0 1 1 1 0
            1 0 0 0 0 0 1
              1 0 1 1 0 1 1
              1 0 0 0 0 0 1
                  1 1 0 1 0
```

1.111101001 ÷ 1.0000011 = 1.111 **(0.5)**

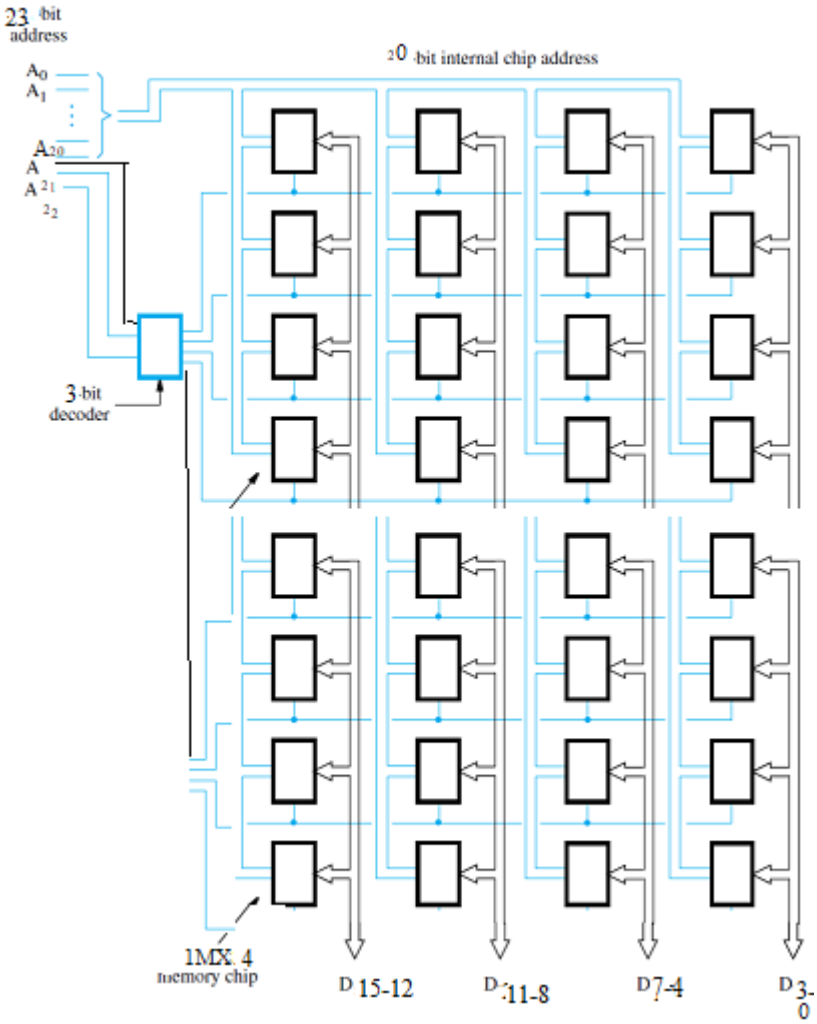
The result is already normalized.

The result in IEEE 32-bit format: 0 10000001 11100000000……. **(0.5)**

Decimal format: 7 **(0.5)**

2 A. Construct a large memory of capacity 8Mx16 using 1M x 4 chips. Draw the structure and indicate clearly, the number of address lines and the data lines in the diagram 3

1



Identifying correct number of rows and colums-> 0.5m
Identifying no. of address lines for Large memory-0.5M
Identifying no. of address lines for small memory-0.5M
Writing decoder with proper inputs and outputs-0.5M
Writing proper data lines : 0.5M
Overall diagram: 0.5M

B. Explain the difference between the two groups of microinstruction based on parallelism and the amount of encoding

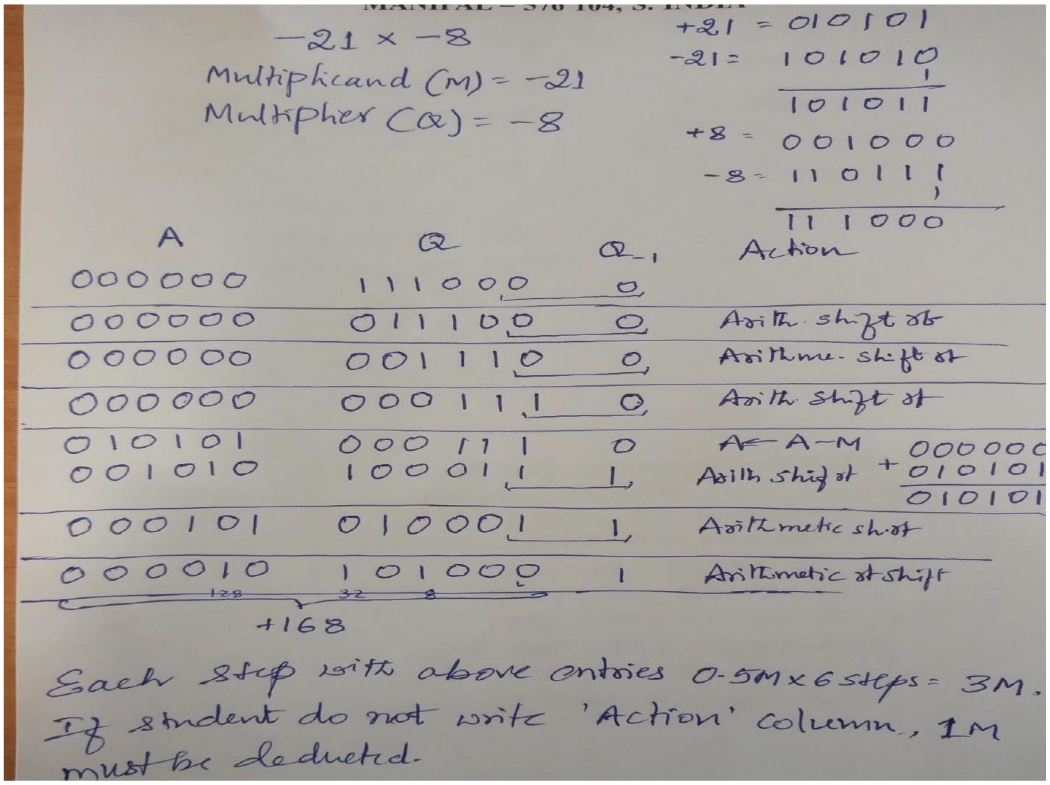
Vertical microinstruction

- Need considerable amount of decoding
- Short microinstruction
- Limited scope for expressing parallelism

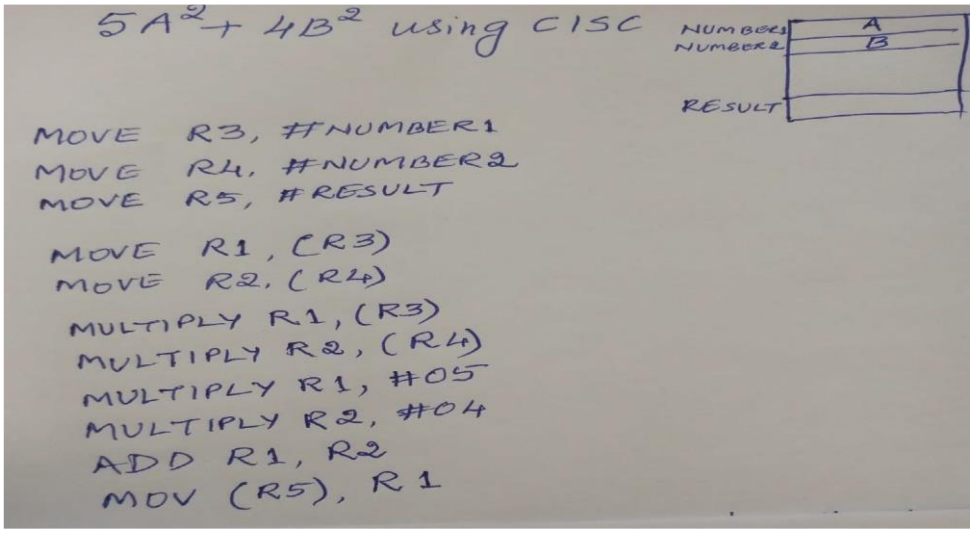
Horizontal microinstruction

- No decoding required
- Long microinstruction
- Capability of expressing a high degree of parallelism

3 Using Booth's algorithm for 2's complement multiplication, show how to multiply the multiplicand (-21) by the multiplier (-8). 3



4 Assume that an A and B are the two unsigned 8-bit numbers which are stored in consecutive memory locations NUMBER1 and NUMBER2. Write a CISC-style program to evaluate $5A^2 + 4B^2$ and store the result in memory location RESULT assuming that the result do not exceed 8-bit. Use memory pointers to access the data from / to memory. Assume that along with the other instructions, *Multiply* instruction is also defined in the instruction set. Given that the system memory is byte addressable. 3



1
1
1

5 Divide 28 by 5 using Restoring division method. Indicate all the steps clearly 3

28/5

A	Q	

00000	11100	Initial values M=00101 -M=11011
00001 11011 11100 00101 00001	11000 11000	Shift A,M to the left A=A-M Set Q0=0, Restore A I Cycle
00011 11011 11110 00101 00011	10000 10000	Shift A,M to the left A=A-M Set Q0=0, Restore A II Cycle
00111 11011 00010	00000 00001	Shift A,M to the left A=A-M Set Q0=1 III Cycle
00100 11011 11111 00101 00100	00010 00011	Shift A,M to the left A=A-M Set Q0=0, Restore A IV Cycle
01000 11011 00011	00100 00101	Shift A,M to the left A=A-M Set Q0=1 V Cycle
Remainder	Quotient	

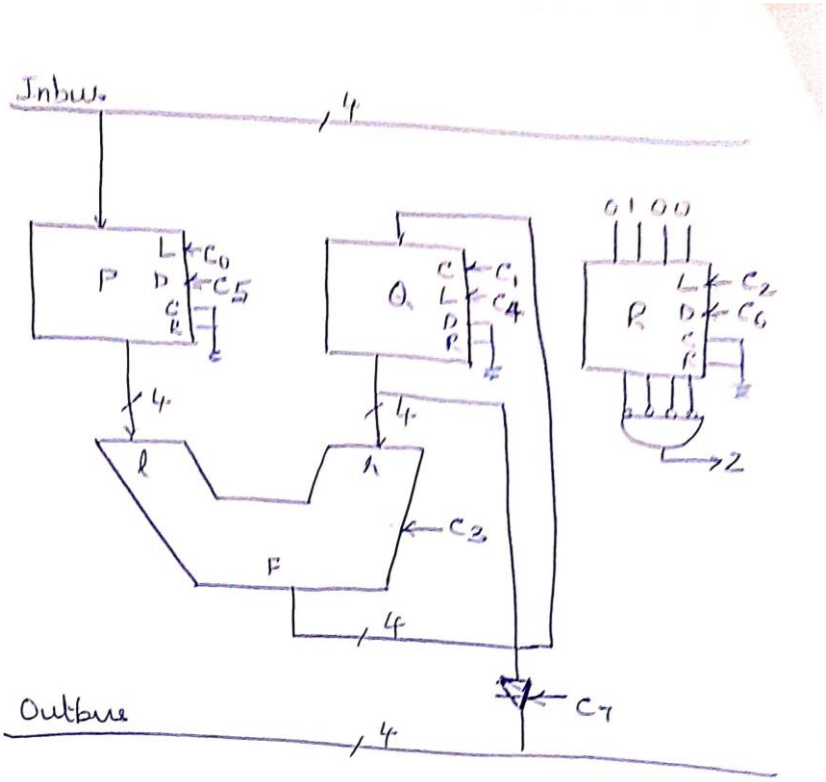
Each step : 0.5 X 5 = 2.5M
Indicating quotient and remainder 0.5M

6 Consider the Register Transfer Description given below: 3

Declare Registers P[4],Q[4],R[4]
Declare buses Inbus[4], Outbus[4]
Start: P←Inbus, Q←0, R←4;

Loop: Q←P+Q;
P←P-1
R←R-1;
If R<> 0 then go to Loop
Outbus = Q;
Halt: go to Halt

Design a neat processing section identifying all the control points



Writing 4 blocks: 0.5M
Showing width of data path and inputs: 0.5M
Identifying control signals and output:2M
For any mistake : 0.5M deducted