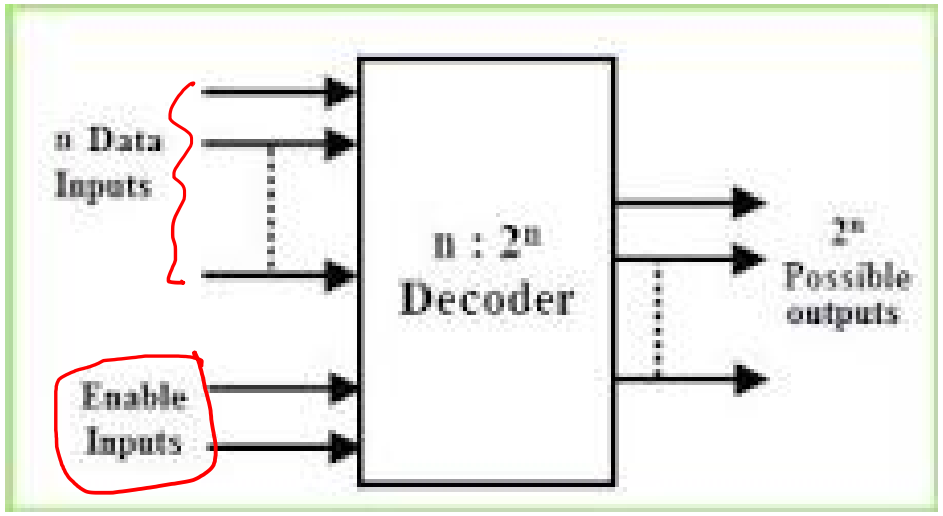
DECODERS AND ENCODERS

Students are advised to write down the notes for every lecture

Decoder:

- Decoder is a combinational circuit
- Converts a binary information from n-input lines to a maximum of 2^n unique output lines (n-to- 2^n line decoder) and one or more enable inputs.Ex: 2-to-4 line, 3-to-8 line..etc
- In standard decoders, only one output line will be active at a time corresponding to the input binary combination.



Ex: 2-bit

2 : 4 decoder

D_3	D_2	D_1	D_0
0	0	x	x	x	✓
0	1	x	x	✓	x
1	0	x	✓	x	x
1	1	✓	x	x	x

1 : 2 bit line

2 : 4 line

3 : 8

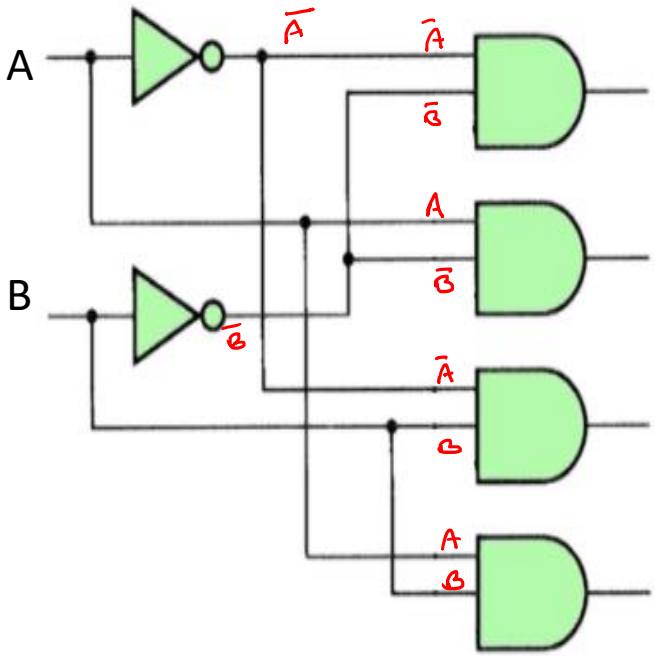
4 : 16 decoder

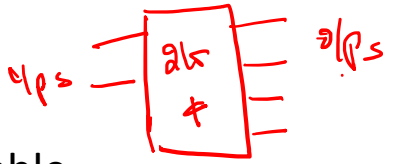
n bit : 2^n line decoder

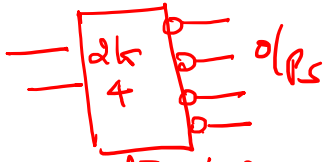
2-to-4 line decoder

Circuit Diagram

Truth table







NAND Gates at output array

B	A	D_3	D_2	D_1	D_0
0	0	1	1	1	0
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	1	1	1

M_3 M_2 M_1 M_0

Active low outputs

Truth table for Active HIGH o/p outputs

I/P B	I/P A	D_3	D_2	D_1	D_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

m_3 m_2 m_1 m_0

Active HIGH outputs

$\bar{B}\bar{A} = m_0$

$\bar{B}A$ m_1

$B\bar{A}$ m_2

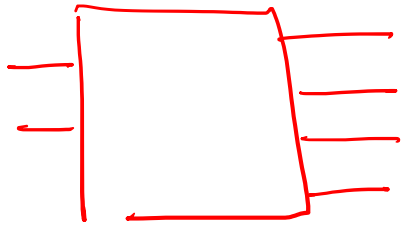
BA m_3

$\bar{A}\bar{B}$ $m_0 = M_0$

$m_1 = M_1$

$m_2 = M_2$

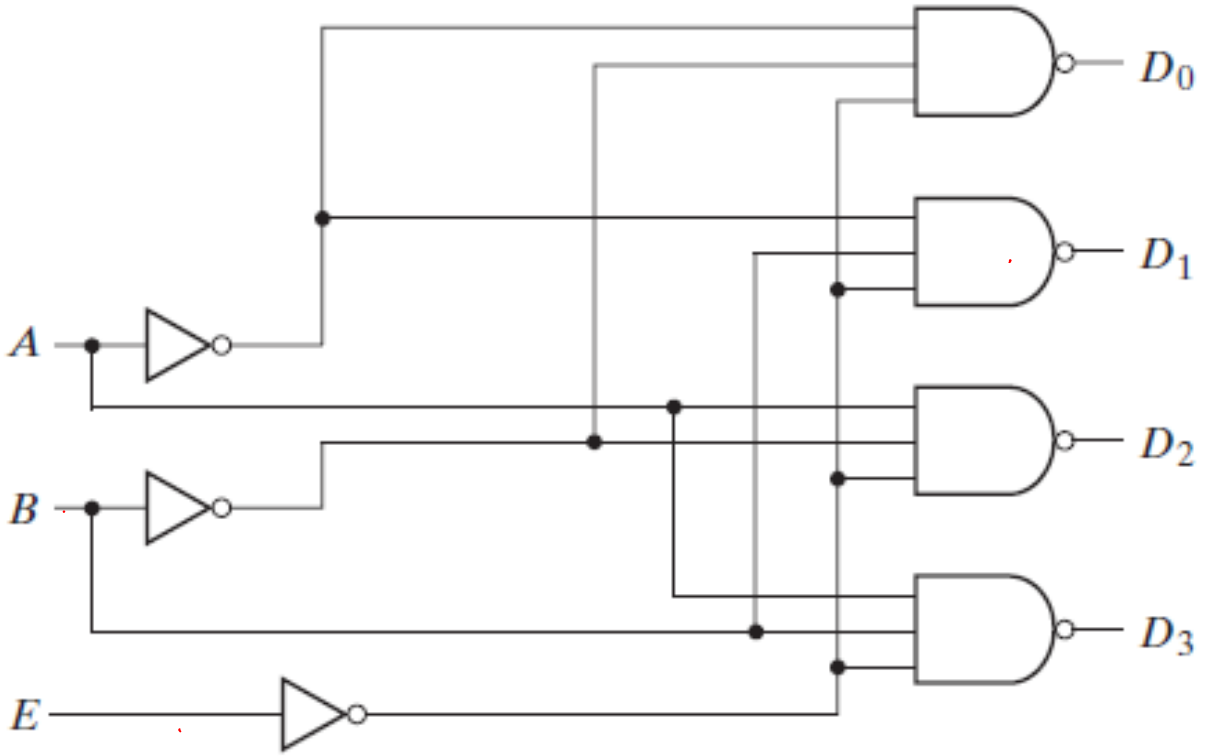
Note: $\overline{m_3} = M_3$



with outputs HIGH

Active HIGH output with NAND Gates at outputs → Active LOW o/ps

2-to-4 line decoder with active low output & enable input active low



(a) Logic diagram

E	A	B	D_0	D_1	D_2	D_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

(b) Truth table

Write the truth table ,logic diagram and block diagram of 3-to-8 line decoder

- Note: Unless specified, assume the output and enable input to be active low

Inputs				Outputs							
E	A	B	C	D0	D1	D2	D3	D4	D5	D6	D7
1	x	x	x	1	1	1	1	1	1	1	1
0	0	0	0	0	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1
0	1	1	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	0

Expressions for o/p variables

Question should arise and are

Q1. Are there any enable i/ps ?

Q2 If enables are there, then are they active low / active HIGH ?

Q3. Whether o/p lines are active low/high ?

$D_0 = \overline{E}\,\overline{A}\,\overline{B}\,\overline{C}$

$D_1 = \overline{E}\,\overline{A}\,\overline{B}C$

$D_2 = \overline{E}\,\overline{A}B\overline{C}$

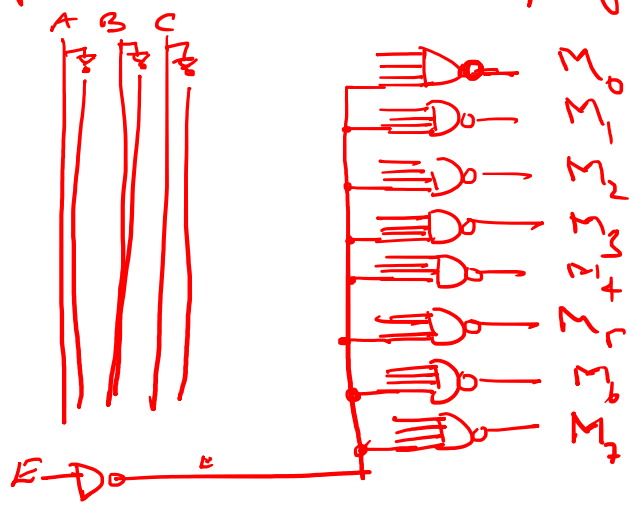
$D_3 = \overline{E}\,\overline{A}BC$

$D_4 = \overline{E}A\overline{B}\overline{C}$

$D_5 =$

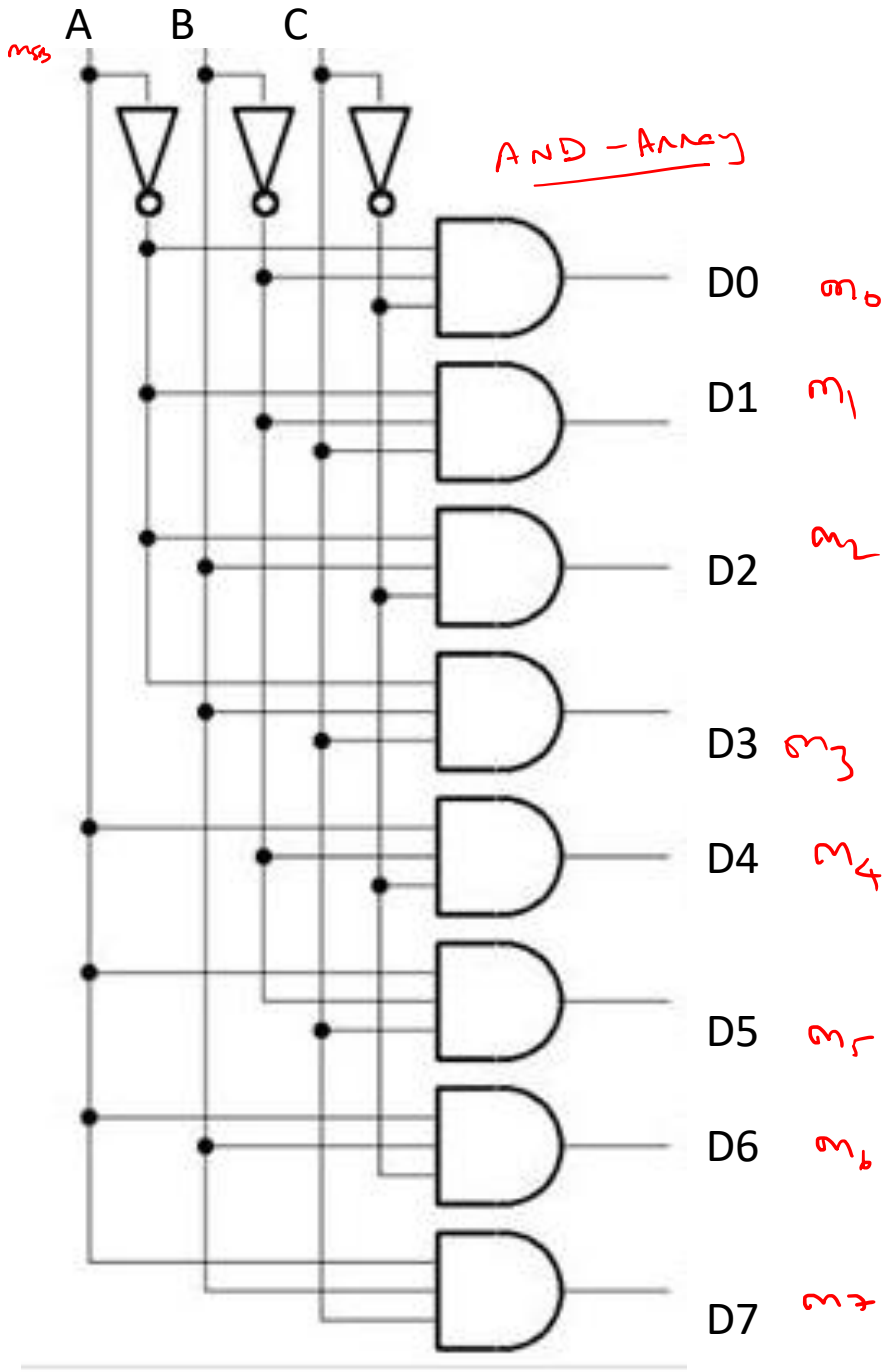
$D_6 =$

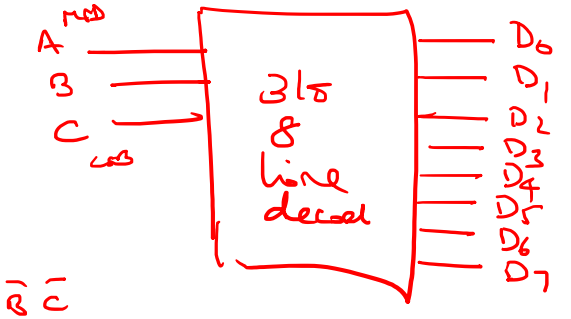
$D_7 =$



Active High o/ps

How do you input enable E to the circuit?

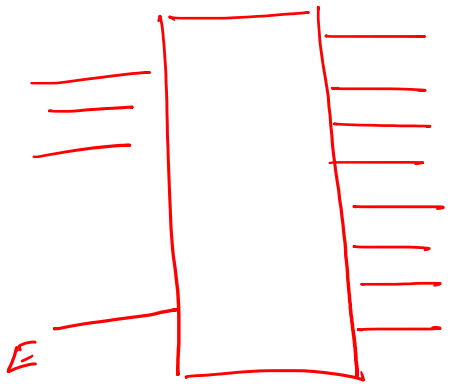


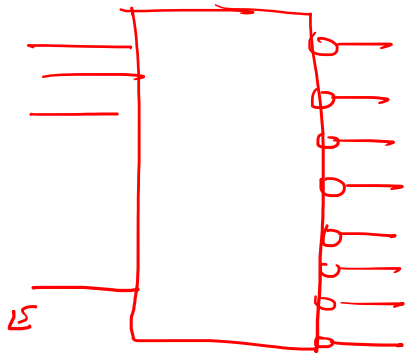


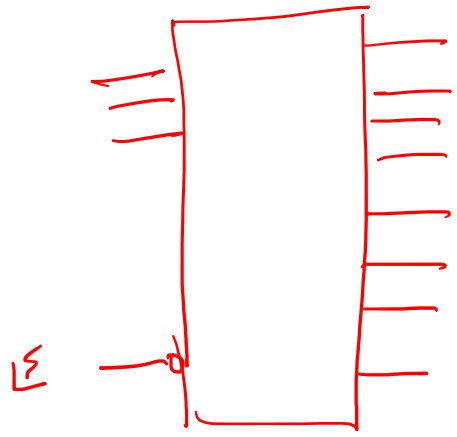
$D_0 = \bar{A}\bar{B}\bar{C}$
$D_1 = \bar{A}\bar{B}C$
$D_2 = \bar{A}B\bar{C}$
$D_3 = \bar{A}BC$
$D_4 = A\bar{B}\bar{C}$
$D_5 = A\bar{B}C$
$D_6 = AB\bar{C}$
$D_7 = ABC$

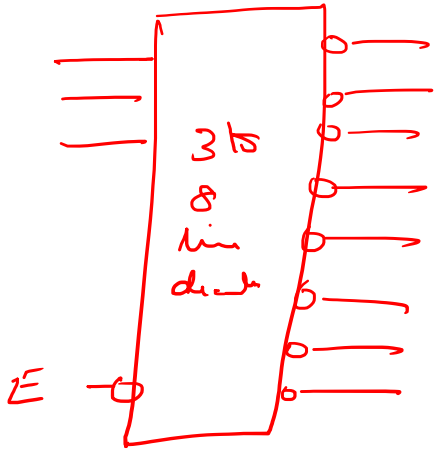
Active High o/p

Block diagram of 3-to-8 line decoder

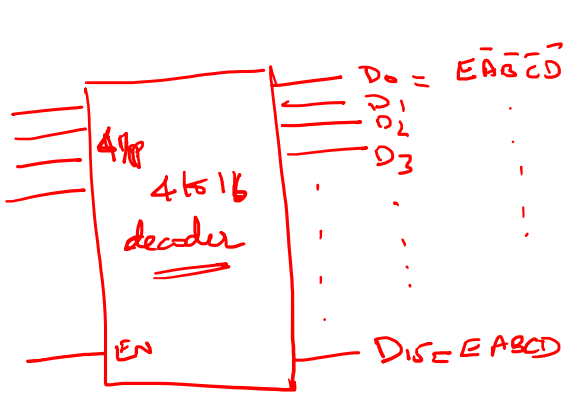


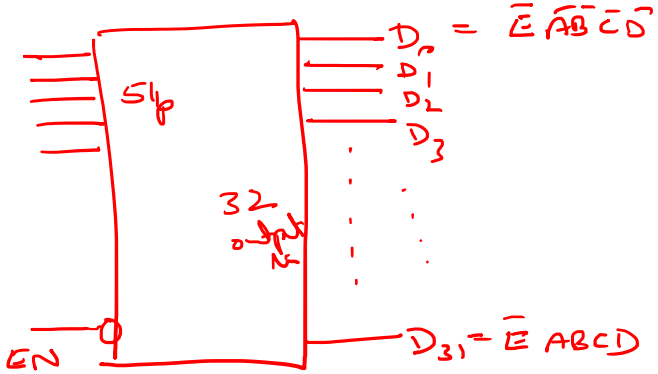






Discussion of 4-to-16 and 5-to-32 line decoders

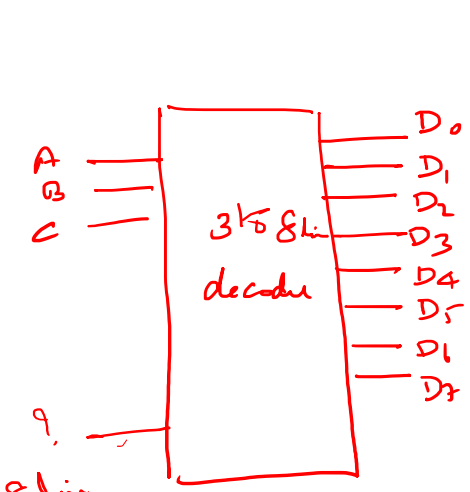


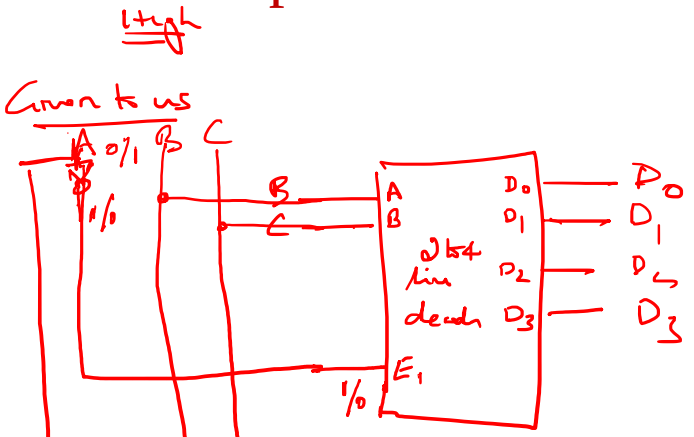


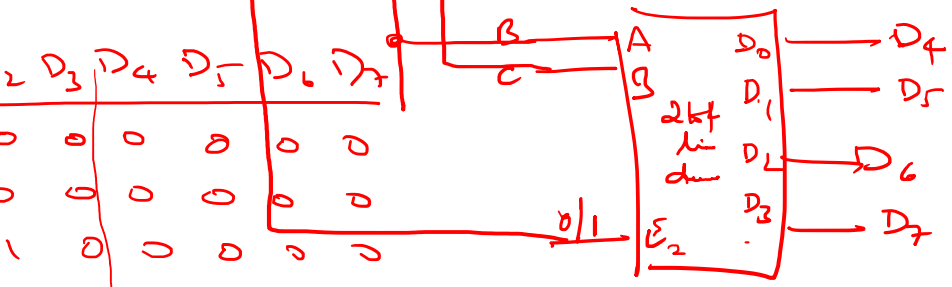
Design 3-to-8 line decoder using minimum number of:

1. 2-to-4 decoders with enable input and one external gate
2. 2-to-4 decoders with enable inputs only

Design 3-to-8 line decoder using minimum number of:
2-to-4 decoders with enable input and one external gate







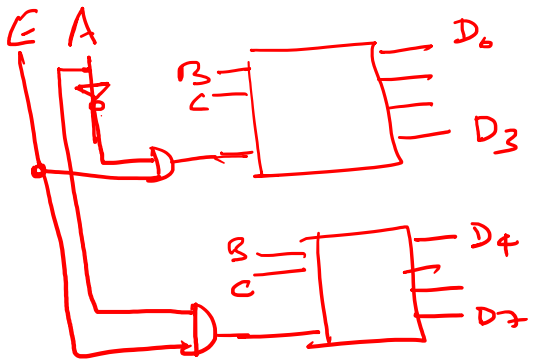
3 to 8 line

A	B	C	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

E	A	E_1	E_2
1	0	1	0
1	1	0	1
0	0	x	x
0	1	x	x

$E_1 = E\bar{A}$

$E_2 = EA$



Design 3-to-8 line decoder using minimum number of 2-to-4 decoders only