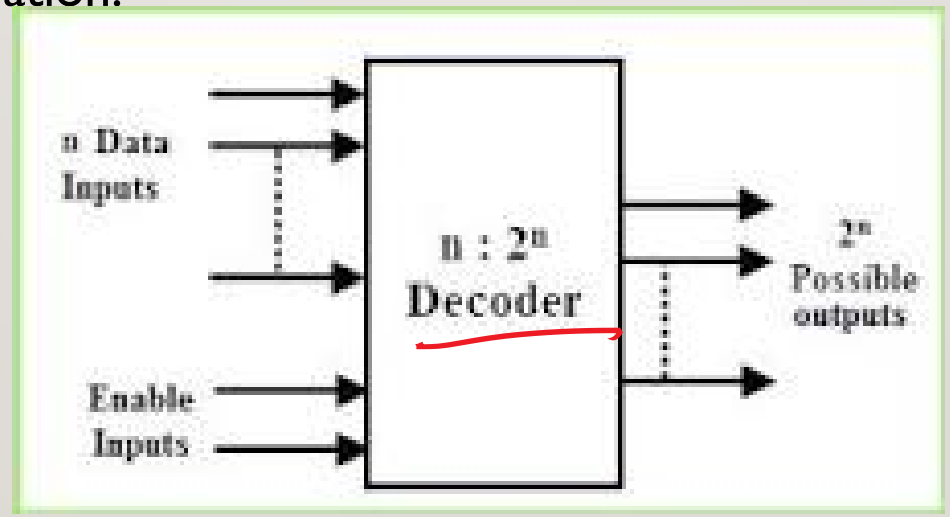
DECODERS AND ENCODERS

STUDENTS ARE ADVISED TO WRITE DOWN THE NOTES FOR EVERY LECTURE

DECODER:

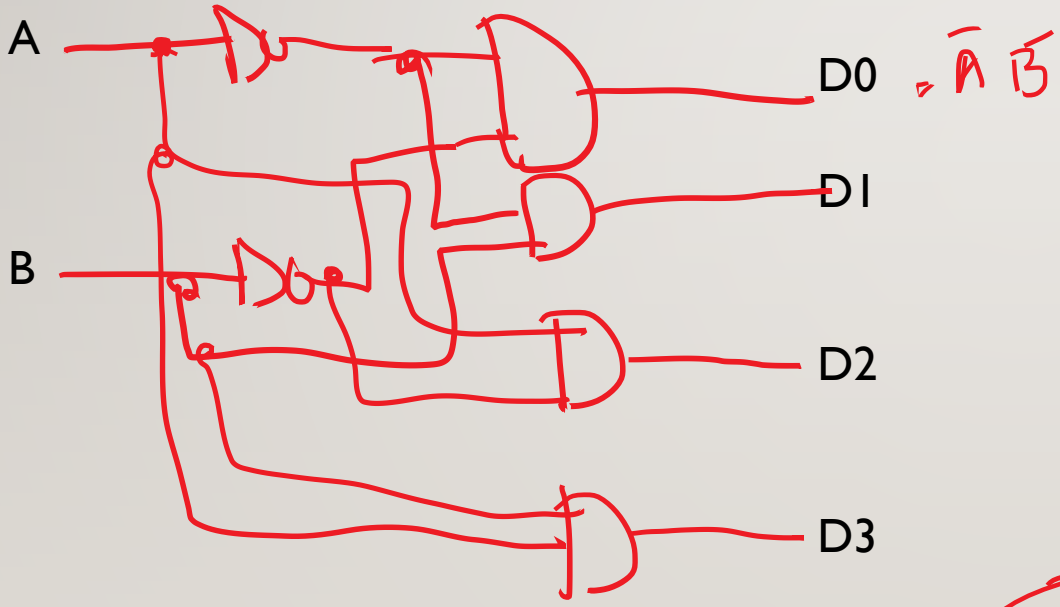
- A combinational circuit
- Converts a binary information from n-input lines to a maximum of 2^n unique output lines (n-to- 2^n line decoder) and one or more enable inputs. Ex: 2-to-4 line, 3-to-8 line..etc
- In standard decoders, only one output line will be active at a time corresponding to the input binary combination.



2-to-4 line decoder

Active high O/P.

Circuit Diagram



$D_0 = \bar{A}\bar{B}$

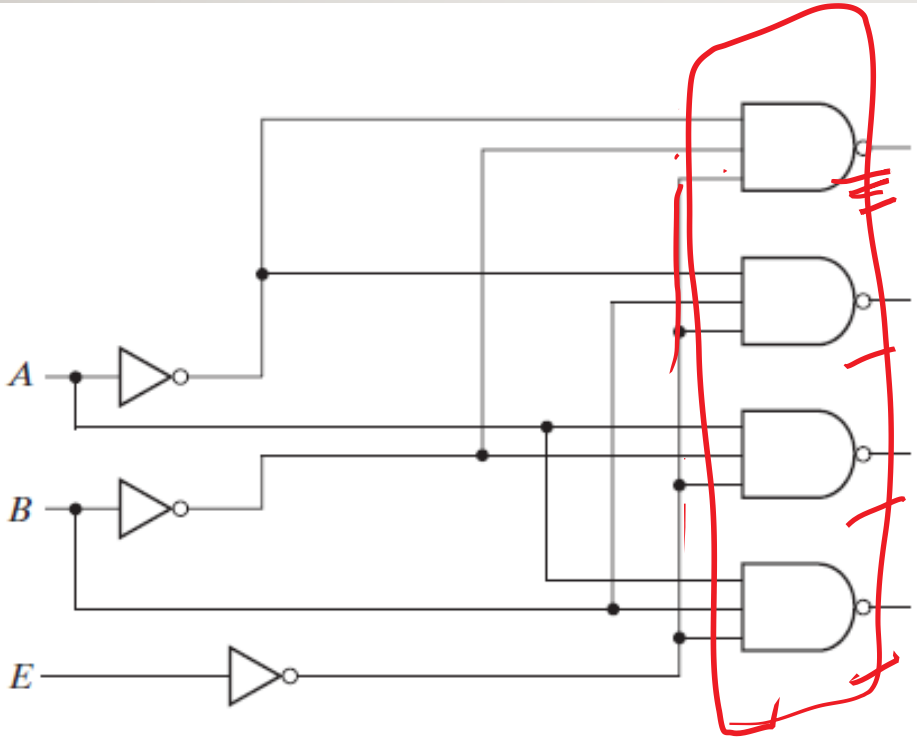
Truth table

	A	B	D_0	D_1	D_2	D_3
0	0	0	1	0	0	0
1	0	1	0	1	0	0
2	1	0	0	0	1	0
3	1	1	0	0	0	1

$D_0 = \bar{A}\bar{B}$; $D_1 = \bar{A}B$; $D_2 = A\bar{B}$

$D_3 = AB$

2-to-4 line decoder with active low output & enable input



(a) Logic diagram

E	A	B	D_0	D_1	D_2	D_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

(b) Truth table

$D_0 = (E + A + B) \cdot \bar{E}\,\bar{A}\,\bar{B}$

$D_1 = E + A + \bar{B} = \overline{(\bar{E}\,\bar{A}\,B)}$

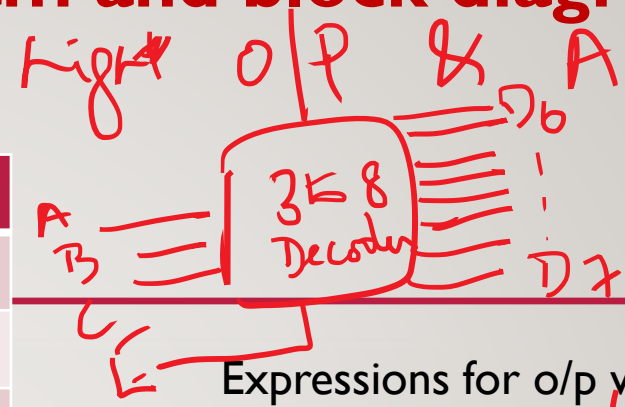
$D_2 = \overline{(E + \bar{A} + B)} = E\,A\,\bar{B}$

$D_3 = \overline{(E + A + \bar{B})} = E \cdot AB$

Write the truth table ,logic diagram and block diagram of 3-to-8 line decoder

Inputs				Outputs							
E	A	B	C	D0	D1	D2	D3	D4	D5	D6	D7
0	X	X	X	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	1	0	0	0	0	0	0
1	0	1	0	0	0	1	0	0	0	0	0
1	0	1	1	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	0	0	1	0	0
1	1	1	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1

Active high O/P & Active high Enable.



Expressions for o/p variables

$D_0 = E \cdot \bar{A}\bar{B}\bar{C}$

$D_1 = E\bar{A}\bar{B}C$

$D_2 = E\bar{A}B\bar{C}$

$D_3 = E\bar{A}BC$

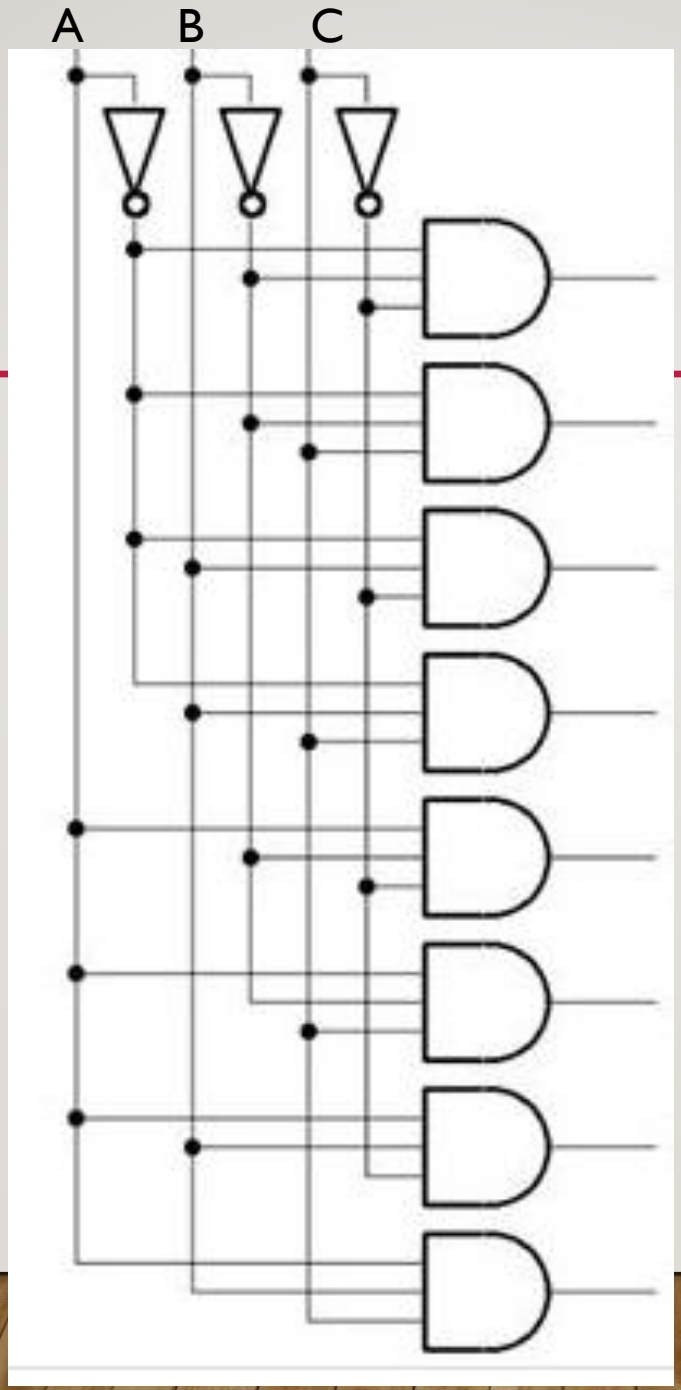
$D_4 = EA\bar{B}\bar{C}$

$D_5 = EA\bar{B}C$

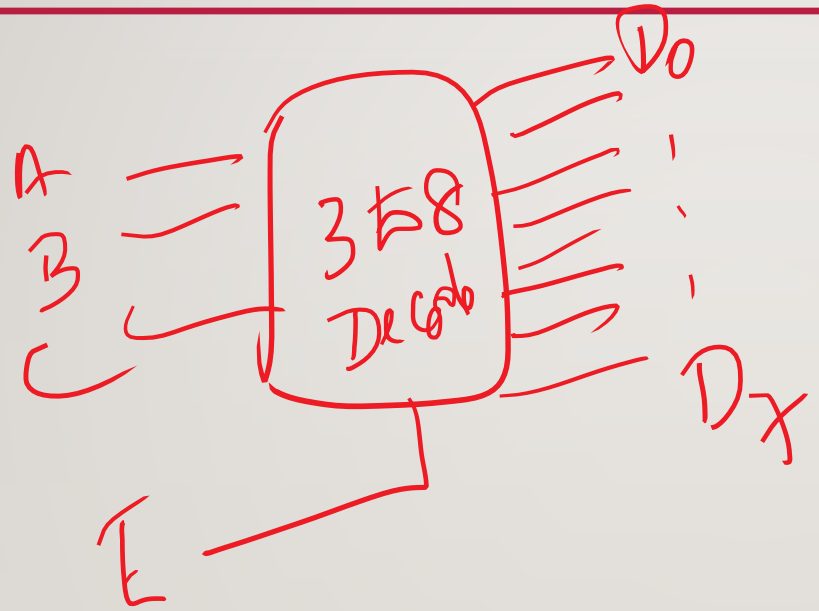
$D_6 = EAB\bar{C}$

$D_7 = EABC$

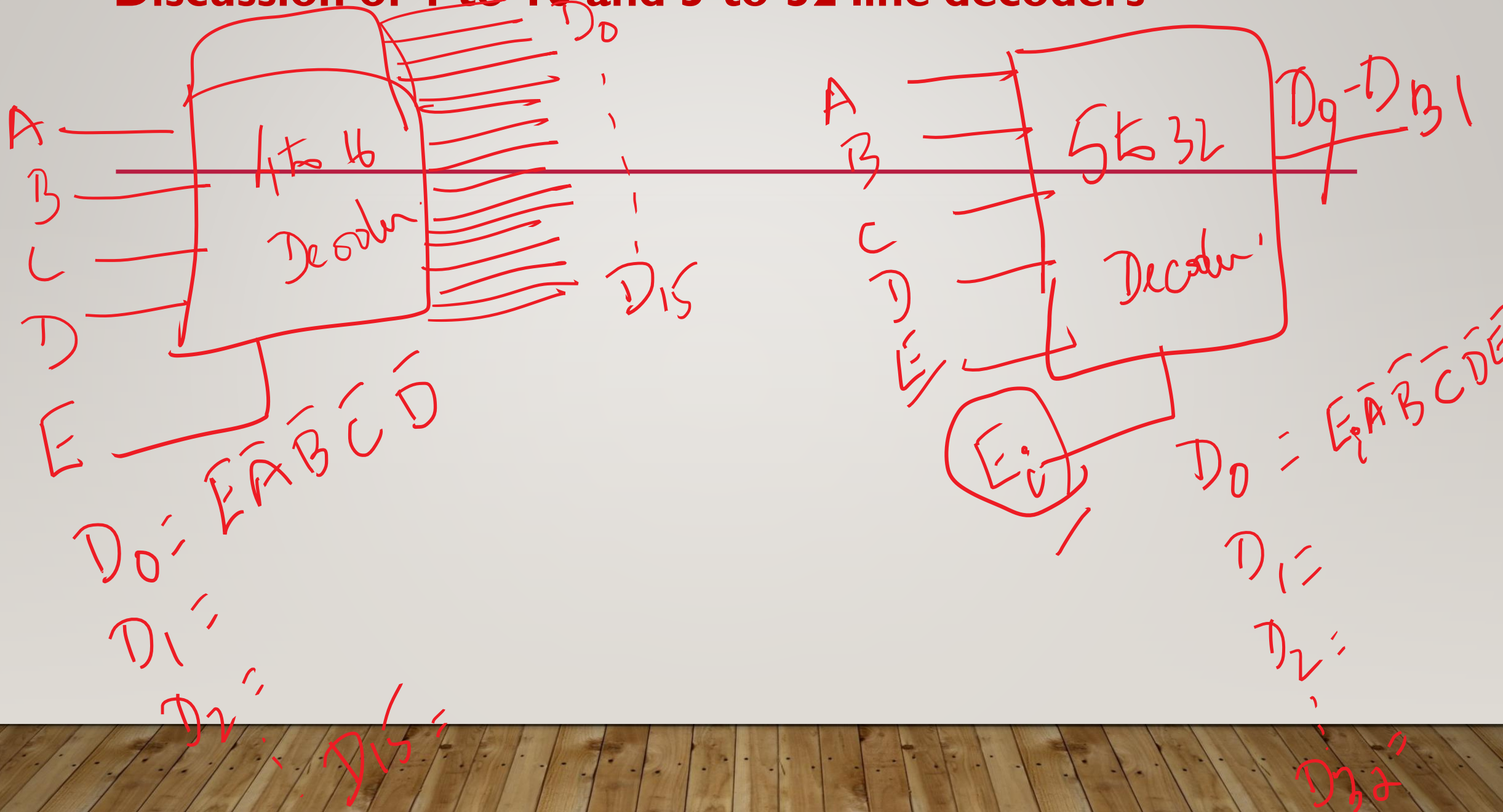
How do you input enable E to the circuit?



BLOCK DIAGRAM OF 3-TO-8 LINE DECODER



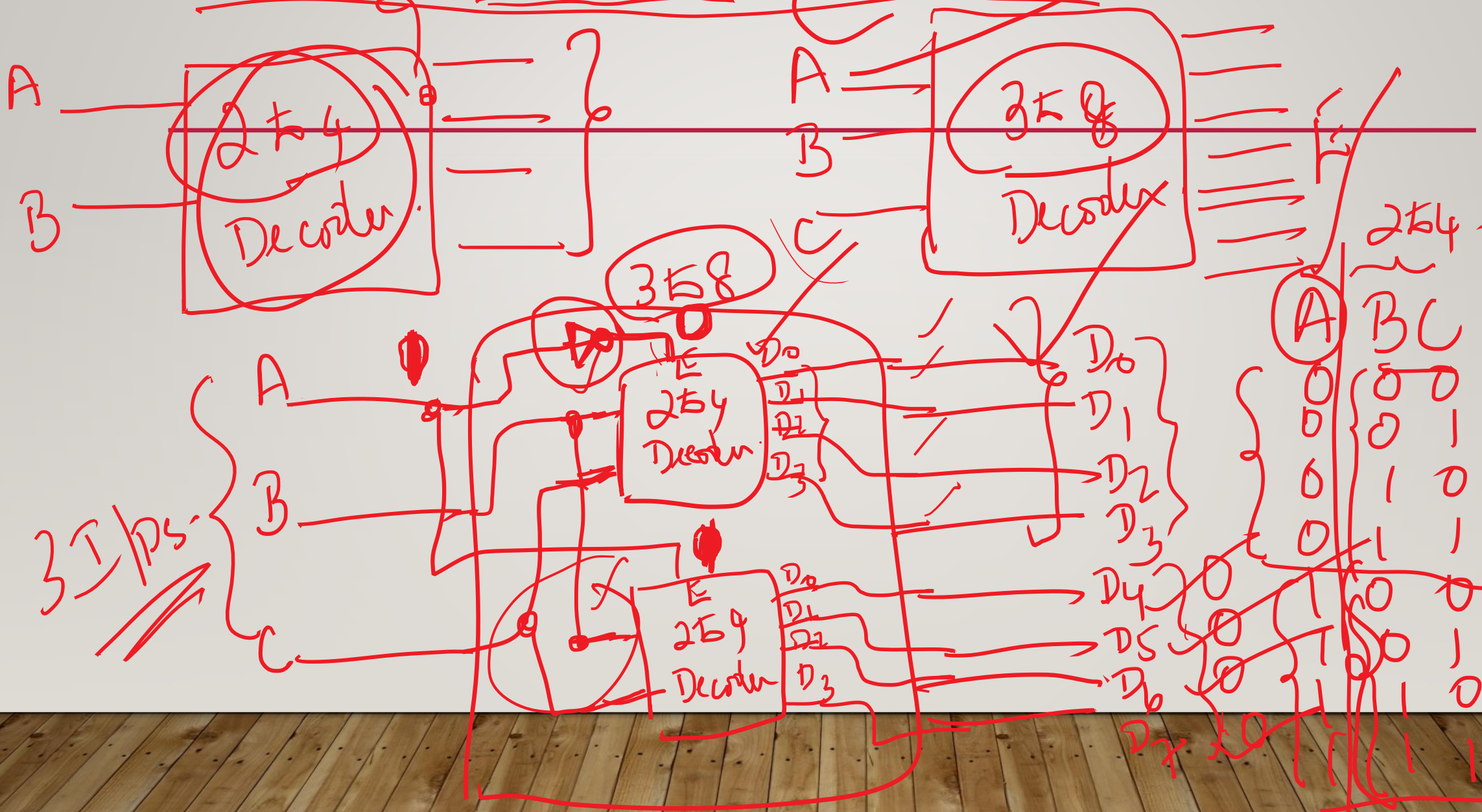
Discussion of 4-to-16 and 5-to-32 line decoders



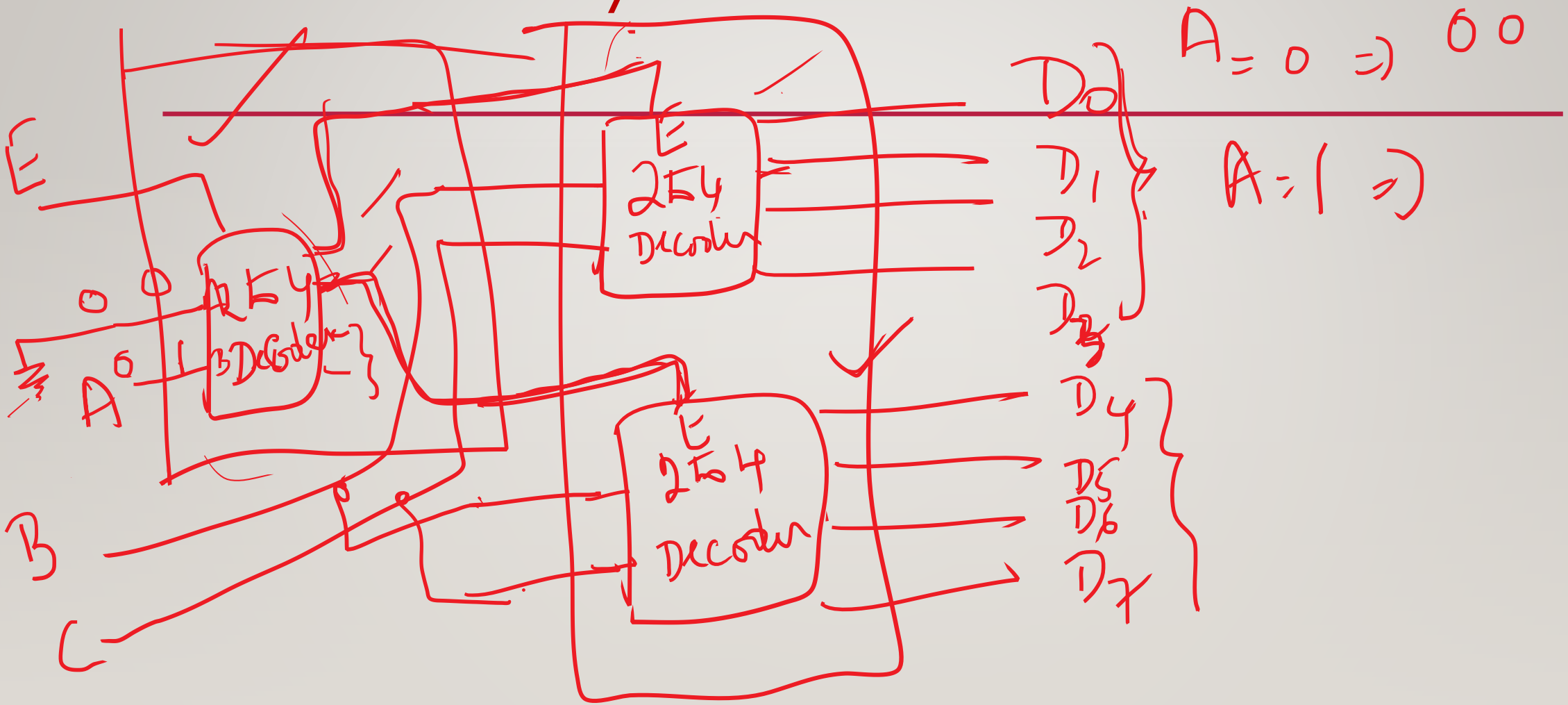
Design 3-to-8 line decoder using minimum number of:

1. 2-to-4 decoders with enable input and one external gate
2. 2-to-4 s with enable inputs only

Design 3-to-8 line decoder using minimum number of:
2-to-4 decoders with enable input and one external gate



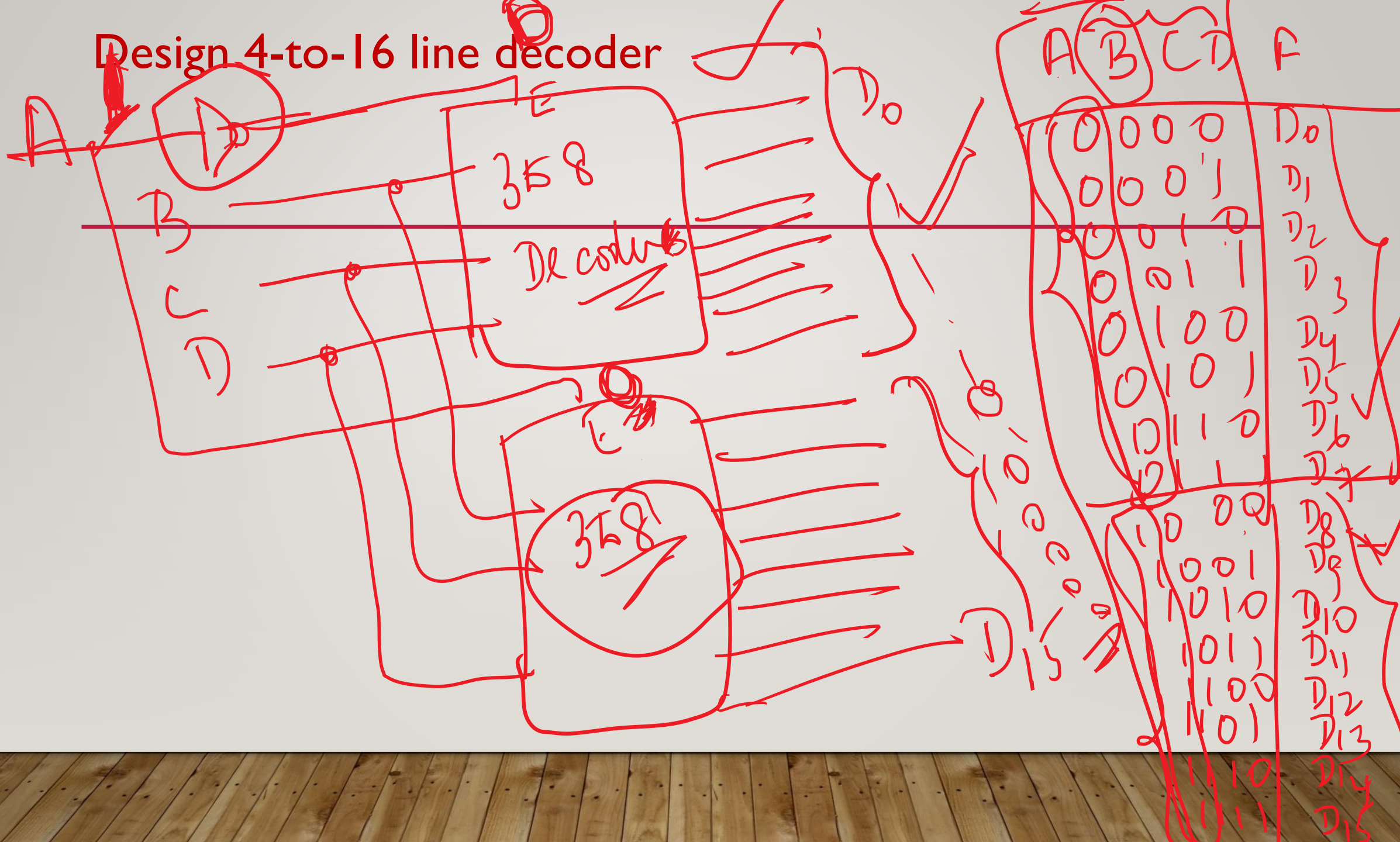
Design 3-to-8 line decoder using minimum number of 2-to-4 decoders only



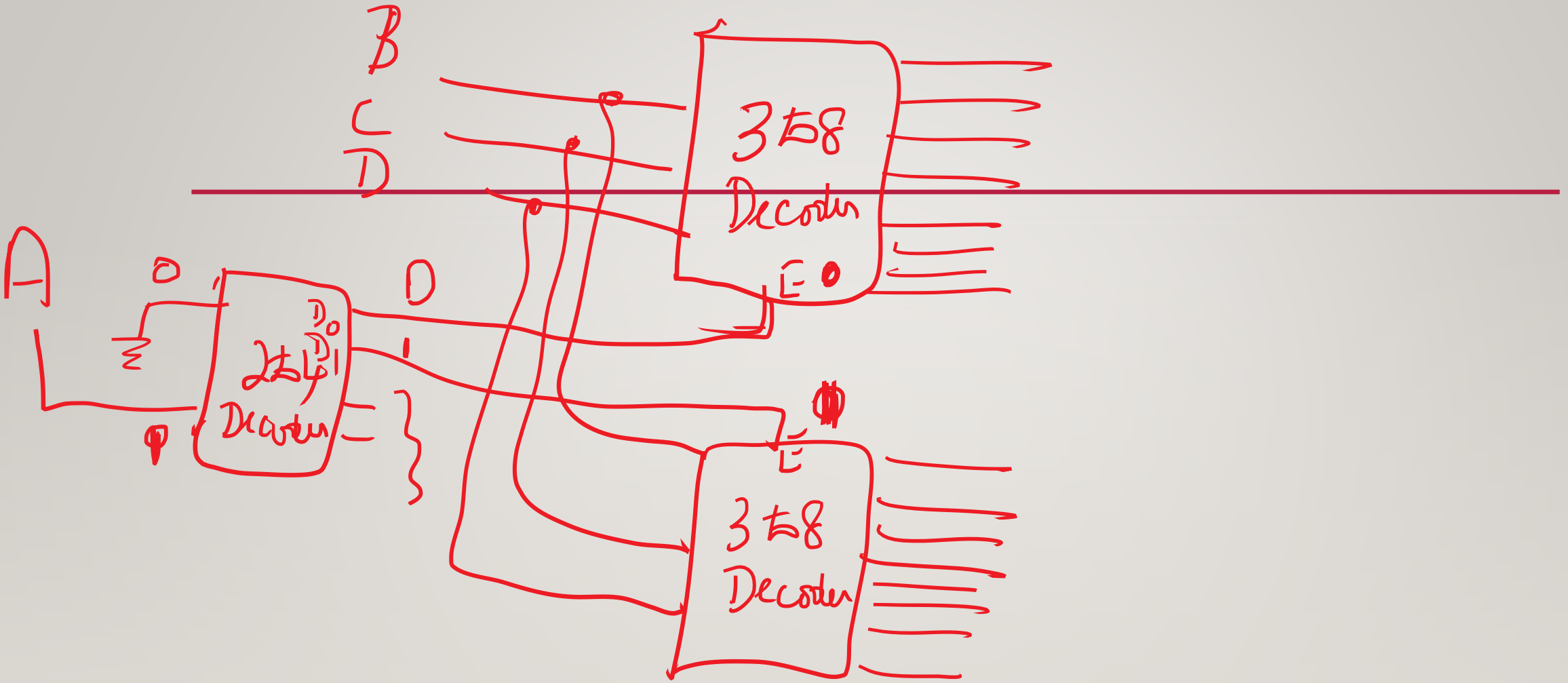
Design 4-to-16 line decoder using minimum number of

1. 3-to-8 decoders with enable input and one external gate
2. Only 3-to-8 and 2-to-4 line decoders with enable inputs
3. Only 2-to-4 line decoders with enable inputs

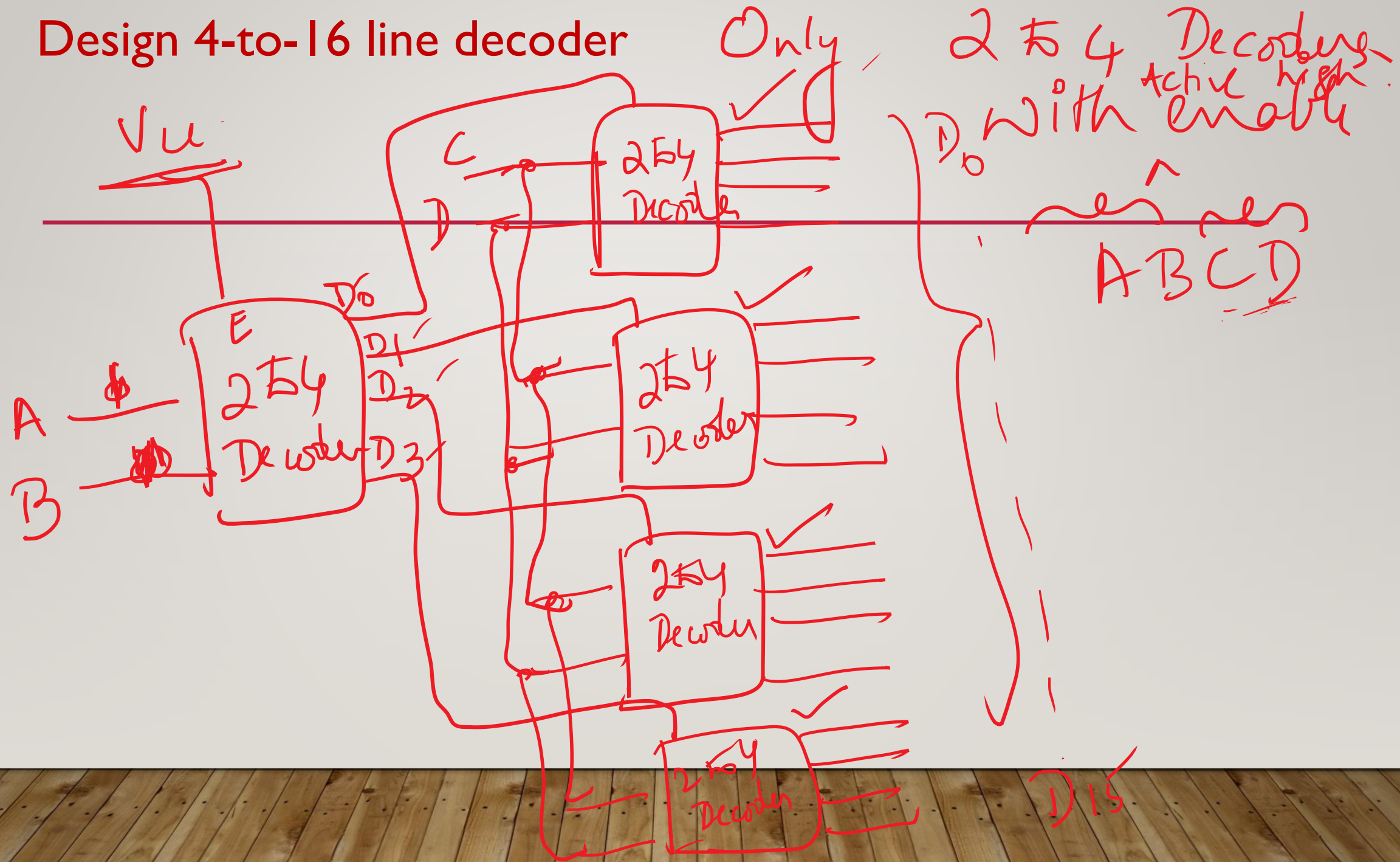
Design 4-to-16 line decoder



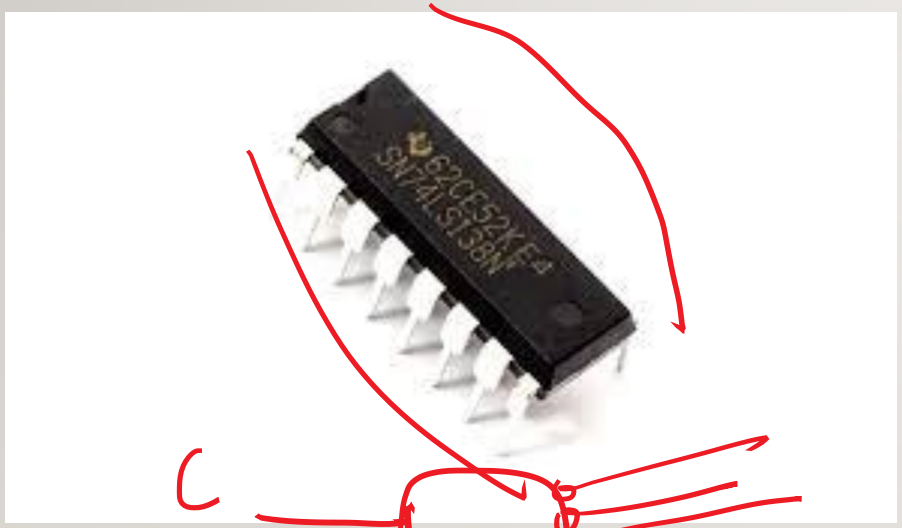
Design 4-to-16 line decoder

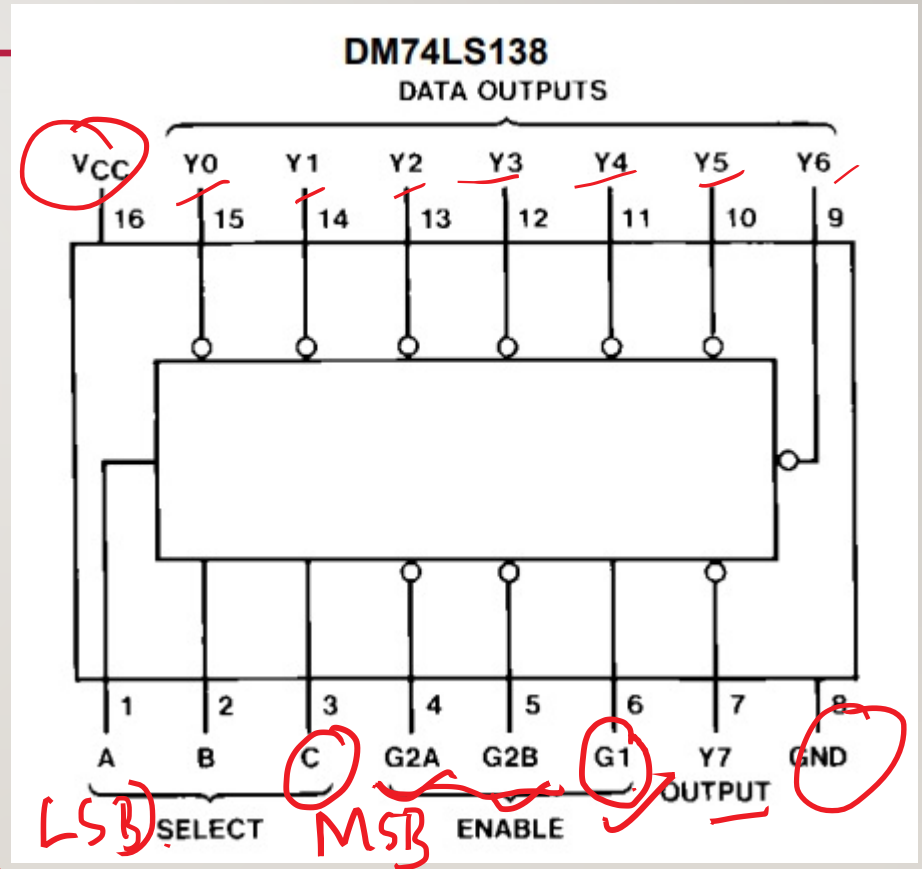


Design 4-to-16 line decoder

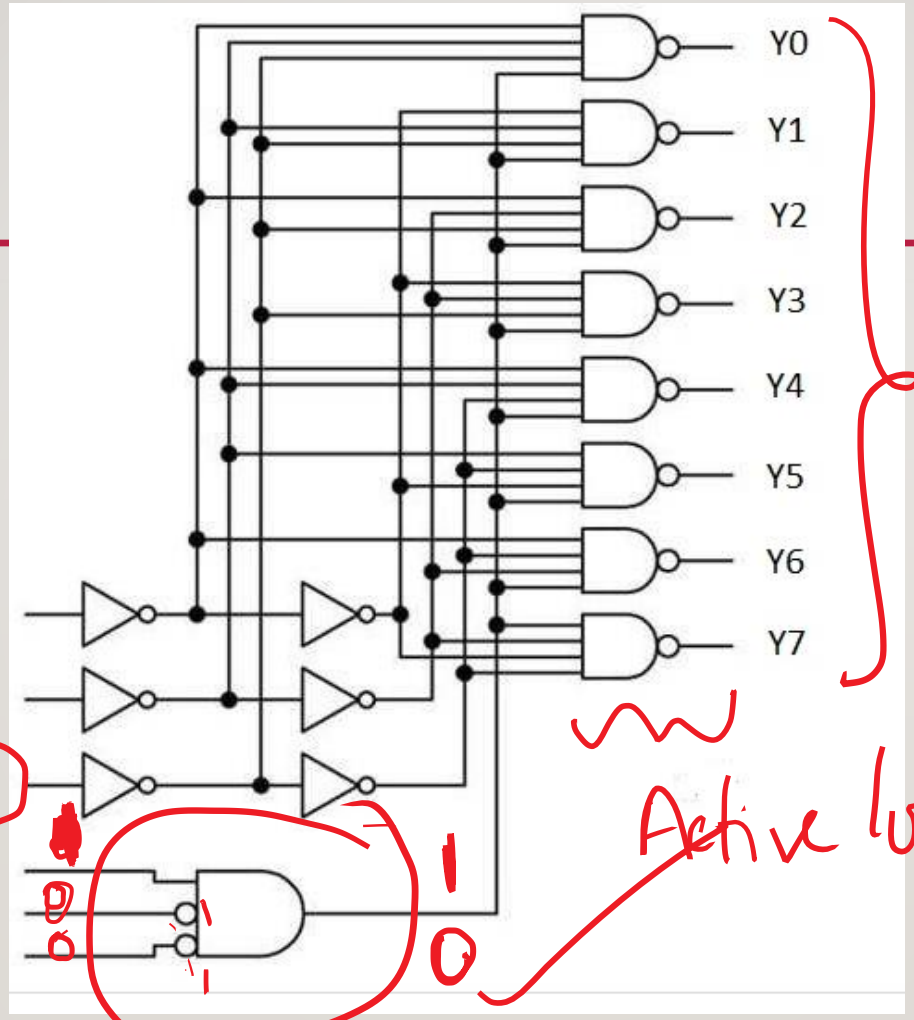


74138 IC: 3-to-8 line decoder with active low output

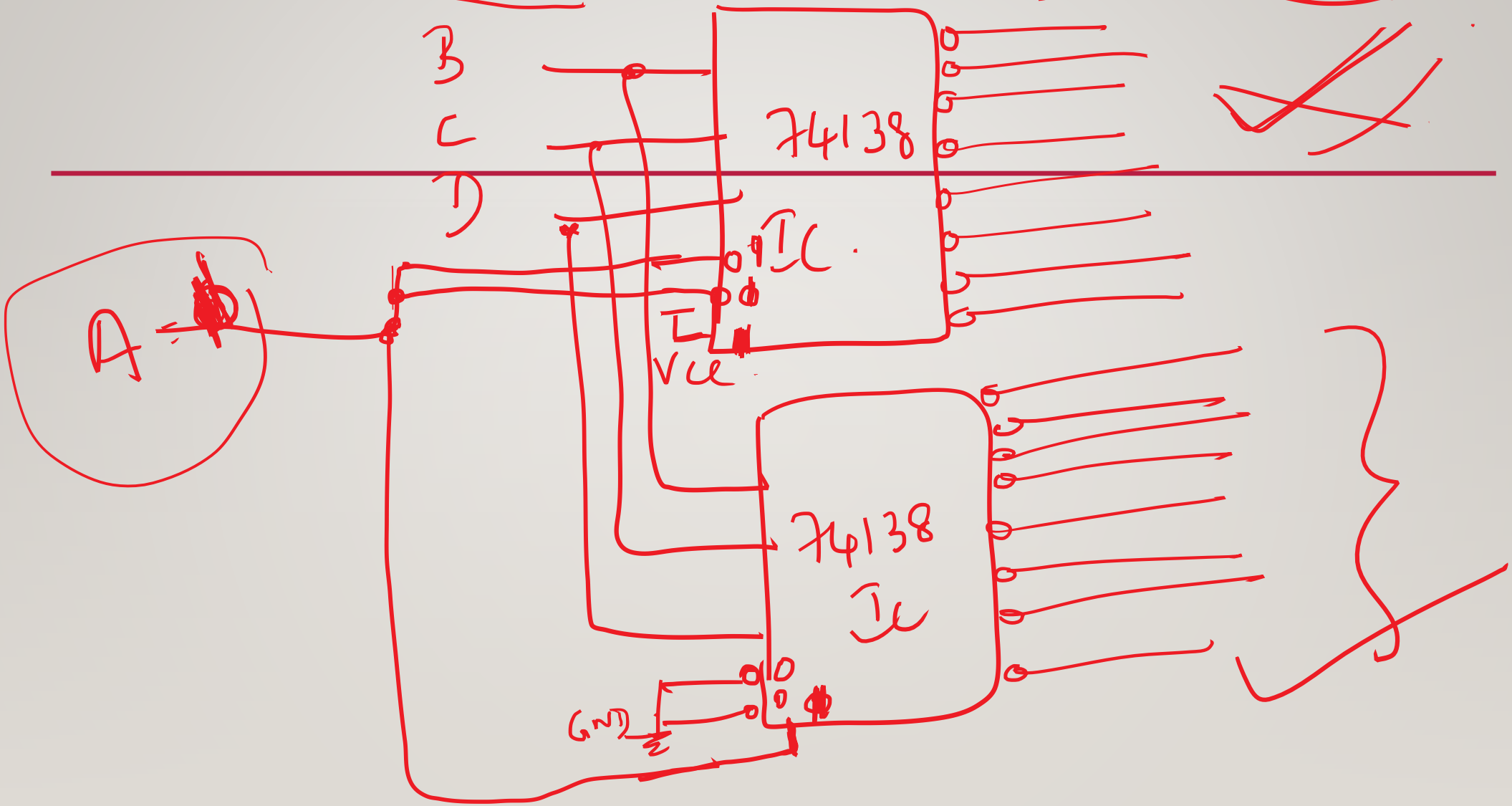




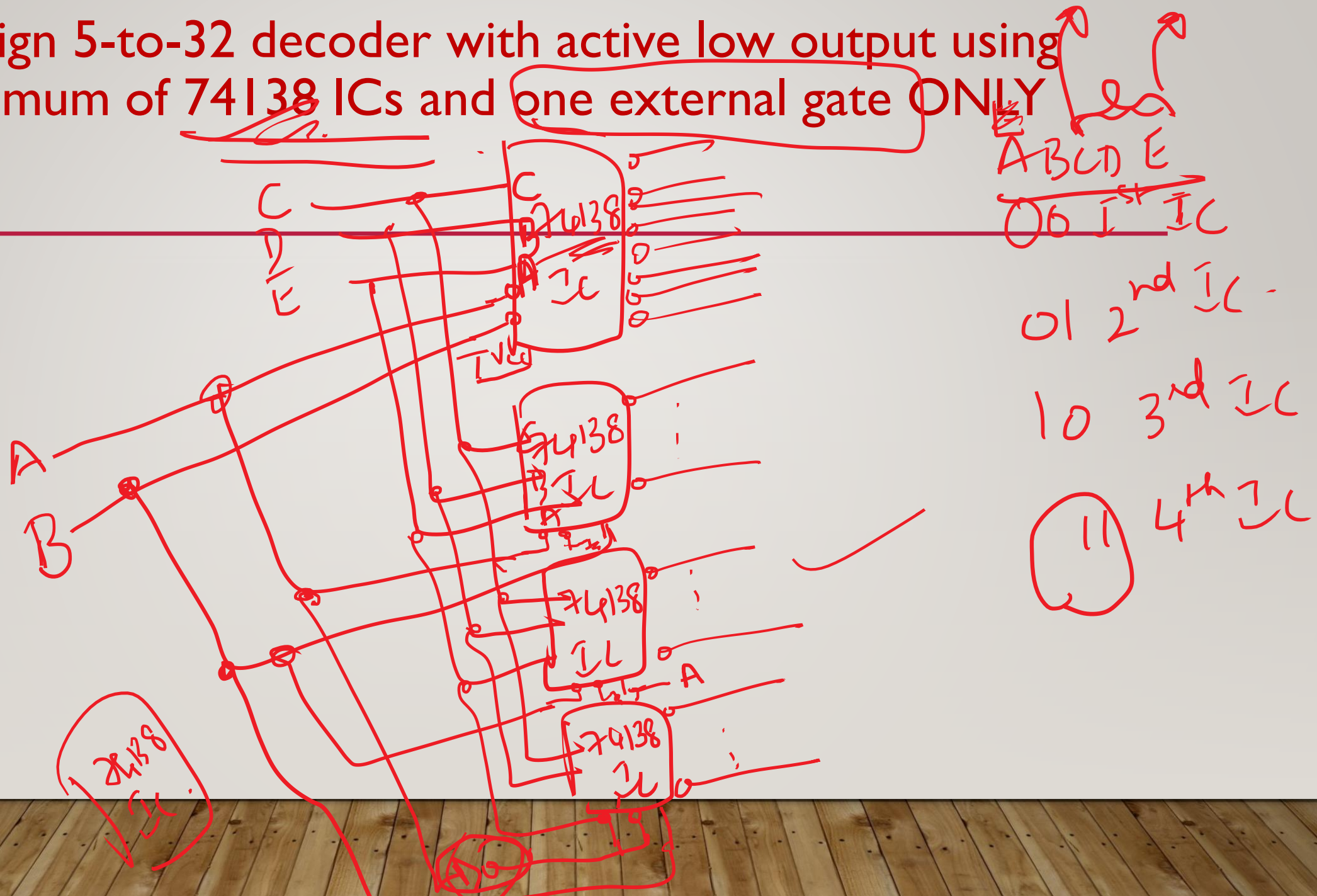
74138 IC internal diagram



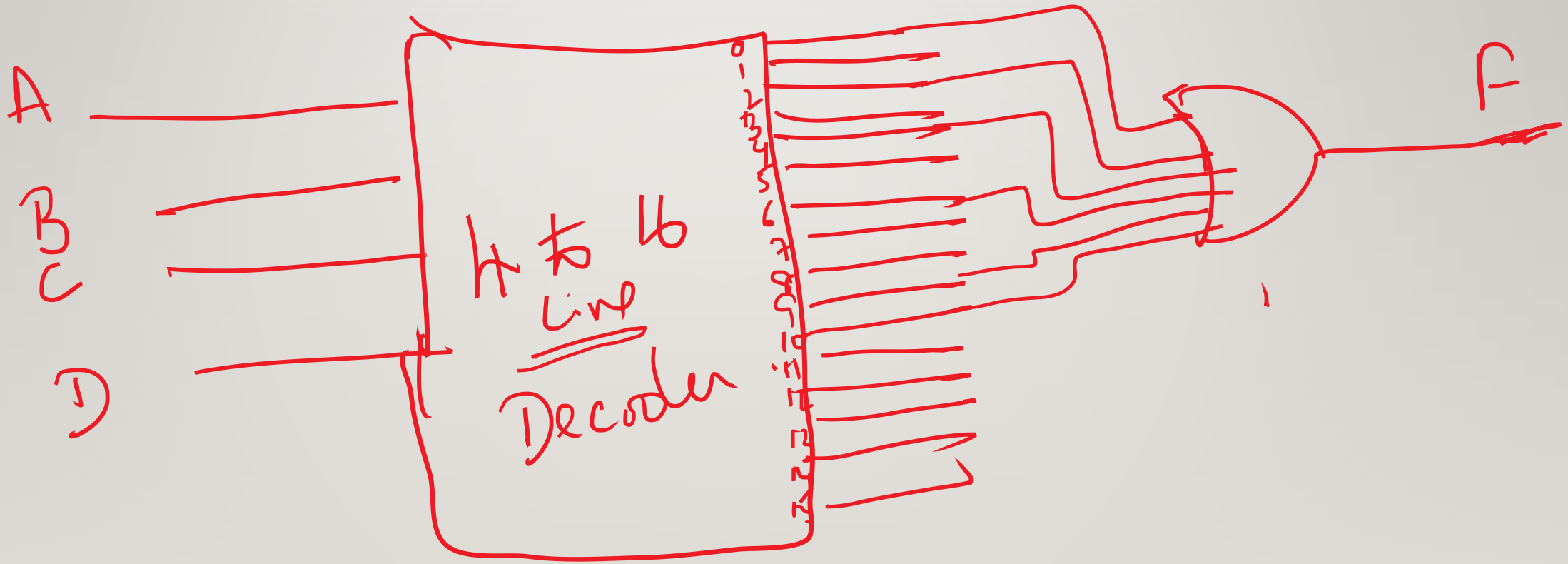
Design 4-to-16 decoder using minimum of 74138 ICs ONLY



Design 5-to-32 decoder with active low output using minimum of 74138 ICs and one external gate ONLY



Implement f(A,B,C,D) = Σm(0,2,4,6,9,10) using suitable decoder and external gates



Design a full adder using 3-to-8 line decoder and external gates

Inputs			Outputs	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$Sum = \Sigma(1, 2, 4, 7)$$

$$Carry = \Sigma(3, 5, 6, 7)$$