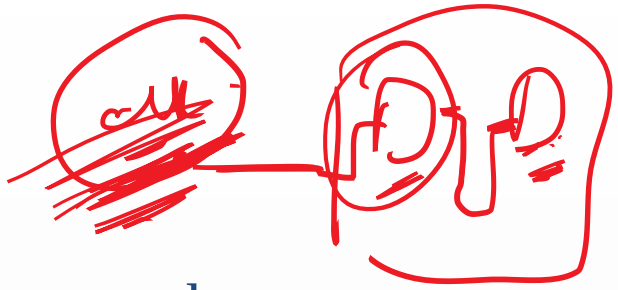
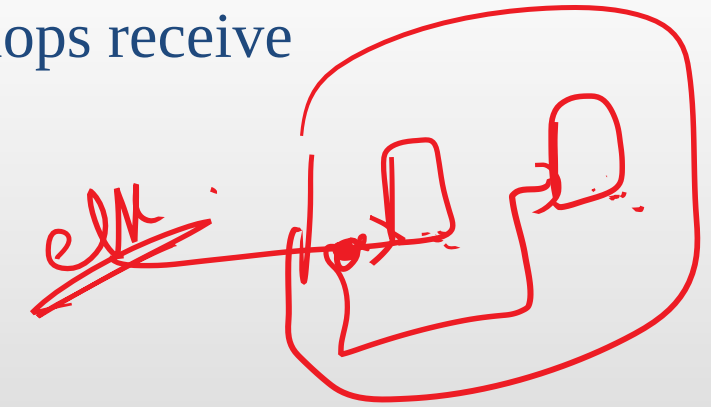
ASYNCHRONOUS COUNTER(RIPPLE COUNTER)

Counters:

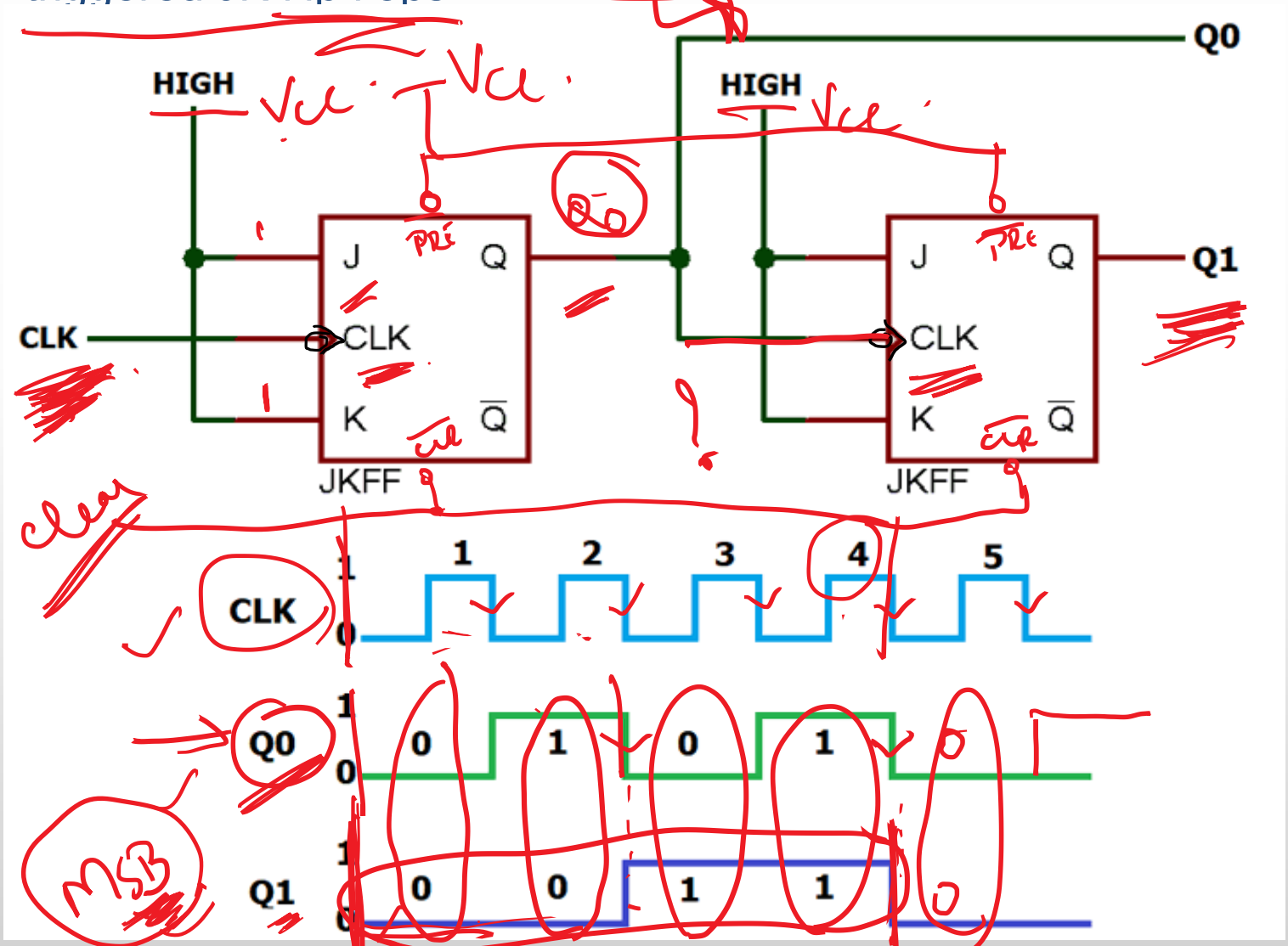


- Register that goes through prescribed sequence of states upon the application of input pulses is called a counter.
- There are 2 types of counters:
  - *Asynchronous counters (Ripple counters) :* Clock inputs are triggered by transitions of other flipflop.
  - *Synchronous counters :* The clock inputs of all flip flops receive common clock.

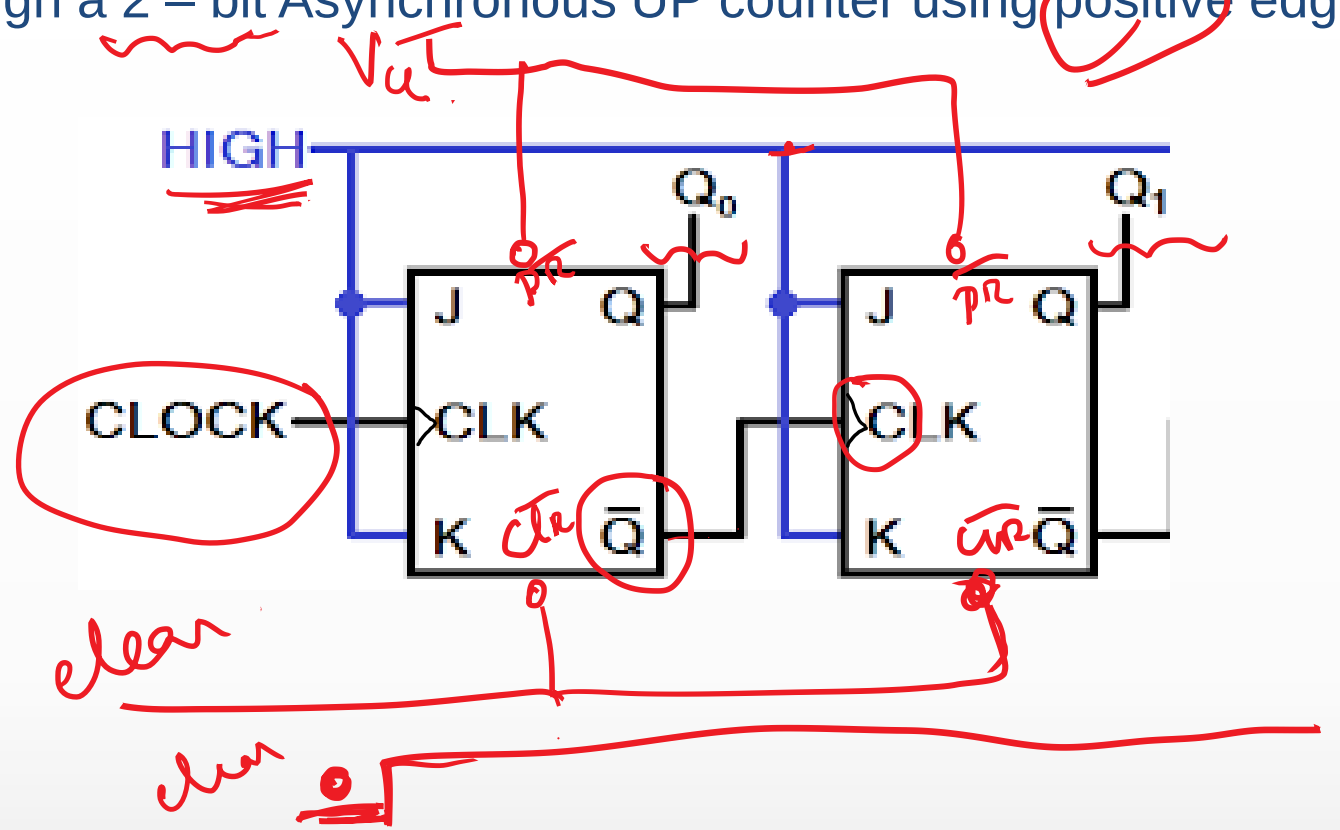


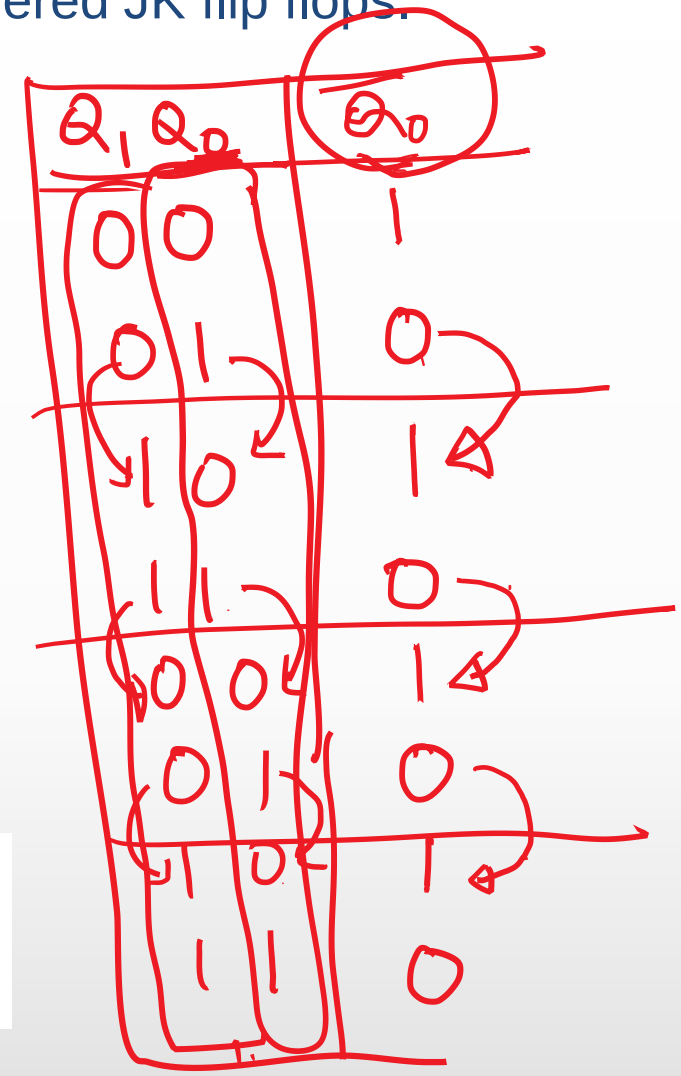
Asynchronous counters (Ripple counters)

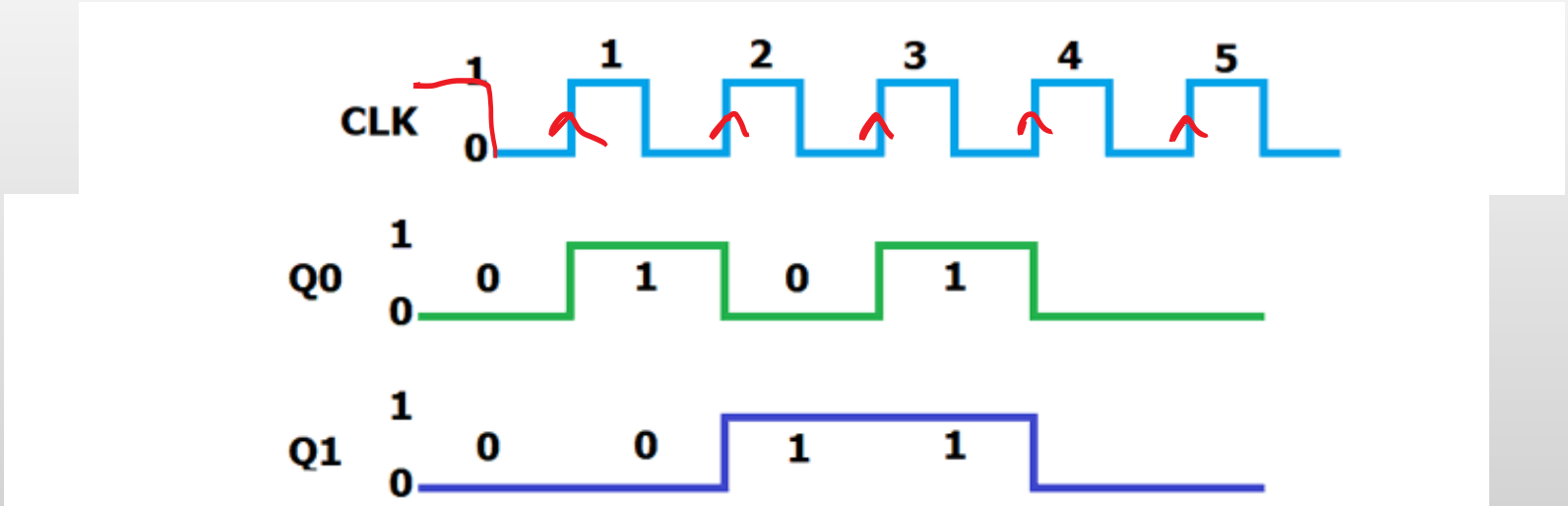
- Design a 2 – bit (MOD 4/ Divide by 4) Asynchronous UP counter using negative edge triggered JK flip flops.



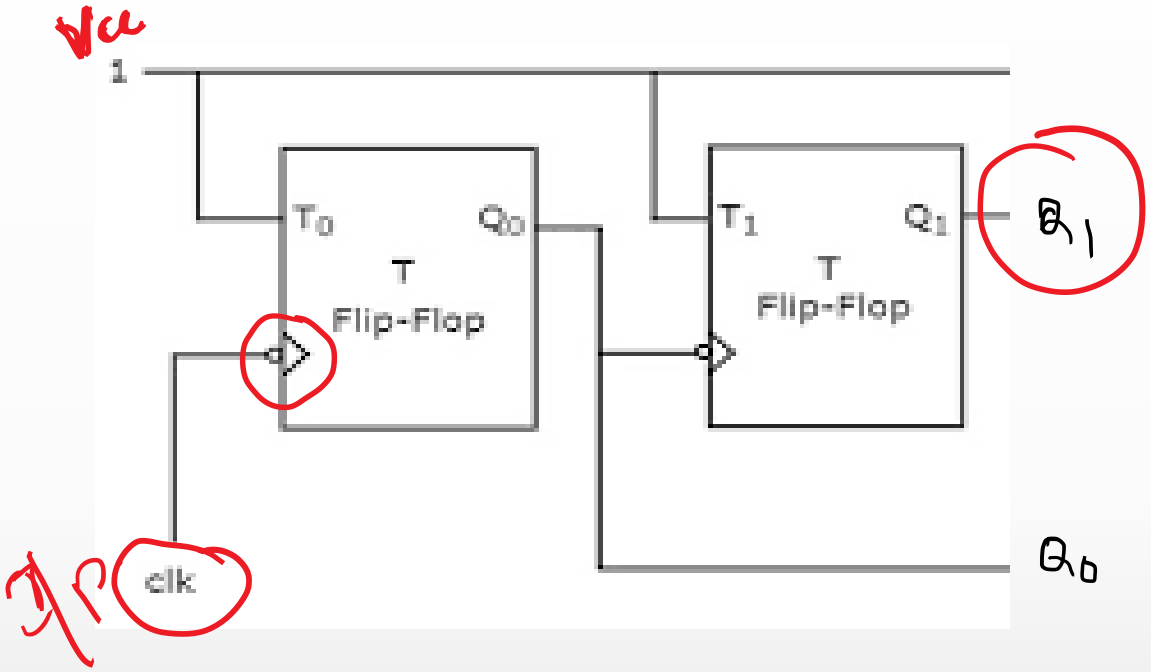
- Design a 2 – bit Asynchronous UP counter using positive edge triggered JK flip flops.



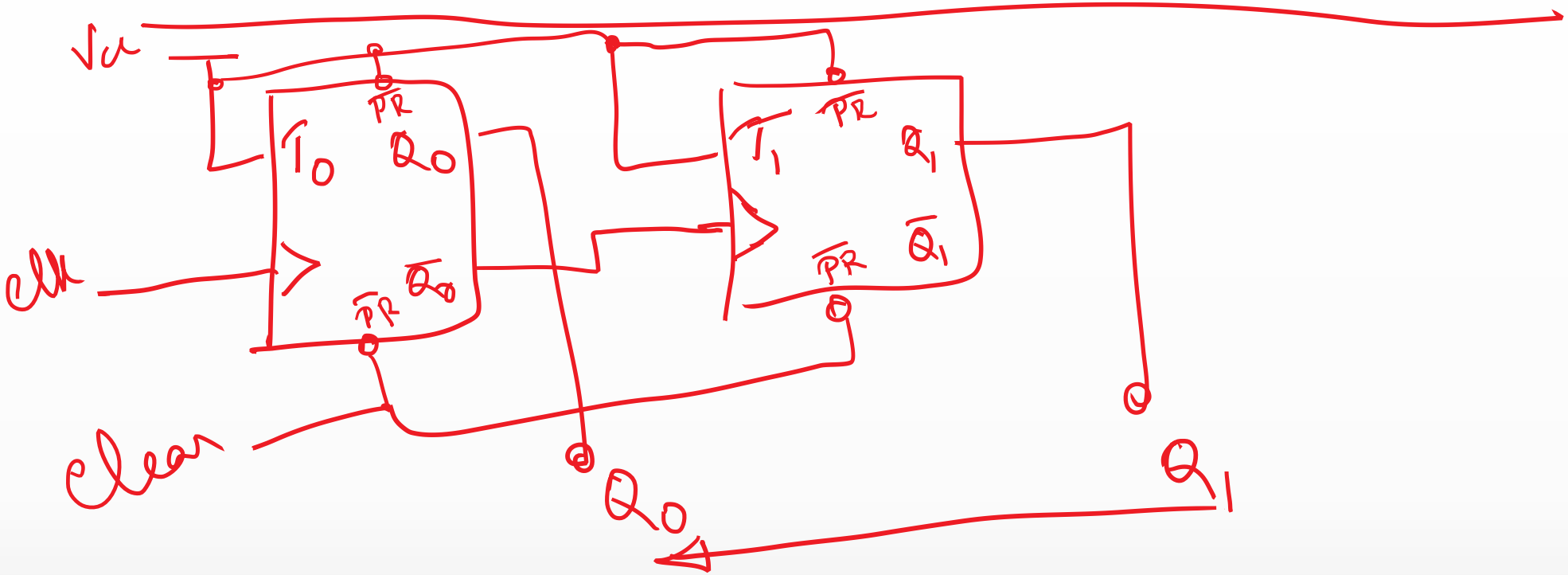




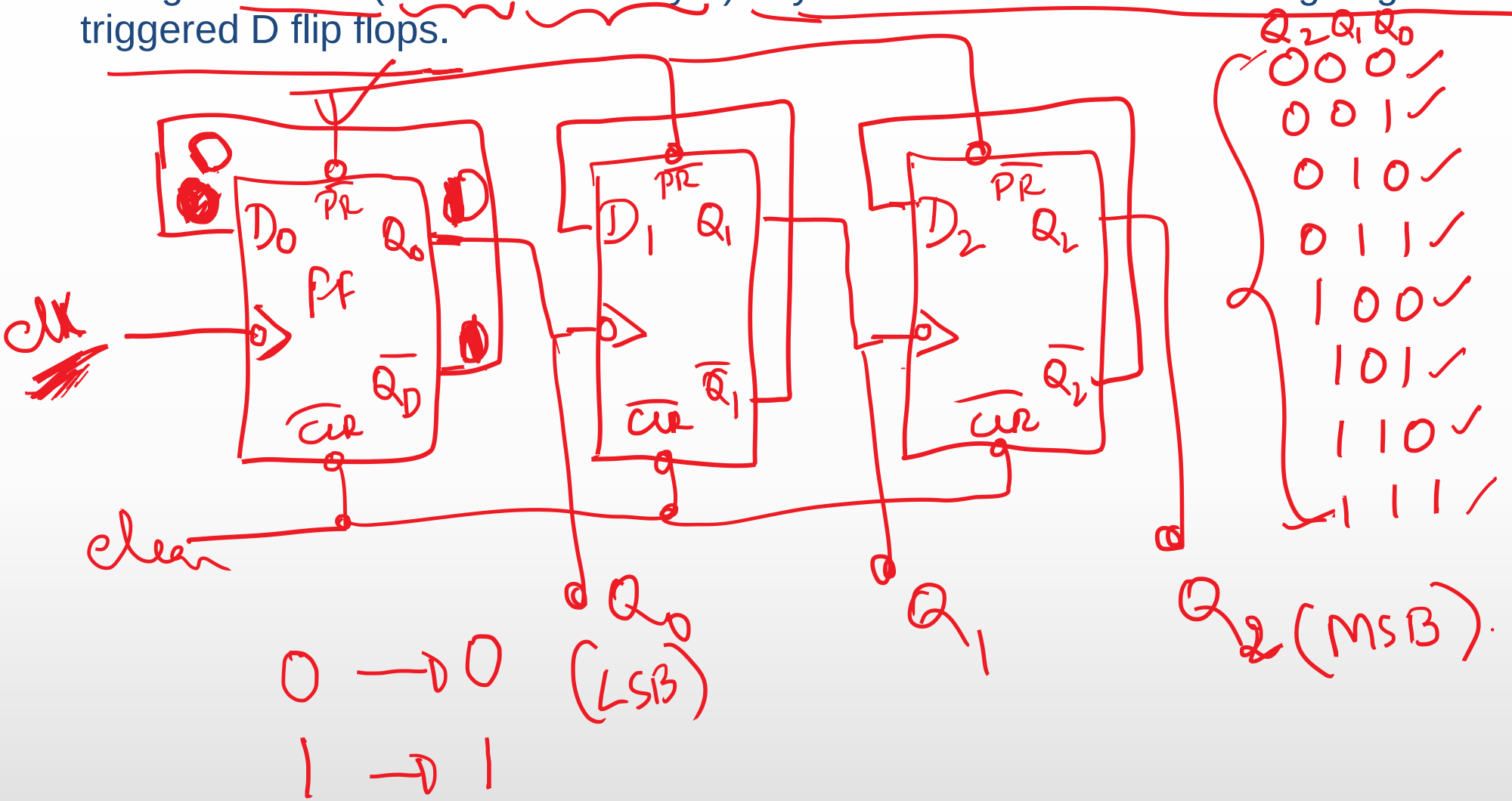
- Design a 2 – bit Asynchronous UP counter using negative edge triggered T flip flops.



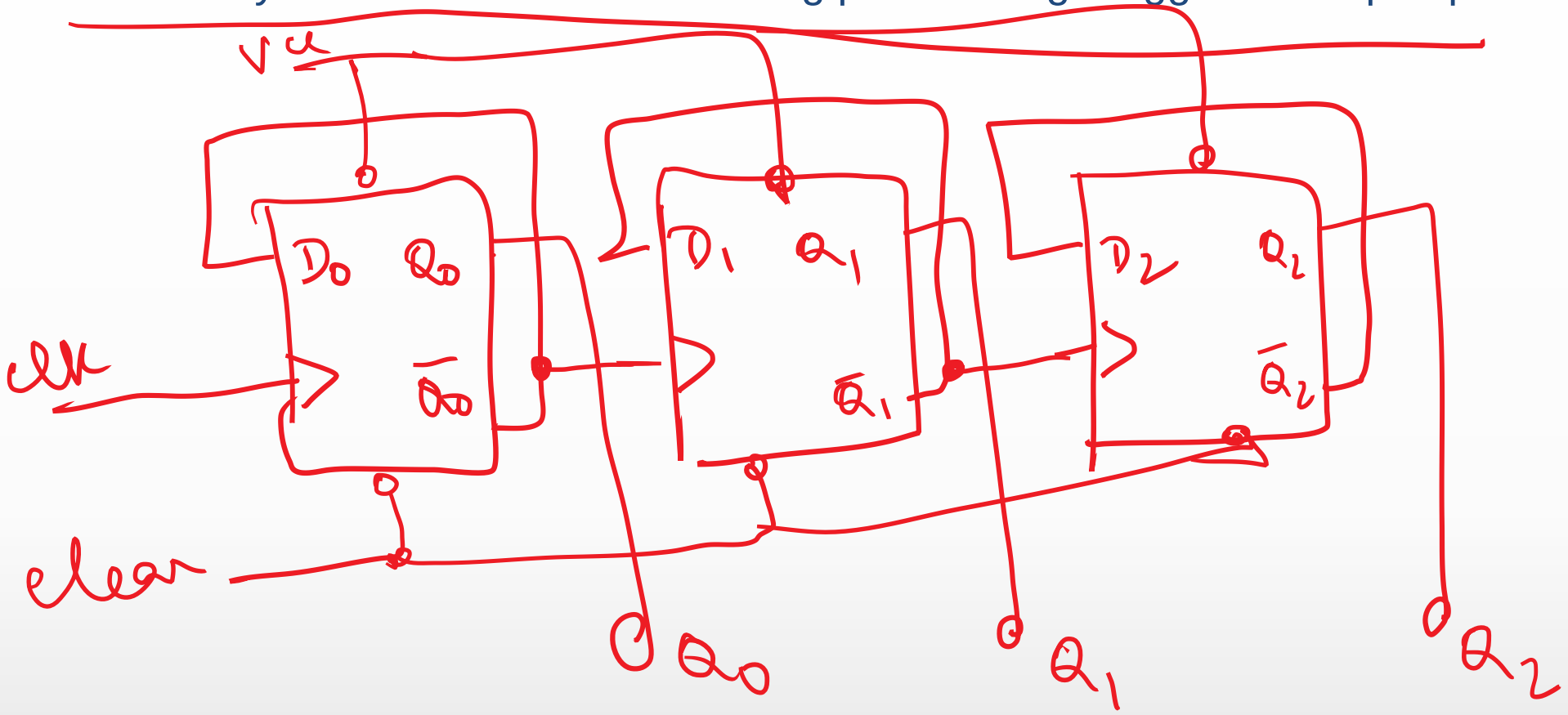
- Design a 2 – bit Asynchronous UP counter using positive edge triggered T flip flops.



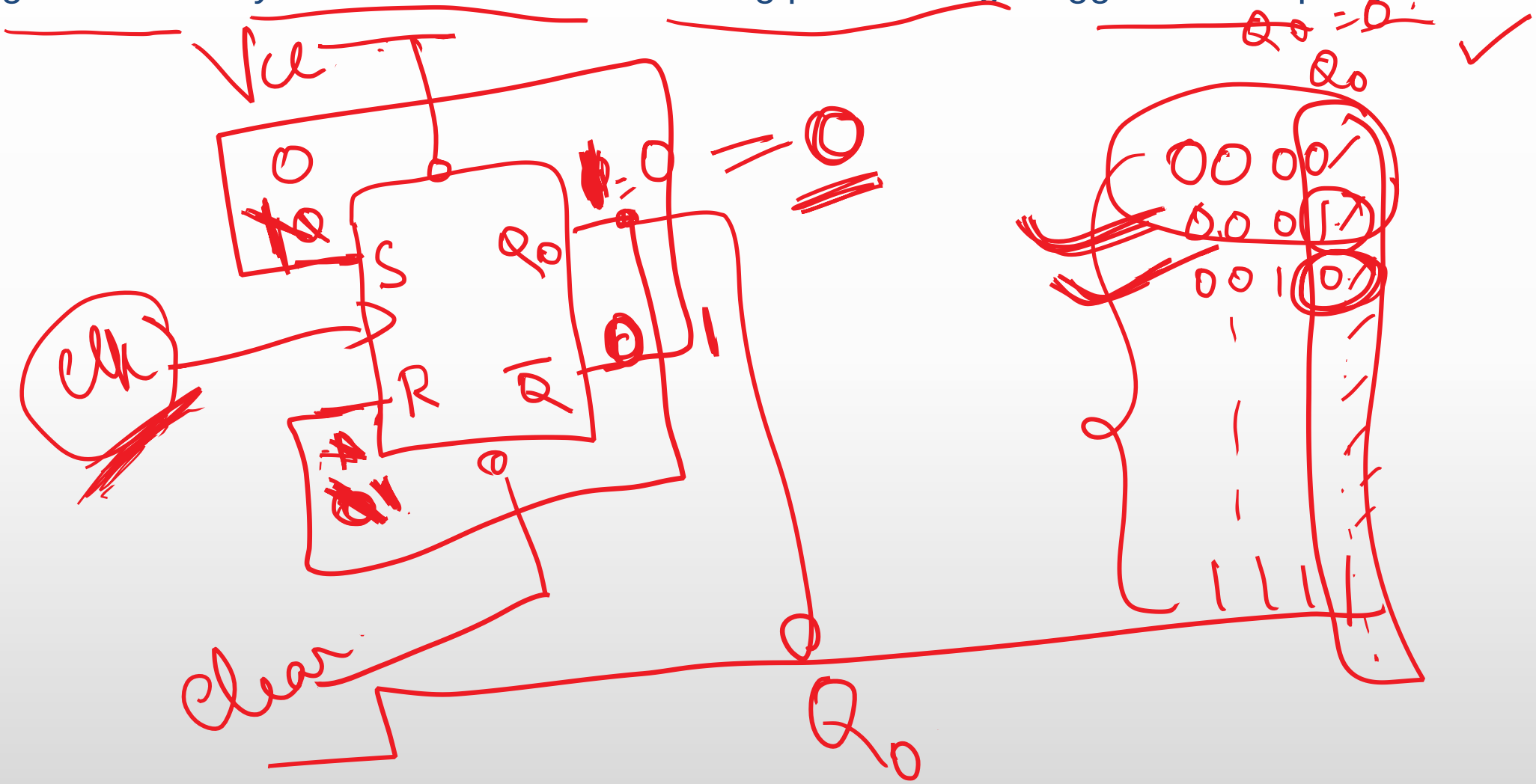
- Design a 3 – bit (MOD 8/Divide by 8) Asynchronous UP counter using negative edge triggered D flip flops.



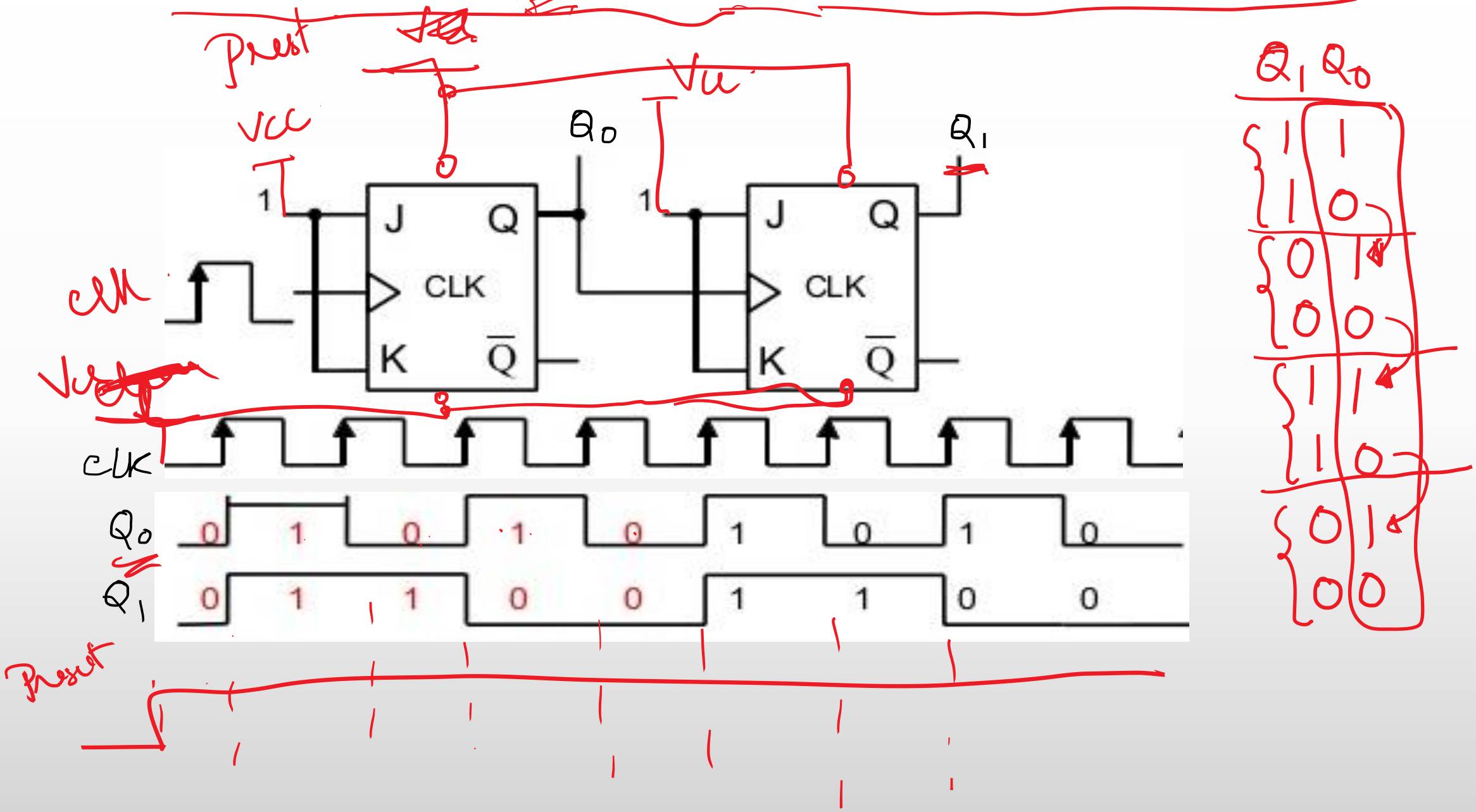
- Design a 3 – bit Asynchronous UP counter using positive edge triggered D flip flops.



- Design a 4 – bit (MOD 16/ Divide by 16) Asynchronous UP counter using negative edge triggered SR flip flops.
- Design a 4 – bit Asynchronous UP counter using positive edge triggered SR flip flops.

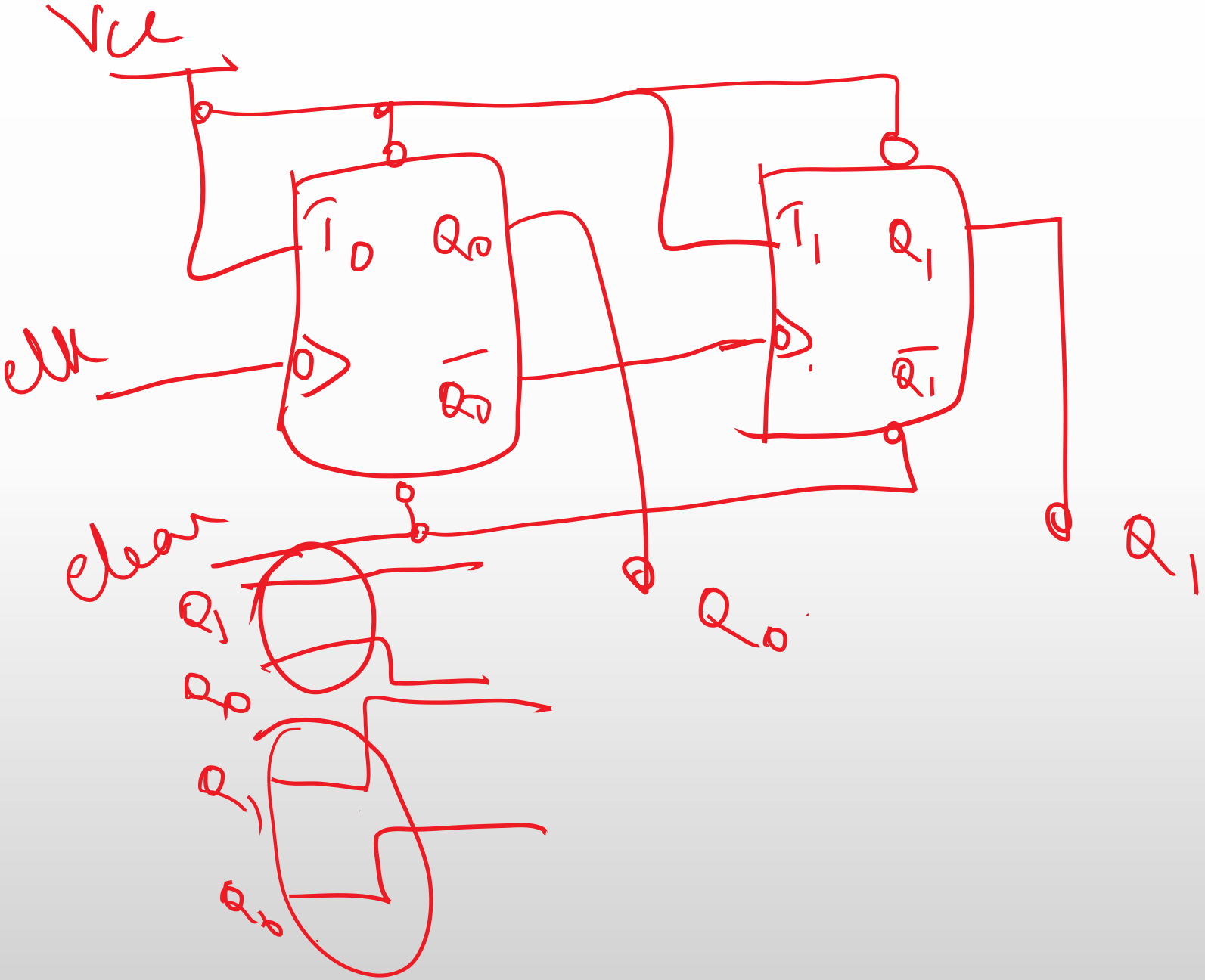


- Design a 2 – bit Asynchronous DOWN counter using positive edge triggered JK flip flops.

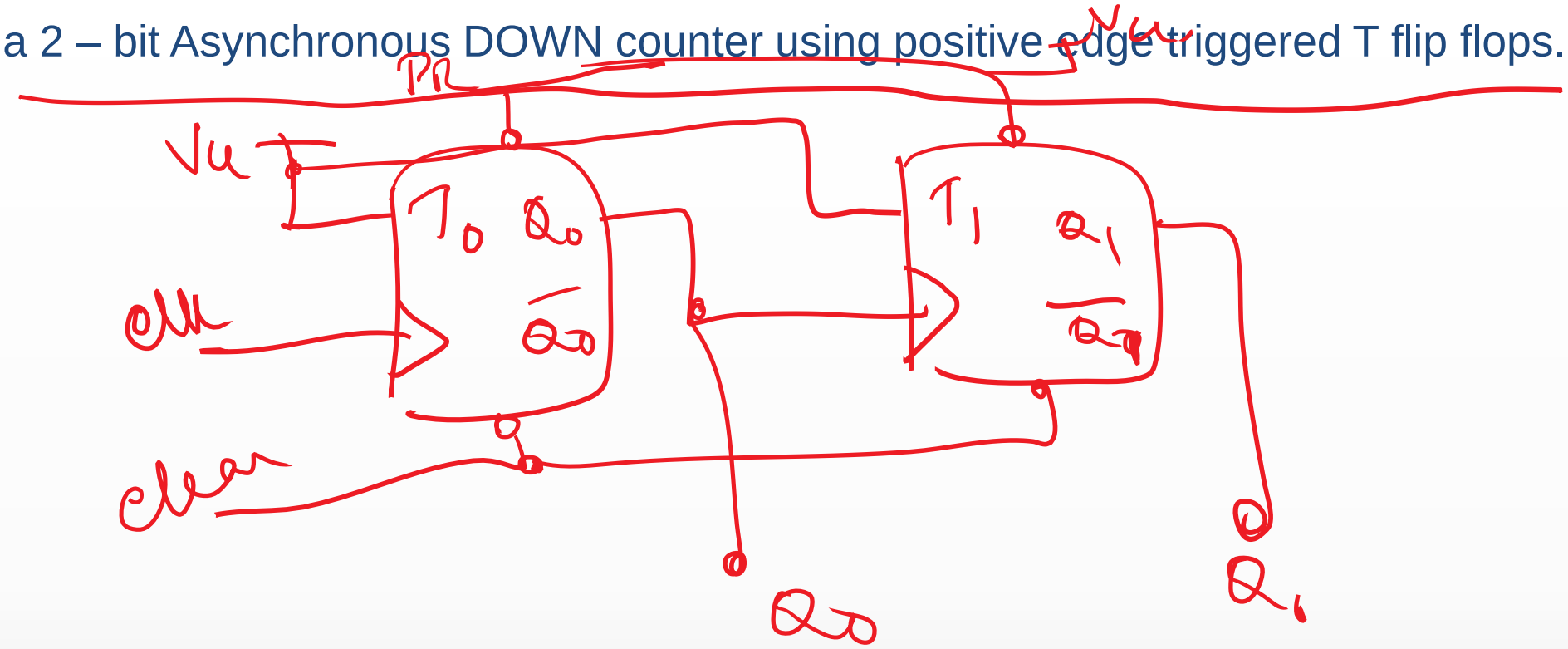


- Design a 2 – bit Asynchronous DOWN counter using negative edge triggered JK flip flops.

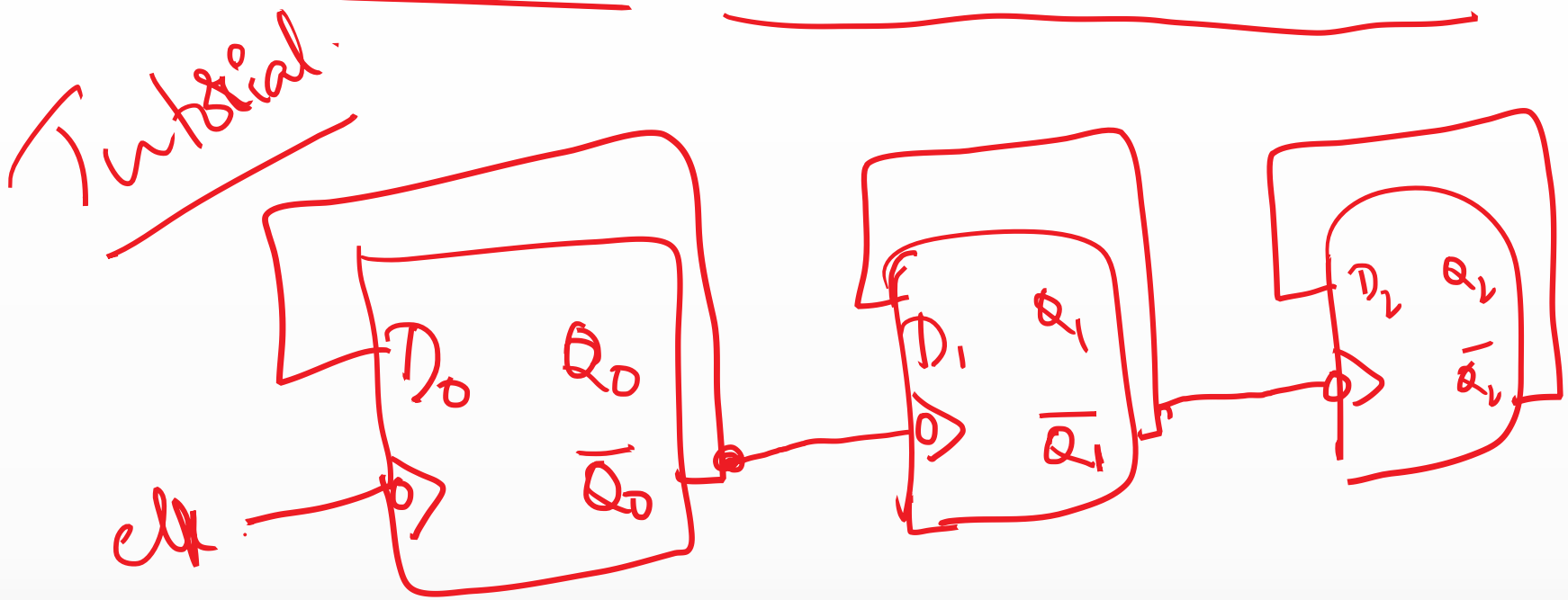
- Design a 2 – bit Asynchronous DOWN counter using negative edge triggered T flip flops.



- Design a 2 – bit Asynchronous DOWN counter using positive edge triggered T flip flops.



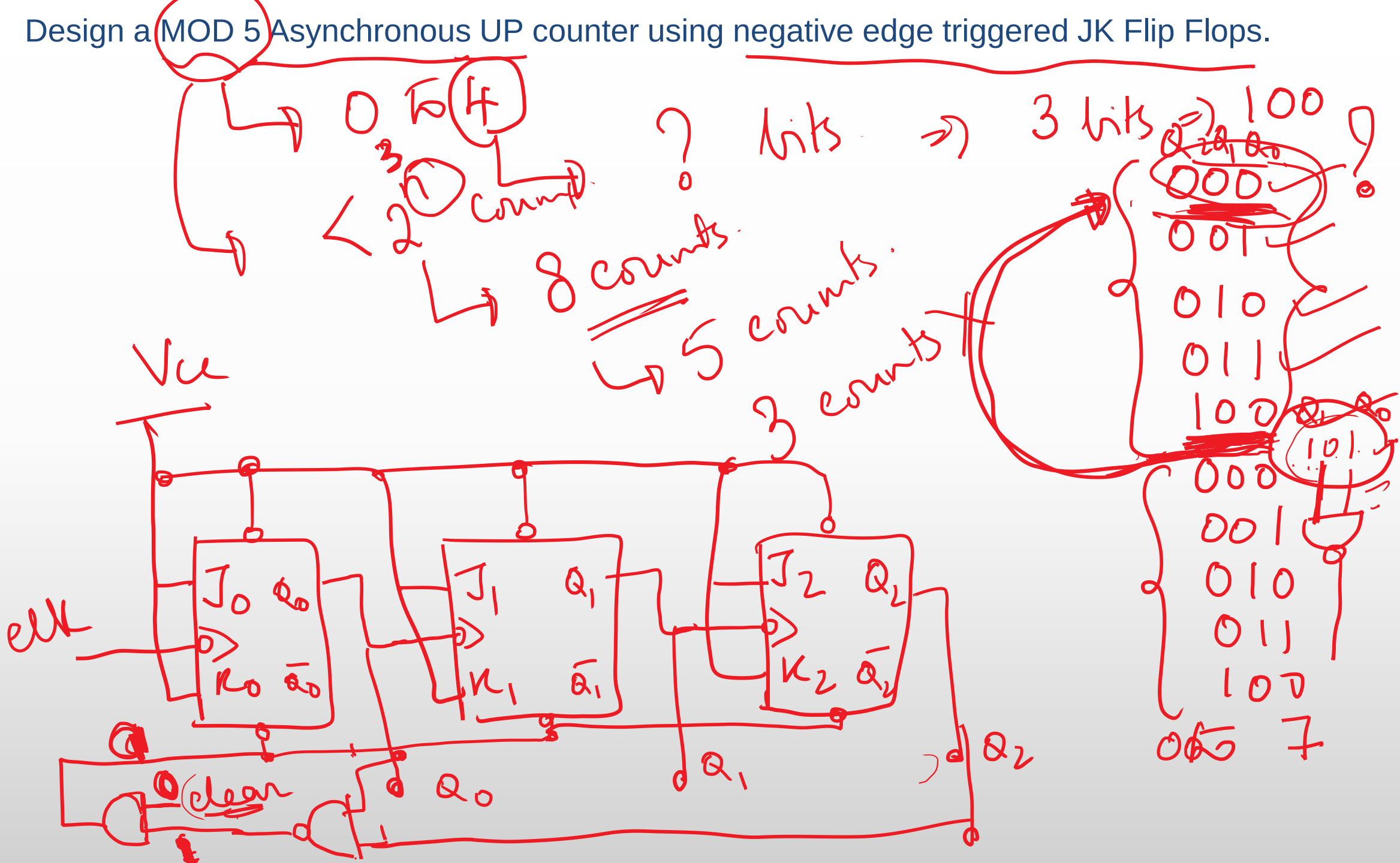
- Design a 3 – bit Asynchronous DOWN counter using negative edge triggered D flip flops.



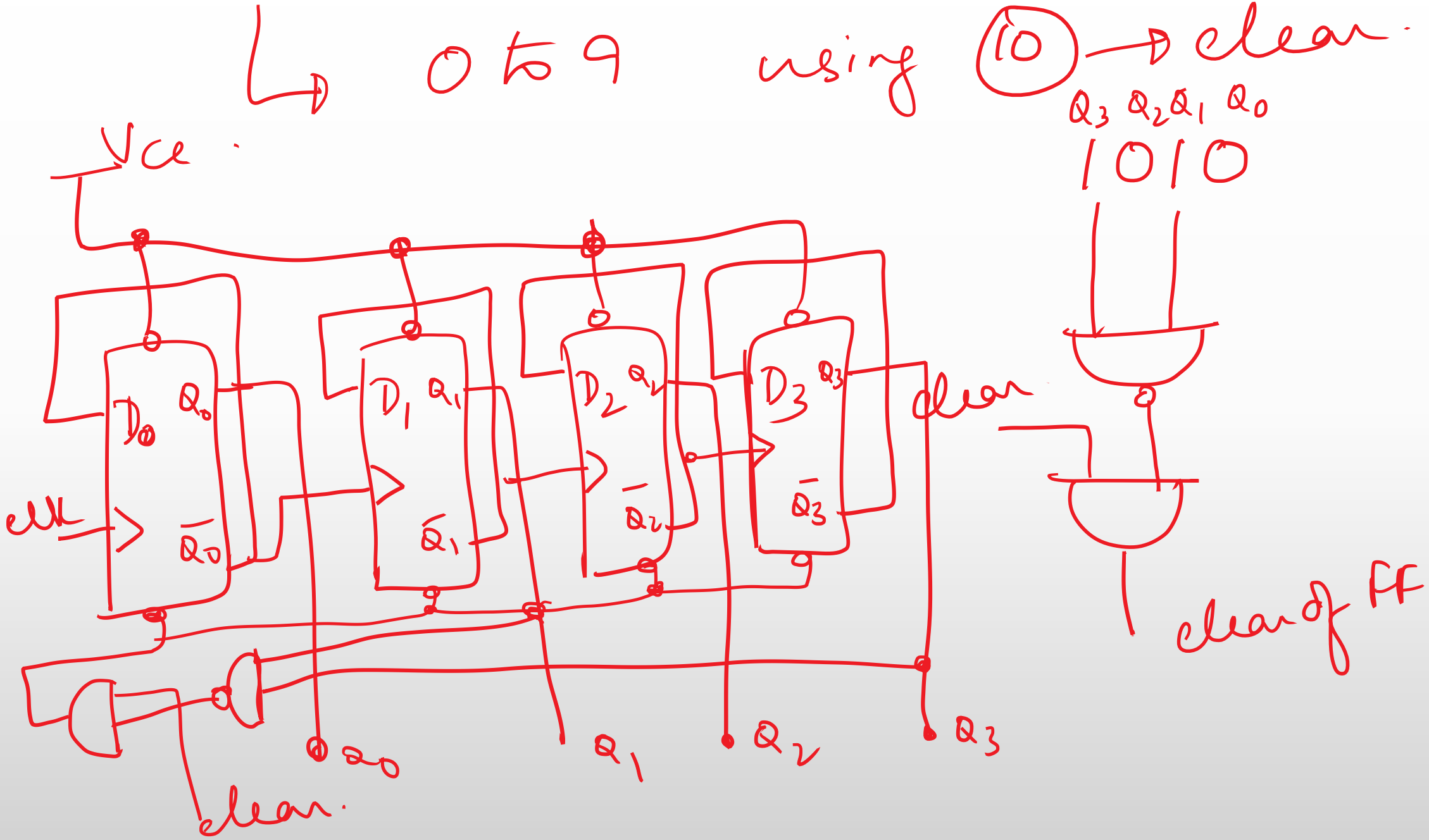
- Design a 3 – bit Asynchronous DOWN counter using positive edge triggered D flip flops.

- Design a 4 – bit Asynchronous DOWN counter using negative edge triggered SR flip flops.
- Design a 4 – bit Asynchronous DOWN counter using positive edge triggered SR flip flops.

- Design a MOD 5 Asynchronous UP counter using negative edge triggered JK Flip Flops.

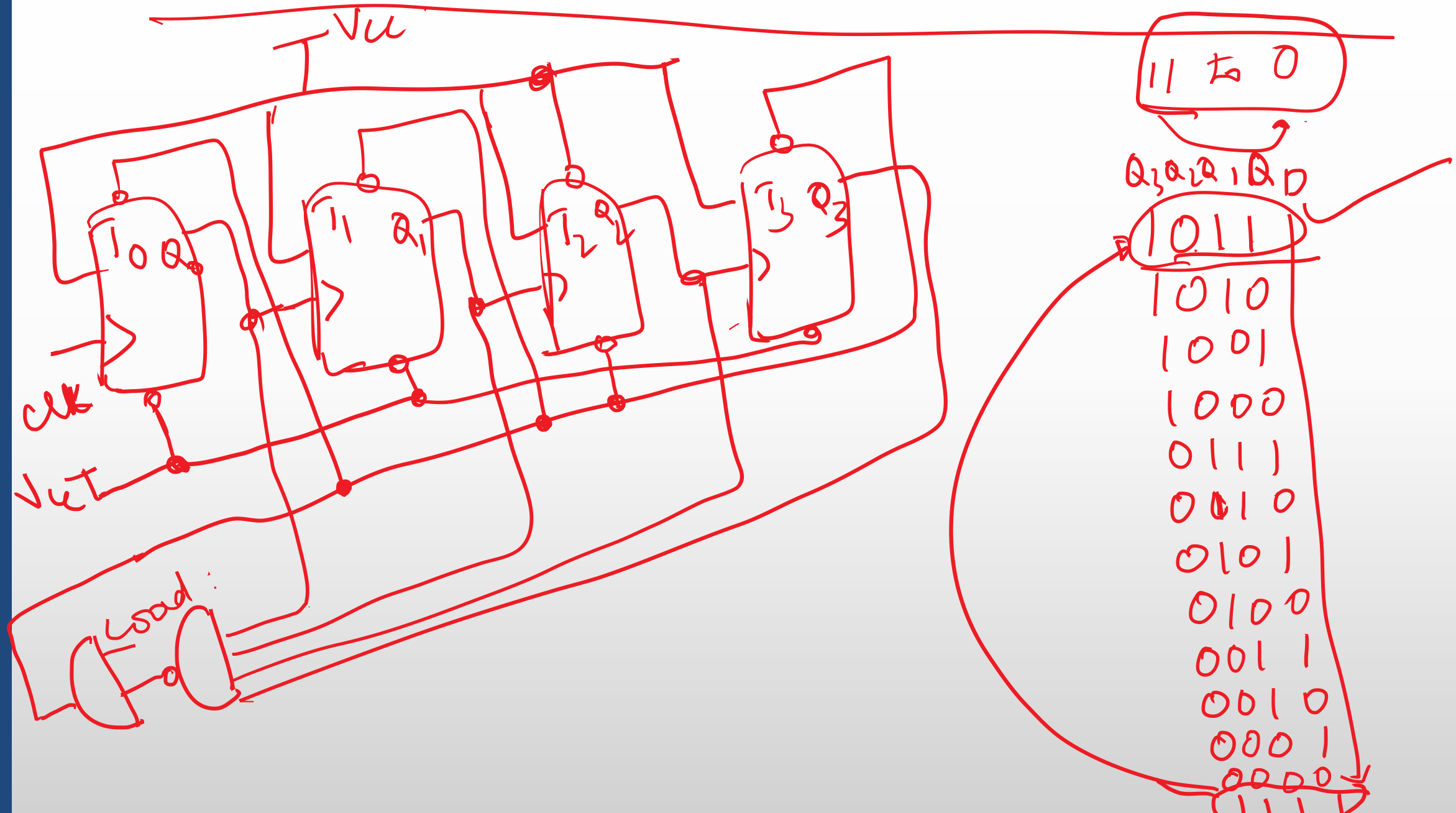


- Design a MOD 10 Asynchronous UP counter using positive edge triggered D Flip Flops.

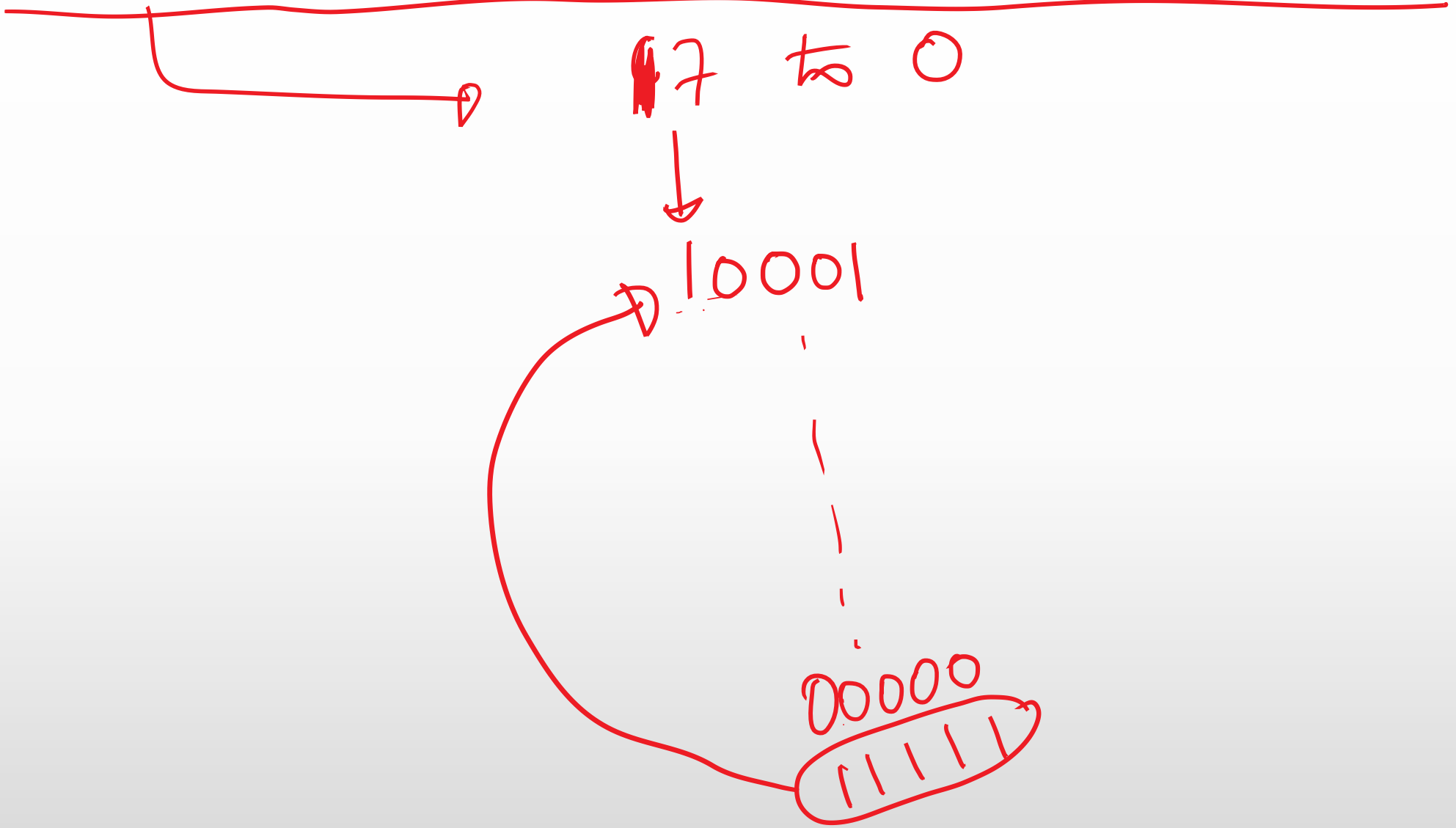


MOD 16

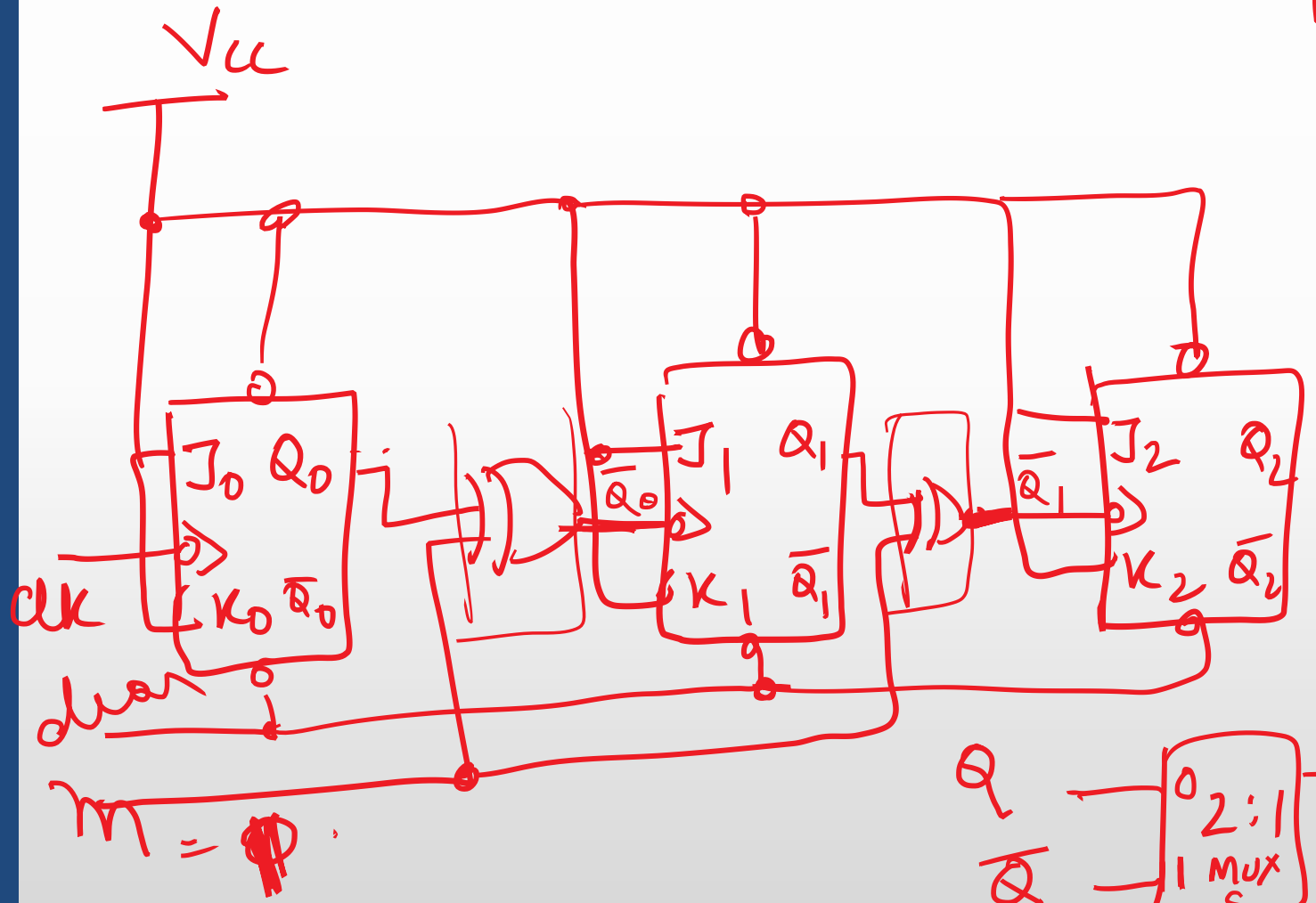
- Design a MOD 12 Asynchronous DOWN counter using positive edge triggered T Flip Flops.



- Design a MOD 18 Asynchronous DOWN counter using positive edge triggered JK Flip Flops.



- Design a 3 bit Asynchronous UP/DOWN counter using negative edge triggered JK Flip Flops.



m = 0 ⇒ UP count

m = 1 ⇒ DOWN count.

-ve ⇒ m = 0 ⇒ clk = Q

m = 1 ⇒ clk = Q̄

using Basic gates