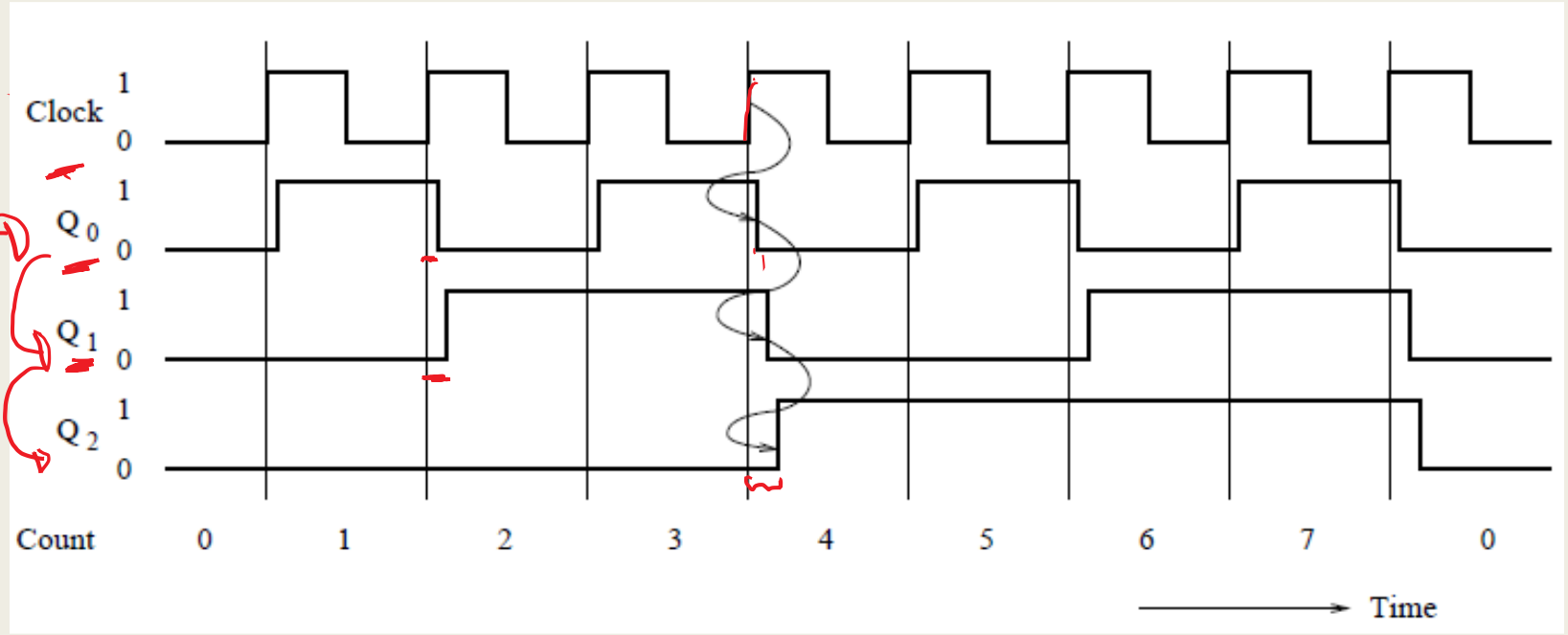
Synchronous counters

- Limitations of asynchronous counters
- Synchronous counter design
- Synchronous counter IC

Limitation of asynchronous counters



Limitations: 1. Not suitable for high frequency applications
2. Not suitable for higher mod counters

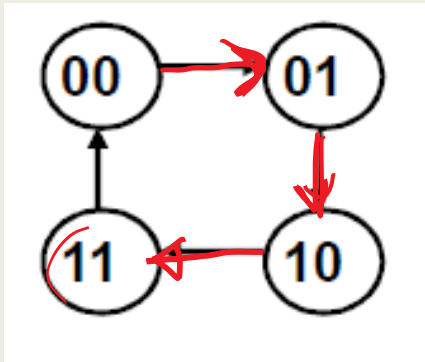
Synchronous counter design

- All the flip flops are clocked simultaneously using same clock.
- Suitable for high frequency applications
- Designed using sequential circuit design process which can be used for any synchronous circuit designs

1. Design 2-bit synchronous binary UP counter using T ffs

- Counter states: 00 → 01 →10 →11

State diagram



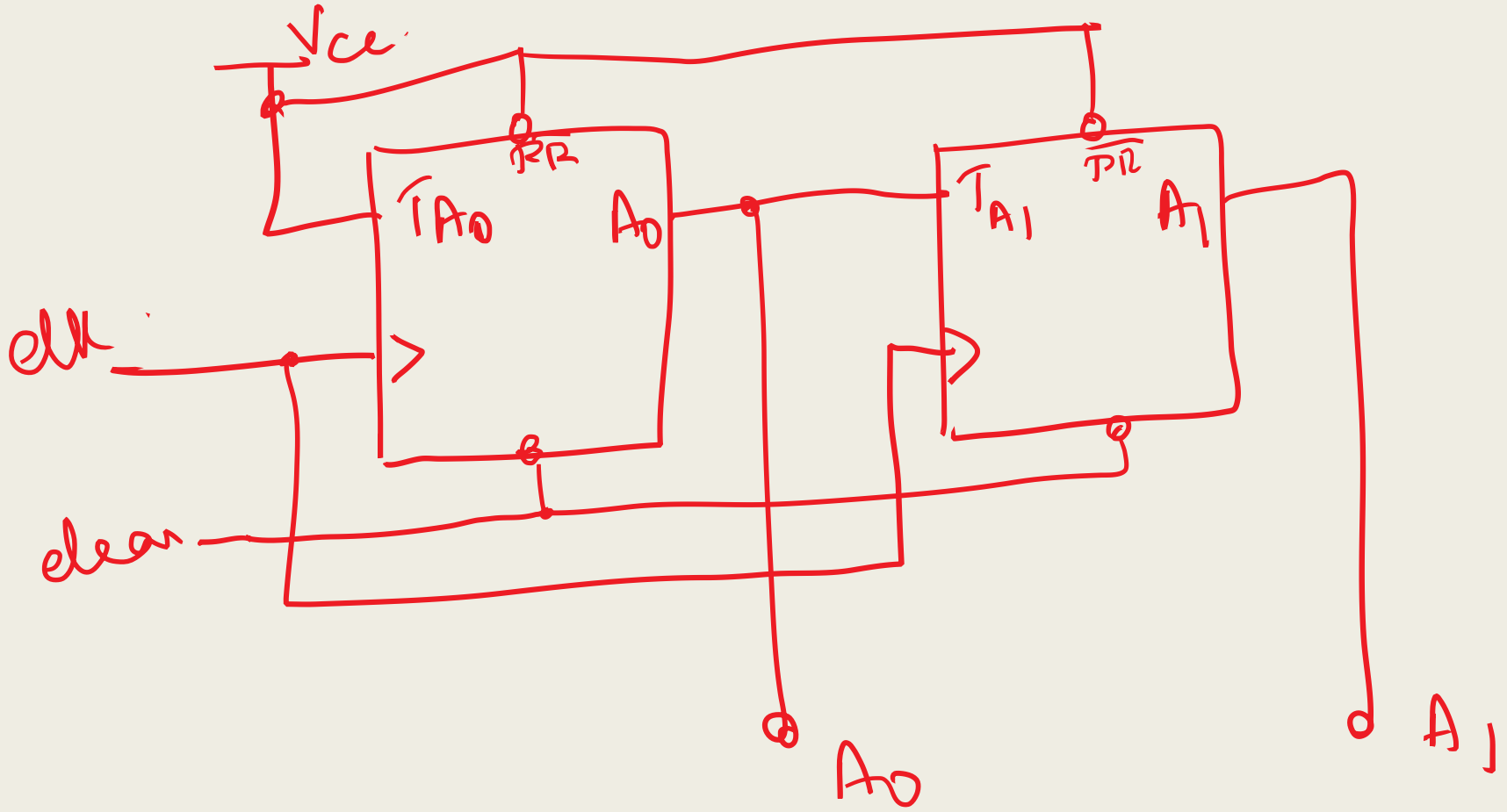
State table

Present state		Next state		Flip-flop inputs	
A_1	A_0	A_1^+	A_0^+	TA_1	TA_0
0	0	0	1	0	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	0	0	1	1

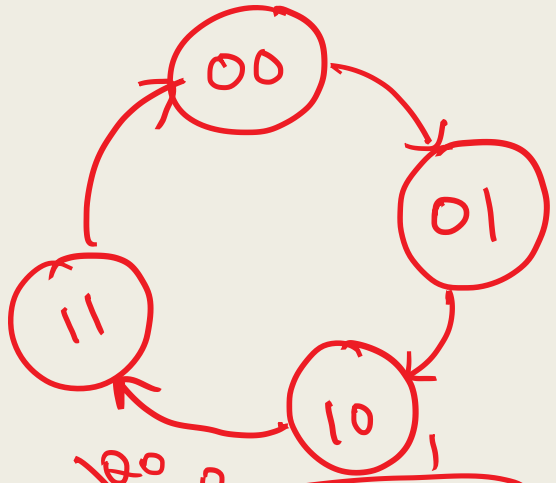
$TA_1 = A_0$

$TA_0 = 1$

2-bit synchronous binary UP counter using T ffs : circuit diagram



2. Design 2-bit synchronous binary UP counter using JK ffs



P.S.	N.S	J_1 K_1	J_0 K_0
Q_1 Q_0	Q_1 Q_0		
0 0	0 1	0 X	1 X
0 1	1 0	1 X	X 1
1 0	1 1	X 0	1 X
1 1	0 0	X 1	X 1

J_1 :-

Q_1 \ Q_0	0	1
0	0	1
1	X	X

$J_1 = Q_0$

K_1 :-

Q_1 \ Q_0	0	1
0	X	X
1	0	1

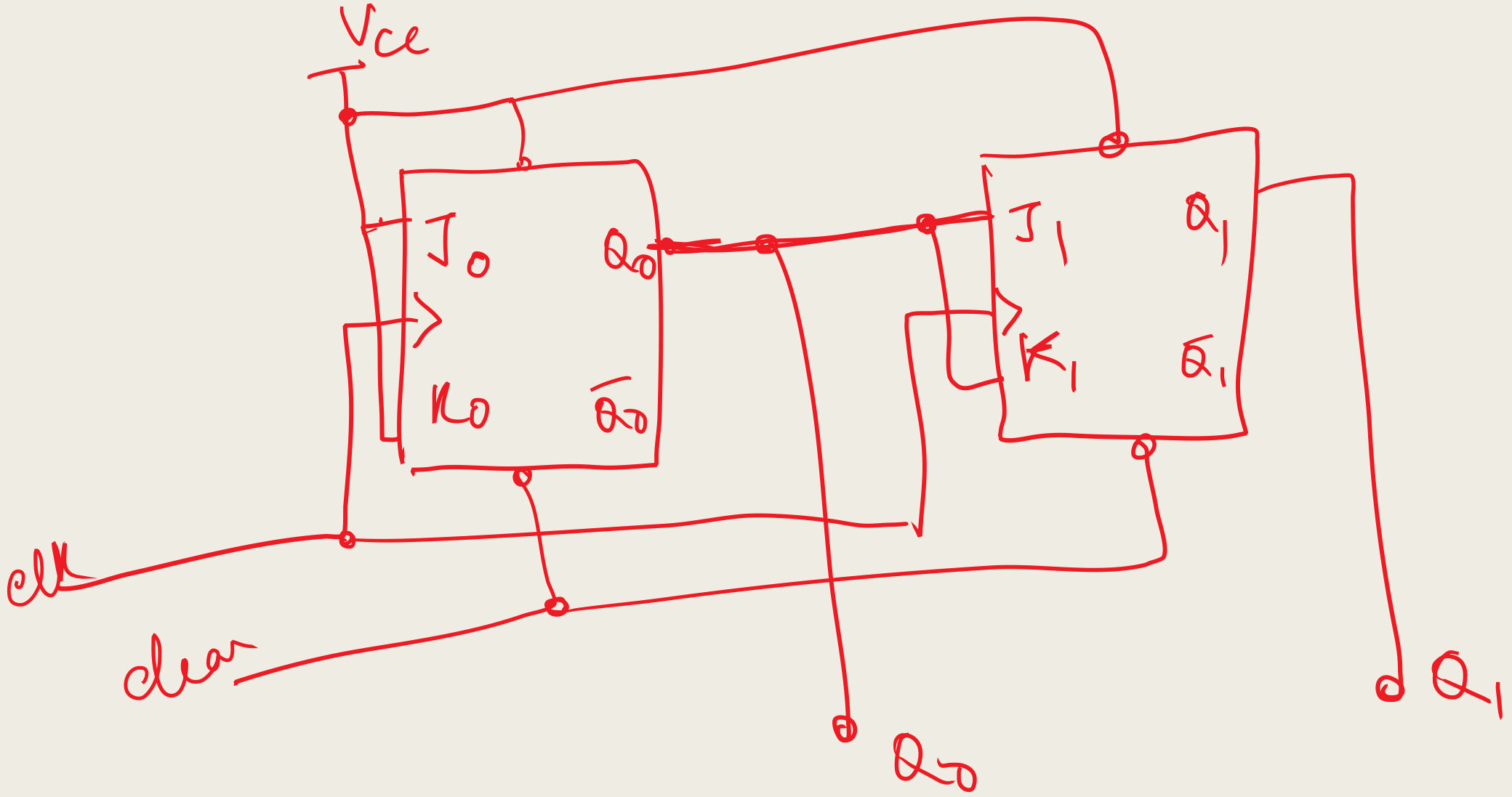
$K_1 = Q_0$

$J_0 = 1$ $\quad K_0 = 1$

FT & JK FF

P.S	N.S	J K
0	0	0 0 / 0 1 } 0X
0 → 1		1 0 / 1 1 } 1X
1	1	0 0 / 1 0 } X0
1 → 0 → 1		1 1 / 0 1 } X1

2-bit synchronous binary UP counter using JK ffs contd..

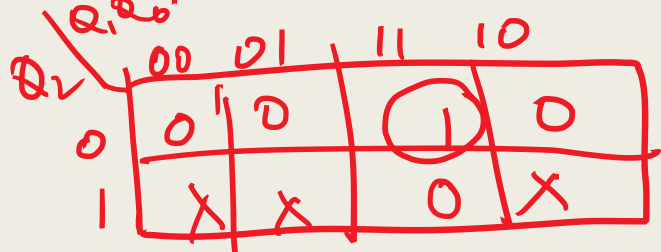


3. Design 3-bit synchronous binary UP counter (MOD 8) using SR ffs

FT of SR ff.

P.S. $Q_2\ Q_1\ Q_0$	N.S $Q_2\ Q_1\ Q_0$	$S_2\ R_2$	$S_1\ R_1$	$S_0\ R_0$
0 0 0	0 0 1	0 x	0 x	1 0
0 0 1	0 1 0	0 x	1 0	0 1
0 1 0	0 1 1	0 x	x 0	1 0
0 1 1	1 0 0	1 0	0 1	0 1
1 0 0	1 0 1	x 0	0 x	1 0
1 0 1	1 1 0	x 0	1 0	0 1
1 1 0	1 1 1	x 0	x 0	1 0
1 1 1	0 0 0	0 1	0 1	0 1

$Q \to Q$	S	R	
0 → 0	0	0	0x
	0	1	
0 → 1	1	0	
1 → 1	0	0	x0
	1	0	
1 → 0	0	1	



$S_2 = \bar{Q}_2 Q_1 Q_0$

$R_2 = Q_2 Q_1 Q_0$

3-bit synchronous binary UP counter (MOD 8)using SR ffs

$S_2 =$

$R_2 =$

$S_1 =$

$R_1 =$

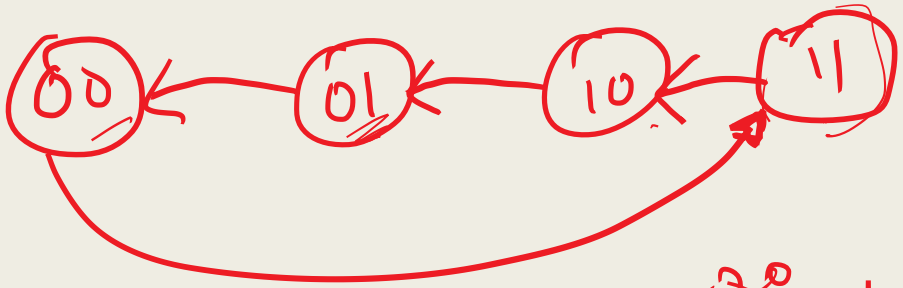
$S_0 =$

$R_0 =$

4. Draw the circuit of 3-bit synchronous binary up counter (MOD 8) using T ffs

- Analyse the previous examples and draw the circuit directly without the design steps.

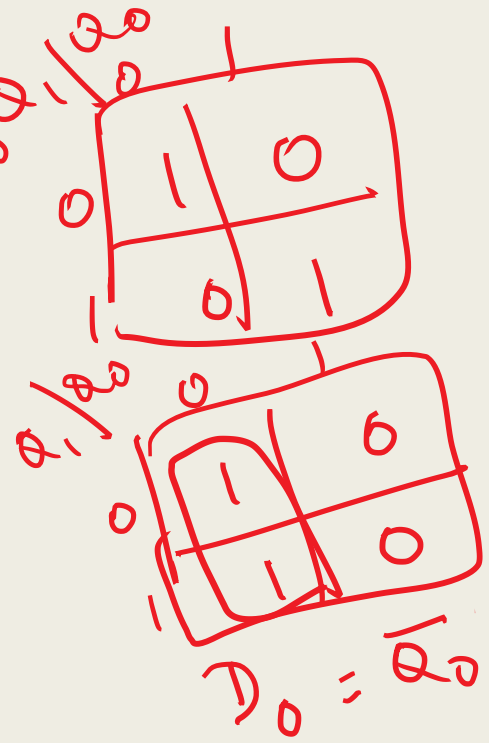
5. Design 2-bit synchronous binary down counter (MOD 4) using D ffs



P.S	N.S	
Q_1Q_0	Q_1Q_0	D_1 D_0
0 0	1 1	1 1
0 1	0 0	0 0
1 0	0 1	0 1
1 1	1 0	1 0

$D_1 = \bar{Q}_1\bar{Q}_0 + Q_1Q_0$

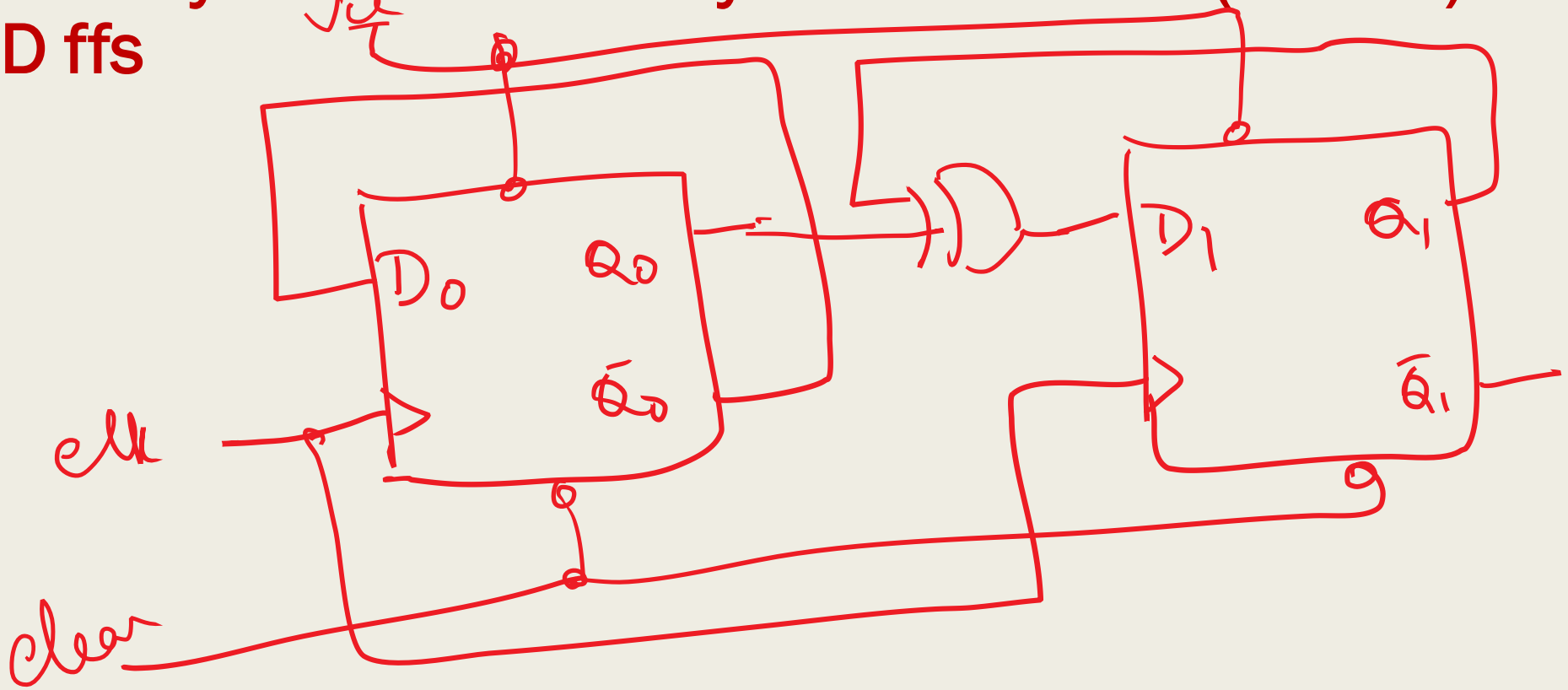
$D_1 = (Q_1 \odot Q_0)$



$D_1 =$

$D_0 =$

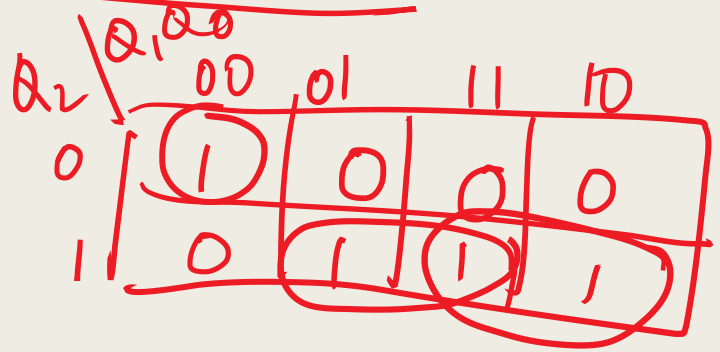
2-bit synchronous binary down counter (MOD 4) using D ffs



6. Design 3-bit synchronous binary down counter (MOD 4) using D ffs

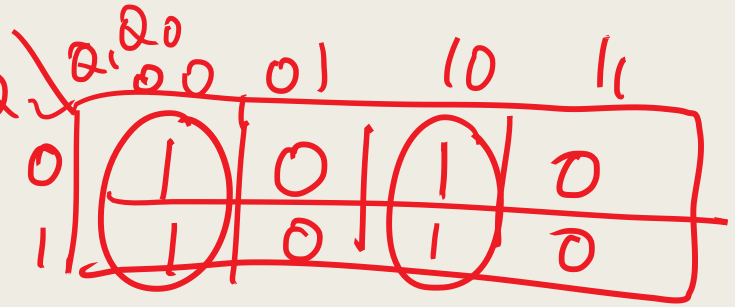
P.S.	N.S	
$Q_2Q_1Q_0$	$Q_2Q_1Q_0$	$D_2\ D_1\ D_0$
000	111	111
001	000	000
010	001	001
011	010	010
100	011	011
101	100	100
110	101	101
111	110	110

D_2 :-



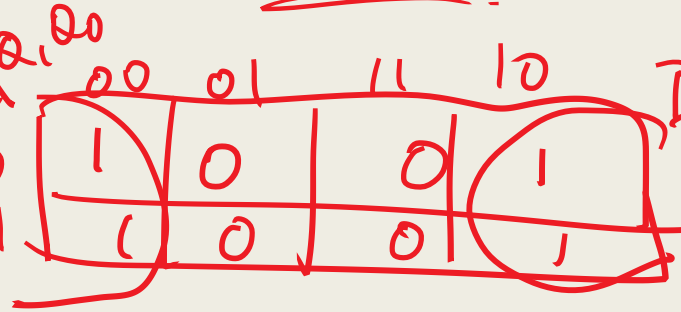
$D_2 = \bar{Q}_2\bar{Q}_1\bar{Q}_0 + Q_2Q_0 + Q_2Q_1$

D_1 :-



$D_1 = \bar{Q}_1\bar{Q}_0 + Q_1\bar{Q}_0$

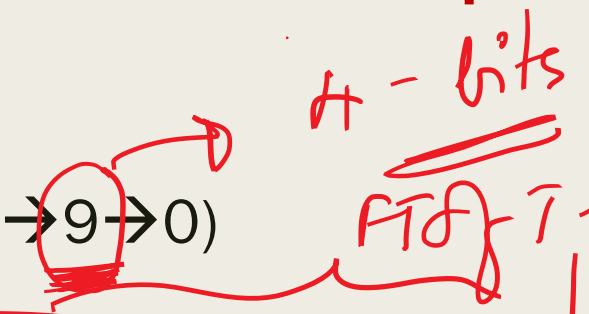
D_0 :-



$D_0 = \bar{Q}_0$

7. Design decade (BCD) synchronous up counter (MOD 10)using T ffs

- (0→1→2→3→4→5→6→7→8→9→0)



P.S $Q_3Q_2Q_1Q_0$	N.S $Q_3Q_2Q_1Q_0$	T_3	T_2	T_1	T_0
0 0 0 0	0 0 0 1	0	0	0	1
0 0 0 1	0 0 1 0	0	0	1	1
0 0 1 0	0 0 1 1	0	0	0	1
0 0 1 1	0 1 0 0	0	1	1	1
0 1 0 0	0 1 0 1	0	0	0	1
0 1 0 1	0 1 1 0	0	0	1	1
0 1 1 0	0 1 1 1	0	0	0	1
0 1 1 1	1 0 0 0	1	1	1	1
1 0 0 0	1 0 0 1	0	0	0	1
1 0 0 1	0 0 0 0	1	0	0	1

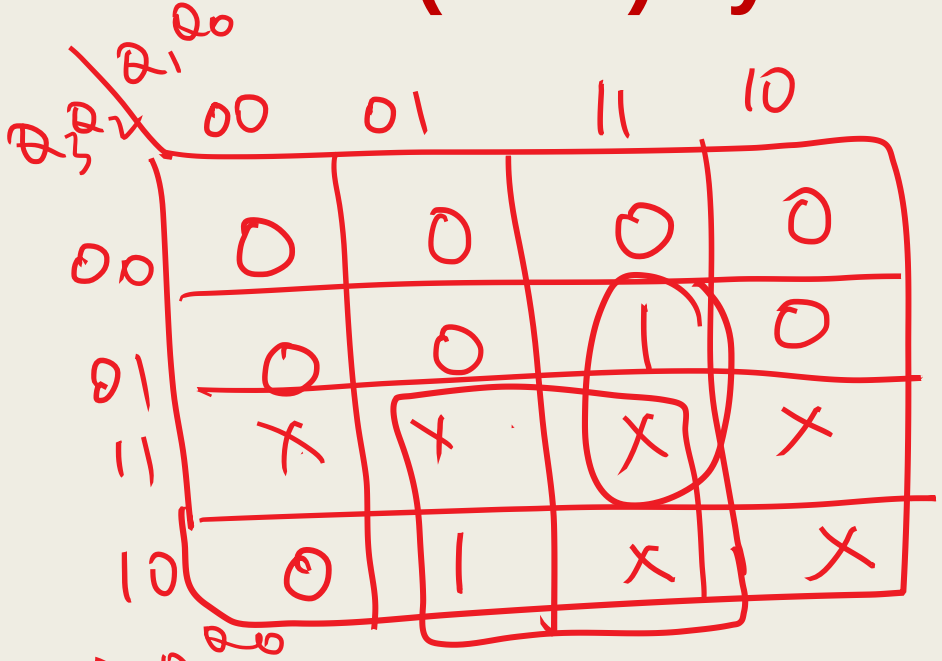
$T_3 =$

$T_2 =$

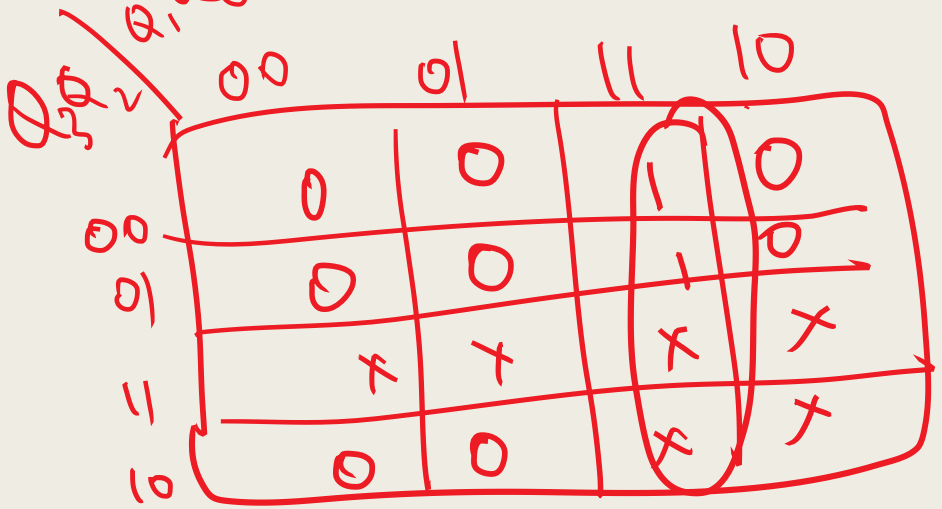
$T_1 =$

$T_0 =$

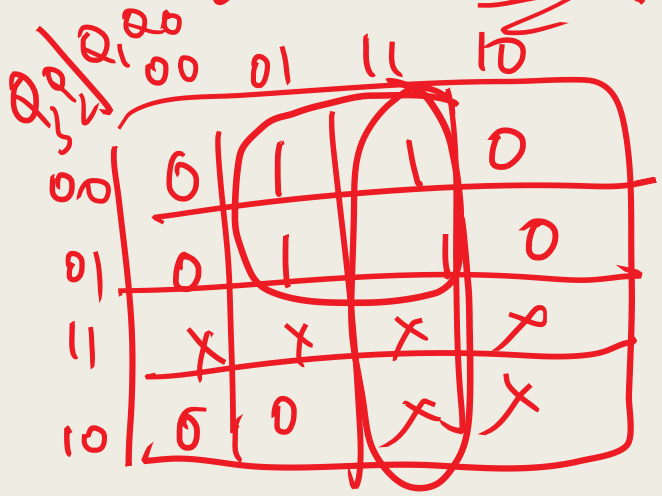
Decade (BCD) synchronous up counter contd..



$$T_3 = Q_3Q_0 + Q_1Q_0$$

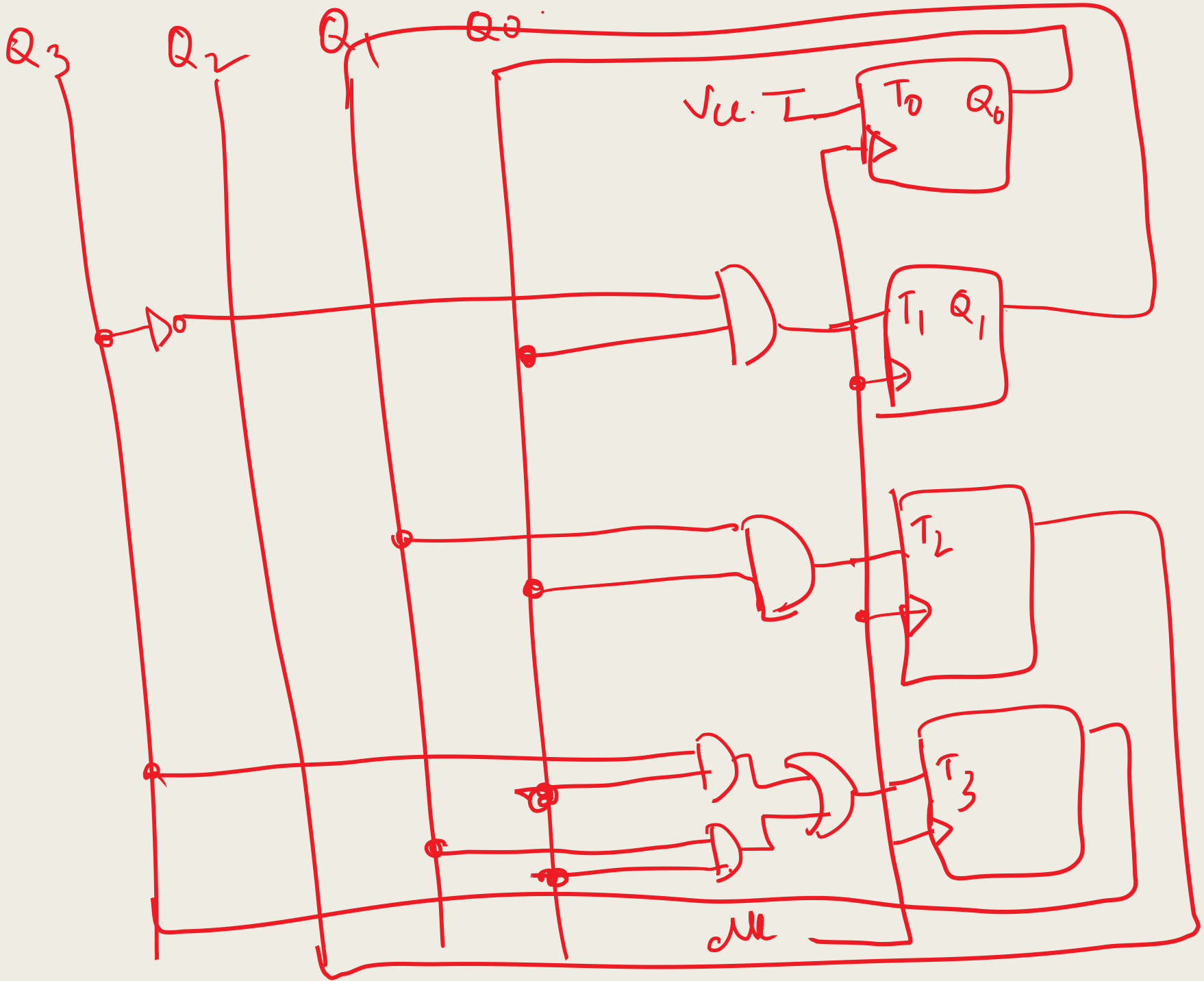


$$T_2 = Q_1Q_0$$



$$T_1 = \overline{Q_3}Q_0$$

$$T_0 = 1$$


Q3
Q2
Q1
Q0
Vcc
T0
Q0
T1
Q1
T2
T3

- Questions: ?