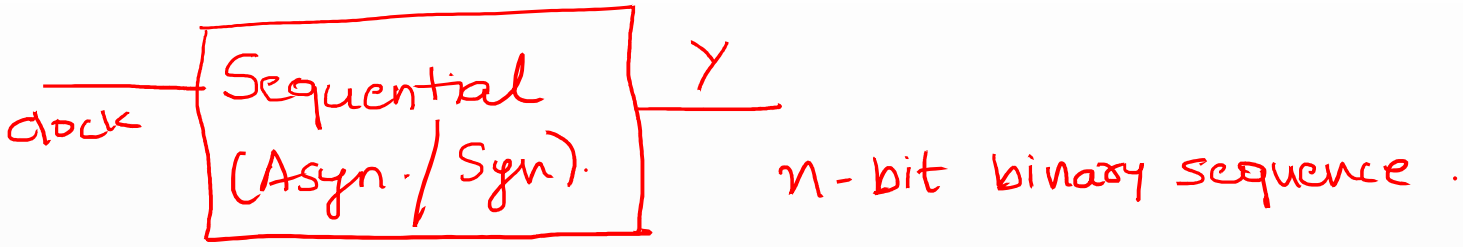
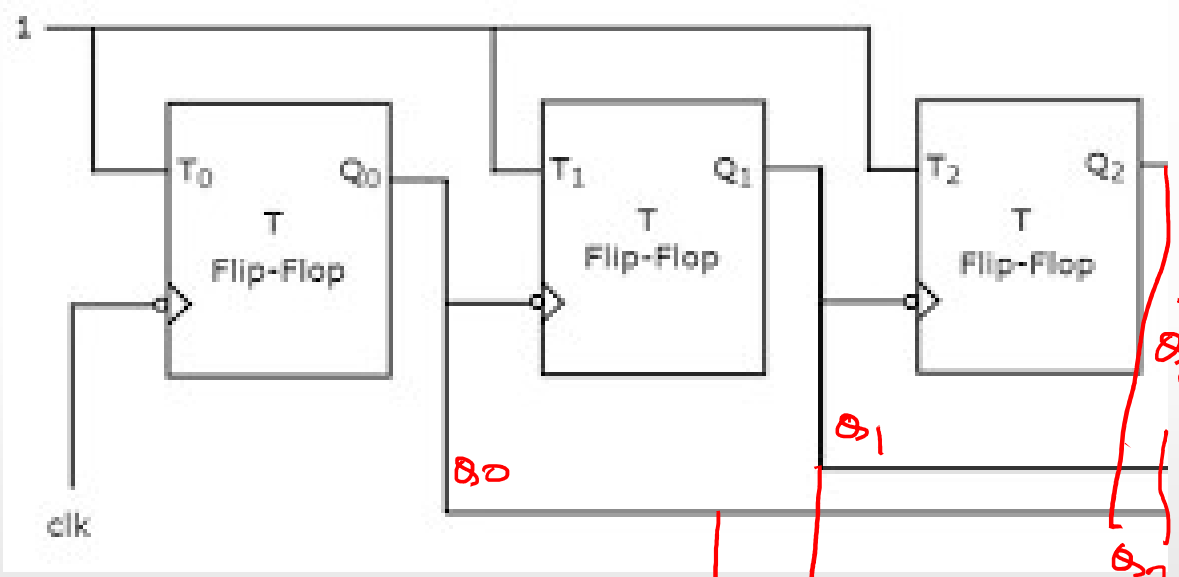
SEQUENCE GENERATORS, SHIFT REGISTERS AND SHIFT REGISTER COUNTERS

Sequence generator:



Sequence Generator

- Design a sequence generator circuit to generate the sequence 10111100 using Asynchronous counter. Use negative edge triggered T flip flop for the design.
  - *MOD 8 counter*



8-bit

MOD-8

8-states

1st clk

$Y(Q_2, Q_1, Q_0)$

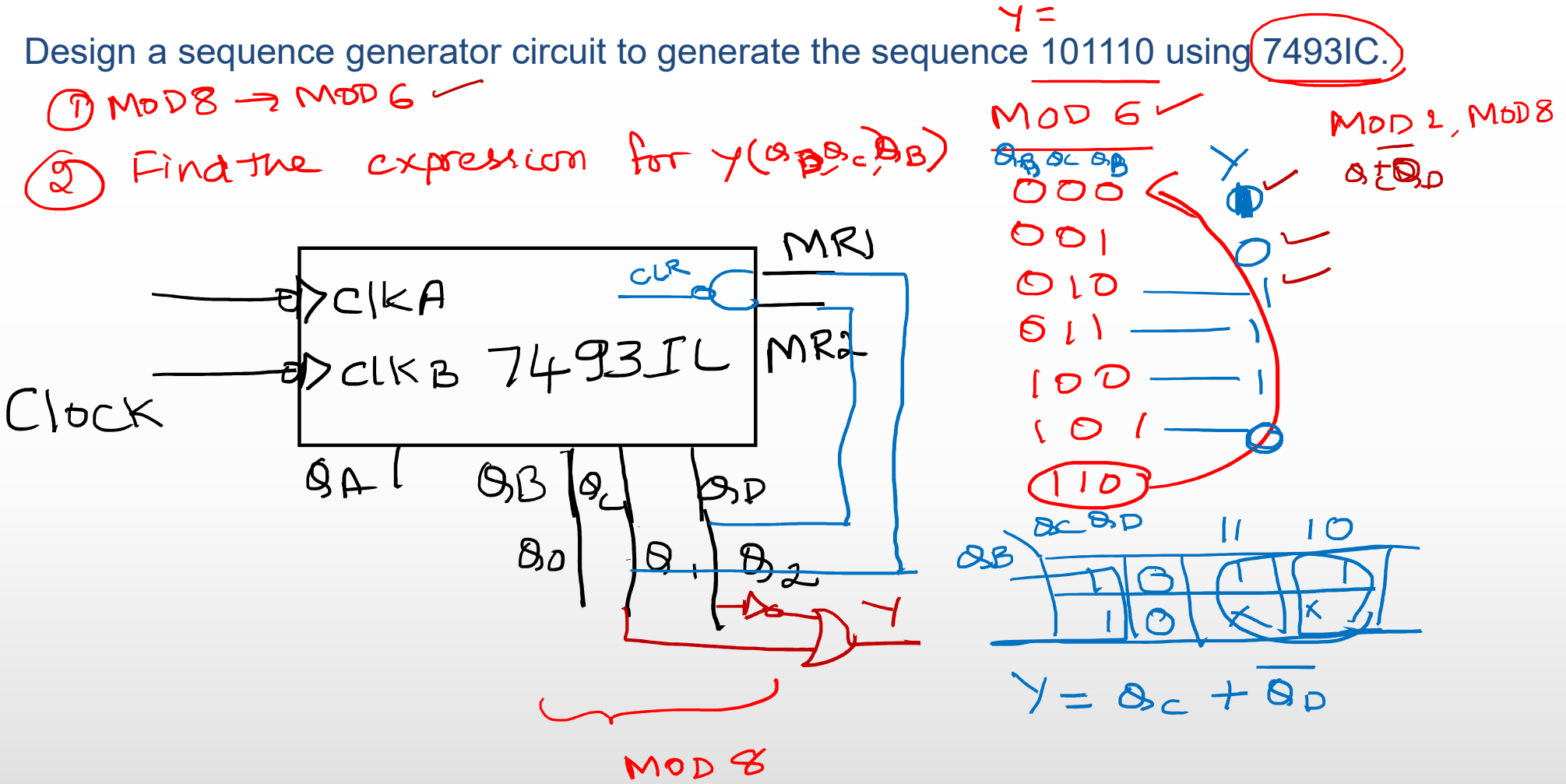
Q_1Q_0 / Q_2	00	01	11	10
Q_2	1	0	1	1
	1	1	0	0

$Y = Q_1Q_0 + Q_2Q_1 + \overline{Q_2}\,\overline{Q_1}$

8th clk

Q2	Q1	Q0	Y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

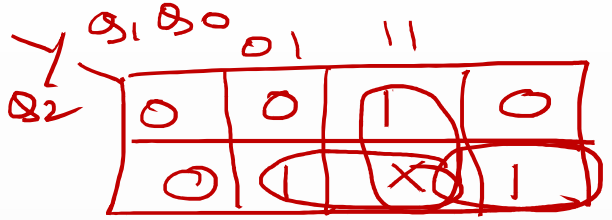
- Design a sequence generator circuit to generate the sequence 101110 using 7493IC.



- Design a sequence generator circuit to generate the sequence 0001011 using synchronous counter. Use D flip flop for the design.

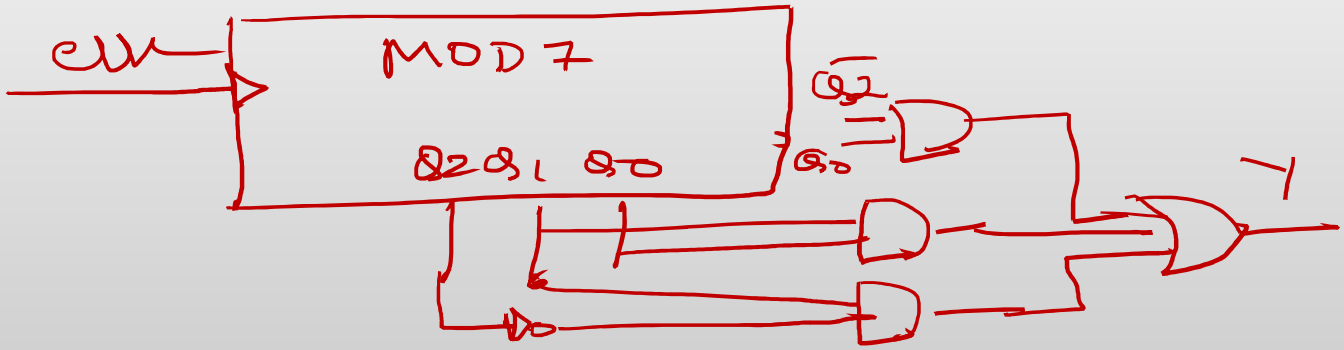
~~3~~-bit MOD 7 0–1–2 ··· 6

Present	Next state	$D_2 D_1 D_0$	Y
000	001	001	0
001	010	010	0
010	011	011	0
011	100	100	1
100	101	101	0
101	110	110	1
110	000	000	1
111	000	000	X



$Y = Q_1Q_0 + \bar{Q}_2Q_0 + \bar{Q}_2Q_1$

Derive the expressions for $D_2 D_1 D_0$



Generate the sequence: 10101 11100 using

74193 IC & external gates.

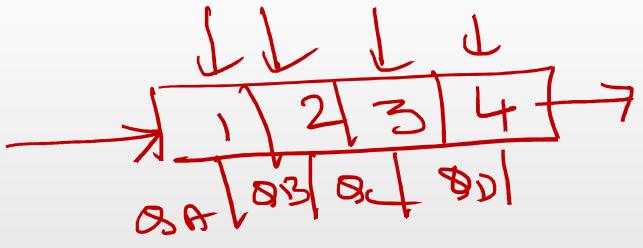
Try

Registers

C = A + B

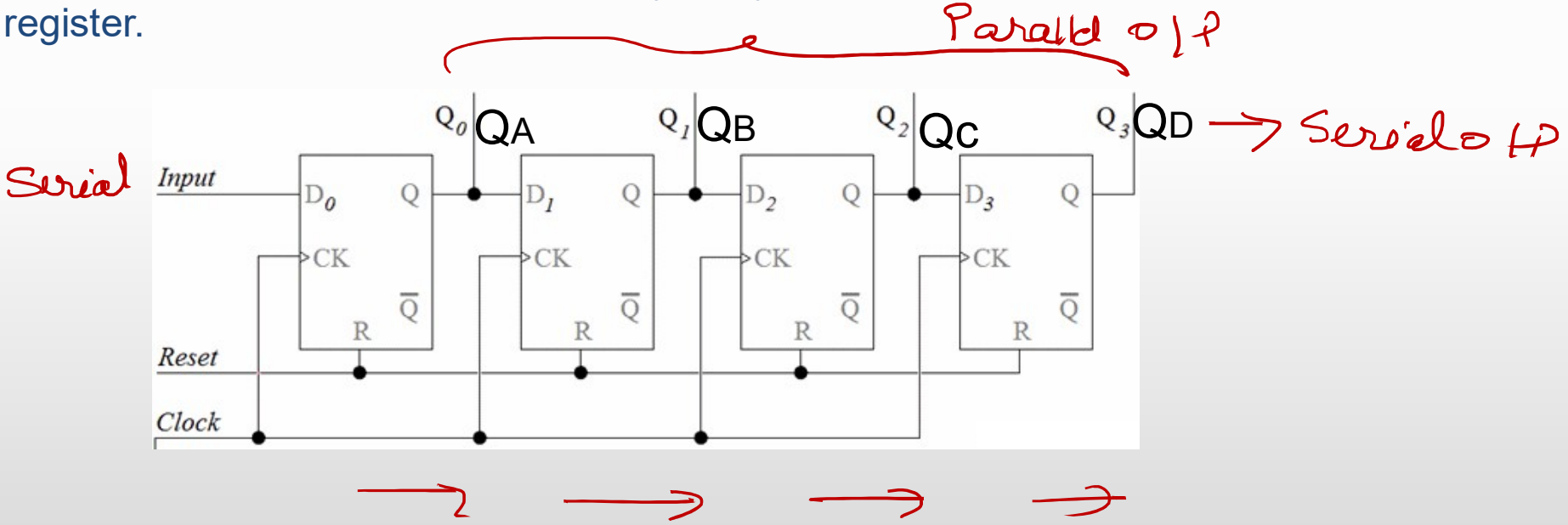
n - bit register

- Register is a group of flip flops (D, or SR,or JK)
- Each flip flop can store one-bit data. n-bit register can hold n-bit data.
- There are two ways to shift the data into the register and two ways to shift the data out of the register.
- Accordingly: 4 categories of shift register are
  - *Serial in Serial out (SISO)*
  - *Serial In parallel out (SIPO)*
  - *Parallel in Serial out (PISO)*
  - *Parallel in parallel out (PIPO)*

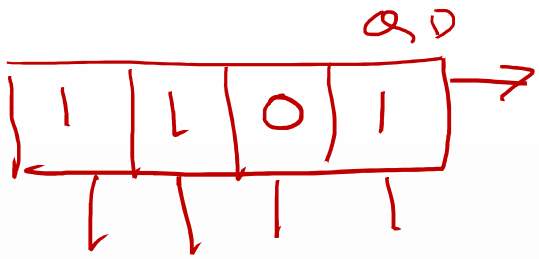


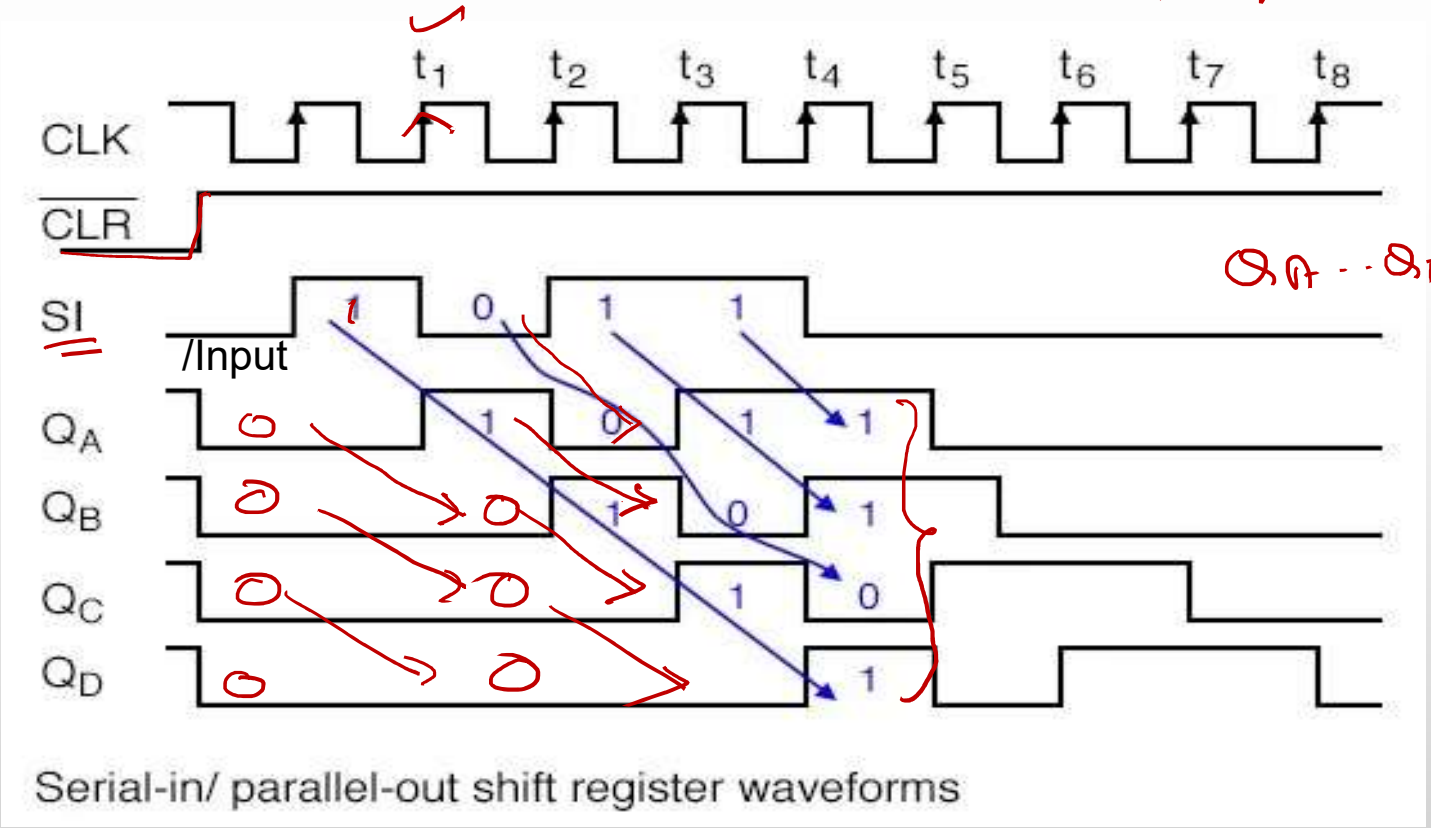
SISO and SIPO Register

- Simple 4-bit shift register is shown below (Reset is nothing but clear input)
- Register is cleared using reset/clear input.
- It can be used as Serial-in serial out (at Q_D) and Serial-in parallel out shift register.



4-bit shift register (Serial-in)



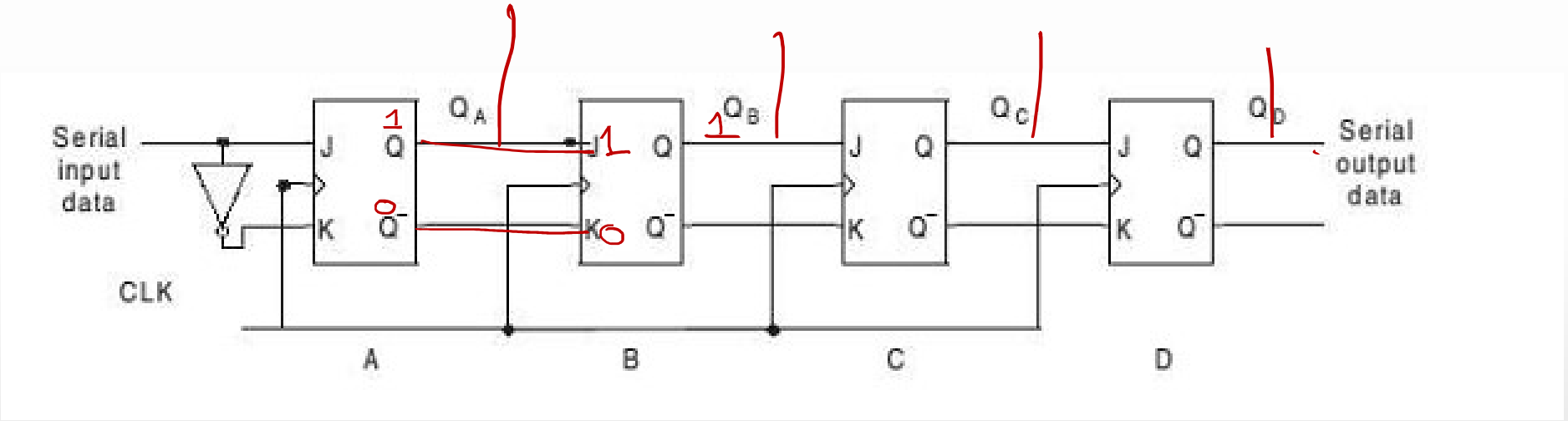


Serial-in/ parallel-out shift register waveforms

$Q_A \ldots Q_D = 1101$

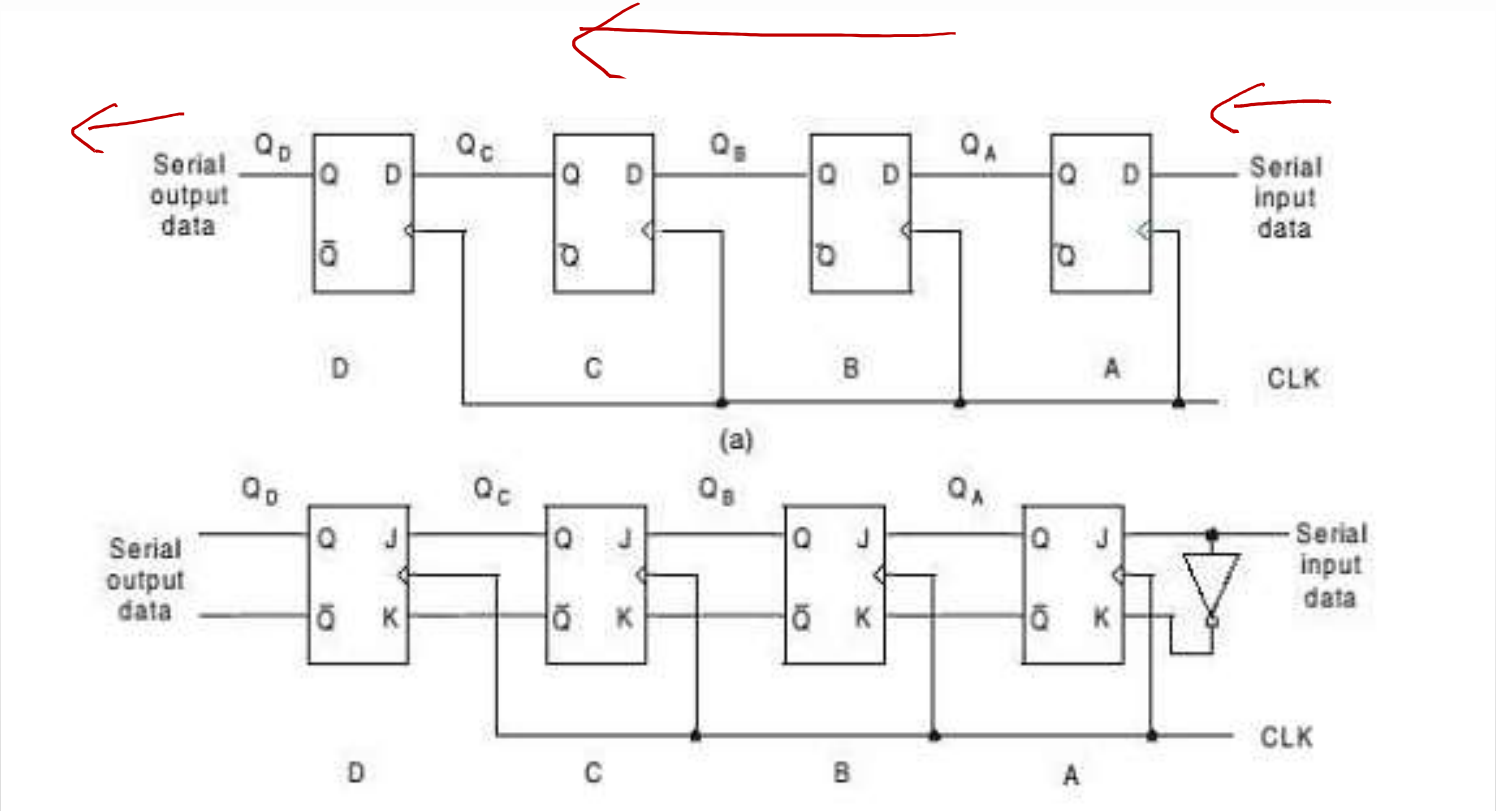
SISO

SISO and SIPO Register using JK ffs

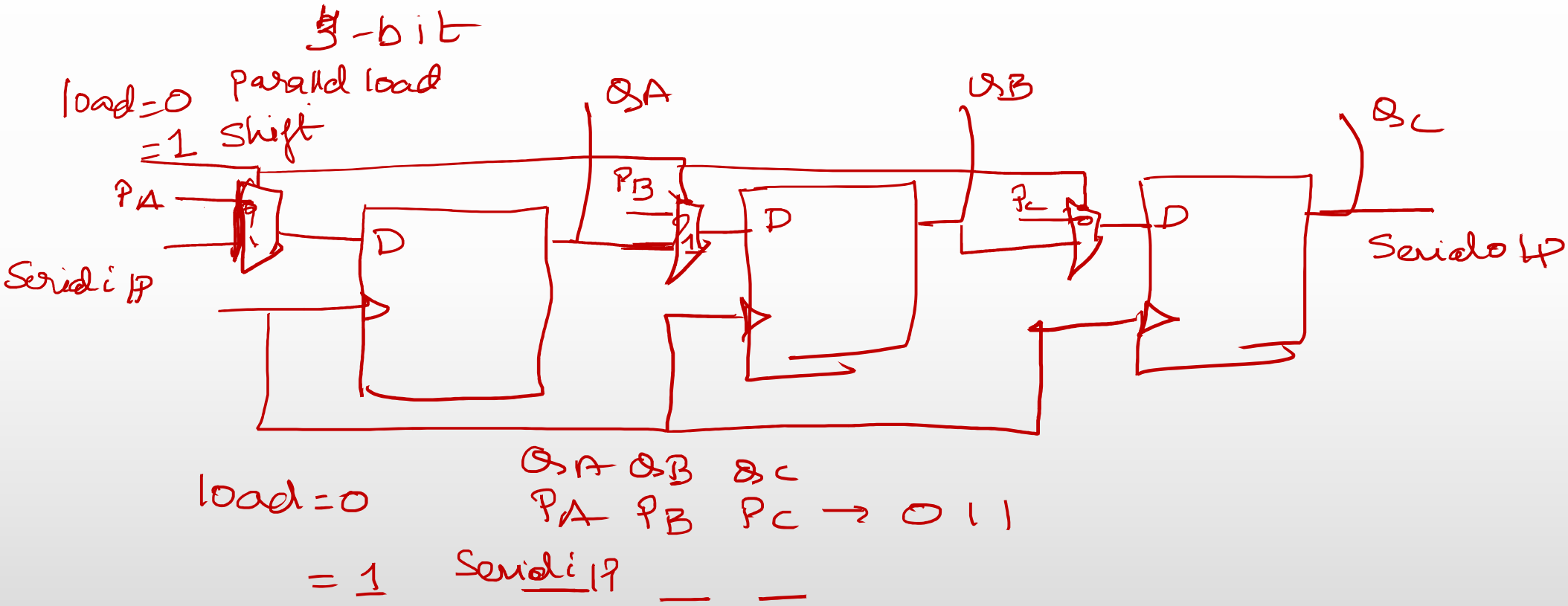


SR-ffs

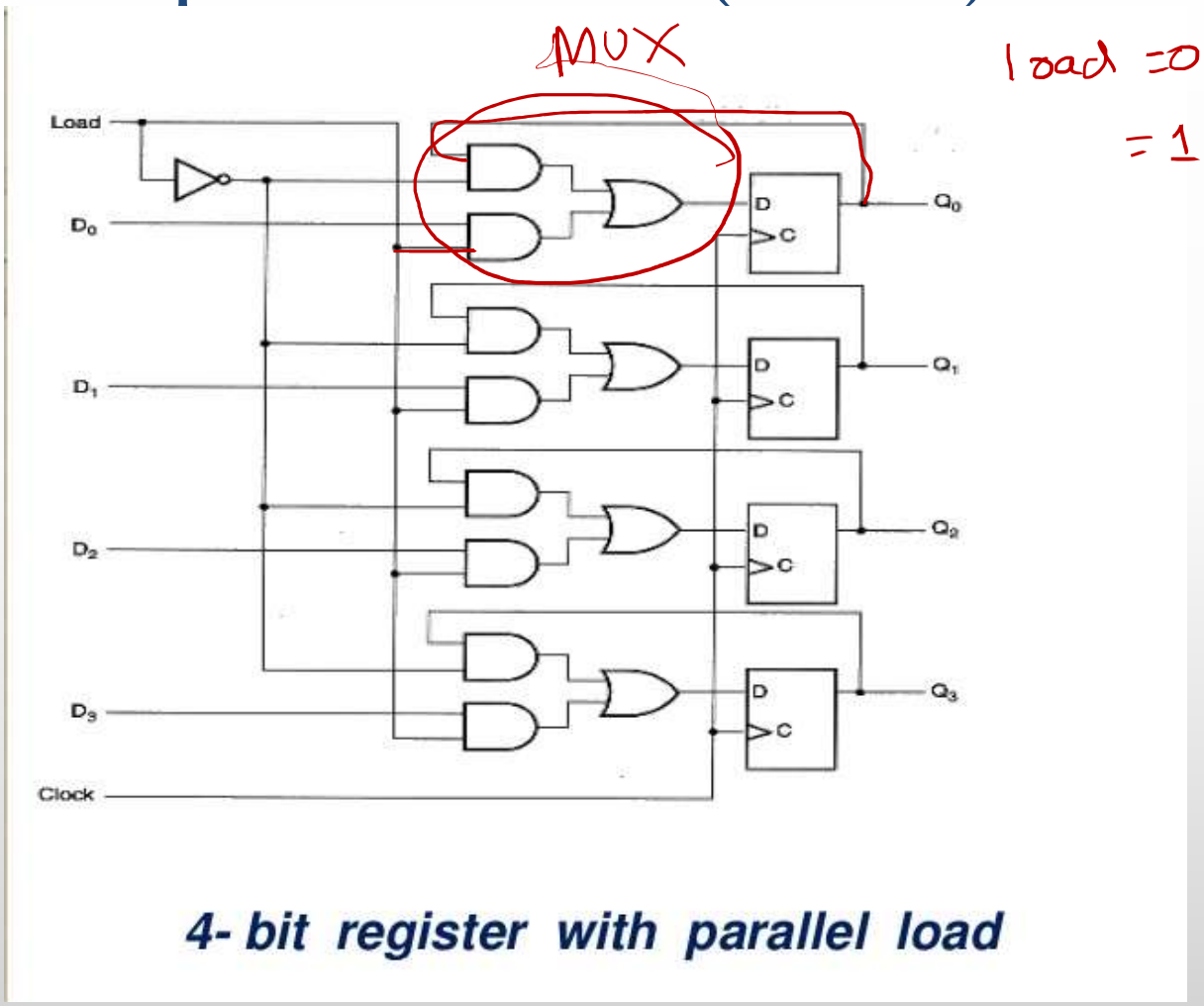
SISO and SIPO register with shift left



Register with parallel load (PISO or PIPO)



Register with parallel load (PIPO)

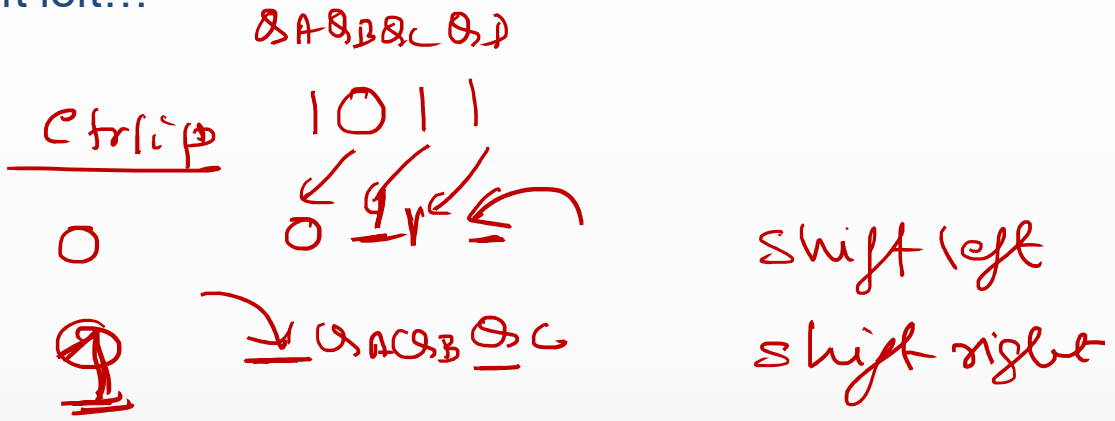


4- bit register with parallel load

4-bit bidirectional shift register using D/SR/JK ffs

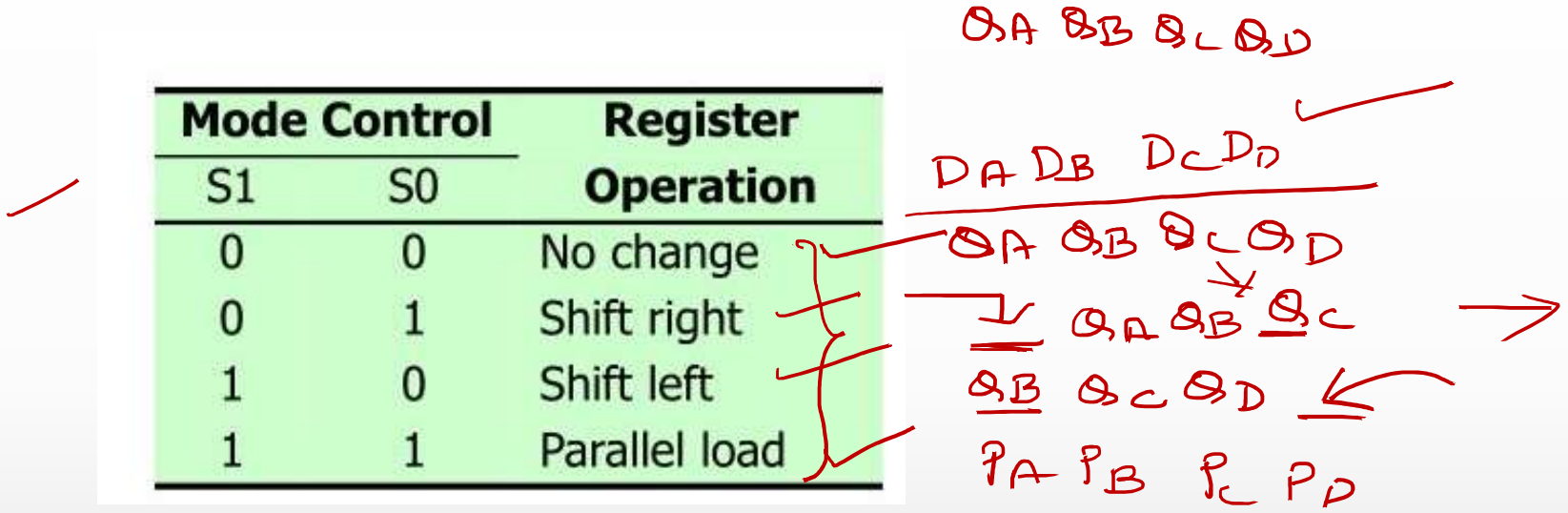
- If shift left/right =0, shift right else shift left…

- **Solve it by yourself…**

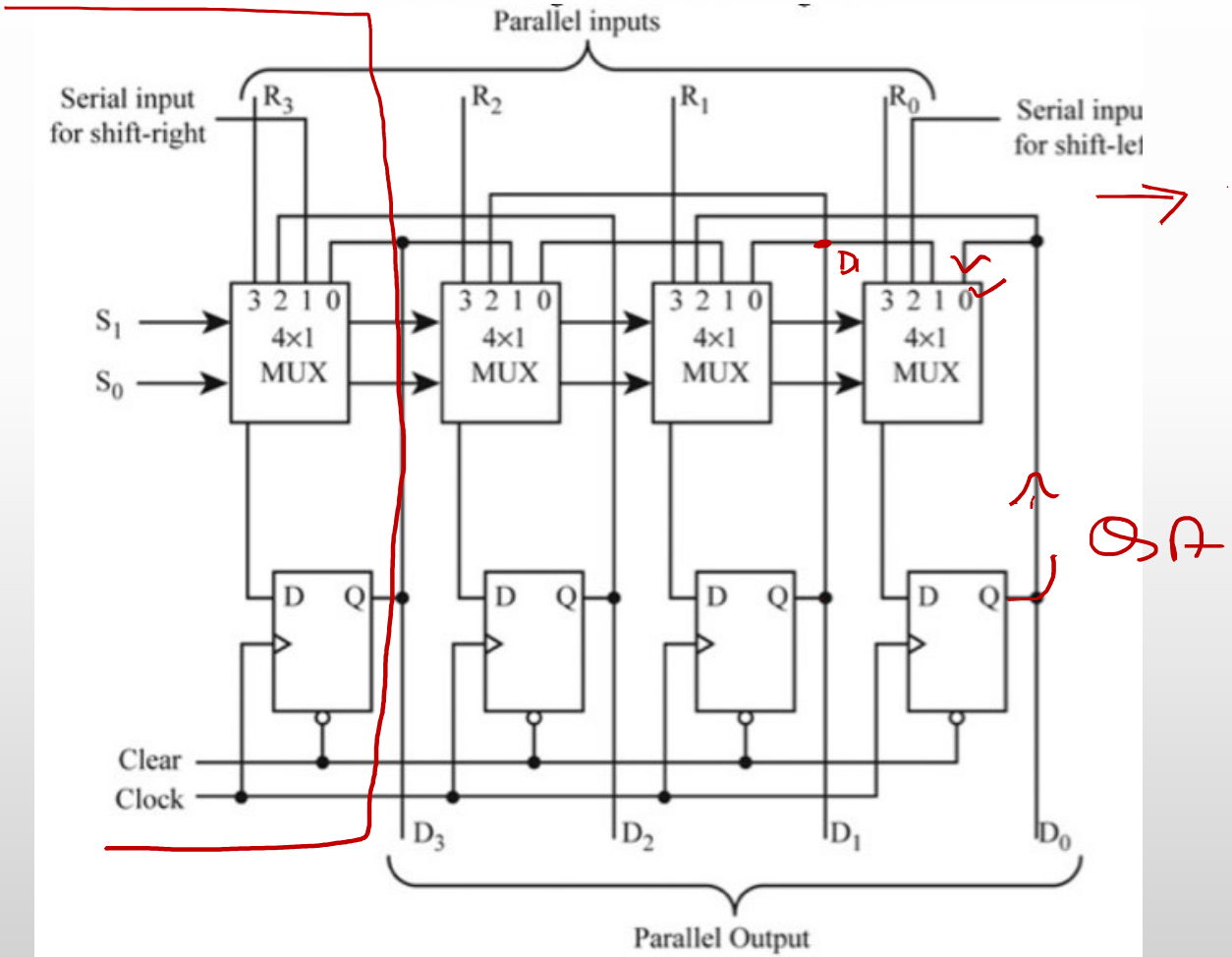


4-bit universal shift register

Mode Control		Register
S1	S0	Operation
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load



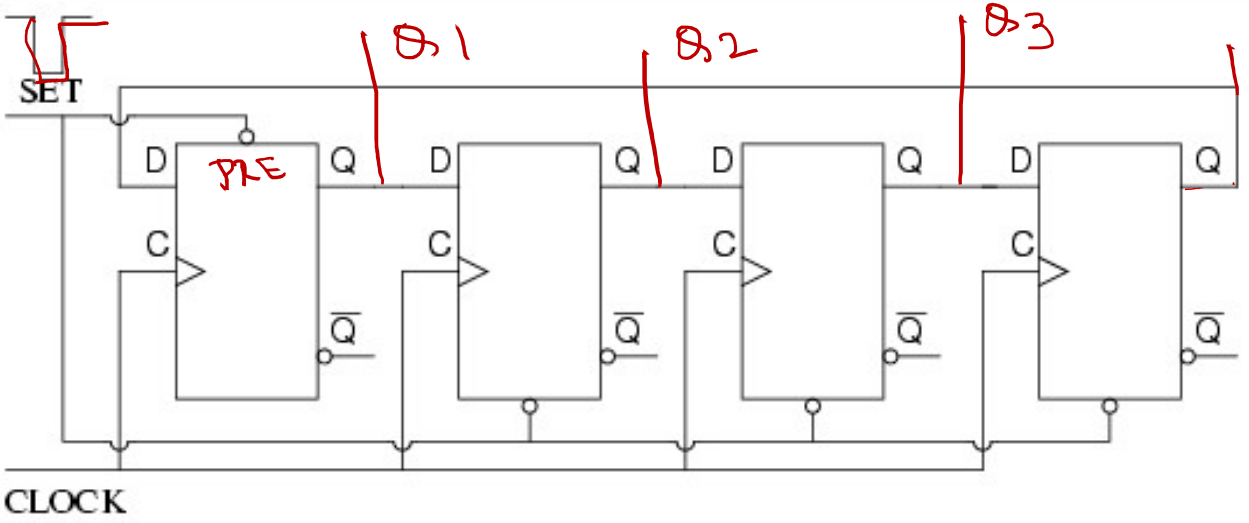
4-bit universal shift register



Shift register counters:

- Ring counter
- Johnson counter /Twisted-ring counter

Ring counter



Set one stage, clear three stages

SISO – right

MOD 4 Ring counter

N-bit Ring counter

MOD-N

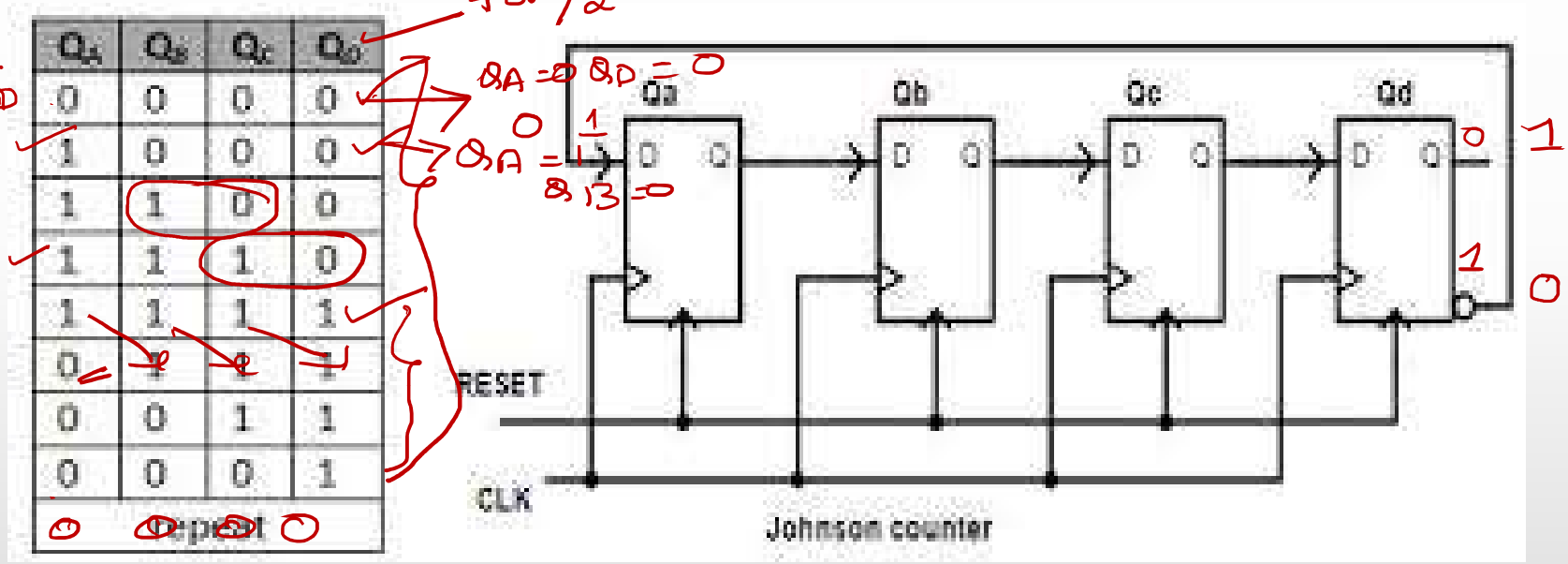
Clock Cycle	Q_1	Q_2	Q_3	Q_4
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	1	0	0	0
6	0	1	0	0

Bit-pattern repeats for every 4 clock cycles

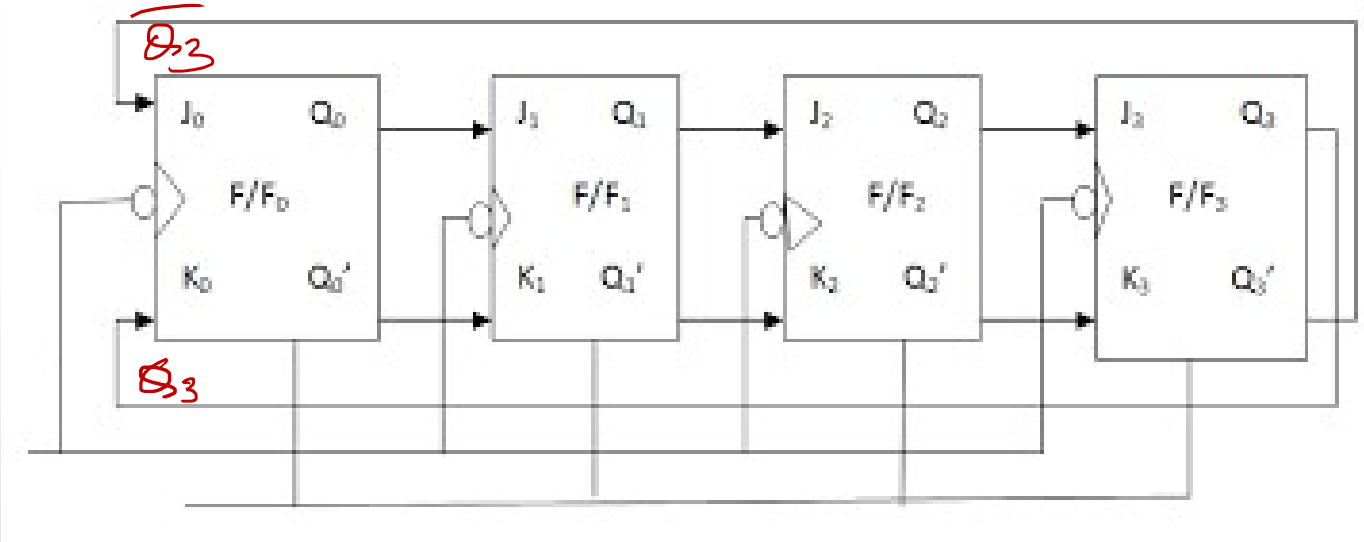
Johnson counter /Twisted-ring counter

4 ffs = 8 states = MOD 8 counter

Q_A	Q_B	Q_C	Q_D
0	0	0	0
1	0	0	0
1	1	0	0
1	1	1	0
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1
0	Repeat		0



Johnson counter /Twisted-ring counter using JK ffs



Design a sequence generator to generate the sequence "00100" using:

a. Ring counter and external gates
b. Johnson counter and external gates

For you to try !