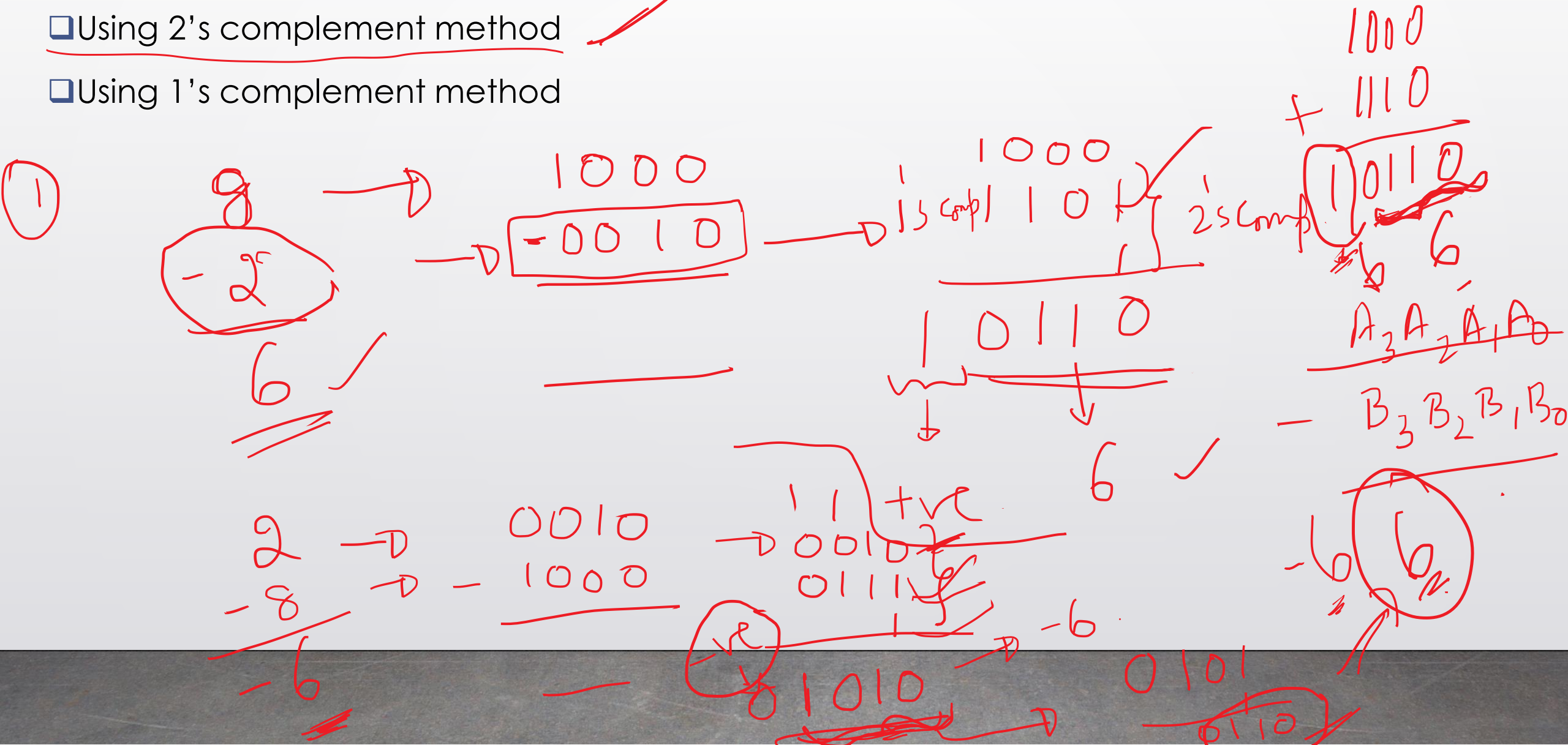
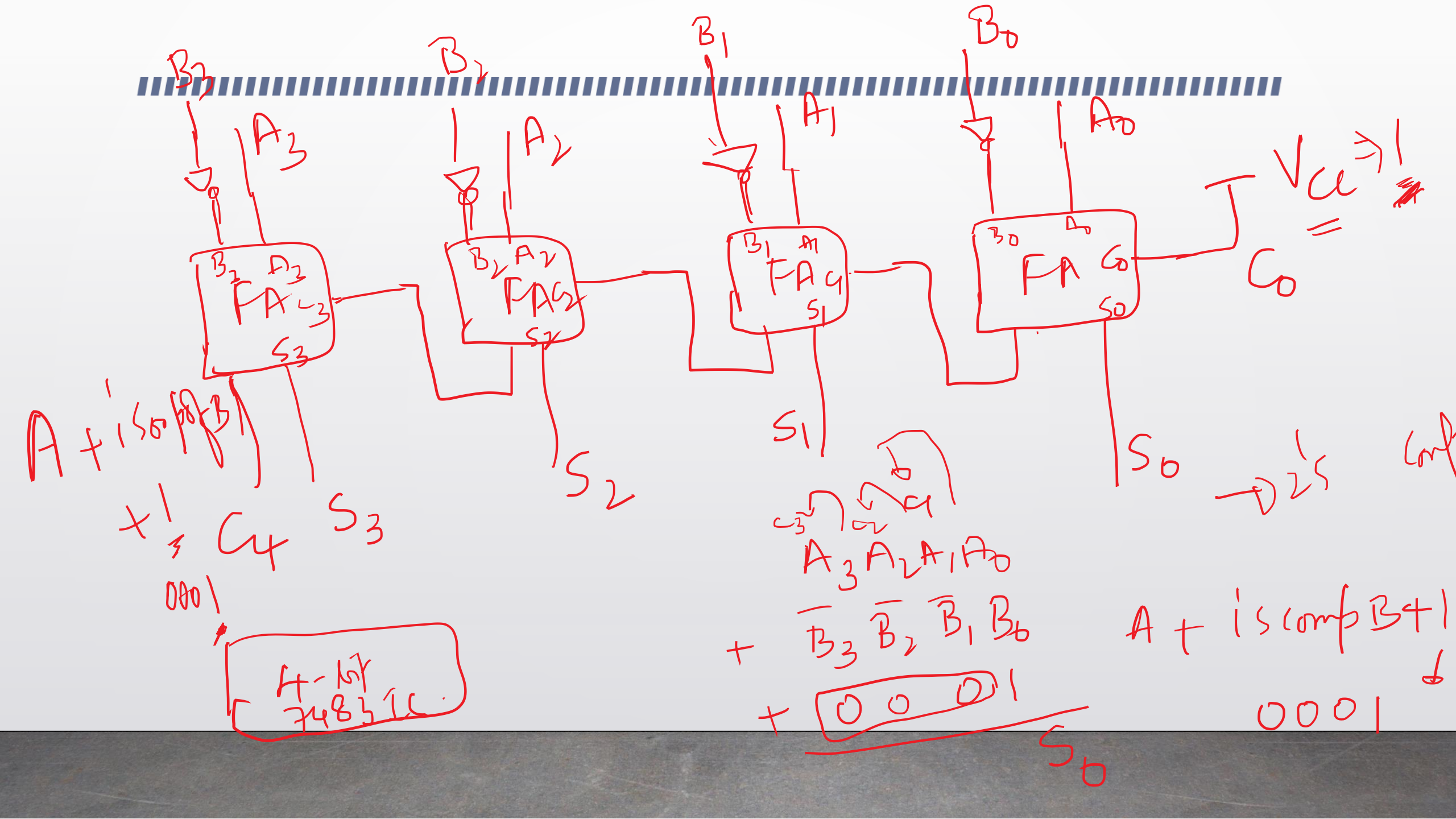
Binary adders and subtractors

- Half adder, full adder, parallel adder
- Half subtractor , full subtractor, parallel subtractor
- Subtraction using complements, parallel adder/subtractor
- Carry Look ahead adder, Decimal adder

Subtraction using complements

- Using 2's complement method
- Using 1's complement method




B3
B2
B1
B0
A3
A2
A1
A0
FA
C3
C2
C1
C0
Vcc
S3
S2
S1
S0
A + is0 B3
+1
C4
S3
0001
4-bit 7483 IC
A3 A2 A1 A0
+ B3 B2 B1 B0
+ 0 0 0 1
S0
A + is comp B+1
0001

1's Complement Subtraction

8 → 1000 → 1000
-2 → -0010 → +1101
6 ← +1 ← (1)0101
5 + 1

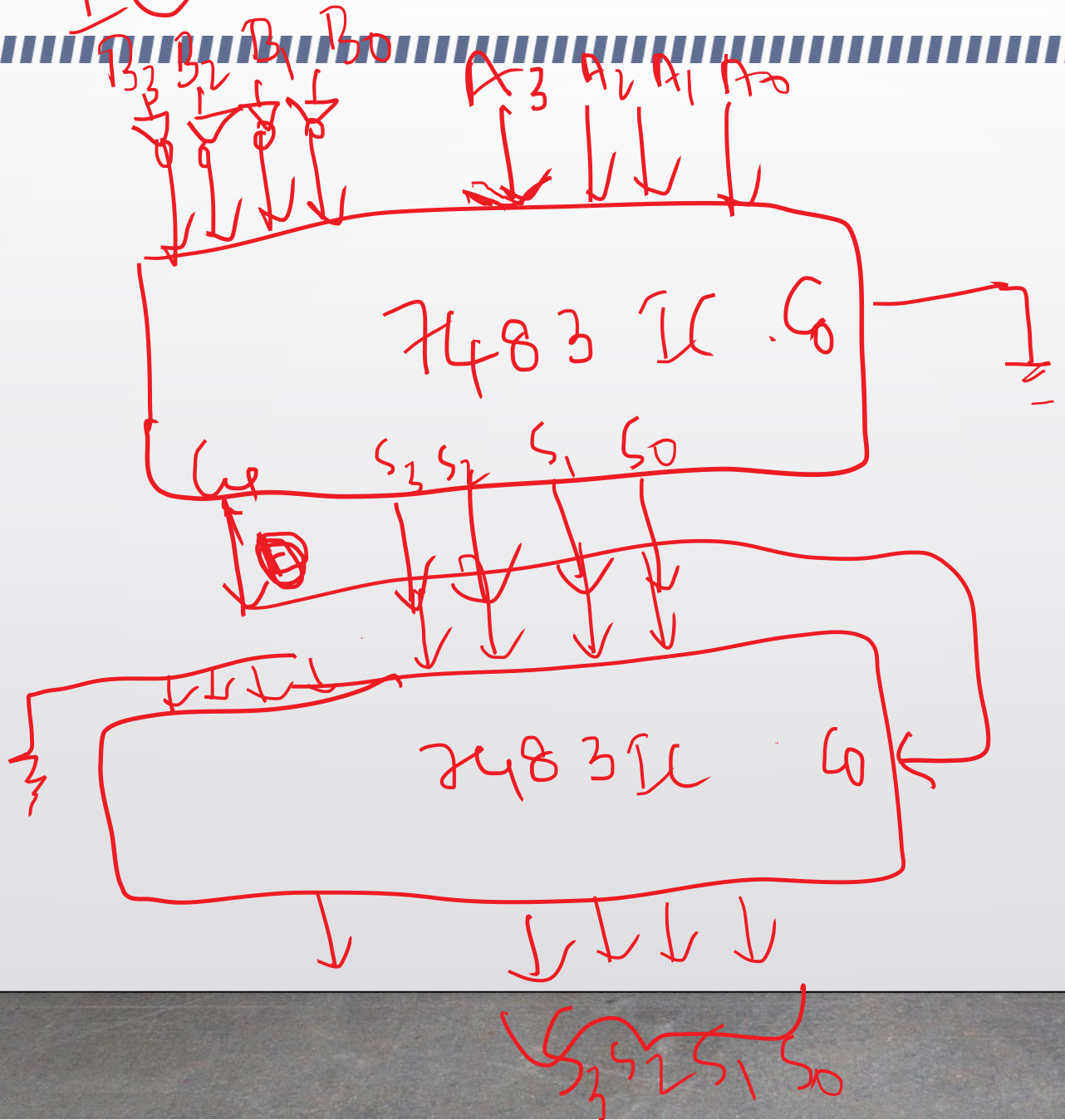
7 → 0111 → 0111
-5 → -0101 → 1010
2 ← +1 ← (1)0001
+1

2 → 0010 → 0010 → 6
-8 → -1000 → 0111
-6 ← +1 ← (0)1001

0110
-6

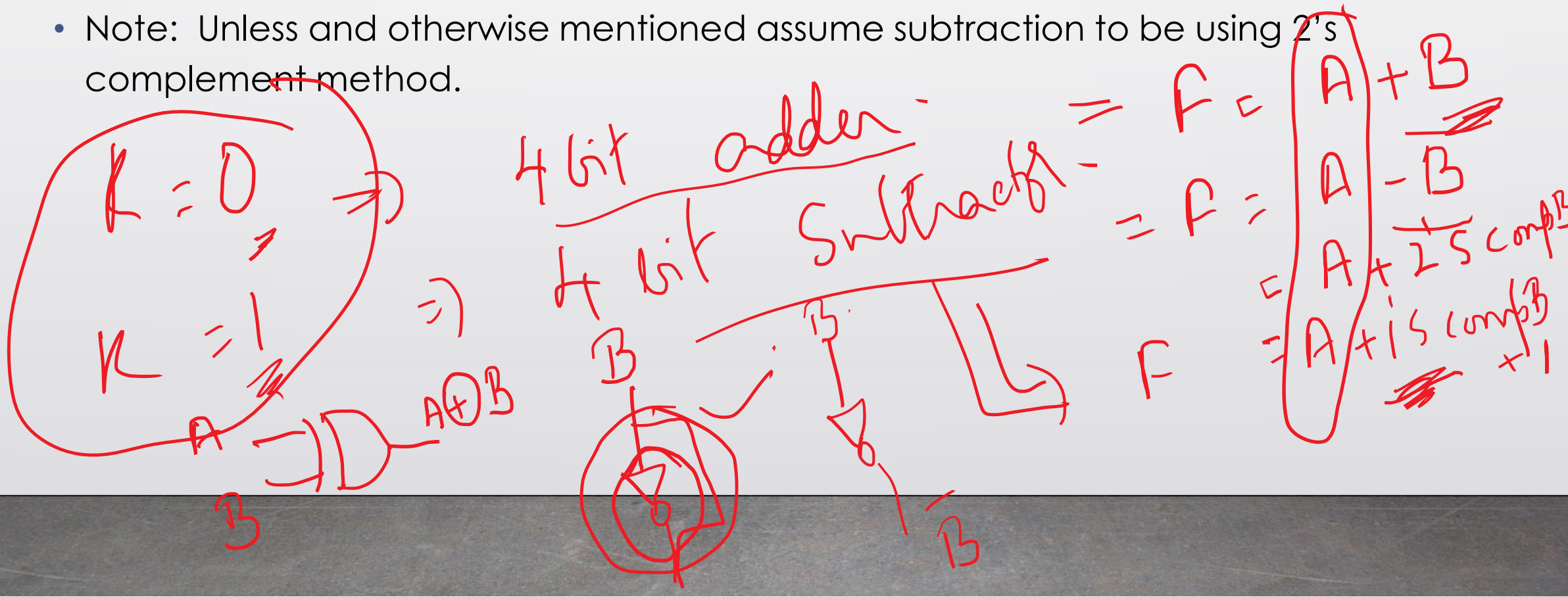
5 → 0101 → 0010
-7 → -0111 → 1000
-2 ← +1 ← (0)1101
-2 → 0010

7483 IC

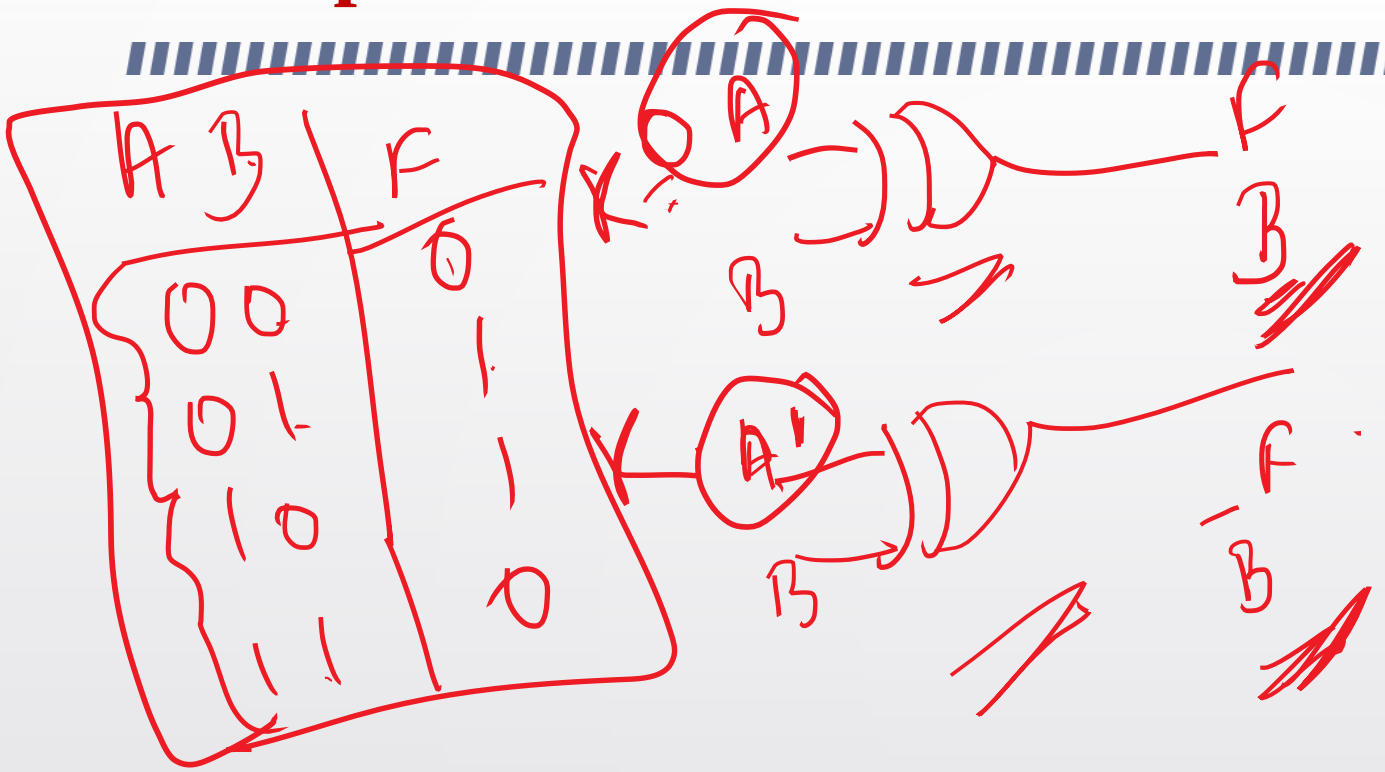


4-bit parallel adder/subtractor :

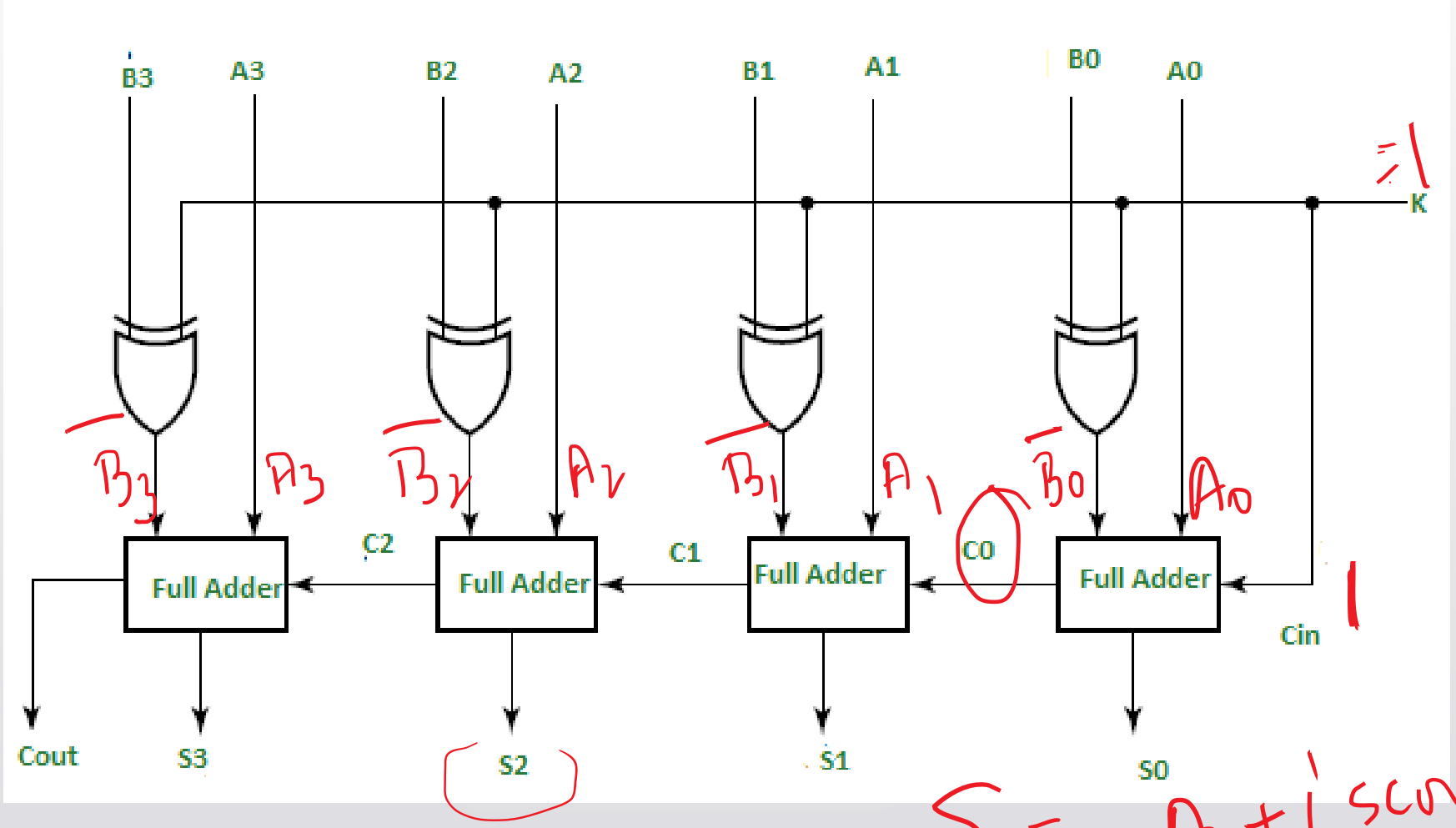
- Design a 4-bit adder/ subtractor using FA blocks or 7483 IC and minimum external gates, i.e. if the control input bit K=0, the circuit should add the input numbers or if K=1, the circuit should subtract the two numbers using 2's complement method.
- Note: Unless and otherwise mentioned assume subtraction to be using 2's complement method.



4-bit parallel adder/subtractor :



4-bit parallel adder/subtractor :

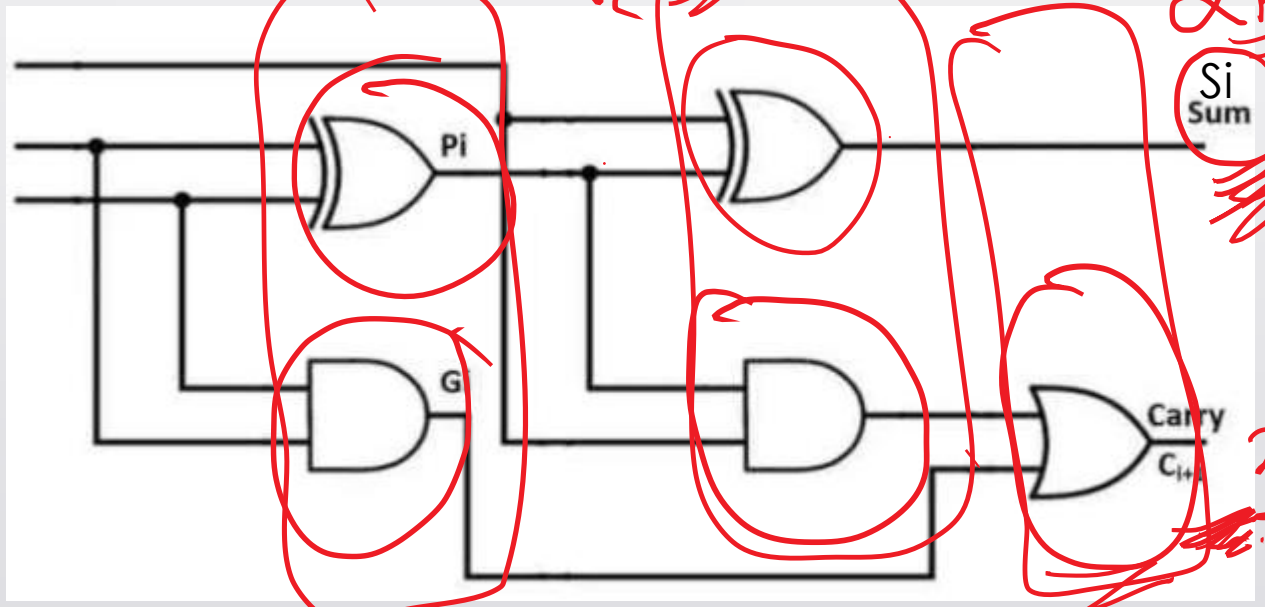


$S = A + \text{i'scomp of } B + 1$

$= A - B$

Carry Look Ahead (CLA) Adder

- Propogation delay in Full Adder is $3T_g$ with respect to following circuit, where Tg is the propagation delay of a gate. All the gates are assumed to have a propagation delay of Tg.
- Pi is the carry propagate term and Gi is the carry generate term



$$Pi = Ai \oplus Bi$$

$$Gi = Ai.\ Bi$$

$$Si =$$

$$Ci+1 =$$

CLA continued

4 - bit adder

- Carry generation in CLA from A_i, B_i, and C_0
- Co= input carry

C1 = $C_0 P_0 + G_0 = C_0(A_0 \oplus B_0) + A_0 B_0$

C2= $C_1 P_1 + G_1 = (C_0 P_0 + G_0) P_1 + G_1$

$= G_1 + P_1 G_0 + P_1 P_0 C_0$

C3= $C_2 P_2 + G_2 = (G_1 + P_1 G_0 + P_1 P_0 C_0) P_2 + G_2$

$= G_2 + P_2 G_1 + P_1 P_2 G_0 + P_0 P_1 P_2 C_0$

$C_4 = G_3 + P_3 G_2 + P_2 P_3 G_1 + P_1 P_2 P_3 G_0 + P_0 P_1 P_2 P_3 C_0$

CLA Continued

- Expressions for sum

S0 = $A_0 \oplus B_0 \oplus C_0 = P_0 \oplus C_0$

S1= $A_1 \oplus B_1 \oplus C_1$

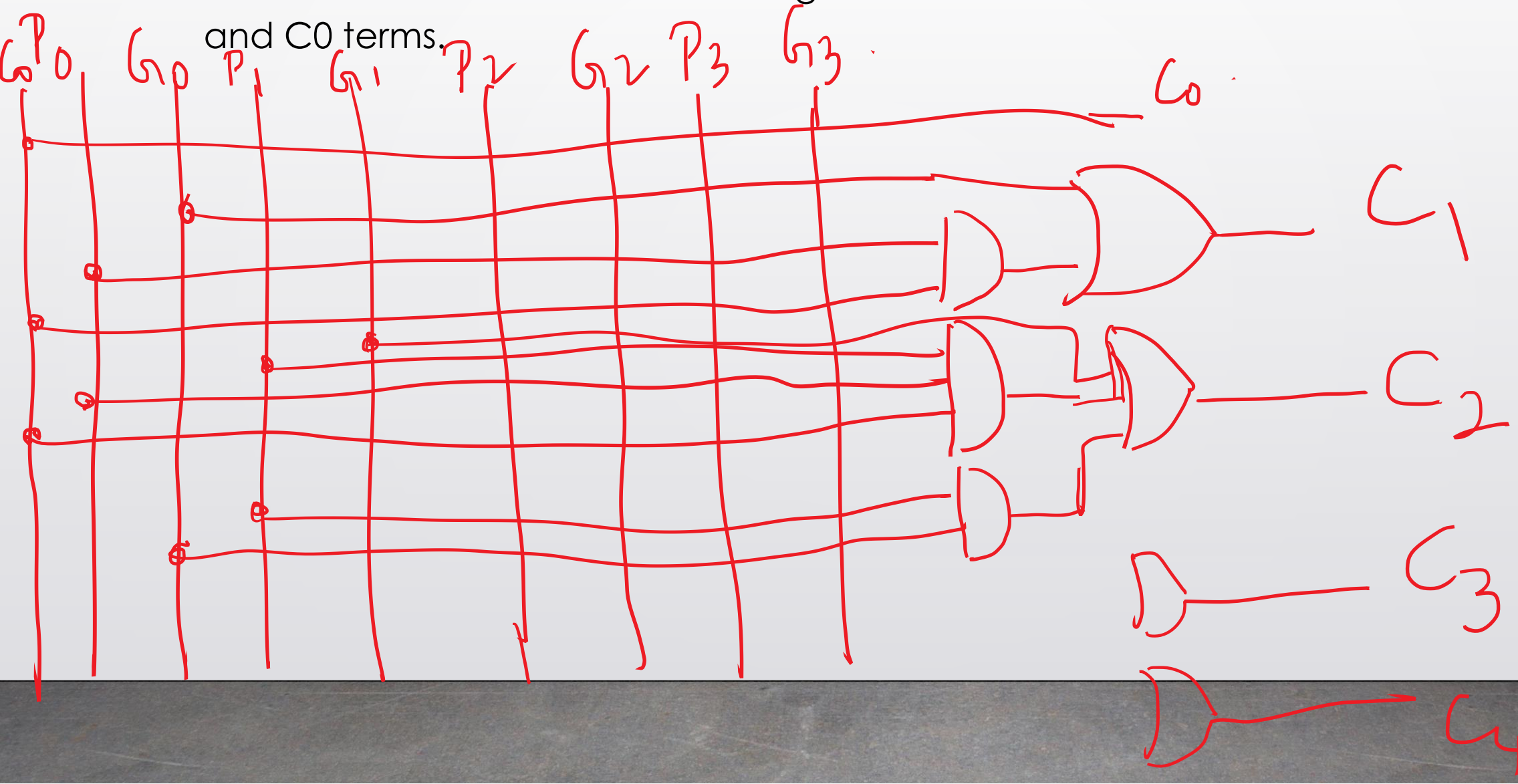
S2 = $A_2 \oplus B_2 \oplus C_2$

S3 = $A_3 \oplus B_3 \oplus C_3$

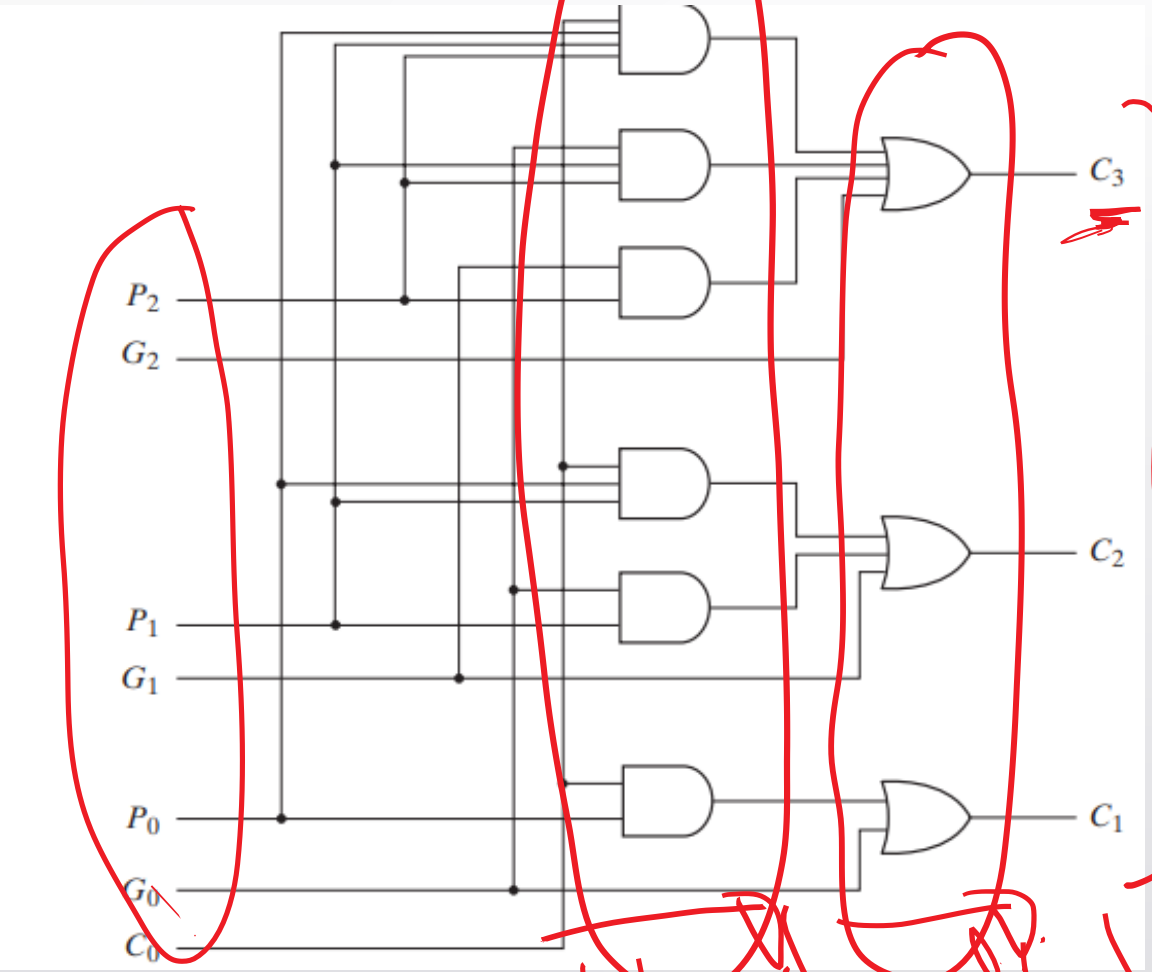
C4 =

CLA: Carry look ahead generator circuit

- Draw the combinational circuit to generate C1, C2 and C3 from Pi , Gi and C0 terms.

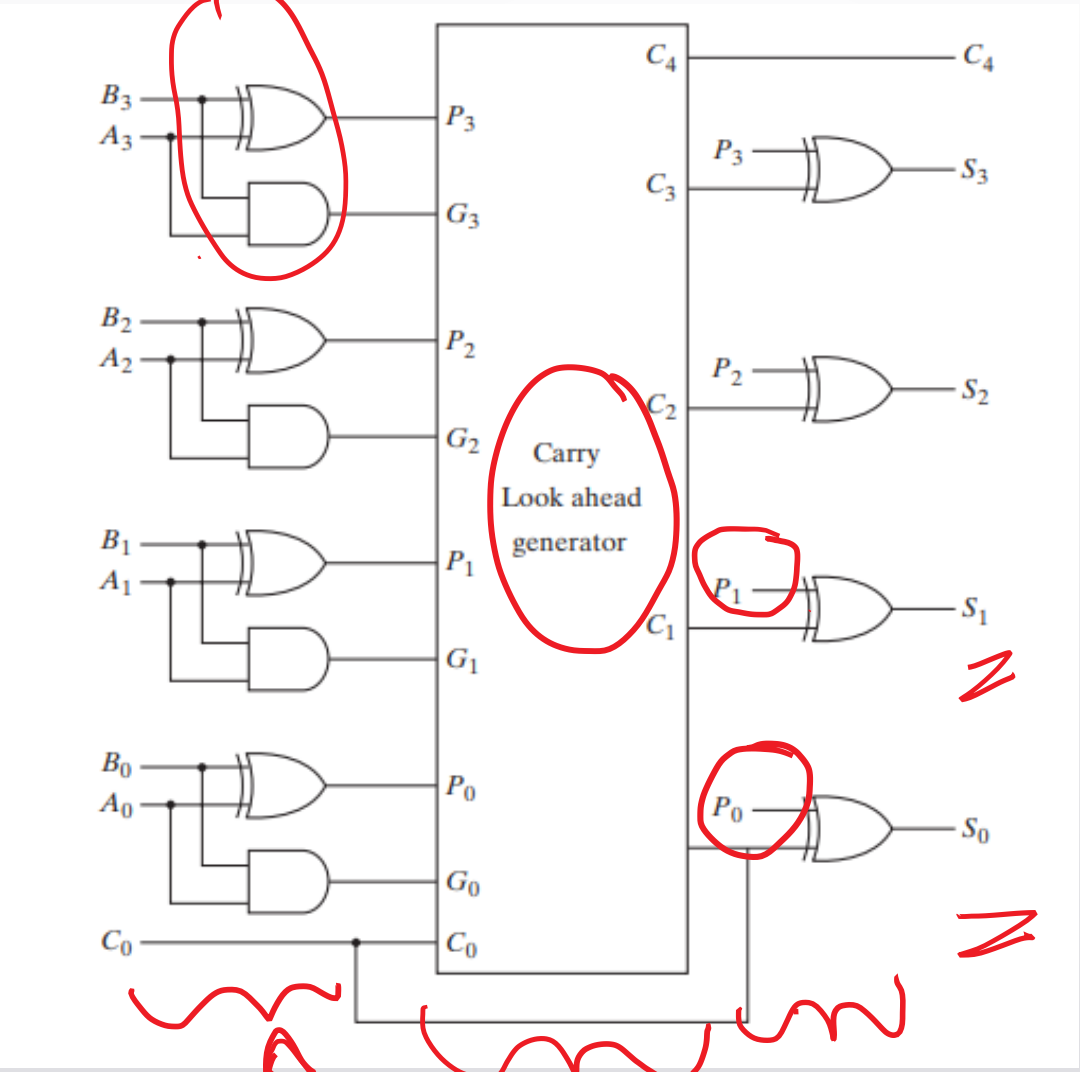


CLA: Carry look ahead generator circuit



Time required to generate C1,C2,C3 in terms of Tg?

4-bit CLA



Time required to generate S1,S2,S3,C4 in terms of Tg?

Comparison

- CLA or CPA…which is better?

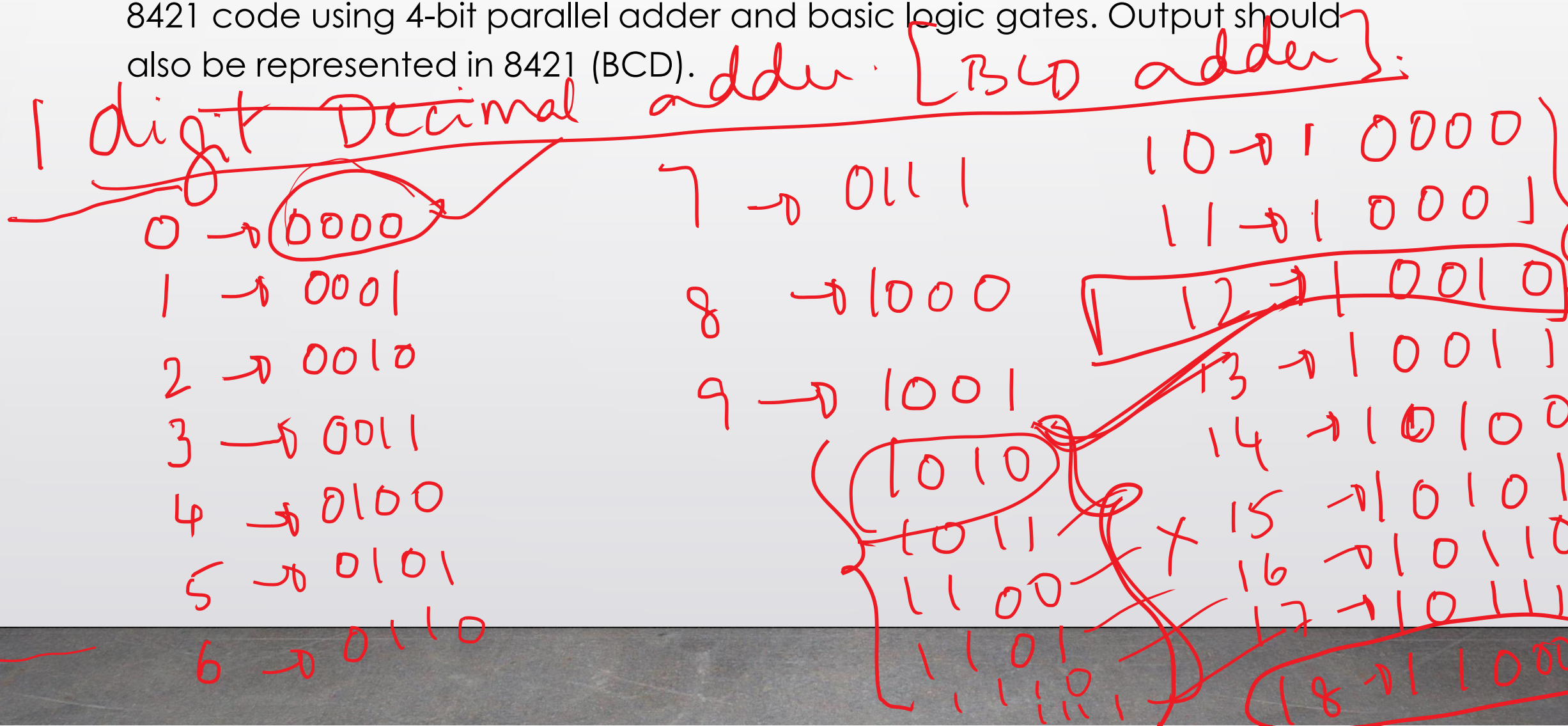
4-bit CLA is 3 times faster than 4-bit Ripple carry Adder.

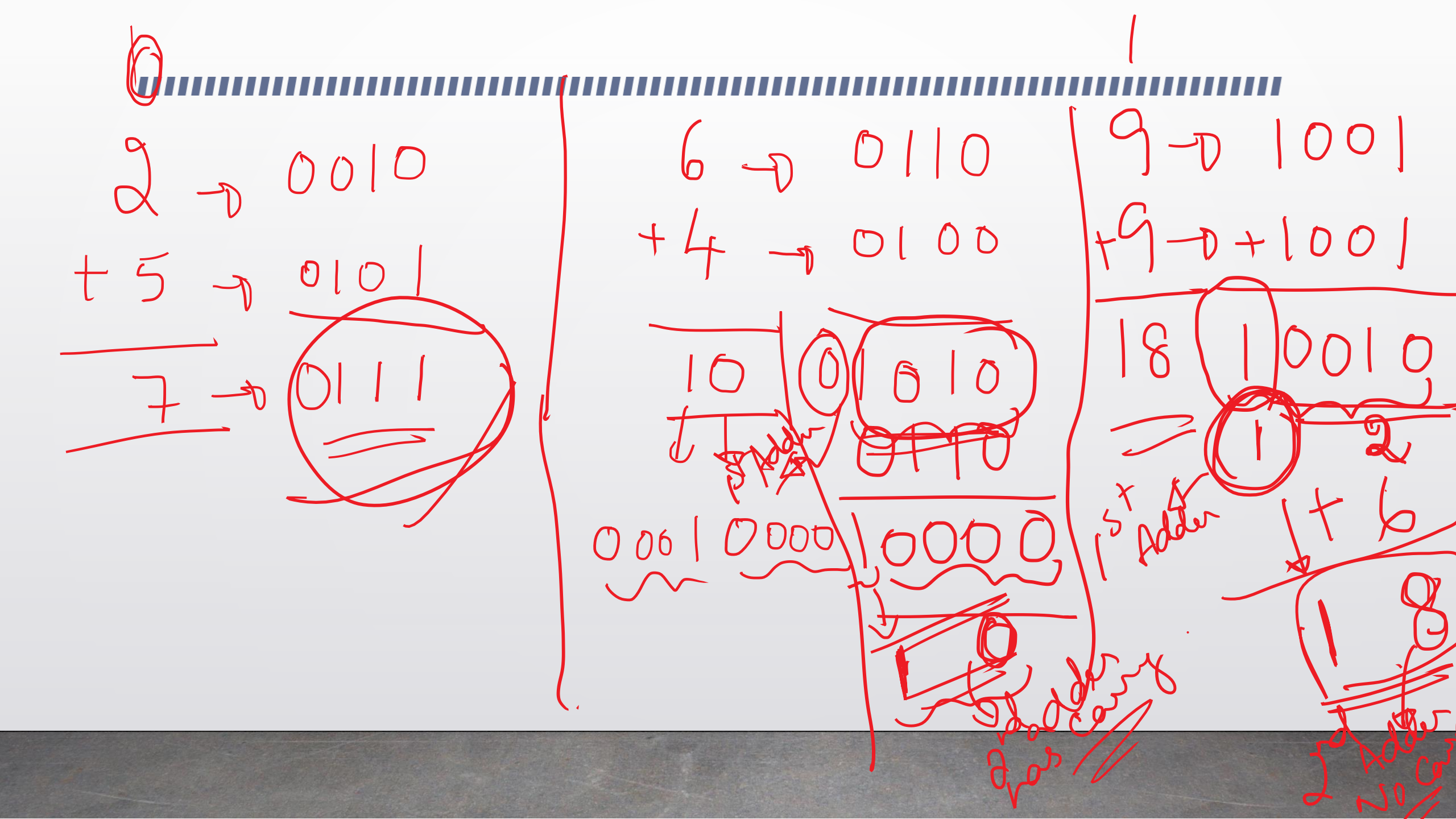
BCD adder

Decimal adder: Used to add decimal numbers represented in binary coded form

Decimal adder:

- Design a decimal adder to add two, single digit decimal numbers input in 8421 code using 4-bit parallel adder and basic logic gates. Output should also be represented in 8421 (BCD).




0
1
2 → 0010
+5 → 0101
7 → 0111
6 → 0110
+4 → 0100
10 0 1010
1st Adder
0 0010 0000
1000
Adder carry
9 → 1001
+9 → +1001
18 1 0010
1
2
+6
1st Adder
1 8
1 Adder
No Carry

BCD ADDER: TRUTH TABLE

Binary Sum					BCD Sum					Decimal
K	Z_8	Z_4	Z_2	Z_1	C	S_8	S_4	S_2	S_1	
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	2
0	0	0	1	1	0	0	0	1	1	3
0	0	1	0	0	0	0	1	0	0	4
0	0	1	0	1	0	0	1	0	1	5
0	0	1	1	0	0	0	1	1	0	6
0	0	1	1	1	0	0	1	1	1	7
0	1	0	0	0	0	1	0	0	0	8
0	1	0	0	1	0	1	0	0	1	9
0	1	0	1	0	1	0	0	0	0	10
0	1	0	1	1	1	0	0	0	1	11
0	1	1	0	0	1	0	0	1	0	12
0	1	1	0	1	1	0	0	1	1	13
0	1	1	1	0	1	0	1	0	0	14
0	1	1	1	1	1	0	1	0	1	15
1	0	0	0	0	1	0	1	1	0	16
1	0	0	0	1	1	0	1	1	1	17
1	0	0	1	0	1	1	0	0	0	18
1	0	0	1	1	1	1	0	0	1	19

$F_1 = Z_8Z_4 + Z_8Z_2$

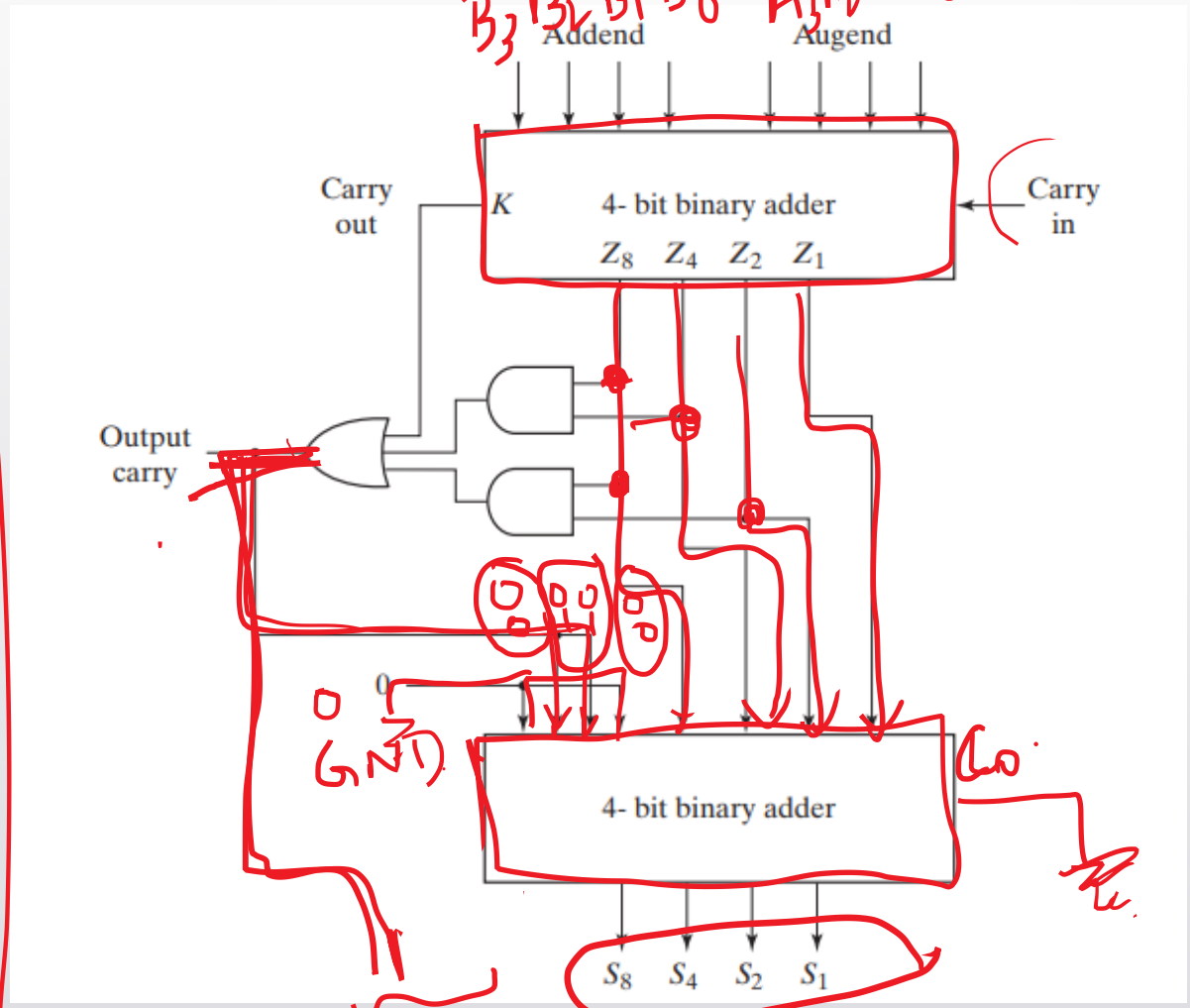
$F = K + F_1$

$F = K + Z_8Z_4 + Z_8Z_2$

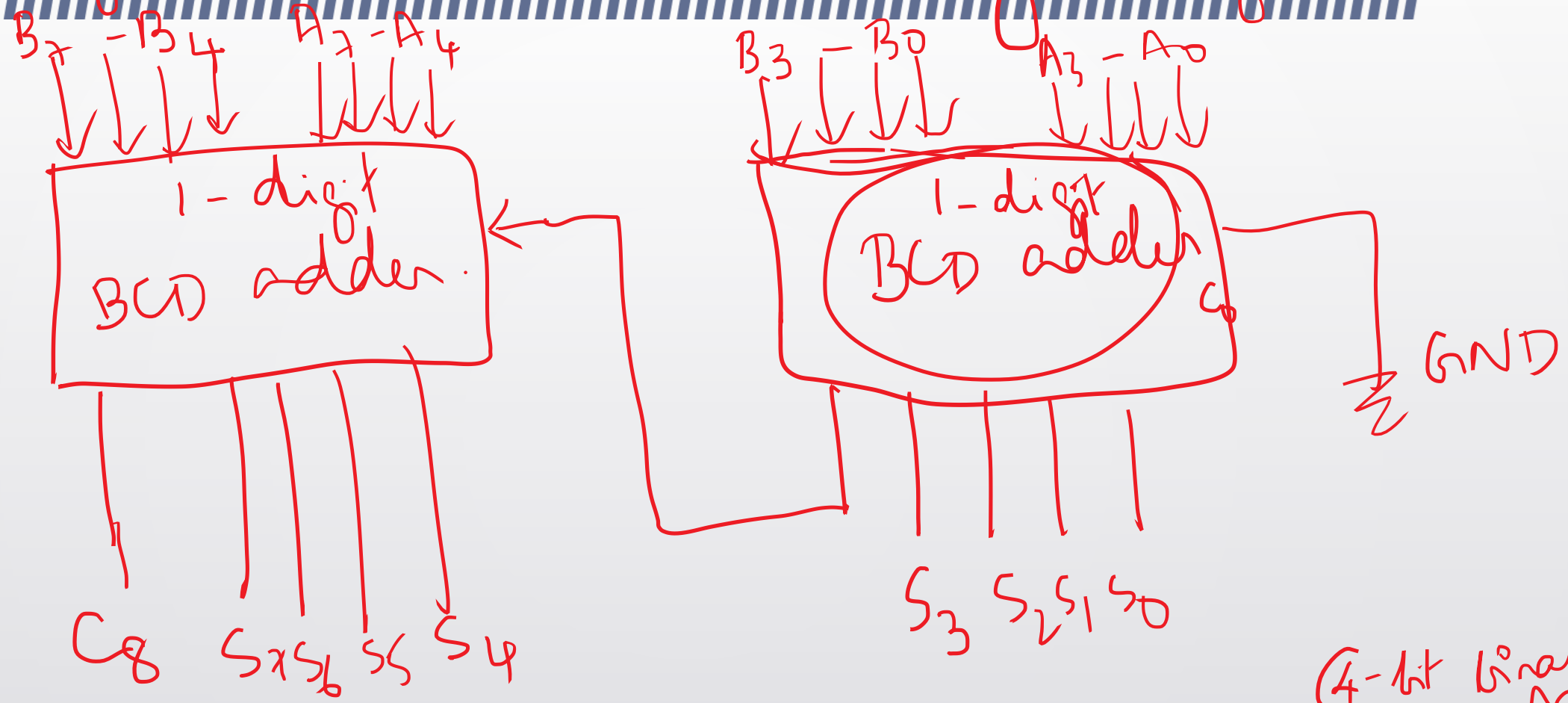
BCD ADDER

- Binary sum can be converted to BCD by adding 6 to binary sum.
- 6 needs to be added only when binary sum is > 9 or $(1001)_2$
- Referring the truth table, write the expression for F such that, F=1 if binary sum is > 9 else F=0

Block diagram of BCD adder



2-digit BCD adder using 1-digit BCD adder



Design 2-digit BCD adder using 7483 IC's & external gates.

(4-bit binary Adder)

Reference:

- Digital design , third edition by morris mano, chapter 4

. Slides are used only as a supporting material to teach the subject.

. Students should write down the notes and read the text book.

Questions?