MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

COURSE PLAN

Department	:	Computer Science and Engineering
Course Name & code	:	COMPUTER ORGANIZATION AND ARCHITECTURE & CSE 2151
Semester & branch	:	THIRD & CSE
Name of the faculty	:	DR. RENUKA A

No of contact hours/week:

L	T	P	C
36	12	0	4

Course Outcomes (COs)

	At the end of this course, the student should be able to:	No. of Contact Hours	Marks
CO1:	Describe the functionalities of the various units of computers and the instruction set architecture.	10	20
CO2:	Appreciate the hardware implementation of addition, subtraction, multiplication and division and perform arithmetic operations.	7	16
CO3:	Design the control unit for simple algorithms	10	20
CO4:	Explain basics of memory system such as cache memories, mapping functions, replacement algorithms and virtual memory concept and design simple memory systems.	10	20
CO5:	Outline the I/O handling techniques and realize the improvement in performance using the concepts of pipelining and parallel processing.	11	24
	Total	48	100

Assessment Plan

Components	Assignments	Sessional Tests	End Semester/ Make-up Examination
Duration	20 to 30 minutes	60 minutes	180 minutes
Weightage	20 % (4 X 5 marks)	30 % (2 X 15 Marks)	50 % (1 X 50 Marks)
Typology of Questions	Understanding/ Comprehension; Application; Analysis; Synthesis; Evaluation	Knowledge/ Recall; Understanding/ Comprehension; Application	Understanding/ Comprehension; Application; Analysis; Synthesis; Evaluation
Pattern	Answer one randomly selected question from the problem sheet (Students can refer their class notes)	MCQ: 10 questions (0.5 marks) Short Answers: 5 questions (2 marks)	Answer all 5 full questions of 10 marks each. Each question may have 2 to 3 parts of 3/4/5/6/7 marks
Schedule	4, 7, 10, and 13th week of academic calendar	Calendared activity	Calendared activity
Topics Covered	Quiz 1 (L 1--6 & T 1-2) **(CO1)**	Test 1 (L 1-16 & T 1-5) **(CO1-CO3)**	Comprehensive examination covering full syllabus. Students are expected to answer all questions **(CO1-CO5)**
	Quiz 2 (L **7-13** & T 3-4) **(CO1-CO2)**		
	Quiz 3 (L 14-22 & T 5-7) **(CO3)**	Test 2 (L 17-27 & T 6-9) **(CO3-CO4)**	
	Quiz 4 (L 23-32 & T 8-10) **(CO4-CO5)**		

Lesson Plan

L. No.	Topics	Course Outcome Addressed
L0	INTRODUCTION TO THE COURSE	CO
L1	BASIC STRUCTURE OF COMPUTERS: COMPUTER TYPES, FUNCTIONAL UNITS	CO1
L2	BASIC OPERATIONAL CONCEPTS, NUMBER REPRESENTATION	CO1
L3	ARITHMETIC OPERATIONS	CO1
T1	Tutorial 1 on Number representation and Arithmetic Operations	CO1
L4	CHARACTER REPRESENTATION, FLOATING POINT REPRESENTATION, IEEE STANDARD FLOATING POINT REPRESENTATION	CO1
L5	FLOATING POINT ARITHMETIC- ADDITION, SUBTRACTION	CO2
L6	FLOATING POINT ARITHMETIC- MULTIPLICATION, DIVISION, GUARD BITS AND TRUNCATION	CO2
T2	Tutorial 2 on Floating point arithmetic	CO2

L7	INSTRUCTION SET ARCHITECTURE: MEMORY LOCATIONS AND ADDRESSES, MEMORY OPERATIONS	CO1
L8	INSTRUCTIONS AND INSTRUCTION SEQUENCING	CO1
L9	ADDRESSING MODES, CISC INSTRUCTION SETS, RISC AND CISC STYLES	CO1
L10	EXAMPLE PROGRAMS	CO1
T3	Tutorial 3 on Memory addressing , Addressing modes, RISC and CISC	CO1
L11	ARITHMETIC AND LOGIC UNIT: HARDWARE FOR ADDITION AND SUBTRACTION MULTIPLICATION-HARDWARE IMPLEMENTATION-UNSIGNED MULTIPLICATION	CO2
L12	SIGNED MULTIPLICATION, -BOOTHS ALGORITHM	CO2
L13	DIVISION	CO2
T4	Tutorial 4 on Addition, Subtraction and Multiplication and Division in ALU	CO2
L14	CONTROL UNIT: BASIC CONCEPTS-REGISTER TRANSFER NOTATION, HARDWARE IMPLEMENTATION, BASIC RWM UNIT, BUSES-BIDIRECTIONAL, SINGLE BUS, 2 BUS, 3 BUS ORGANIZATION	CO3
L15	DESIGN METHODS-COMPARISON OF HARDWIRED AND MICROPROGRAMMED APPROACH, HARDWIRED CONTROL DESIGN-BOOTHS MULTIPLIER DESIGN	CO3
L16	PROCESSING SECTION DESIGN OF BOOTHS MULTIPLIER	CO3
T5	Tutorial 5 on Processing section Design	CO3
L17	BOOTHS MULTIPLIER CONTROLLER, SEQUENCE COTROLLER DESIGN	CO3
L18	PLA CONTROL UNIT ORGANIZATION OF BOOTH MULTIPLIER	CO3
T6	Tutorial 6 on Controller Design	CO3
L19	MICROPROGRAMMED CONTROL UNIT:WILKE'S DESIGN, MICROPROGRAMMED CONTROL ORGANIZATION	CO3
L20	MICROPROGRAMMED MULTIPLIER CONTROL UNIT FOR BOOTHS MULTIPLIER	CO3
T7	Tutorial 7 on Microprogrammed Control Unit	CO3
L21	MEMORY SYSTEMS: BASIC CONCEPTS, RAM MEMORIES, INTERNAL ORGANIZATION OF MEMORY CHIPS	CO4
L22	STRUCTURE OF LARGER MEMORIES, MEMORY HIERARCHY	CO4
L23	CACHE MEMORIES- MAPPING FUNCTIONS	CO4
L24	PLACEMENT STRATEGIES, REPLACEMENT ALGORITHMS	CO4
T8	Tutorial 8 on Organization of Larger memories, Replacement Algorithms	CO4
L25	EXAMPLE OF MAPPING TECHNIQUES	CO4
L26	PERFORMANCE CONSIDERATIONS, HIT RATE AND MISS PENALTY, CACHES ON THE PROCESSOR CHIP	CO4
L27	VIRTUAL MEMORY, ADDRESS TRANSLATION	CO4

T9	Tutorial 9 on Mapping functions, Hit rate and Miss penalty, Address translation	CO4
L28	MAGNETIC HARD DISKS	CO4
L29	INPUT/OUTPUT ORGANIZATION: ACCESSING I/O DEVICES, I/O DEVICE INTERFACE, PROGRAM-CONTROLLED I/O, INTERRUPTS, ENABLING AND DISABLING INTERRUPTS	CO5
L30	HANDLING MULTIPLE DEVICES, CONTROLLING I/O DEVICE BEHAVIOR, PROCESSOR CONTROL REGISTERS, DMA	CO5
T10	Tutorial 10 on Interrupts	CO5
L31	INTRODUCTION TO PARALLEL ARCHITECTURE: PIPELINING CONCEPTS, PIPELINE ORGANIZATION, ISSUES, DATA DEPENDENCIES	CO5
L32	OPERAND FORWARDING, HANDLING DATA DEPENDENCIES IN SOFTWARE, MEMORY DELAYS	CO5
L33	BRANCH DELAYS, UNCONDITIONAL BRANCHES, CONDITIONAL BRANCHES, BRANCH DELAY SLOT	CO5
T11	Tutorial 11 on Data Dependencies, Branching and Pipelining	CO5
L34	HARDWARE MULTITHREADING, VECTOR (SIMD) PROCESSING	CO5
L35	GRAPHICS PROCESSING UNITS (GPUs), SHARED MEMORY MULTIPROCESSORS, INTERCONNECTION NETWORKS	CO5
L36	CACHE COHERENCE, WRITE-THROUGH PROTOCOL, WRITE-BACK PROTOCOL, SNOOPY CACHES, DIRECTORY BASED CACHE COHERENCE	CO5
T12	Tutorial 12 on multithreading, SIMD, Multiprocessors, Cache coherence	CO5
L/T	Click or tap here to enter text.	

References:

1. Carl Hamacher, ZvonkoVranesic and SafwatZaky, “Computer Organization and Embedded Systems”, Sixth edition, McGraw Hill Publication, 2012.
2. William Stallings, “Computer Organization and Architecture – Designing for Performance”, 9th edition, PHI, 2015.
3. Mohammed Rafiquzzaman and Rajan Chandra, “Modern Computer Architecture”, Galgotia Publications Pvt. Ltd., 2010.
4. D.A. Patterson and J.L.Hennessy, "Computer Organization and Design-The Hardware/Software Interface", Fifth Edition, Morgan Kaufmann, 2014.
5. J.P.Hayes, "Computer Architecture and Organization", McGraw Hill Publication, 1998.
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Submitted by: **DR. RENUKA A**

(Signature of the faculty)

Date: **30-08-2021**

Approved by: **DR. ASHALATHA NAYAK**

(Signature of HOD)

Date: **30-08-2021**

FACULTY MEMBERS TEACHING THE COURSE (IF MULTIPLE SECTIONS EXIST):

FACULTY	SECTION	FACULTY	SECTION
Dr. N. Gopalakrishna Kini	A		
Ms. Shwetha Rai	B		
Dr. Renuka A	C		
Ms. Sucharitha Shetty	D		

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