COMPUTER ORGANIZATION AND ARCHITECTURE

[Revised Credit System]

(Effective from the academic year 2018-19)

SEMESTER - III

Subject Code	**CSE 2151**	**IA Marks**	**50**
Number of Lecture Hours/Week	**04**	**Exam Marks**	**50**
Total Number of Lecture Hours	**48**	**Exam Hours**	**03**

CREDITS - 04

Course objectives: This course will enable students to

- Summarize the fundamental concepts of the organization and architecture of a computer.
- Analyze taxonomy of Execution, Processor, Memory and I/O Units.
- Explain the pipelining principles, Data dependencies and hazards, SIMD and Multiprocessor concepts.

Module -1	**Teaching Hours**
BASIC STRUCTURE OF COMPUTERS: Computer types, Functional units, Basic operational concepts, Number Representation and Arithmetic Operations, Character Representation, Problems. **Text Book 1:** Chapter 1: 1.1, 1.2, 1.3, 1.4, 1.5, 1.9	**5 Hours**
Module -2	
INSTRUCTION SET ARCHITECTURE : Memory locations and addresses, Memory operations, Instructions and Instruction Sequencing, Addressing modes, CISC Instruction Sets, RISC and CISC Styles, Example Programs. **Text Book 1:** Chapter 2: 2.1, 2.2, 2.3, 2.4, 2.10, 2.11, 2.12, 2.15	**5 Hours**
Module – 3	
ARITHMETIC AND LOGIC UNIT: Hardware for addition and subtraction, Multiplication, Hardware implementation, Booth's algorithm, Division, Floating point representation, IEEE standard floating point representation, Floating point arithmetic.	**7 Hours**

Text Book 2: Chapter 10: 10.3, 10.4, 10.5	
Module-4	
CONTROL UNIT: Basic concepts, buses-bidirectional, single bus, 2 bus, 3 bus organization design methods-comparison of hardwired and micro-programmed approach, hardwired control design, Booths multiplier design, processing section design of booths multiplier, Booths multiplier controller, sequence controller design, Micro-programmed control unit: Micro-programmed control organization, Micro-programmed multiplier control unit for booths multiplier. **Text Book 3:** Chapter 4: 4.1 to 4.3.2	**10 Hours**
Module-5	
MEMORY SYSTEMS: Basic concepts, Internal organization of memory chips, Structure of Larger Memories, Memory Hierarchy, Cache memories-mapping functions, Placement strategies, Replacement algorithms, Performance considerations, Virtual memories, Magnetic hard disk **Text Book 1:**Chapter 8: 8.1, 8.2.1, 8.2.5, 8.5, 8.6, 8.6.1, 8.7, 8.8, 8.10, 8.10.1, 8.12 **Text Book 3:** Chapter 5: 5.8	**10 Hours**
Module-6	
INPUT/OUTPUT ORGANIZATION: Accessing I/O devices, I/O Device Interface, Program-Controlled I/O, Interrupts, Enabling and Disabling Interrupts, Handling Multiple Devices, Controlling I/O Device Behavior, Processor Control Registers, Direct Memory Access. **Text Book 1:** Chapter 3: 3.1, 3.1.1, 3.1.2, 3.2, Chapter 8: 8.4	**3 Hours**
Module-7	
INTRODUCTION TO PARALLEL ARCHITECTURE: Pipelining- Basic Concept, Pipeline Organization, Pipelining Issues, Data Dependencies, Operand Forwarding, Handling Data Dependencies in Software, Memory Delays, Branch Delays, Unconditional Branches, Conditional Branches, The Branch Delay Slot, Hardware Multithreading, Vector (SIMD) Processing, Graphics Processing Units (GPUs), Shared-Memory Multiprocessors,	**8 Hours**

Interconnection Networks, Cache Coherence, Write-Through Protocol, Write-Back protocol, Snoopy Caches, Directory-Based Cache Coherence **Text Book 1**: Chapter 6: 6.1 – 6.6, Chapter 12: 12.1 – 12.4	

Course outcomes:

After studying this course, students will be able to:

1. Describe the functionalities of the various units of computers and the instruction set architecture. .
2. Appreciate the hardware implementation of addition, subtraction, multiplication and division and perform arithmetic operations. .
3. Design the control unit for simple algorithms .
4. Explain basics of memory system such as cache memories, mapping functions, replacement algorithms and virtual memory concept and design simple memory systems.
5. Outline the I/O handling techniques and realize the improvement in performance using the concepts of pipelining and parallel processing. .

Text Books:

1. Carl Hamacher, ZvonkoVranesic and SafwatZaky, *Computer Organization and Embedded Systems,* (6e), McGraw Hill Publication, 2012.
2. William Stallings, *Computer Organization and Architecture – Designing for Performance,* (9e), PHI, 2015.
3. Mohammed Rafiquzzaman and Rajan Chandra, *Modern Computer Architecture,* Galgotia Publications Pvt. Ltd., 2010.

Reference Books:

1. D.A. Patterson and J.L.Hennessy, *Computer Organization and Design-The Hardware/Software Interface,* (5e), Morgan Kaufmann, 2014.
2. J.P.Hayes, *Computer Architecture and Organization,* McGraw Hill Publication, 1998.