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MANIPAL INSTITUTE OF TECHNOLOGY
(Constituent Institute of Manipal University)
MANIPAL-576104

III SEMESTER B.TECH.(COMPUTER SCIENCE AND ENGINEERING) DEGREE
MAKE-UP EXAMINATION-DECEMBER 2014
SUBJECT: COMPUTER ORGANIZATION AND DESIGN (CSE 201)
DATE: 30-12-2014

TIME: 3 HOURS MAX.MARKS: 50

Instructions to Candidates

- Answer any **FIVE** full questions.
- Clearly show each step of the calculation wherever required

1.A. Explain the various functional units of the computer.
1.B. Differentiate between register direct and register indirect addressing modes with syntax and examples.
1.C. With a neat diagram of the internal organization of the 4 bit CLA, explain its working. (3+2+5)

2.A. Explain the 4 bit Booths multiplication for 2's complement numbers with a neat flowchart and using this multiply -4 with 6.
2.B. Nonrestoring division avoids the need for restoring after unsuccessful subtraction. Justify with example.
2.C. What are guard bits in IEEE floating point arithmetic? Explain the three truncation methods with examples. (5+2+3)

3.A. Draw the block diagram of AM 2901 bit slice processor
3.B. Briefly explain the three bus architecture of ALU with a neat diagram.

3.C. For the following Register Transfer Description

Declare registers A[8], B[8], C[8];
START: A←0;
B←00001010;
LOOP: A← A+B;
B←A-B;
IF B> 0 then go to LOOP;
C← A;
HALT: go to HALT;

Draw the micro-programmed control unit. Also show the control memory contents. (3+2+5)

4.A. Build hardware to implement each of following register transfer:

a) If X is even then A←B+C
   Else A←(B.C)'
b) If X is zero then A← A+1
   Else A←A-1
c) IF A>B and D[0]=0 then A←B

Assume that A,B,C ,D and X are 4-bit registers

4.B. Differentiate between hardwired and microprogrammed approach of control unit design.

4.C. Explain the role of memory controller with a neat diagram. (6+2+2)

5.A. With diagrams explain the direct and associative mapping functions of cache for the following memory assumptions

a. Main memory is addressable by a 16-bit address and is word addressable
b. Main memory has 4096 blocks of 16 words each
c. Cache consisting of 128 blocks of 16 words each

5.B. Explain the following with respect to memory.

a. write-through protocol
b. locality of reference

5.C. With a neat diagram explain the address translation process in virtual memory.

(5+2+3)

6.A. What are the challenges in handling interrupts in multiple devices and how are they addressed?

6.B. What is DMA and how is it carried out? (5+5)