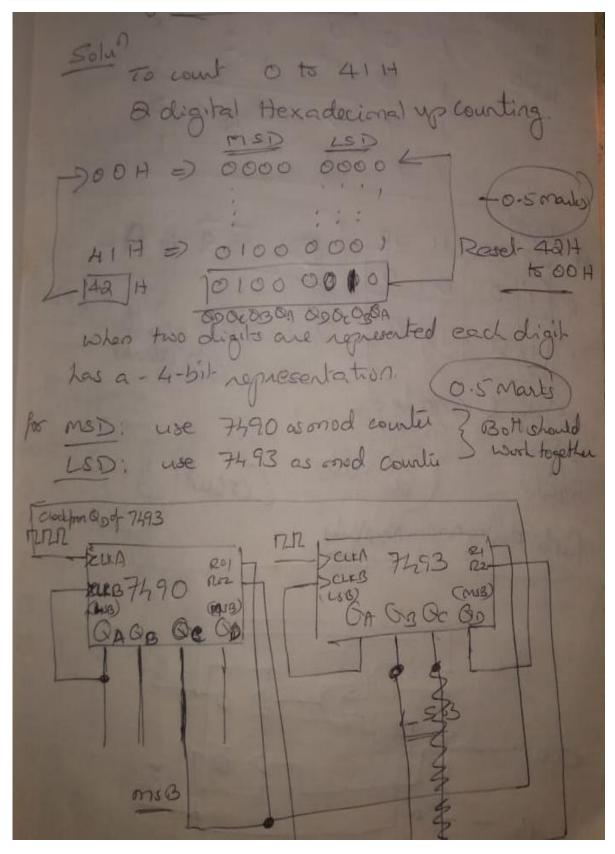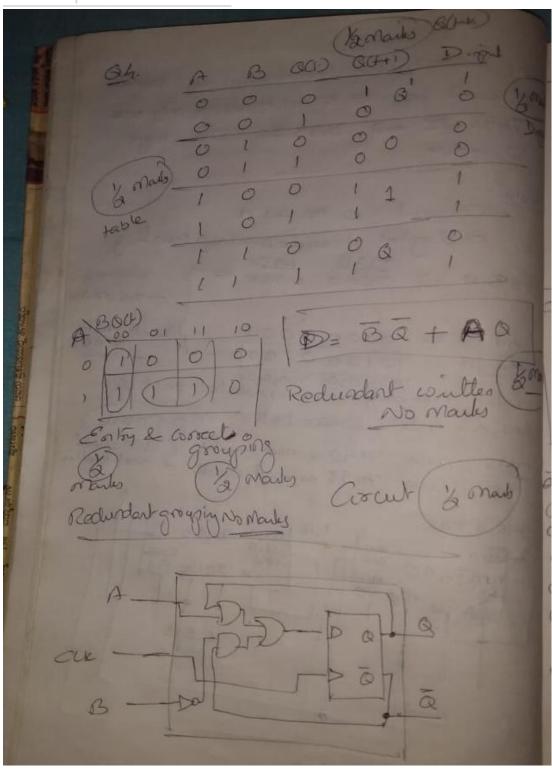Q2. Construct a hexadecimal up counter to count from 0 to 41H using only one 7490 IC and one 7493 IC. Draw the logic diagram.. 3 Marks

Sol^n

To count 0 to 41 H

a digital Hexadecimal up counting.

MSD   LSD

→00H ⇒ 0000   0000 ←

⋮   ⋮ ⋮ ⋮

41 H ⇒ 0100 0000 | Reset 42H

⌐42 H |0100 00 ● 0| to 00 H

$Q_D Q_C Q_B Q_A$ $Q_D Q_C Q_B Q_A$

when two digits are represented each digit

has a - 4-bit representation.   0.5 Marks

for MSD: use 7490 as mod counter } Both should
    LSD: use 74 93 as mod counter } work together

— 0.5 marks

Clock from Q_D of 7493

⌐ЛЛЛ

CLKA   RO1
                        RO2
CLKB 7490   (MSB)
(LSB)
$Q_A Q_B Q_C Q_D$

ЛЛ
CLKA 7493 Q1
CLKB   Q2
(LSB)   (MSB)
$Q_A Q_B Q_C Q_D$

MSB

Q4. Function table defines the working of a fictious AB flip flop. Design the AB flip flop using D flip flop and external gates. **3 Marks**

A	B	Q(t+1)
0	0	Q'
0	1	0
1	0	1
1	1	Q

A —| A   Q |—
B —| B
   —|> Clk

½ Marks (60-K)

Q4.

A	B	Q(t)	Q(t+1)	D input
0	0	0	1	Q'	1
0	0	1	0		0
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	1	1	1
1	0	1	1		1
1	1	0	0	Q	0
1	1	1	1		1

½ marks

table

B Q(t)

A \ 00 01 11 10
0 [1   0   0   0]
) [1   1   1   0]

$$D = B\bar{Q} + AQ$$

Redundant written
No Marks

Entry & correct grouping
½ marks

Redundant grouping No Marks   Circuit ½ marks

Q5. Design a JK flip flop using a basic NOR latch and gates

Q5

Function table of J-K

CLK	J	K	Q(t+1)	(½ marks)
0	X	X	Q(t)	No change
1	0	0	Q(t)	No change
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	Q̄(t)	Toggle

(1 Marks) → excitation Table ⇒

Function table of S-R latch NOR Circuit

Set Reset Q(t+1)

S	R	Q(t+1)	
0	0	Q(t)	No change
0	1	0	Reset
1	0	1	Set
1	1		Invalid

Q(t)	Q(t+1)	Set	Reset
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

&

CLK	J	K	Q(t)	Q(t+1)	Set	Reset
0	0	0	0	0	0	X
0	0	0	1	1	X	0
0	0	1	0	0	0	X
0	0	1	1	1	X	0
0	1	0	0	0	0	X
0	1	0	1	1	X	0
0	1	1	0	0	0	X
0	1	1	1	1	X	0
1	0	0	0	0	0	X
1	0	0	1	1	X	0
1	0	1	0	0	0	X
1	0	1	1	0	0	1
1	1	0	0	1	1	0
1	1	0	1	1	X	0
1	1	1	0	1	1	0
1	1	1	1	0	0	1

(½ Marks) Table Entry

(½ Marks)

Reset

Cuj \\ JQ	00	01	11	10
00	X	0	0	X
01	X	0	0	X
11	0	0	R	0
10	X	0	b	X

Reset = CLK·K·Q

(½ marks)

Cuj \\ JQ	00	01	11	10
00	0	X	X	0
01	0	X	X	0
11	1	X	0	0
10	0	X	0	0

Set

Set = CLK·J·Q̄

Circuit (½ marks)

J ──
CLK ──
K ──

Set
Reset

Q
Q̄