

ICT 2256: COMPUTER ORGANIZATION AND MICROPROCESSOR SYSTEMS [3 credit]

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Syllabus:

Microprocessor 8086 Architecture, Pin diagram, Modes of operation, Segmentation and memory addressing, Addressing modes, Assembler directives, Assembly language development tools, Instruction set, Stacks and subroutine, Macros and procedures, Assembly language programming, Interrupts, BIOS and DOS interrupts, Basic IO interfacing- 8255 Programmable Peripheral Interface, 8254 Programmable Interval Timer, 8259 Programmable Interrupt Counter, Computer Organization: Introduction, Execution Unit - Combinational shifter design, Adders, Arithmetic and Logic Unit design, Multiplication algorithms, Division algorithms., Control Unit-Introduction, Basic concepts, Hardwired and Micro programming approach, Memory Unit, Input & Output.

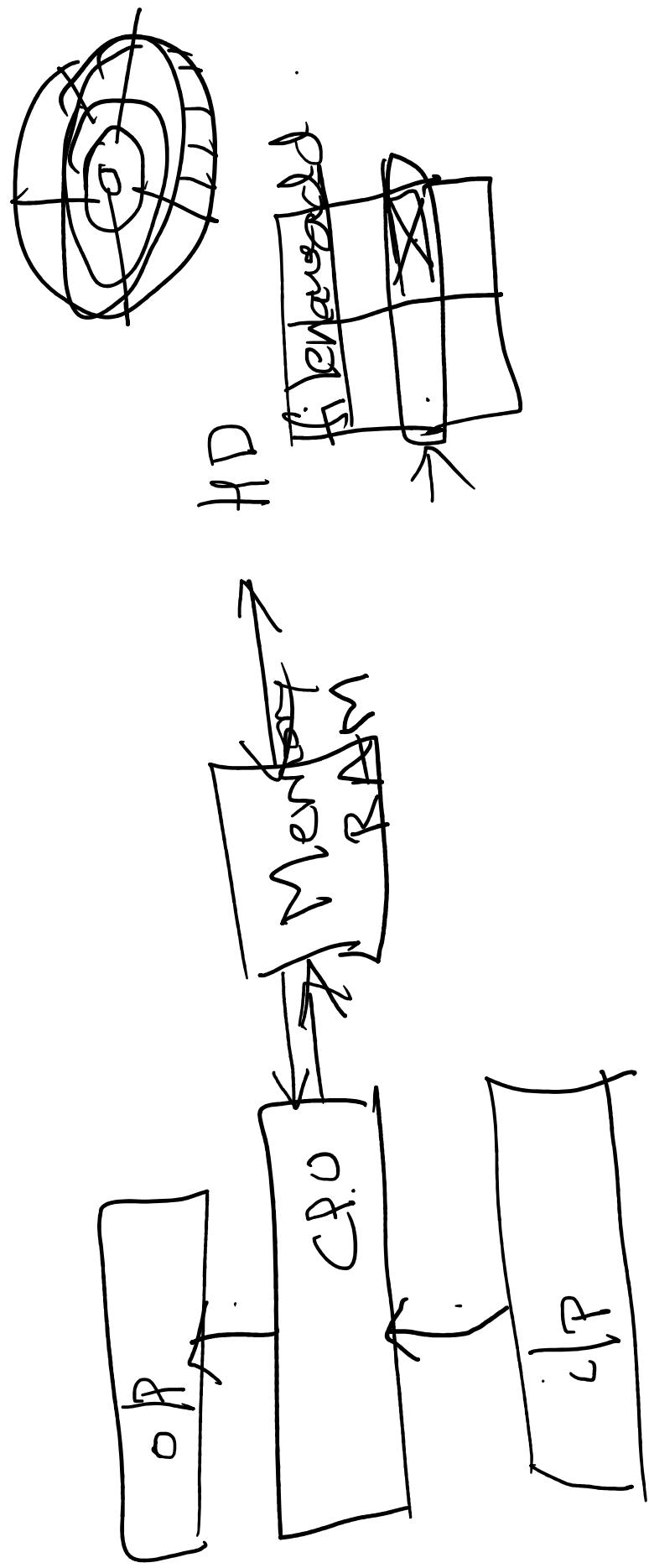
Course Outcomes:

- Recall 8086 architecture
- Write assembly language programs using development tools
- Understand the interfacing of programmable devices to 8086 microprocessor
- Understand the organisation of various parts in computer system
- Design building blocks of computer system

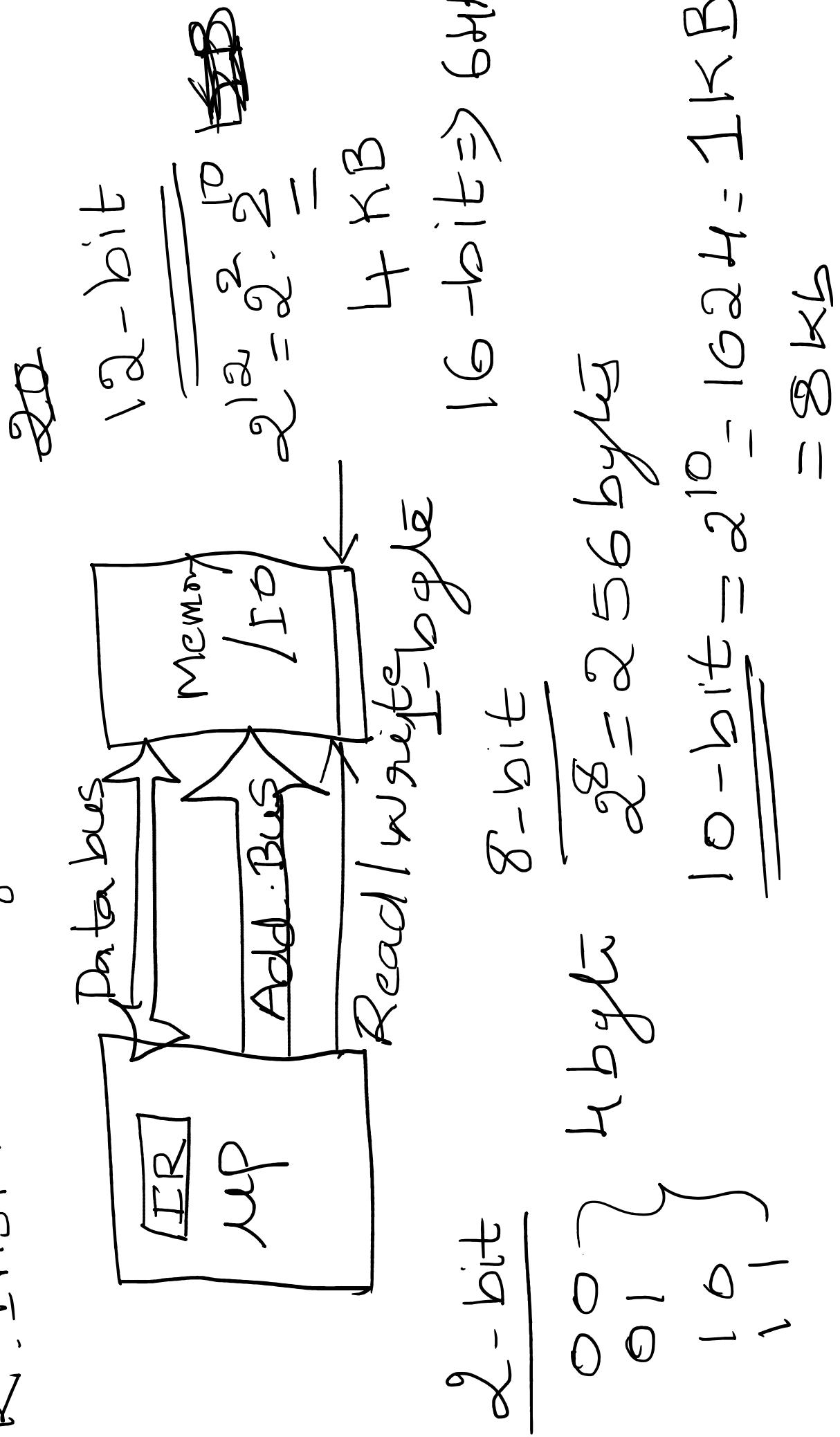
References:

- Hall D.V., *Microprocessors and Interfacing: Programming and Hardware* (3e), Tata McGraw Hill, 2017, ISBN-10: 9781259006159
- Brey B.B., *The Intel Microprocessors: 8086 to Pentium Pro - Architecture, Programming and Interfacing* (8e), Prentice Hall of India, 2012
- Udaykumar K, Umashankar B.S., *Advanced microprocessors and IBM -PC assembly language programming*, McGraw Hill Education, 2017.
- Rafiquzzaman M and Rajan C., *Modern computer Architecture*, Galgotia Publications Pvt. Ltd, 2012.

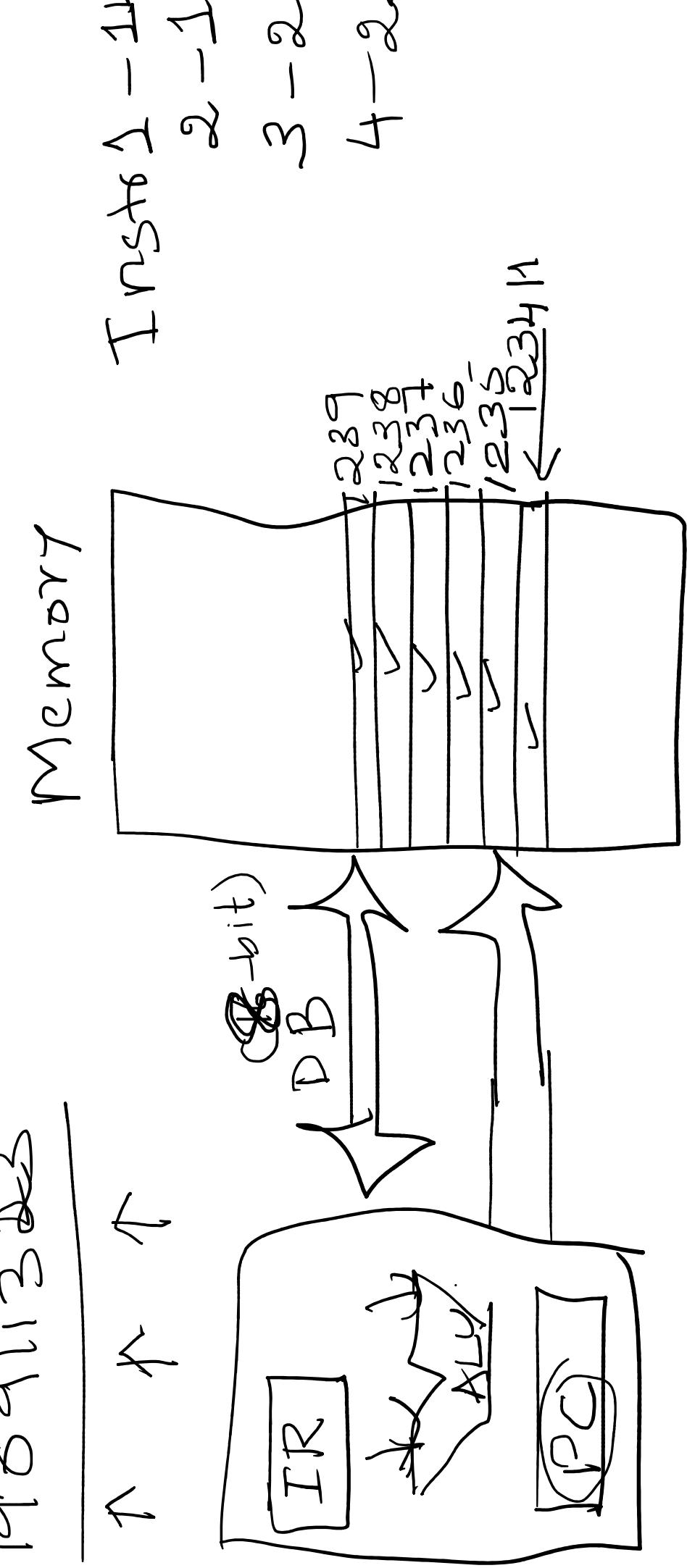
What is a microprocessor?



TR - Instru - Register



PC: Program Counter } Instr. Counter } Instr. Pointers } Instr. } Instr. Counter }



$$2^{20} = 2^{10} \cdot 2^{10} = 1024 \text{ MB} = 1 \text{ GB}$$

$$2^{24} = 16 \text{ MB}$$

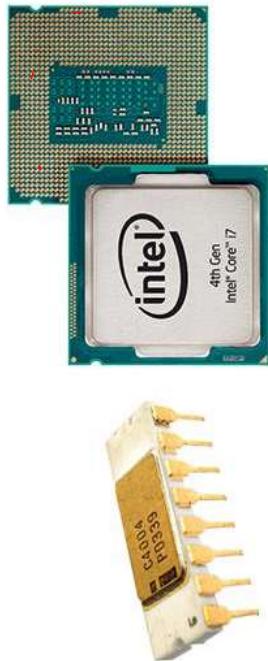
$$2^{30} = 2^{10} \cdot 2^{20} = 1024 \text{ MB} = \frac{1 \text{ GB}}{1 \text{ TB}}$$

$$2^{40}$$

$$\left. \begin{array}{c} 2^0 \\ 2^0 \end{array} \right\} =$$

History of Microprocessor

MP	Introduction	Data Bus	Address Bus
4004	1971	4	8
8008	1972	8	8
8080	1974	8	16
8085	1977	8	16
8086	1978	16 //	20
80186	1982	16	20
80286	1983	16	24
80386	1986	32	32
80486	1989	32	32
Pentium	1993 onwards	32	32
Core solo	2006	32	32
Dual Core	2006	32	32
Core 2 Duo	2006	32	32
Core to Quad	2008	32	32
i3,i5,i7	2010	64 ←	64 ← 0



Few manufacturers

- AMD
- Mitsubishi
- NEC
- OKI
- Toshiba
- Siemens



✓

Basic elements of Microprocessor

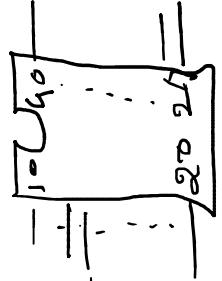
To perform an operation
microprocessor requires:

- Registers
 - Arithmetic and Logic Unit (ALU)
 - Control Logic
 - Instruction register
 - Program counter
 - Bus
- Ans i de up*
- o write*
- Click to add text*
- Internal External (Add. bus / Data bus)*

Basic elements of Microprocessor

Basic elements of Microprocessor

8086 Microprocessor: Features

1. 16-bit \rightarrow ALU, Registers, Data bus \rightarrow 16-lines
2. 20-bit address lines. $2^{20} = 1\text{MB}$
3. 40-pin dual in-line pin package \rightarrow 
4. 5 MHz clock $\underline{\underline{\underline{\underline{\underline{\text{clock}}}}}}$
5. 4-Memory Segmentation: code segment
Data "",
Stack "",
Extra ""
6. 5V, and

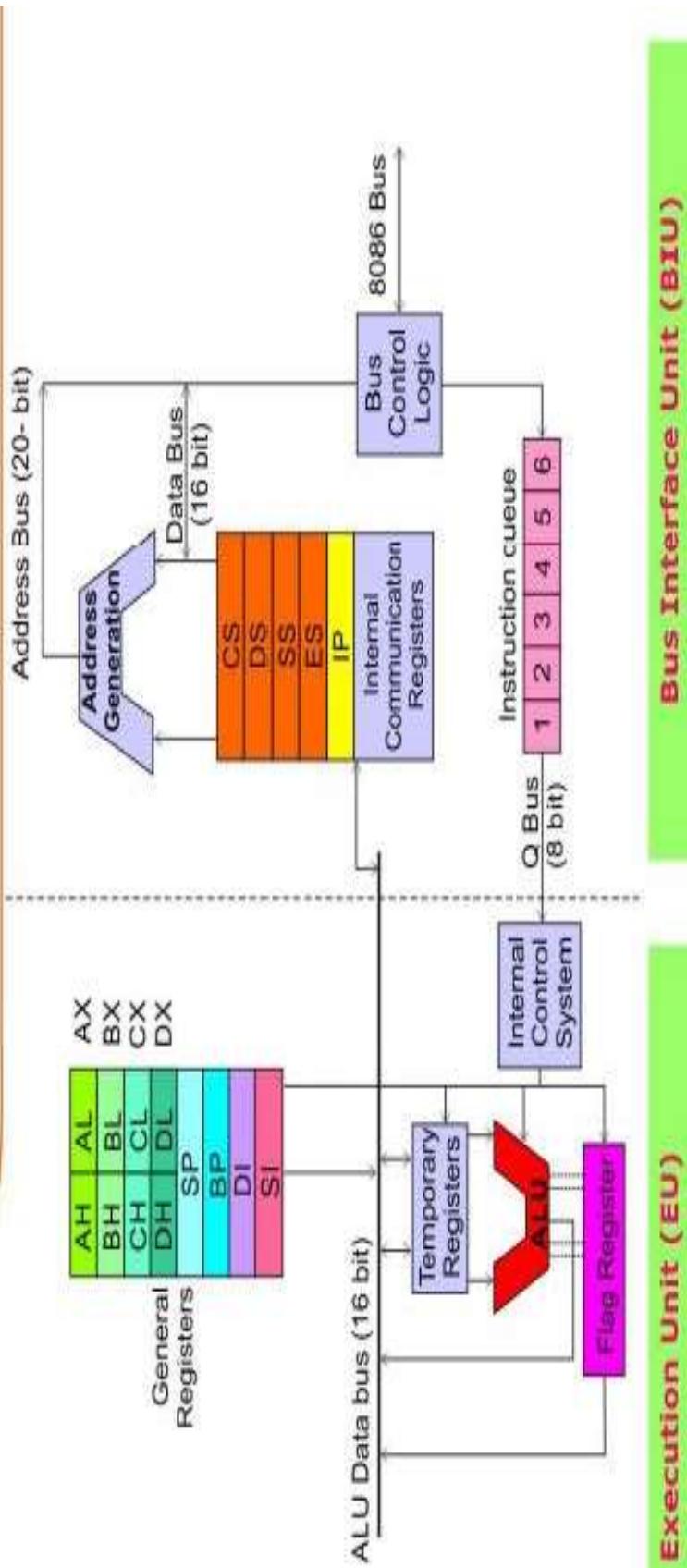
8086 Microprocessor : Features

- ↳ 16 - bit Microprocessor → ALU, Registers, Instructions on 16-bit data -
 - ↳ 16-bit data bus → 20
 - ↳ 20-bit Address bus → 1,048,576 → 1M bytes
 - Higher Address Bits → MS Bits
 - Lower Address Bits → LS Bits
 - ↳ 8-bit

Internal architecture of 8086

8086 Microprocessor

Architecture



Execution Unit (EU)

EU executes instructions that have already been fetched by the BIU.
BIU and EU functions separately.

Bus Interface Unit (BIU)

BIU fetches instructions, reads data from memory and I/O ports, writes data to memory and I/O ports.

Internal architecture of 8086

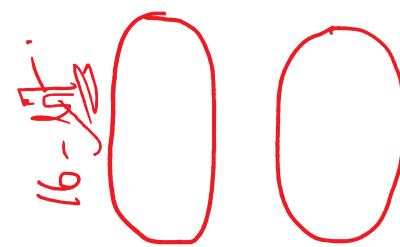
Q

Segment Register



Register

DX
BX
CX
AX



→ 6 - 15K

Instruction Decoder

ADP (A₁₅)

Flag

8086 Microprocessor: Architecture

Two main parts:

1. Bus interface unit (BIU)

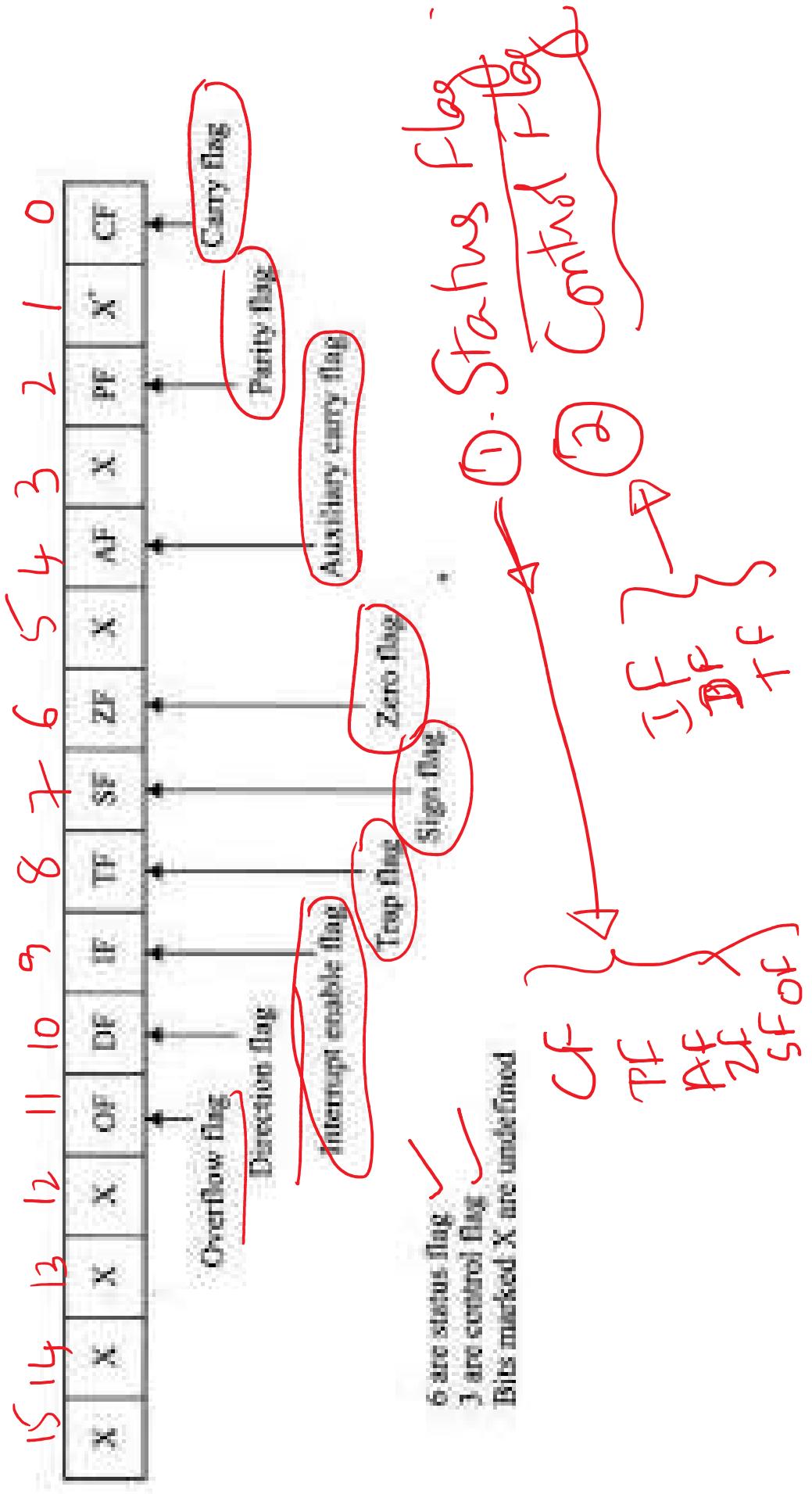
2. Execution Unit

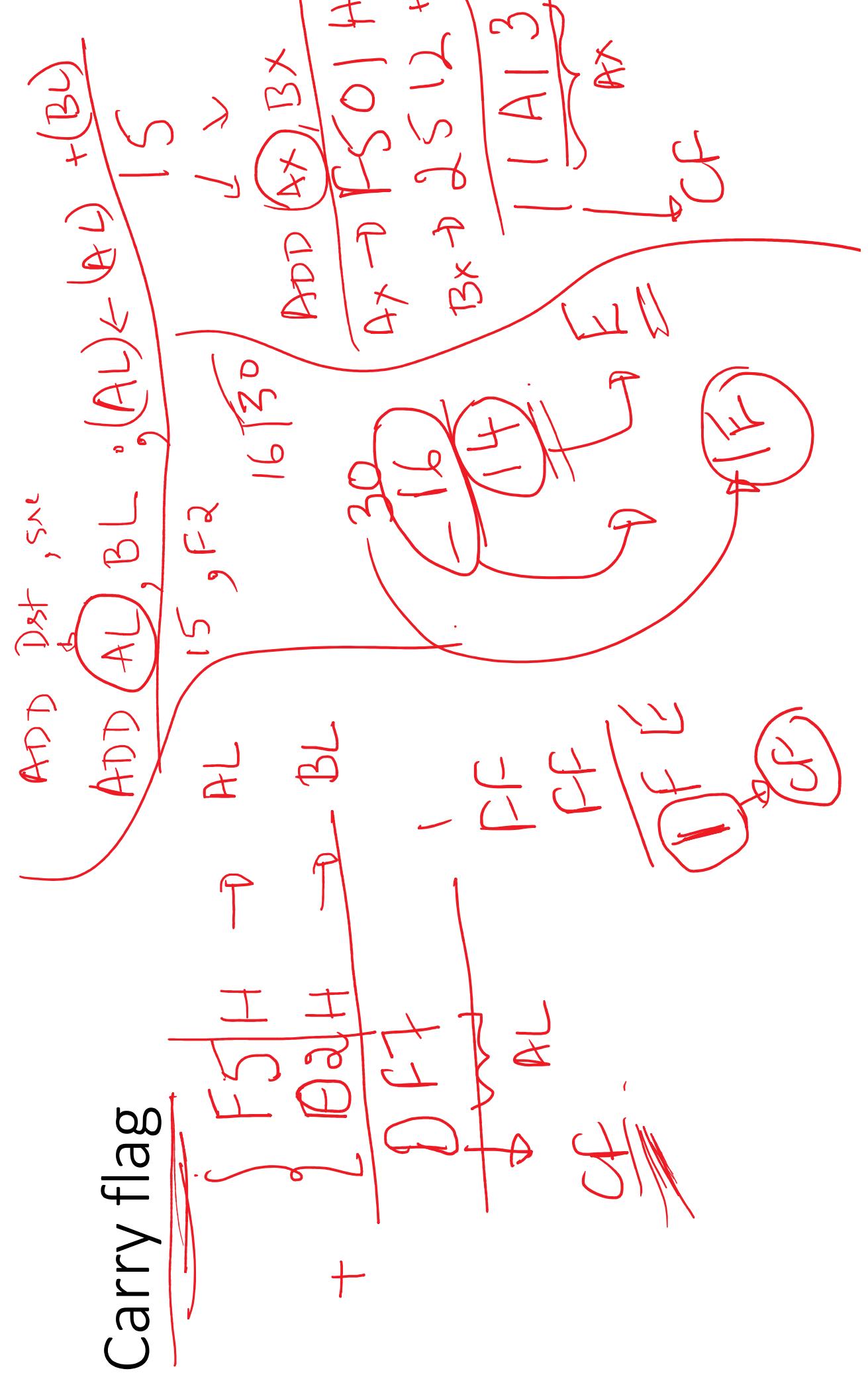
→ Spreads up preexisting

8086 Microprocessor : Execution Unit

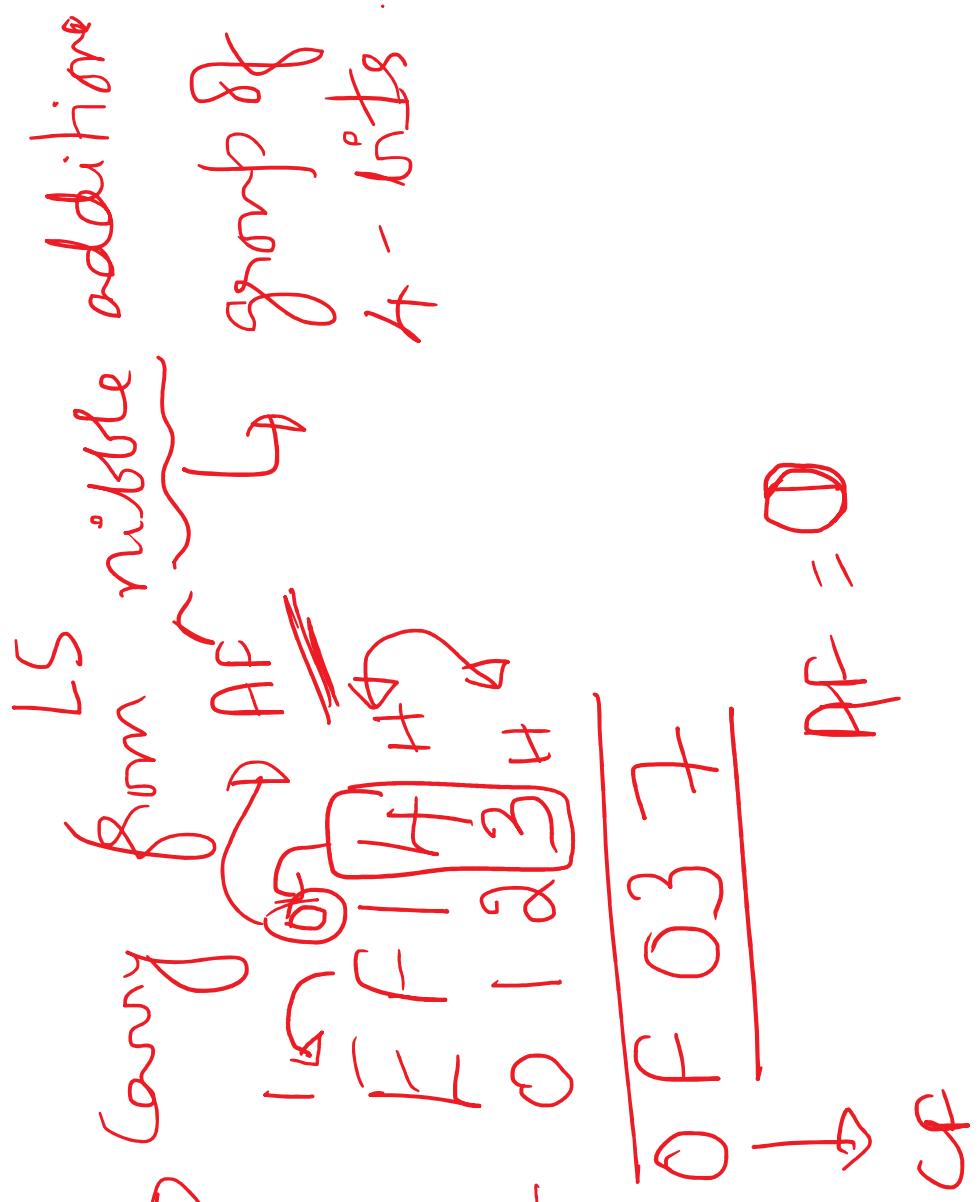
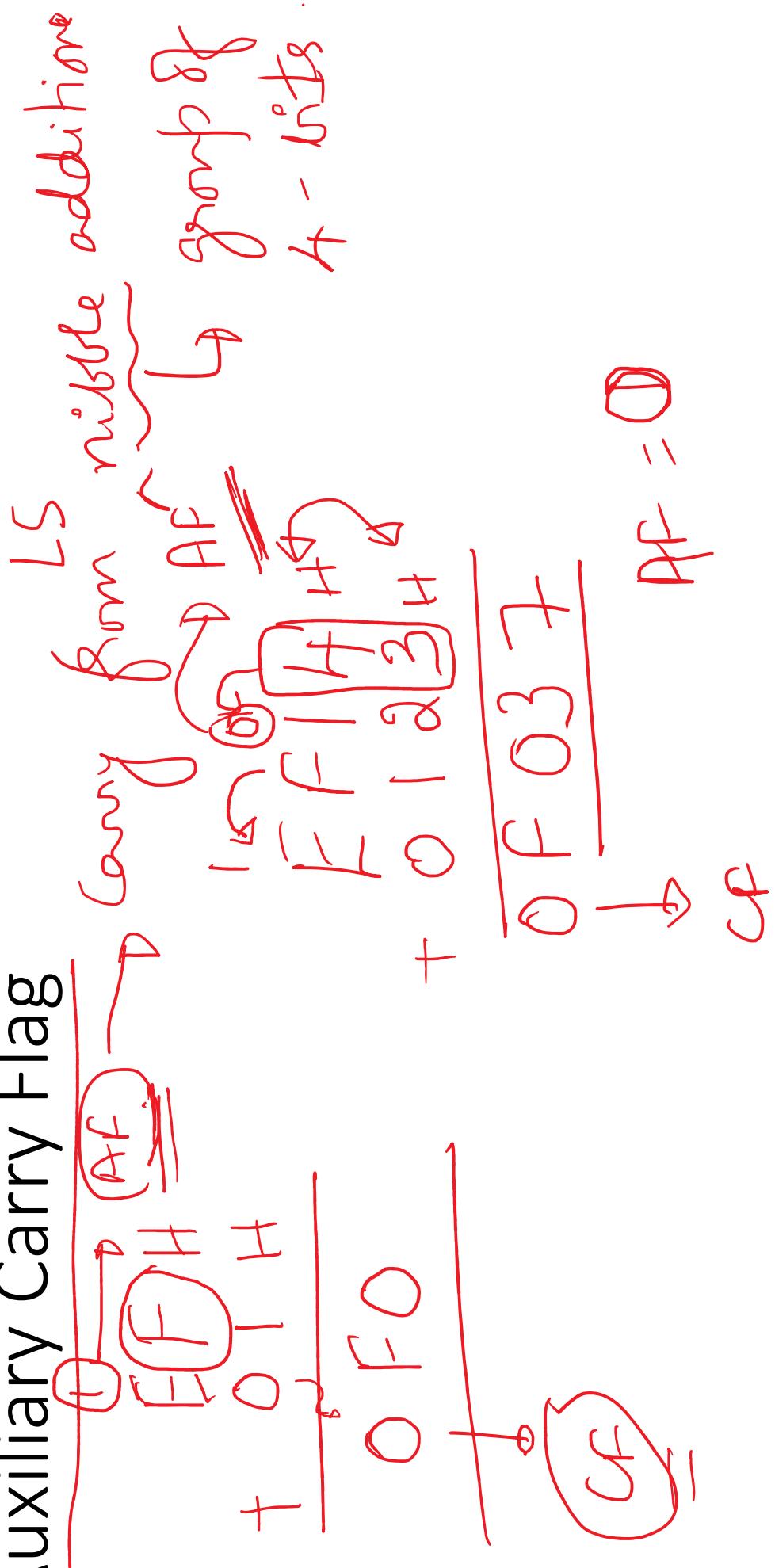
- 16-bit ALU → Add, SUB, DIV, MUL, OR, XOR, AND, SHR, ROTATE.
 - Control system and Instruction decoder
 - 8 16-bit registers:
 - Four 16-bit general purpose registers (AX (Accumulator), BX, CX, DX) OR (4x2)=8 8-bit general purpose registers (AH, AL, BH, BL, CH, CL, DH, DL)
 - Four 16-bit special purpose registers
 - SP – Stack Pointer
 - BP – Base Pointer
 - SI – Source Index
 - DI – Destination Index
 - 16-bit flag register
- (Control part of CPU)*
- Registers*
- Stack*
- Segment Register.*
- Register.*
- Segment Register.*

8086 Microprocessor : Flag register





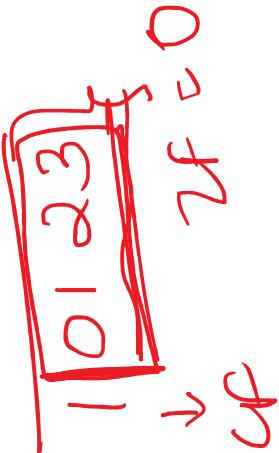
Auxiliary Carry Flag



D
E
F

十一

HODGSON



$$\begin{array}{r}
 00\mid 24 \\
 0023+ \\
 \hline
 0035
 \end{array}$$

卷之三

Zero Flag

2

1

—

A simple red ink sketch of a face. The face has a large, irregular oval shape. It features two large, circular eyes with thick black outlines and small pupils. A wide, horizontal mouth is positioned below the eyes. The sketch is done with a single continuous line.

Digitur

10

6

118

1

0 → 2

Parity Flag

$$\begin{array}{r} 12H \\ + 32H \\ \hline 44 \end{array}$$

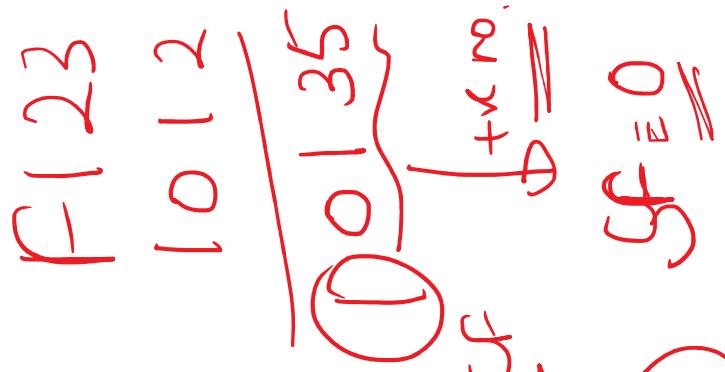
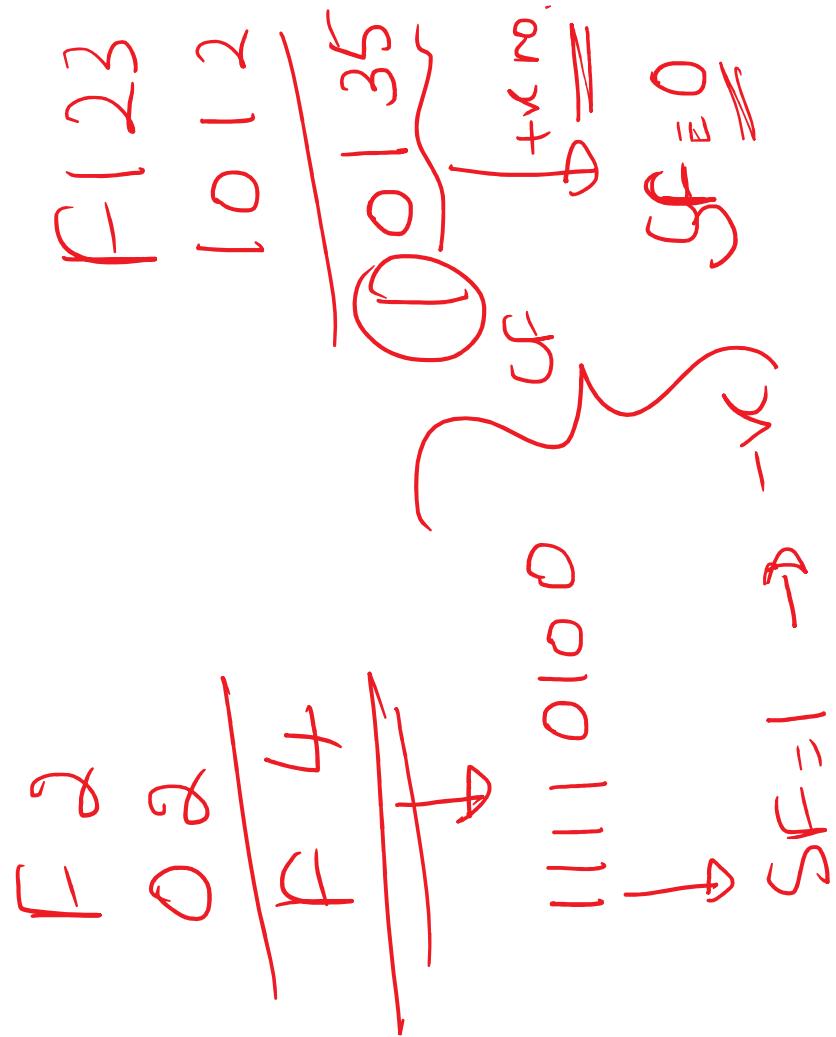
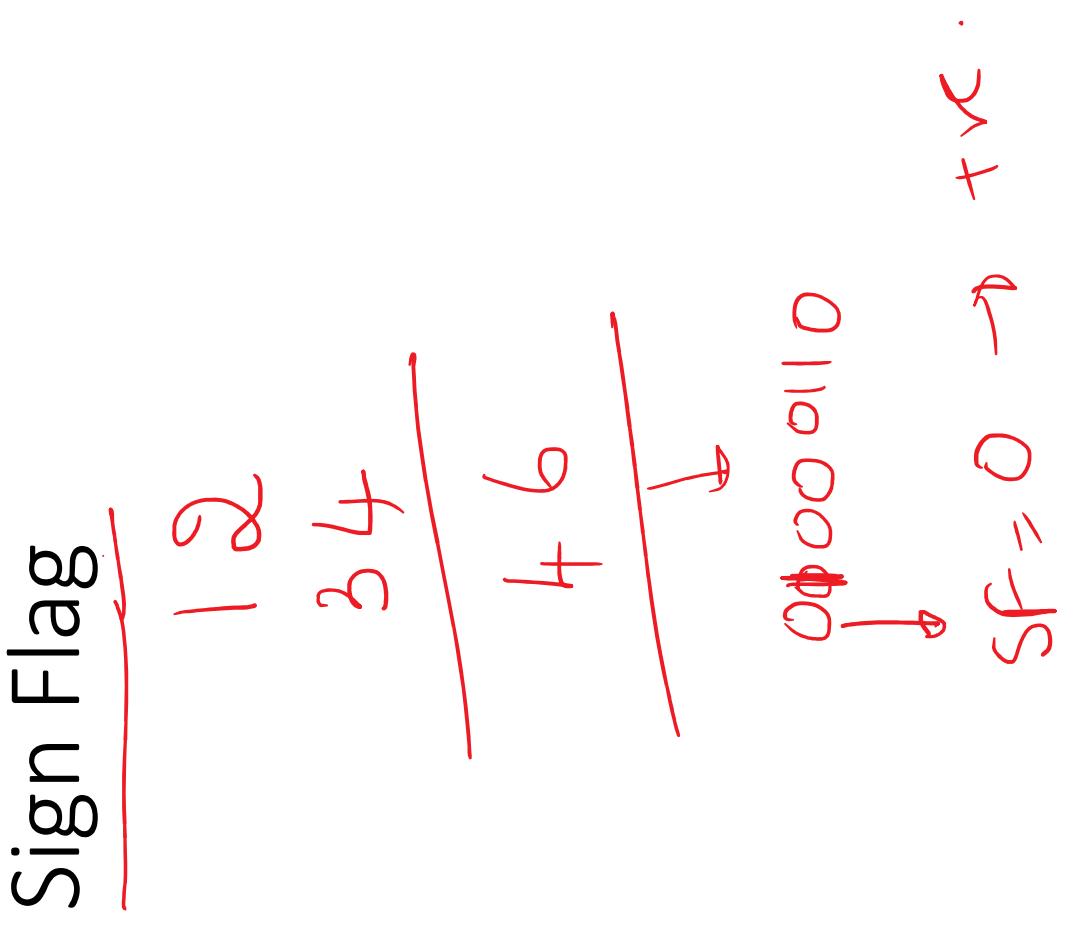
0100 0100
↓-1's →

$$\begin{array}{r} \text{Even parity} \\ 0000000101000100 \\ \hline PF = 1 \end{array}$$

$$PF = 1$$

$$PF = 0$$

$$\begin{array}{r} \text{Even 1's in} \\ 01172H \\ 0032H \\ \hline 0144H \\ 0000000101000100 \\ \hline PF = 1 \end{array}$$



Overflow Flag

11
12
13

178

44

\Rightarrow

$$\begin{array}{r} -\pi \\ +\pi \end{array}$$

Answers

$$\begin{array}{r}
 +v \\
 +ve \\
 \hline
 -v
 \end{array}$$

~~$v_i/v_m + v_r = v - v_e$~~

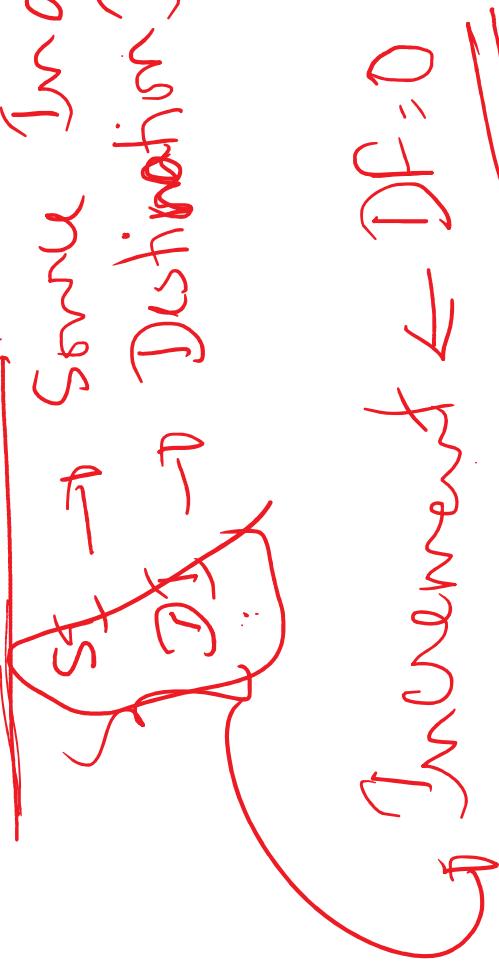
Correct

. 5

Control Flags

- Direction Flag
- Interrupt Flag
- Trap Flag

~~Direction Flag~~



$$DF = \cancel{1} - \cancel{0} \rightarrow DF = 1$$

Decrement

~~Memory~~

Source Index

Destination Index

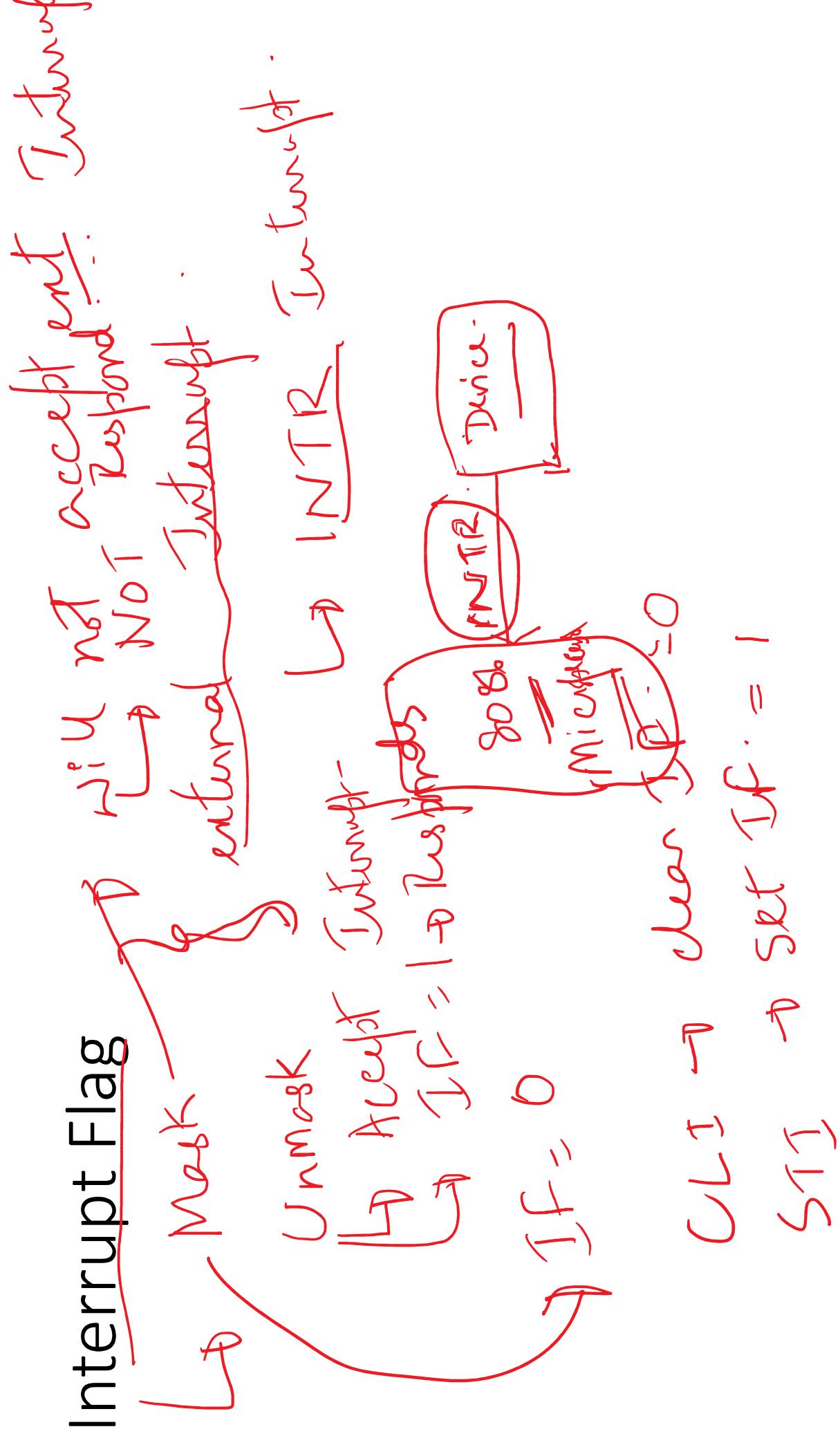


Set Direct flag
Clear Direct flag

STD

C LD

Clear Direct flag

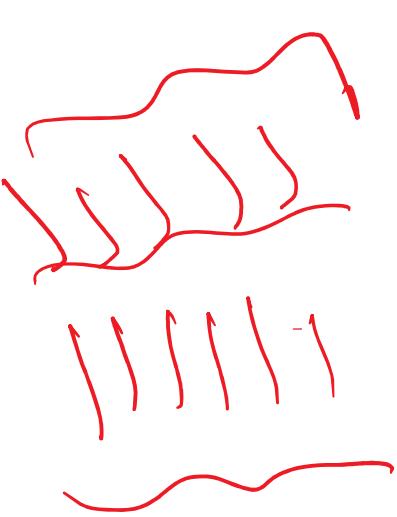


Trap Flag (TF)

$$\text{TF} = 0 \rightarrow$$

$$\text{TF} = 1 \rightarrow$$

Trap Flag (TF)
is interrupted at the
end of every instruction



8086 Microprocessor : Bus Interface Unit

- Segment Registers
 - 4 Segment Registers
 - 16-bit Register
 - Instruction Queue →
 - FIFO Register
 - Instruction Pointer →
 - CS Register
 - 16-bit Register
 - Points to address of next instruction to be fetched & executed.
-
- The diagram illustrates the internal structure of the 8086 Bus Interface Unit. It features a central bus with various components connected to it. On the left, there is a stack of four boxes labeled 'Segment Registers' (BX, BP, SI, DI) and a box labeled 'Instruction Queue' (FIFO Register). A large oval labeled 'Cache' is positioned above the bus. To the right, there is a 'CS Register' (Instruction Pointer) and a '16-bit Register'. Arrows indicate the flow of data between these components and the central bus.

Need of Segmentation in 8086

- ⇒ Doesn't memory using 16-bit
- ⇒ Segmented memory
- ⇒ Speed increases
- ⇒ Multiple segments

Registers

16-bit

using

⇒ Doesn't memory using 16-bit

⇒ Segmented memory

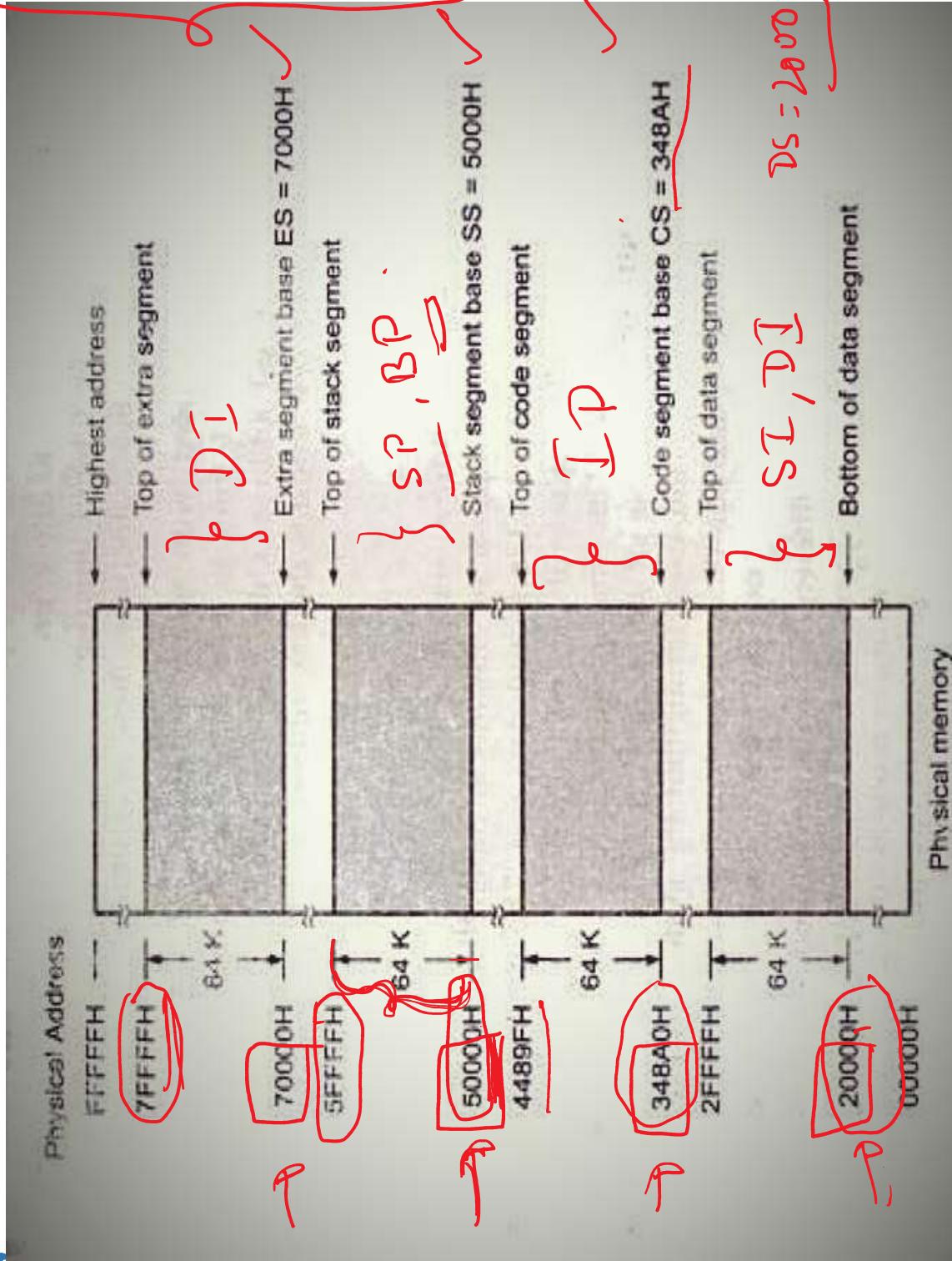
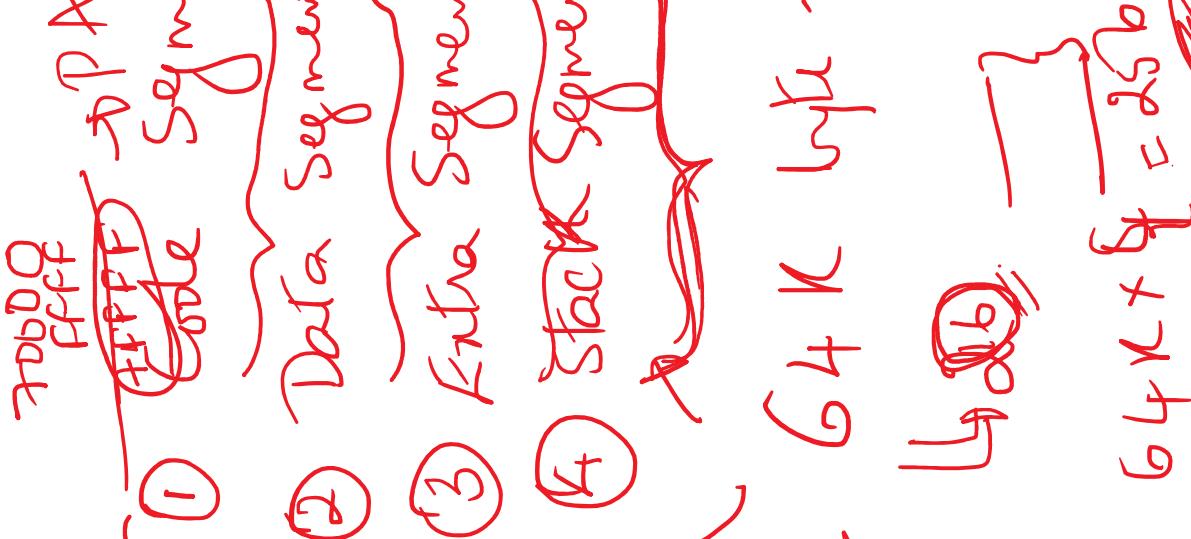
⇒ Speed increases

⇒ Multiple segments

Segmentation in 8086

$$ES = 7000H$$

$$DI = FFFFH$$



8086 Microprocessor : Bus Interface Unit

Segment Registers:

- Extra Segment (ES)
 - Code Segment (CS)
 - Stack Segment (SS)
 - Data Segment (DS)
- Registers {
 Base Register
 Register
 Register
 Register }
- 16 - bits
- Base address
Starting address
Up
- 16-bit
higher
Stack
Register
→
- 16-bit
higher
Stack
Register
→
- Base
address
is
always
lower
- Base
address
is
always
lower

- 20 – bit physical address generation

$$\begin{array}{l} \text{IP} = 123CH \rightarrow \\ \text{CS} = 2345H \rightarrow \\ \text{Physical Address} \rightarrow \\ \hline \text{Physical Address} \rightarrow \\ \text{Offset \& Effective Address} \\ \text{Address of Code Segment} \\ \hline \end{array}$$

2468C, H

$$SI = 1250 + \text{offset}, \quad EA -$$

$$DS = 492BH \rightarrow BA -$$

$$\begin{array}{r} 492BO \\ - 1250 \\ \hline 47506H \end{array}$$

PA =
Physical Address