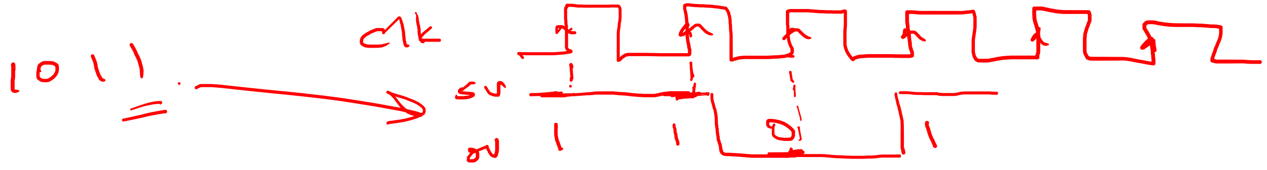
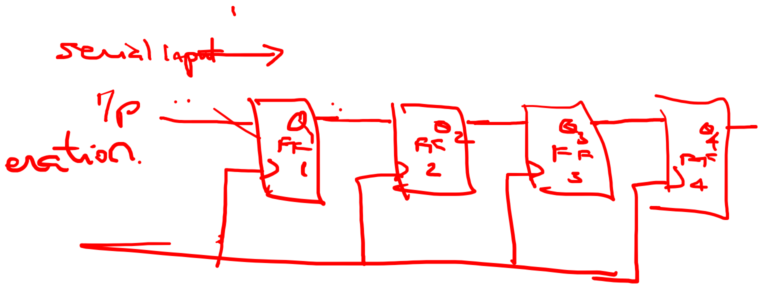
Shift registers and shift register counters

Registers



- Register is a group of flip flops (D, or SR,or JK)
- Each flip flop can store one-bit data. n-bit register can hold n-bit data.
- There are two ways to shift the data into the register and two ways to shift the data out of the register.
- Accordingly: 4 categories of shift register are
  - Serial in Serial out (SISO)
  - Serial In parallel out (SIPO)
  - Parallel in Serial out (PISO)
  - Parallel in parallel out (PIPO)

Example: 4-bit shifting operation.



1 0 1 1

1011

st input

Clk	Q1	Q2	Q3	Q4
	x	x	x	x
	1	x	x	x

serial shift

Simple 4-bit-shift Register

SISO and SIPO Register

1101

MSB LSB
1101

RESET — LOW — HIGH

Q_0 0 —
Q_1 0 —
Q_2 0 — Normal operation
Q_3 0 —

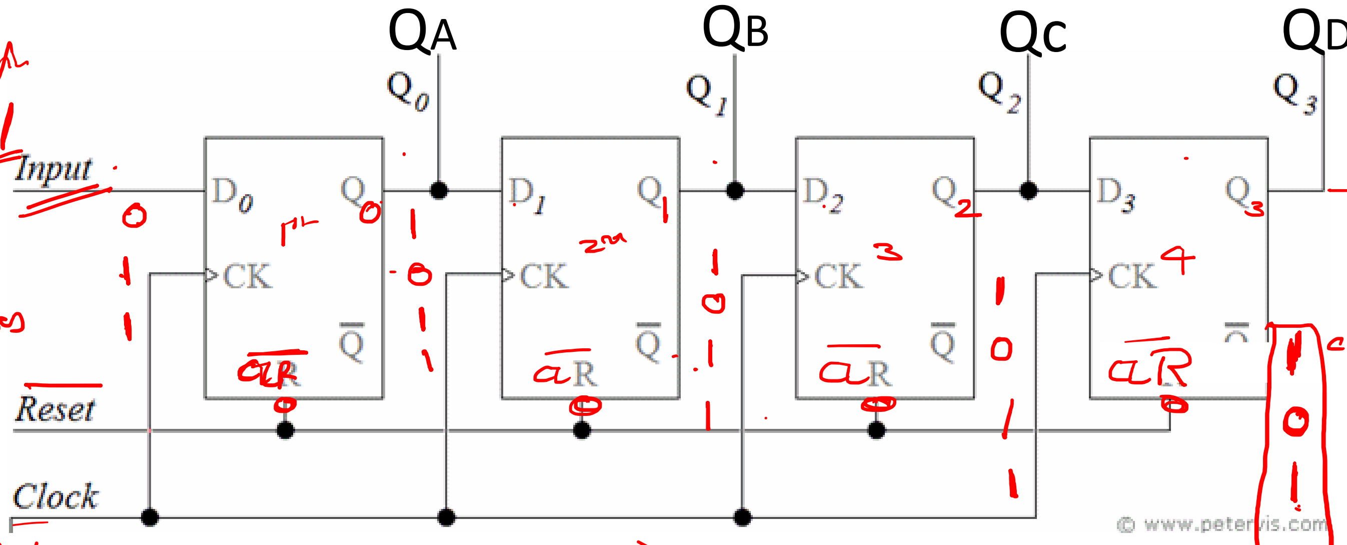
- Simple 4-bit shift register is shown below (Reset is nothing but clear input)

Little endian concept
LSB is first

n-bit
MSB . . . . . LSB

- Register is cleared using reset/clear input.
- It can be used as Serial-in serial out (at Q_D) and Serial-in parallel out shift register.

Ex: Look
1 1 0 1



In a n-bit shift register
there requires n-clock pulses
to store the n-bit data serially

at 1st clock pulse
1st bit (LSB) is available o/p serially

positive edge triggered clocks

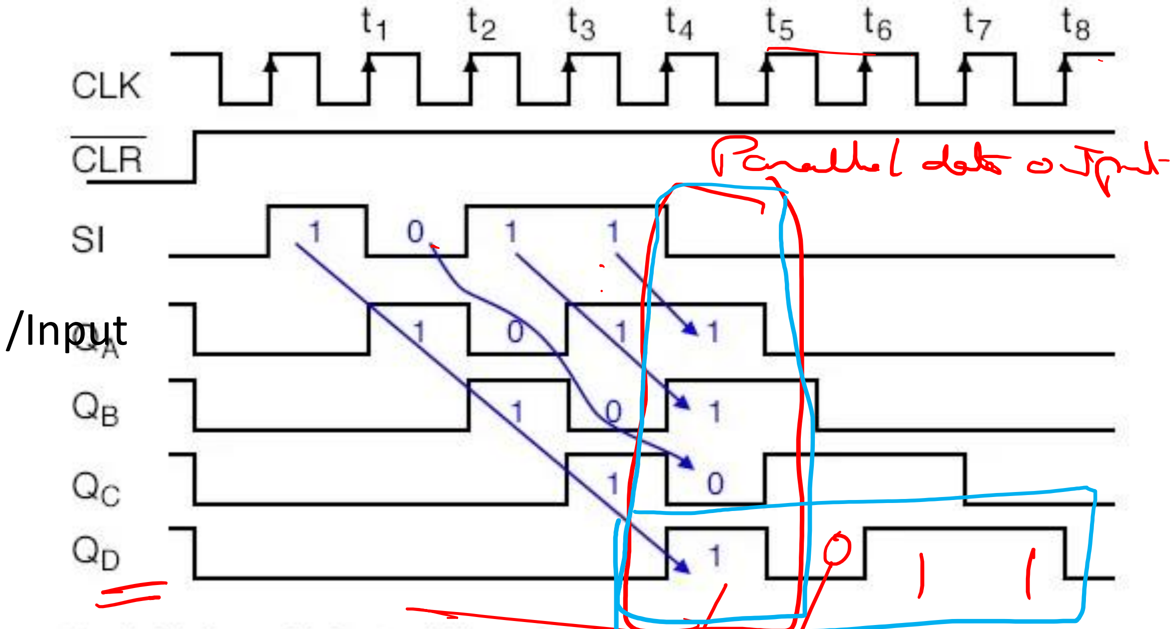
these requires (2n-1) clock pulses
for completely flush out data serially at o/p

1 0 1 1

1 1 0 1 →

clk	input	Q_0	Q_1	Q_2	Q_3
1	1	×	×	×	×
0	0	1	×	×	×
1	1	0	1	×	×
1	1	1	0	1	×
		1	1	0	1

4-bit shift register (Serial-in)



Serial-in/ parallel-out shift register waveforms

with n-bit shift register

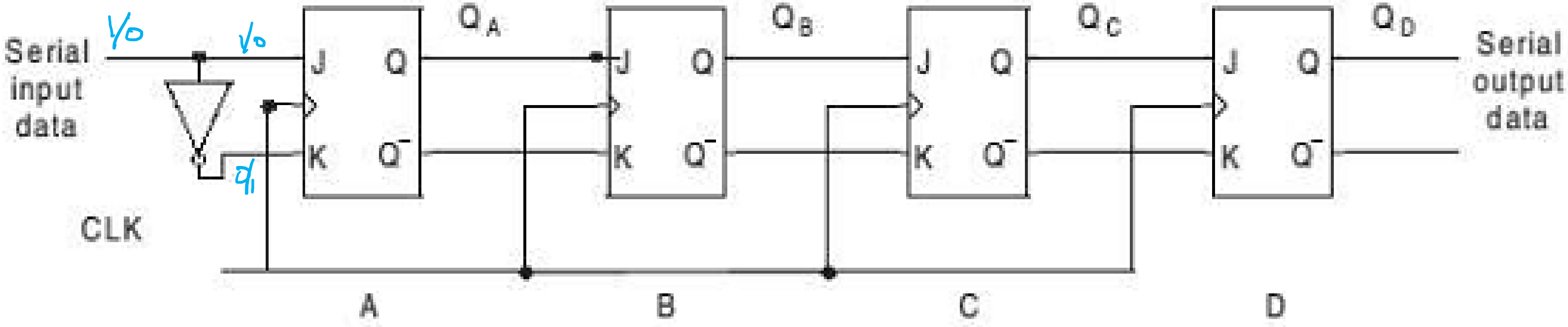
→ parallel

2n-clk

→ n-bit serial clk

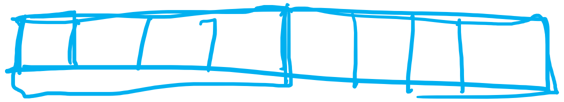
Serial output

SISO and SIPO Register using JK ffs



□ 1/0

memory units



n-bit data

→ shift-Right-2

Shift-Left by 1 bit

1 0 1 1 →

shift Right LSB first then MSB

shift Left MSB first

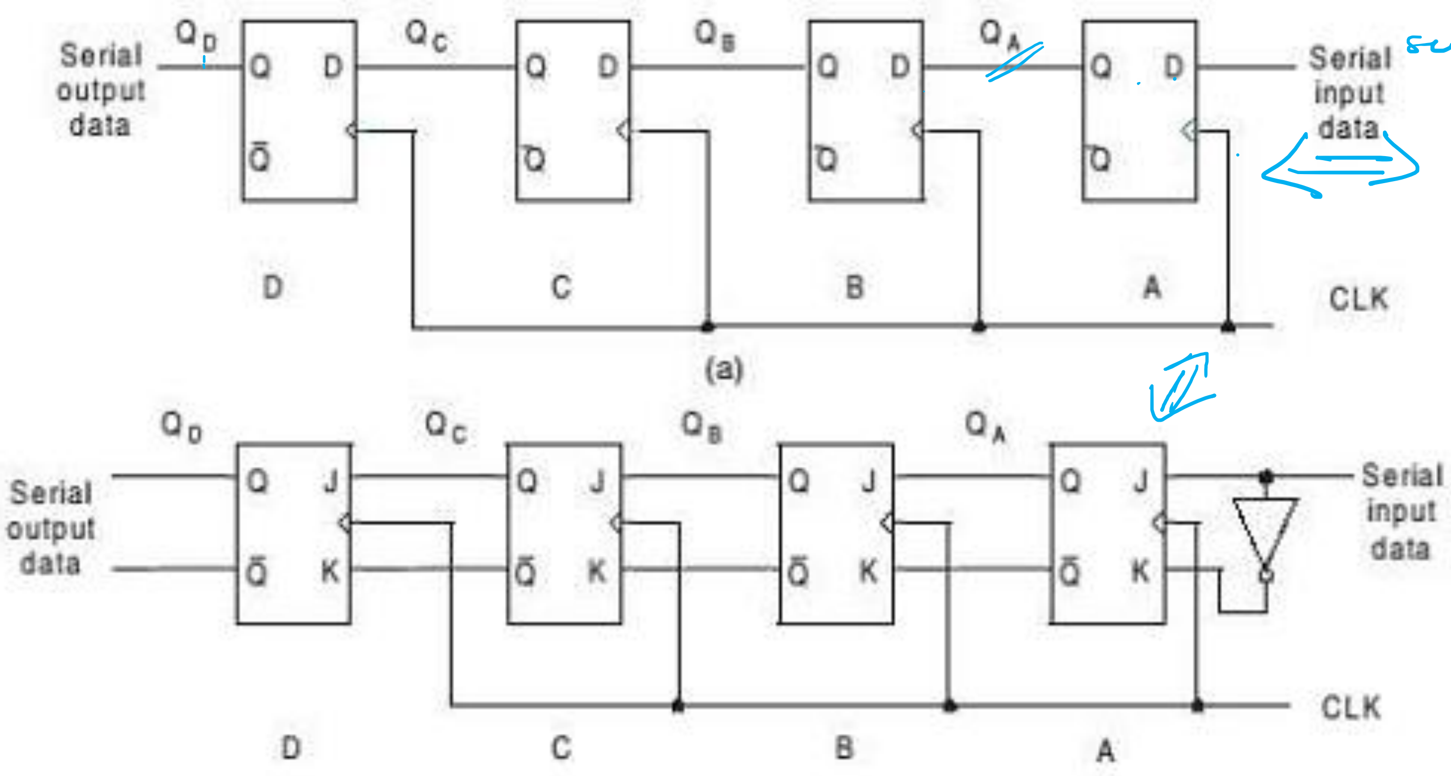
SISO and SIPO register with shift left

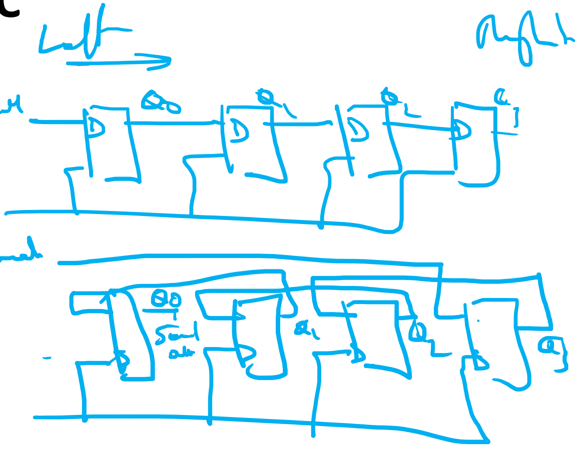
MSB 1 0 1 1 LSB

Right ~~Shift~~ shift

Ex 1 0 1 1

shift	Q_D	Q_C	Q_B	Q_A
1st				1
2nd			1	0
3rd		1	0	1
4th	1	0	1	1
5	0	1	1	X
6	1	1	X	X
7	1	X	X	X





Q_0 Q_1 Q_2 Q_3

shift Right 1 → 1

shift Left

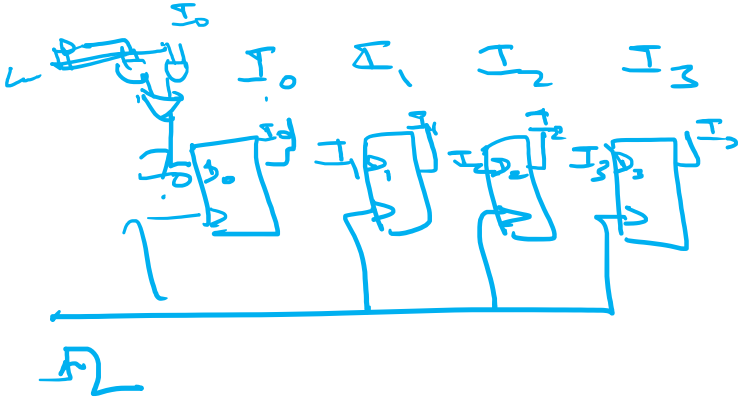
1 1 1

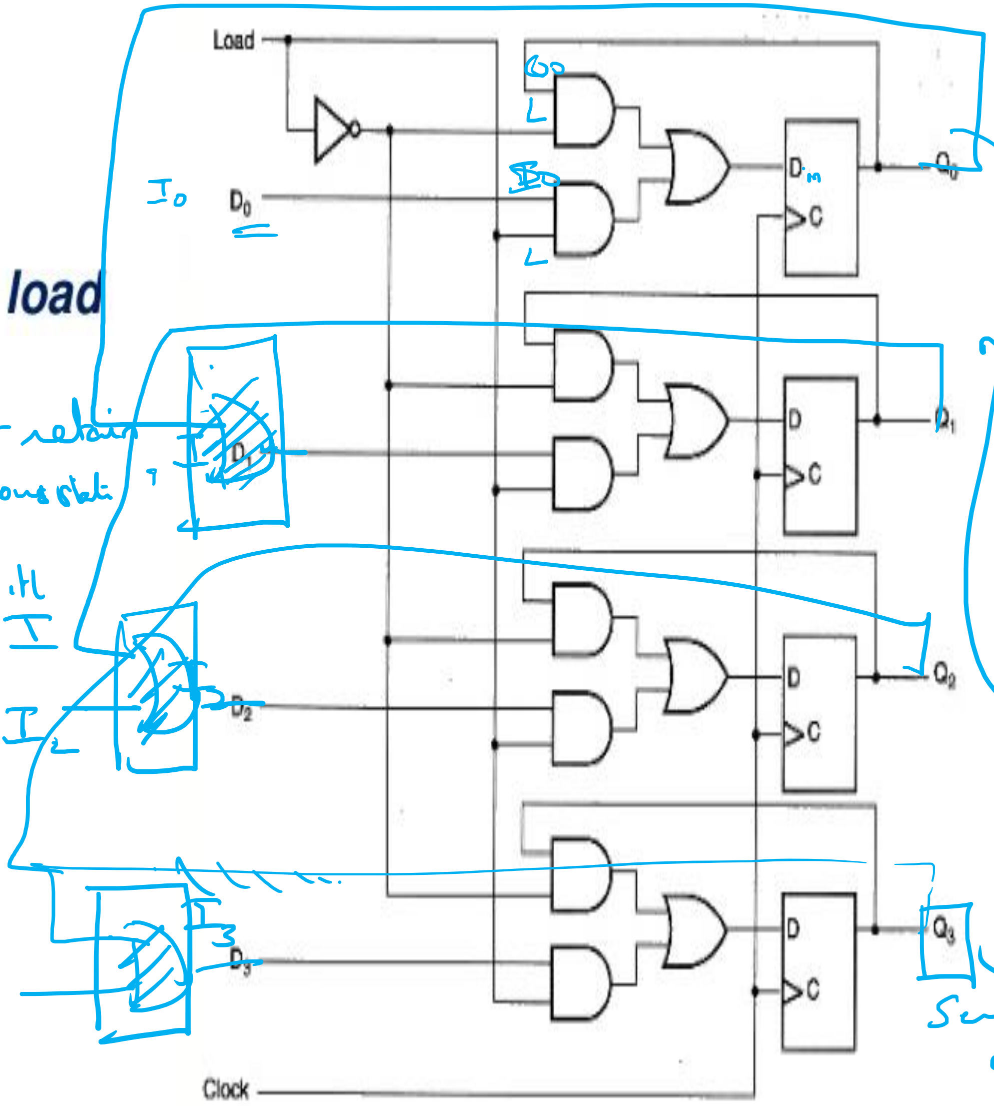
Register with parallel load (PISO or PIPO)

4- bit register with parallel load

If Load = 0 No loading ff's must retain previous state

If Load = 1 ff's should be loaded with input data I





$D_{in} = Q_0 \overline{Load} + I_0 \, Load$

Load = 0

$D_{in} = Q_0 \cdot 1 + I_0 \cdot 0$

$D_{in} = Q_0$

Next clock pulse Returns $Q_0 = Q_0$

Load = 1

$D_{in} = Q_0 \cdot 0 + I_0 \cdot 1$

$D_{in} = I_0$

Next clock pulse $Q_0 = I_0$

parallel out

4-bit bidirectional shift register using D/SR/JK ffs

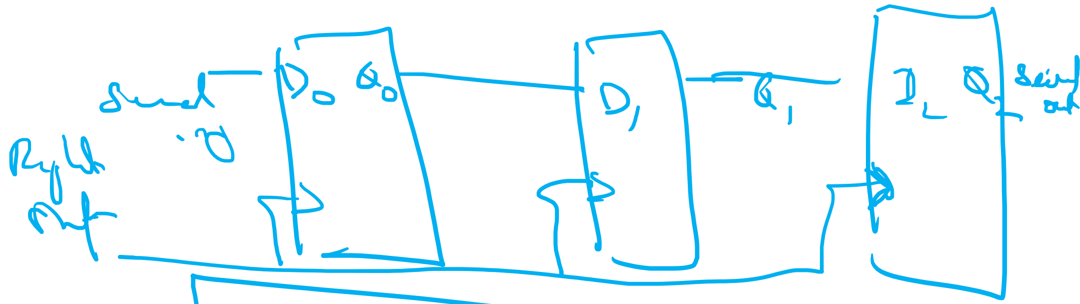
- If shift left/right =0, shift right else shift left…

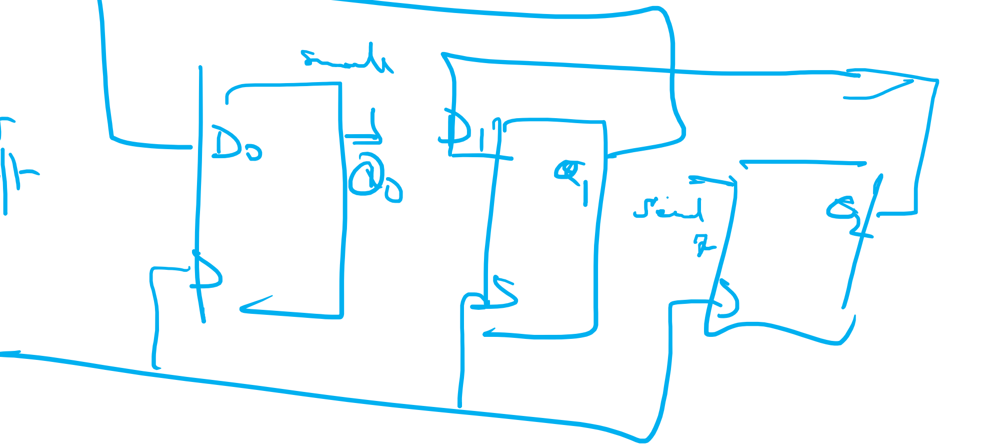
left/$\overline{\text{right}}$

0 → right shift

1 → left shift

- **Solve it by yourself…**



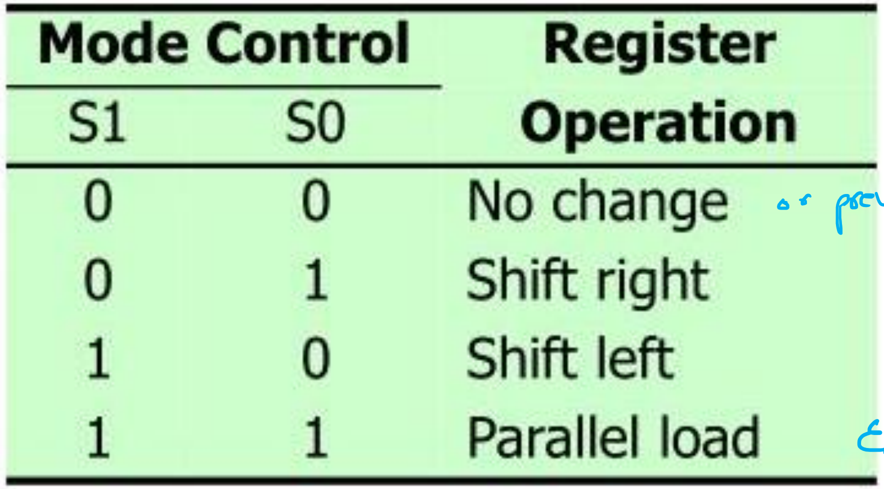


left/$\overline{\text{right}}$

left/right		D_0	D_1	D_2	o/p Left shift
0	I	I_0	Q_0	Q_1	Q_2
1		Q_1	Q_2	I_0	Q_1

4-bit universal shift register

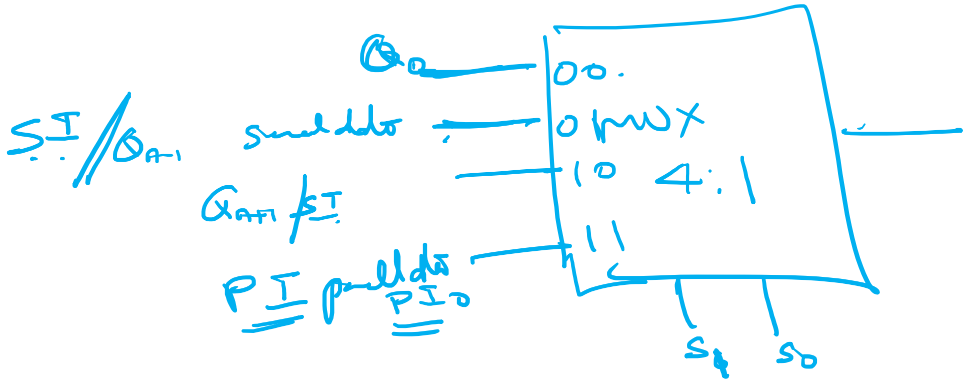
External control input



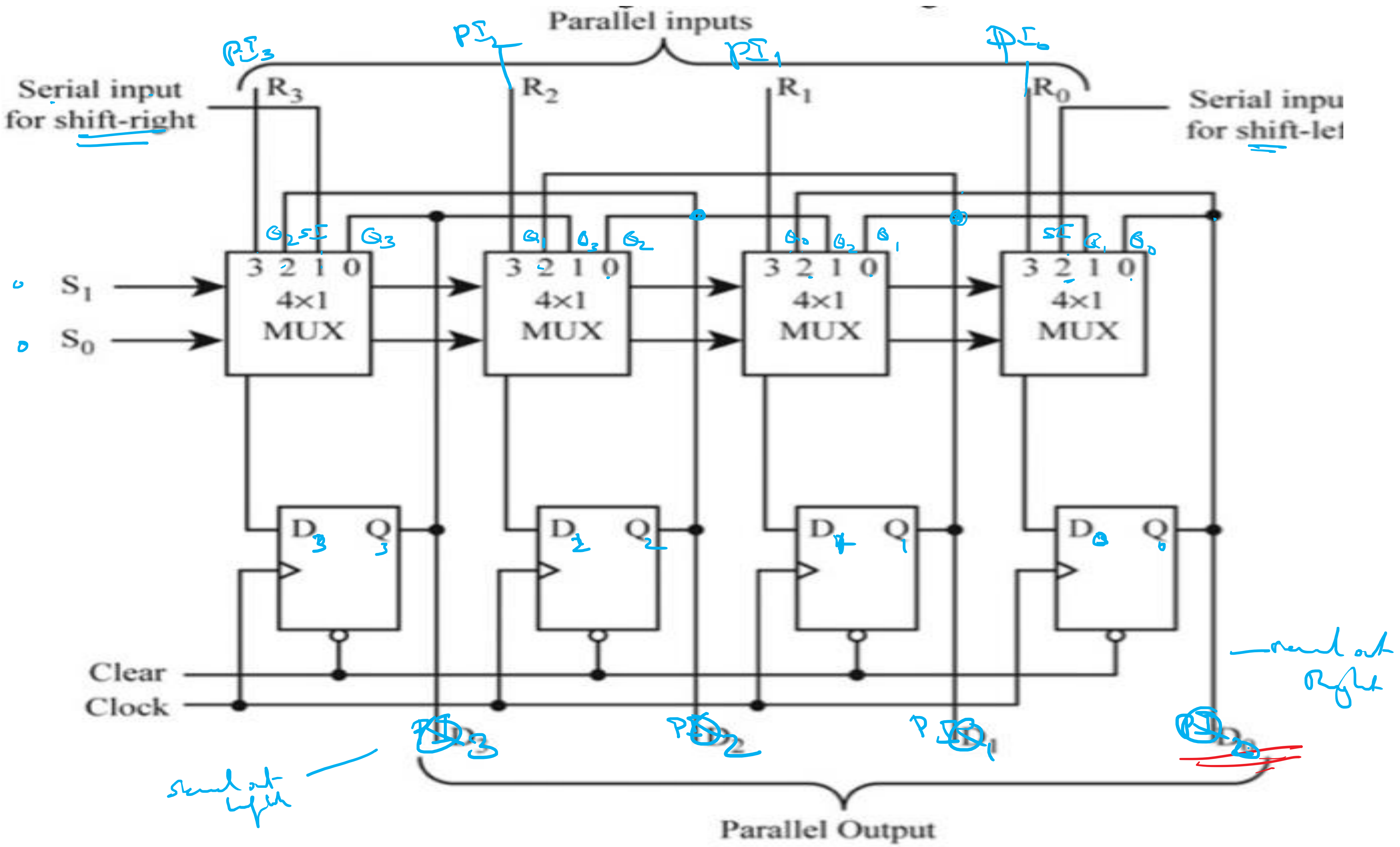
Mode Control		Register Operation
S1	S0	
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

or previous state

External parallel Data loaded onto the n-bit register

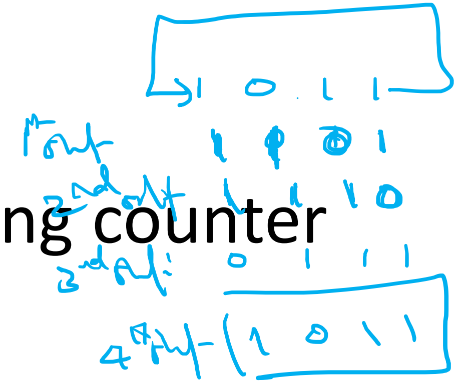


4-bit universal shift register



Shift register counters:

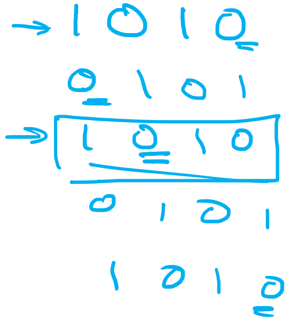
- Ring counter
- Johnson counter /Twisted-ring counter



Initial data stored in register are shifted in a circular manner

n-bit shift register will n-clock pulses original sequence/state re-appears

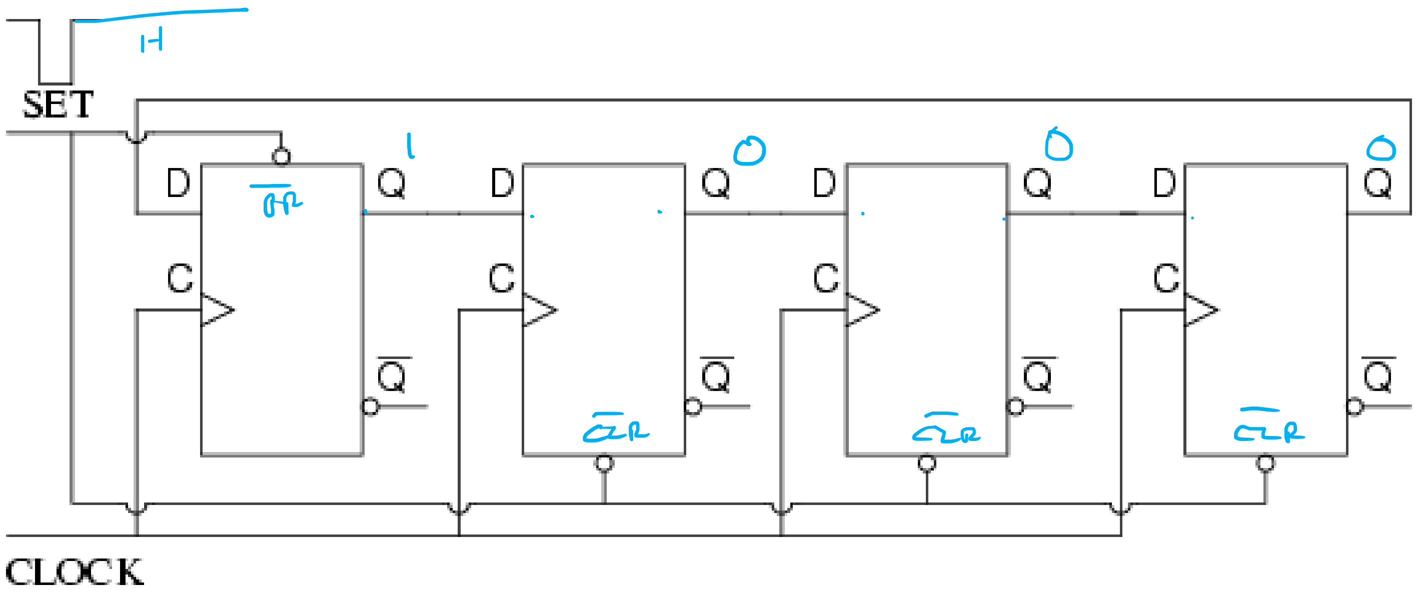
However there are riders



0000

1111

Ring counter



Set one stage, clear three stages

Clock Cycle	Q_1	Q_2	Q_3	Q_4
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	1	0	0	0
6	0	1	0	0
.	.	.	.	.
.	.	.	.	.

Bit-pattern repeats for every 4 clock cycles

1 0 0 0
0 1 0 0
0 0 1 0
0 0 0 1

Not to uses

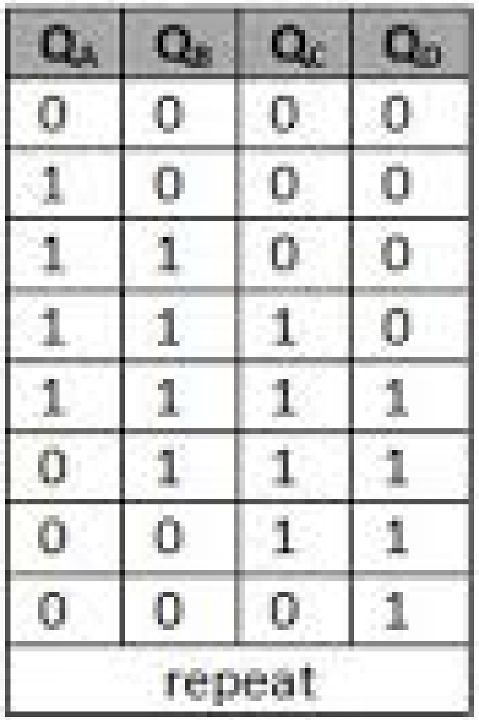
0000

1111

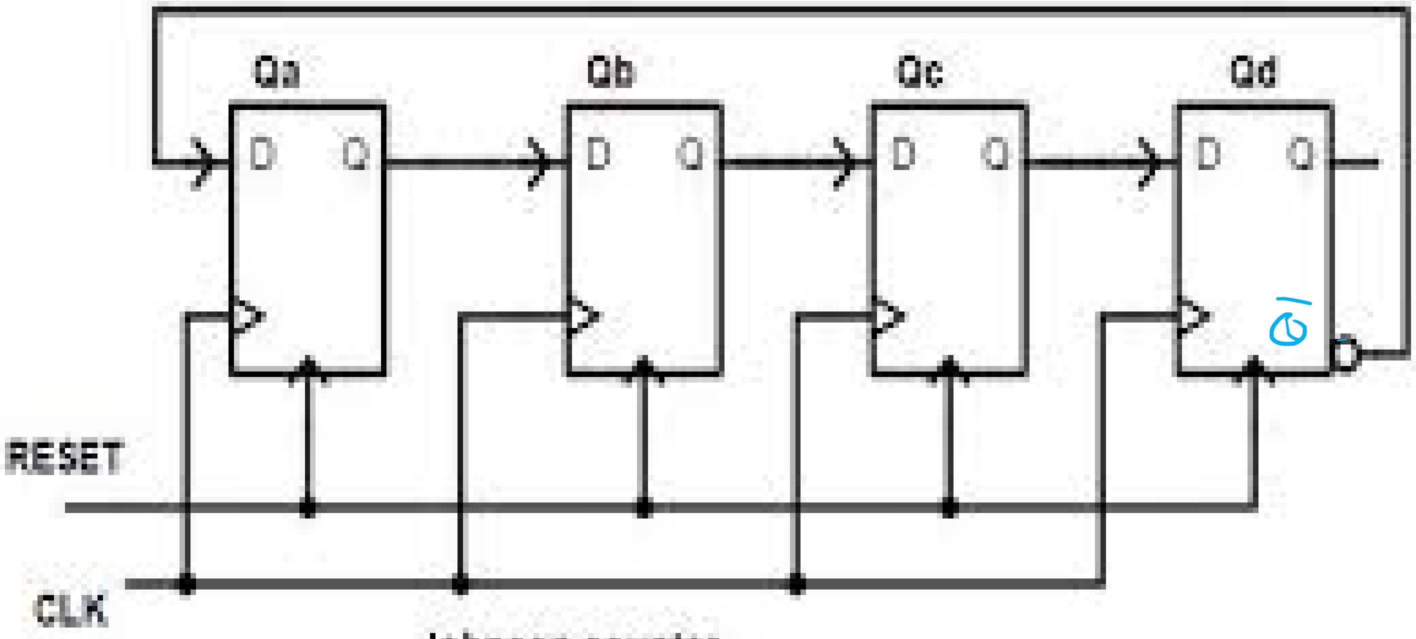
1010

0101

Johnson counter /Twisted-ring counter



Q_A	Q_B	Q_C	Q_D
0	0	0	0
1	0	0	0
1	1	0	0
1	1	1	0
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1
repeat			



Johnson counter

0 0 0 0
1 0 0 0
1 1 0 0
1 1 1 0
1 1 1 1
0 1 1 1
0 0 1 1
0 0 0 1
0 0 0 0

2n clock pulses

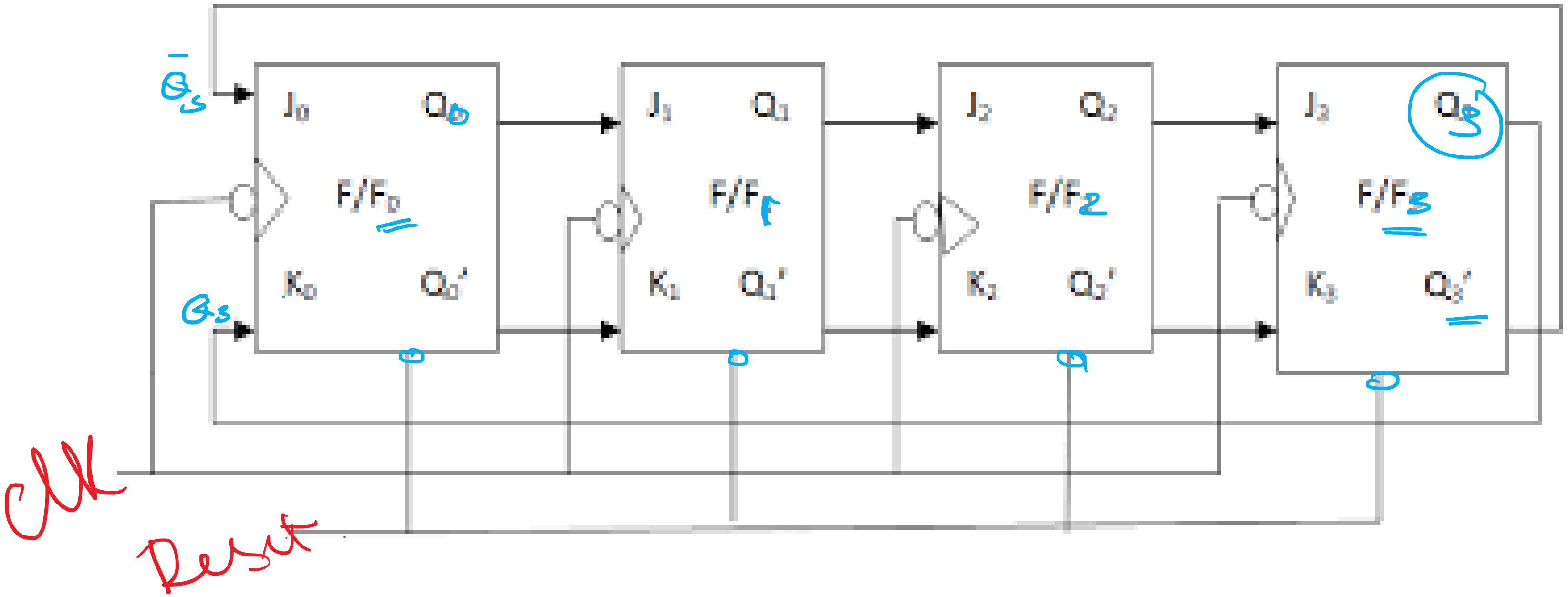
1 0 1 0.
1 1 0 1.
0 1 1 0.
1 0 1 1.
0 1 0 1.
0 0 1 0.
1 0 0 1.
0 1 0 0.
1 0 1 0

2n clock

Johnson counter /Twisted-ring counter using JK ffs

0 0 0 0

2n



$\bar{Q}_3$
J0
Q0
F/F0
K0
Q0'
Q_3
J1
Q1
F/F1
K1
Q1'
J2
Q2
F/F2
K2
Q2'
J3
Q3
F/F3
K3
Q3'
0
0
0
0
Clk
Reset