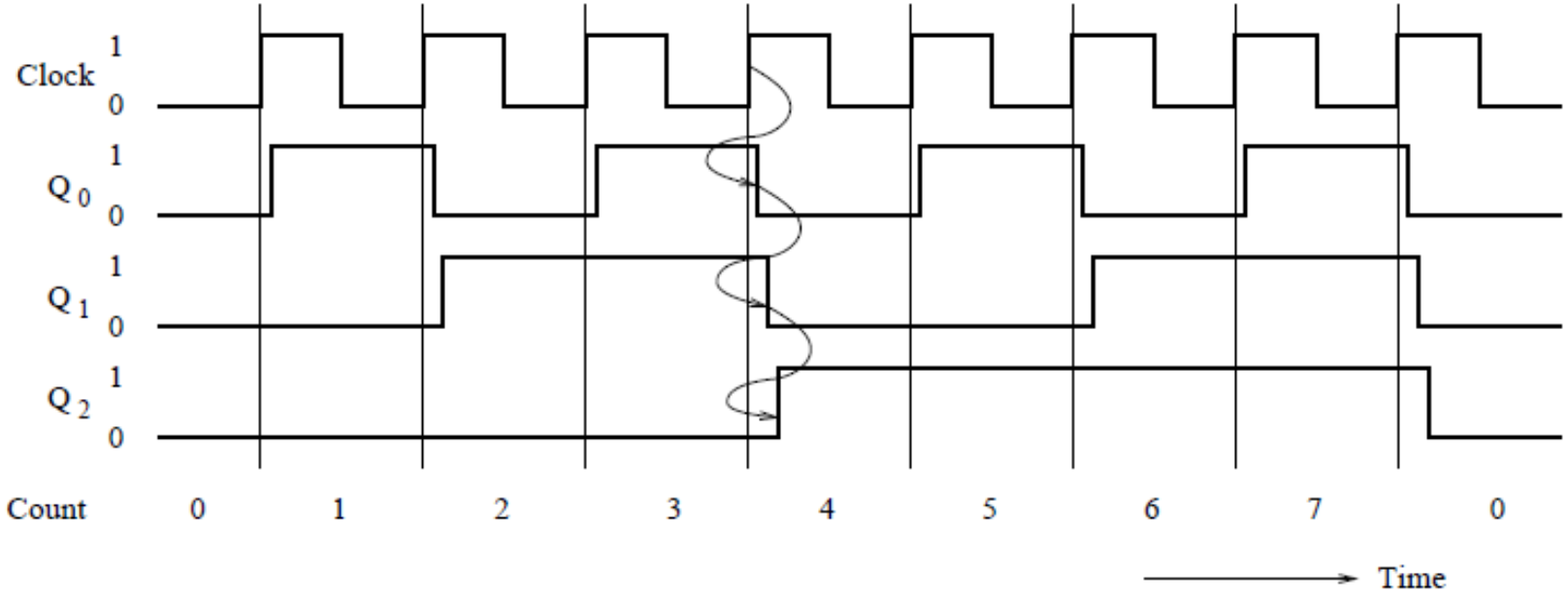
Synchronous counters

- Limitations of asynchronous counters
- Synchronous counter design
- Synchronous counter ICs

Limitation of asynchronous counters



Limitations: 1. Not suitable for high frequency applications

2. Not suitable for higher mod counters

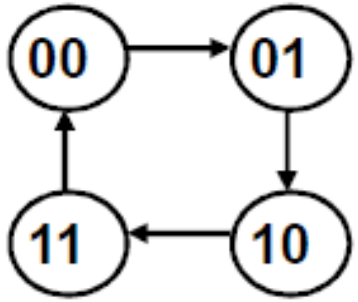
Synchronous counter design

- All the flip flops are clocked simultaneously using same clock.
- Suitable for high frequency applications
- Designed using sequential circuit design process which can be used for any synchronous circuit designs

1. Design 2-bit synchronous binary UP counter using T ffs

- Counter states: 00 → 01 →10 →11

State diagram



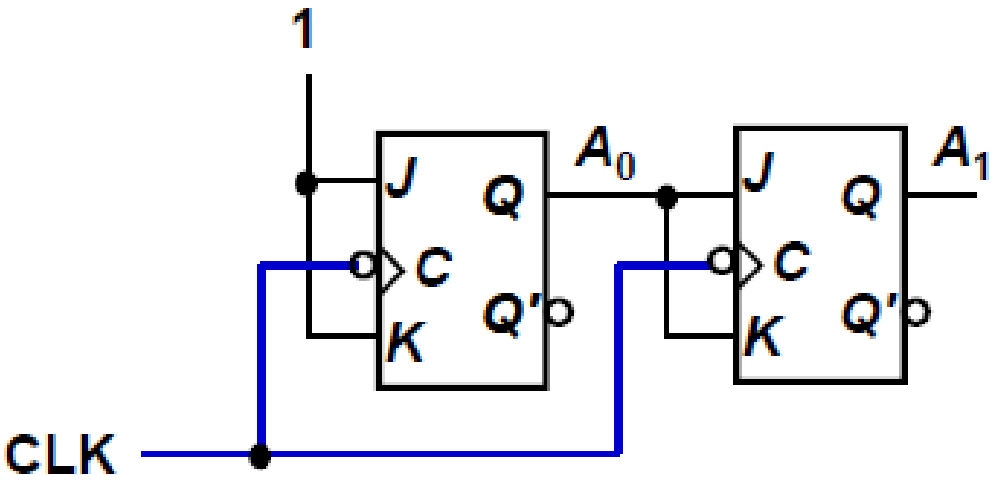
State table

Present state		Next state		Flip-flop inputs	
A_1	A_0	A_1^+	A_0^+	TA_1	TA_0
0	0	0	1	0	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	0	0	1	1

$TA_1 = A_0$

$TA_0 = 1$

2-bit synchronous binary UP counter using JK ffs : circuit diagram



2. Design 2-bit synchronous binary UP counter using JK ffs

2-bit synchronous binary UP counter using JK ffs contd..

3. Design 3-bit synchronous binary UP counter (MOD 8)using SR ffs

3-bit synchronous binary UP counter (MOD 8)using SR ffs

4. Draw the circuit of 3-bit synchronous binary up counter (MOD 8) using T ffs

- Analyse the previous examples and draw the circuit directly without the design steps.

5. Design 2-bit synchronous binary down counter (MOD 4) using D ffs

2-bit synchronous binary down counter (MOD 4) using D ffs

6. Design 3-bit synchronous binary down counter (MOD 4) using D ffs

7. Design decade (BCD) synchronous up counter (MOD 10)using T ffs

- (0→1→2→3→4→5→6→7→8→9→0)

Decade (BCD) synchronous up counter contd..

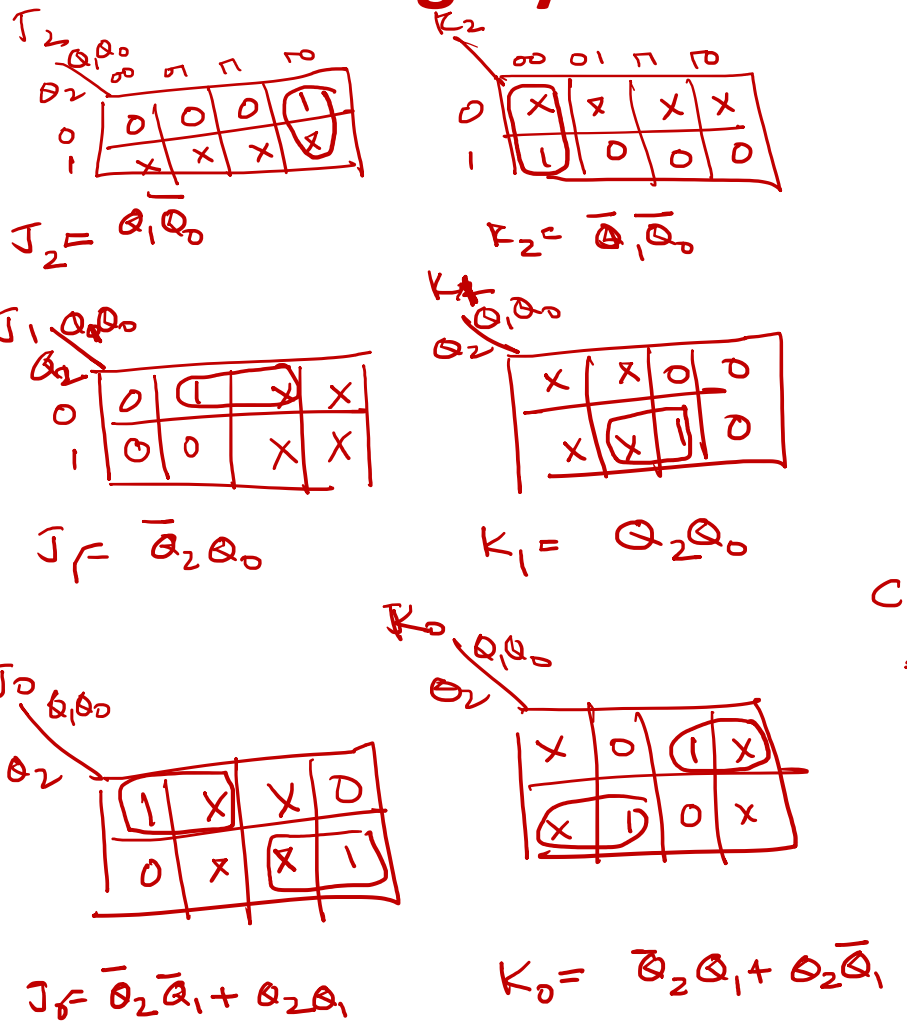
Synchronous counters

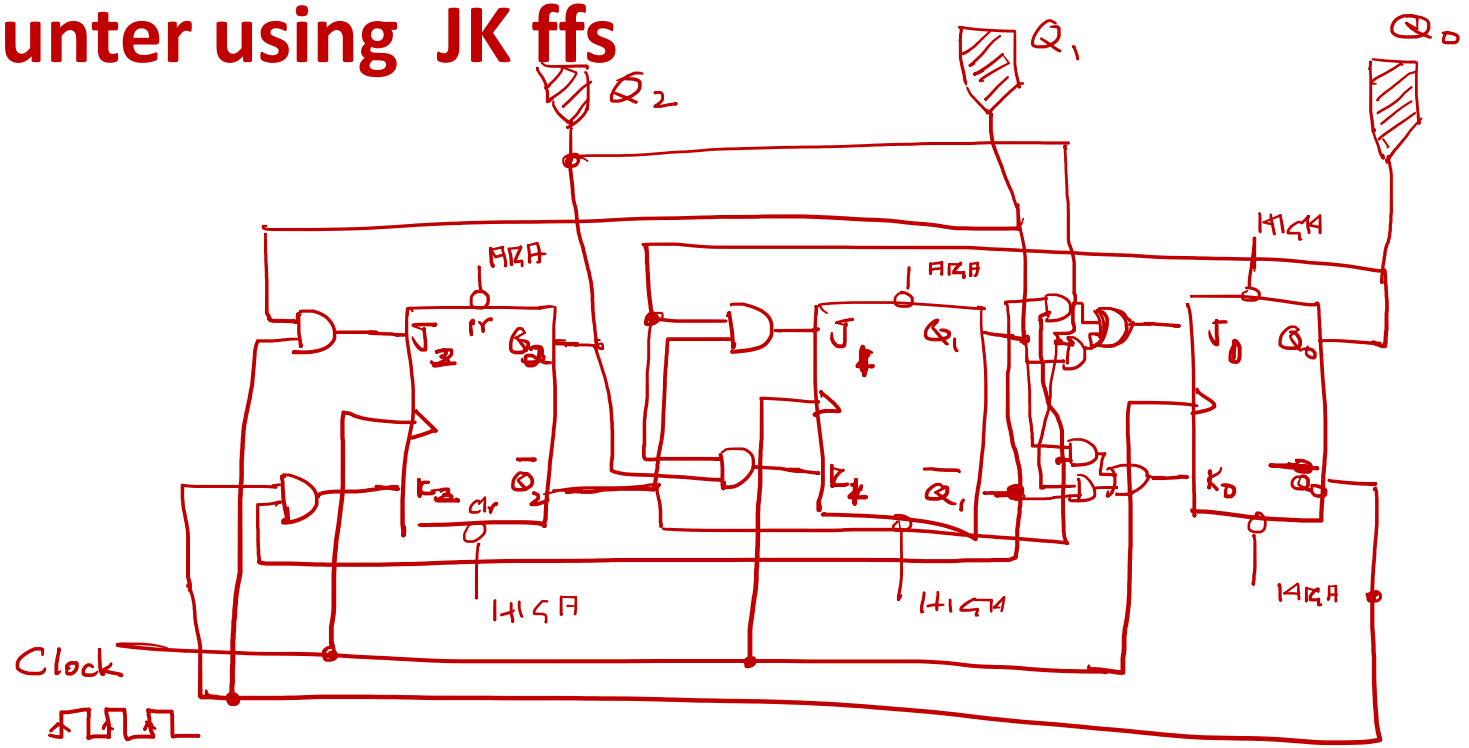
- Limitations of asynchronous counters
- Synchronous counter design
- Synchronous counter ICs

Synchronous counter design

- All the flip flops are clocked simultaneously using same clock.
- Suitable for high frequency applications
- Designed using sequential circuit design process which can be used for any synchronous circuit designs

3-bit gray code counter using JK ffs





Tutorial or Work-out question for you

Design 3-bit Gray code down counter using -ve edge triggered JK flip flop

8. Design 3-bit gray code counter using JK ffs

Next State table

Decimal Number	3-bit Binary	3-bit Gray Code
0	000	000
1	001	001
2	010	011
3	011	010
4	100	110
5	101	111
6	110	101
7	111	100
8		
9		

cannot be represented using only 3 bits

Binary → Gray

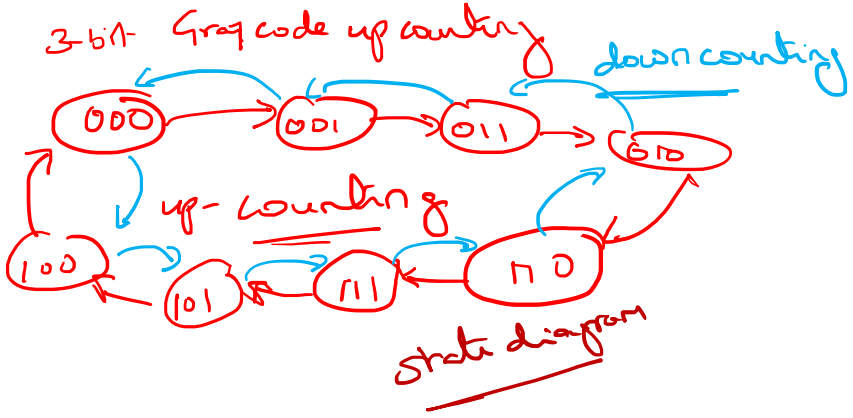
first bit → first bit

second bit → second bit

third bit → third bit

1. up counting
2. down counting

3 bit → 3 JK flipflops



	present state $Q_2 Q_1 Q_0$	Next state $Q_2 Q_1 Q_0$	MSB $J_2 K_2$	$J_1 K_1$	LSB $J_0 K_0$
m_0	0 0 0	0 0 1	0 X	0 X	1 X
m_1	0 0 1	0 1 1	0 X	1 X	X 0
m_3	0 1 1	0 1 0	0 X	X 0	X 1
m_2	0 1 0	1 1 0	1 X	X 0	0 X
m_6	1 1 0	1 1 1	X 0	X 0	1 X
m_7	1 1 1	1 0 1	X 0	X 1	X 0
m_5	1 0 1	1 0 0	X 0	0 X	X 1
m_4	1 0 0	0 0 0	X 1	0 X	0 X

Pr	Next	J	K	
0	0	0	X	
0	1	1	X	Set / Toggle
1	0	X	1	Reset / Toggle
1	1	X	0	no change / Set

from function table of JK

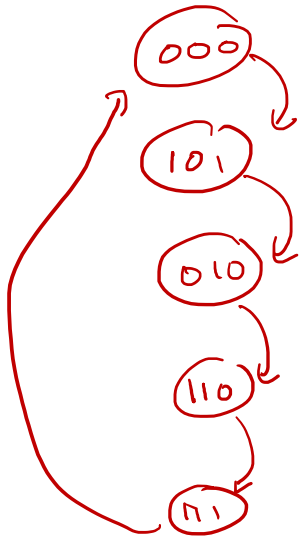
present state	Next state	$J_2 K_2$	$J_1 K_1$	$J_0 K_0$
m_0 000	001	0 X	0 X	1 X
m_1 001	011	0 X	1 X	X 0
m_2 010	110	1 X	X 0	0 X
m_3 011	010	0 X	X 0	X 1
m_4 100	000	X 1	0 X	0 X
m_5 101	100	X 0	0 X	X 1
m_6 110	111	X 0	X 0	1 X
m_7 111	101	X 0	X 1	X 0

Design 3-bit synchronous counter to count according to the given sequence using D ffs.

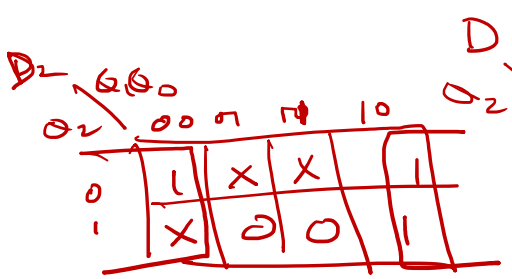
used states & counting

- 0→5→2→6→7→0

unused states states: 1, 3, 4,



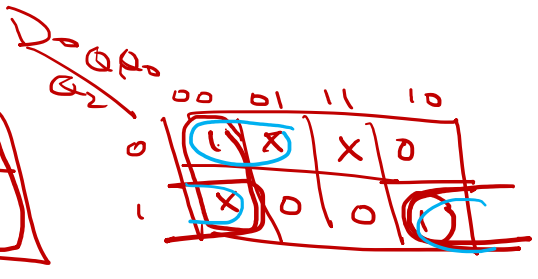
	PS $Q_2Q_1Q_0$	NS $Q_2Q_1Q_0$	D_2	D_1	D_0
m_0	0 0 0	1 0 1	1	0	1
m_1	0 0 1	X X X	X	X	X
m_2	0 1 0	1 1 0	1	1	0
m_3	0 1 1	X X X	X	X	X
m_4	1 0 0	X X X	X	X	X
m_5	1 0 1	0 1 0	0	1	0
m_6	1 1 0	1 1 1	1	1	1
m_7	1 1 1	0 0 0	0	0	0



$D_2 = \bar{Q}_0$

$D_1 = Q_1\bar{Q}_0 + \bar{Q}_1Q_0$

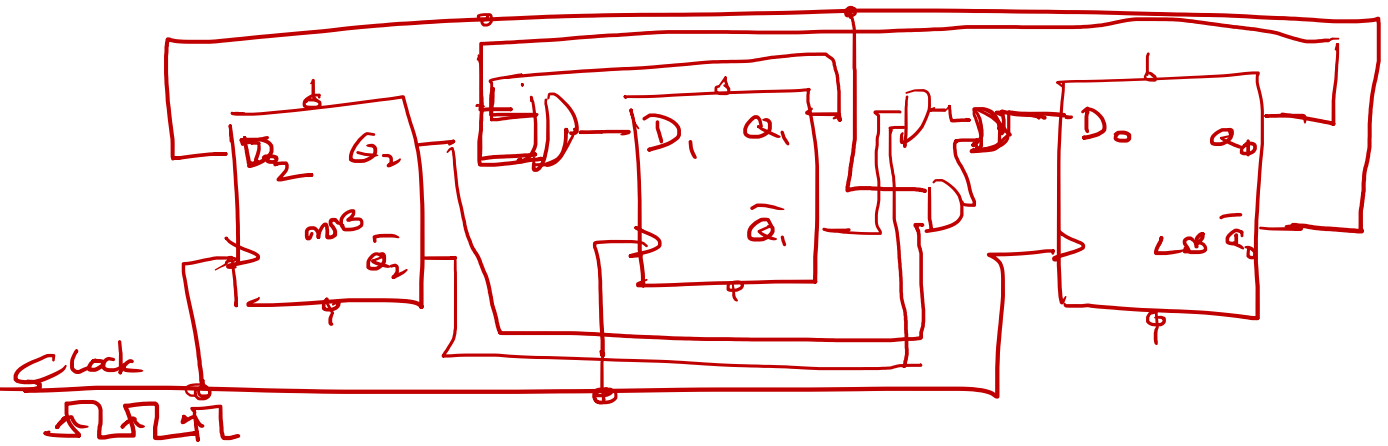
$D_1 = Q_1 \oplus Q_0$



$D_0 = \bar{Q}_1\bar{Q}_0 + Q_2\bar{Q}_0$

or

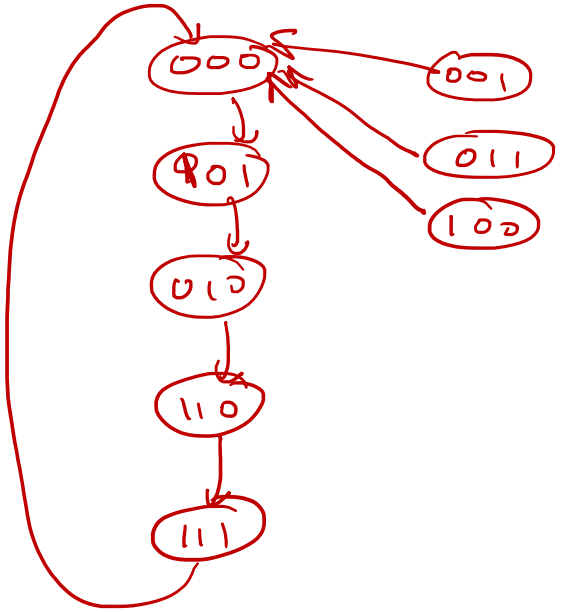
$D_0 = \bar{Q}_2\bar{Q}_1 + Q_2\bar{Q}_0$



Eg:

Design 3-bit synchronous counter to count according to the given sequence using D ffs. All the undefined states should go to state 0.---Self correcting counters.

- 0→5→2→6→7→0



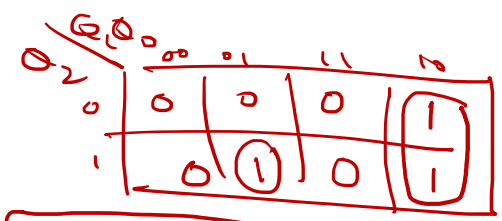
P.S $Q_2Q_1Q_0$	N.S $Q_2Q_1Q_0$
000	101
001	000
010	110
011	000
100	000
101	010
110	111
111	000

Same as above

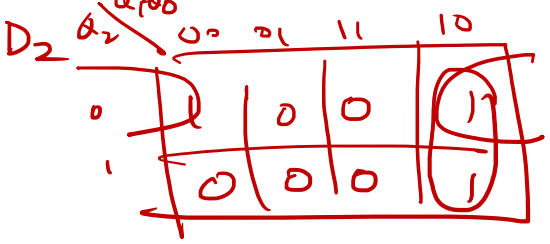
D_2	D_1	D_0
1	0	1
0	0	0
0	1	0
1	1	0
0	0	0
0	0	0
0	1	0
0	1	0
0	0	0

$D_0 = \bar{Q}_2\bar{Q}_1\bar{Q}_0$

$D_1 = m_2 + m_5 + m_6$



$D_1 = Q_1\bar{Q}_0 + Q_2\bar{Q}_1Q_0$



$D_2 = Q_1\bar{Q}_0 + \bar{Q}_2\bar{Q}_0$

please Draw the circuit

$$D_0 = \bar{Q}_2 \bar{Q}_1 \bar{Q}_0$$

$$D_1 = Q_1 \bar{Q}_0 + Q_2 \bar{Q}_1 Q_0$$

$$D_2 = Q_1 \bar{Q}_0 + \bar{Q}_2 \bar{Q}_0$$

Design 3-bit synchronous counter to count according to the given sequence using D ffs. All the undefined states should go to next valid/defined state.

- 0→5→2→6→7→0

Next Valid code

Next Valid code for unused code

001 → 010
011 → 101
100 → 101

Assuming we are going upwards

Downwards
000
010
010

Active High Asynchronous input

What is Defined state Ex. all unused codes go to Valid code say 110

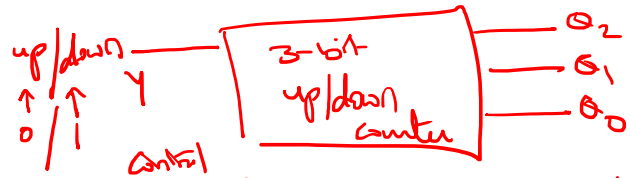
001 → 110
011 → 110
100 → 110

9. Design a 3-bit up/down synchronous binary counter using T ffs

Active low / Active High

up down
0 / 1

- If control input up/down = 0, counter should count upwards from the present count or else it has to count downwards from the present count.



control
external I/p

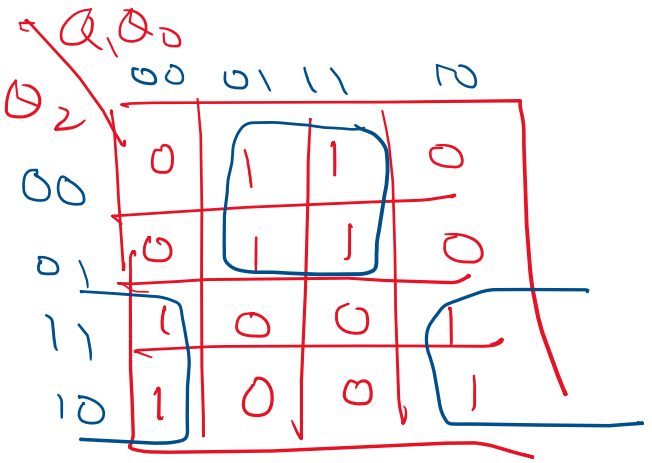
3-bit counting

	PS			NS					
	Y	Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	T_2	T_1	T_0
up	0	0	0	0	0	0	1	0	0	1
	0	0	0	1	0	1	0	0	1	1
	0	0	1	0	0	1	1	0	0	1
	0	0	1	1	1	0	0	1	1	1
	0	1	0	0	1	0	1	0	0	1
	0	1	0	1	1	1	0	0	1	1
	0	1	1	0	1	1	1	0	0	1
	0	1	1	1	0	0	0	1	1	1
down	1	0	0	0	1	1	1	0	0	1
	1	0	0	1	0	0	0	0	1	1
	1	0	1	0	0	0	1	0	0	1
	1	0	1	1	0	1	0	0	1	1
	1	1	0	0	0	1	1	0	0	1
	1	1	0	1	1	0	0	1	1	1
	1	1	1	0	1	0	1	0	0	1
	1	1	1	1	1	1	0	0	1	1

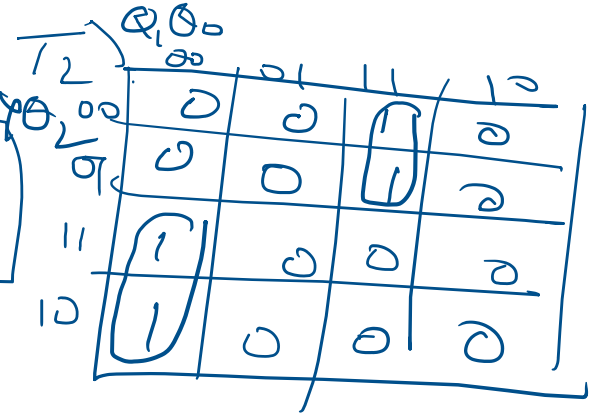
$T_0 = 1$

$T_1 = \bar{Y}Q_0 + Y\bar{Q}_0$

$T_1 = Y \oplus Q_0$



$T_2 = \bar{Y}Q_1Q_0 + Y\bar{Q}_1\bar{Q}_0$



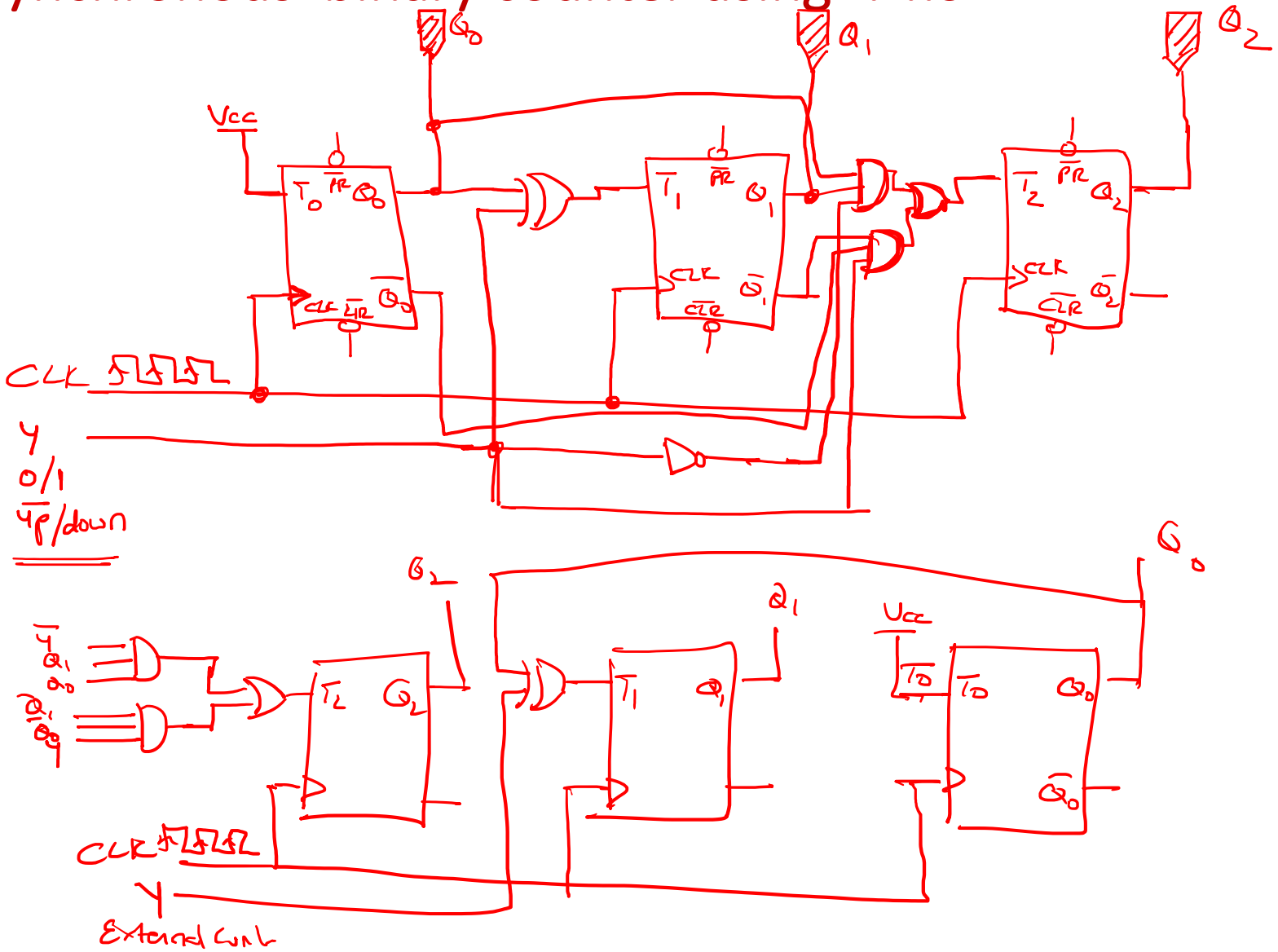
3-bit up/down synchronous binary counter using T ffs

$T_0 = 1$

$T_1 = \bar{Y}Q_0 + Y\bar{Q}_0$

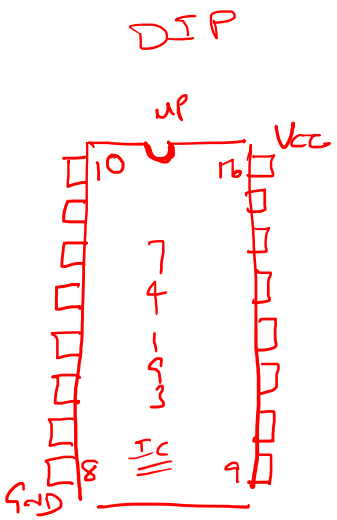
$= Y \oplus Q_0$

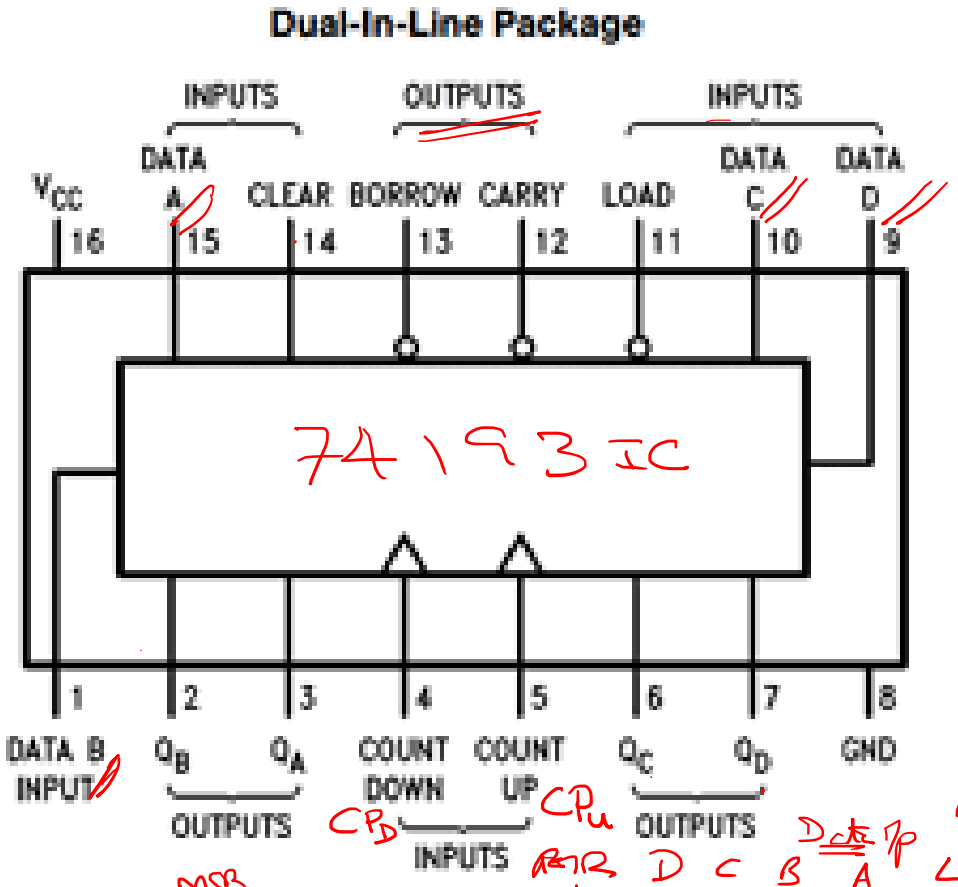
$T_2 = \bar{Y}Q_1Q_0 + Y\bar{Q}_1\bar{Q}_0$



74193 IC: 4-bit up/down synchronous counter

MOD-16 counter 0000 to 1111





Q_D is the MSB and Q_A is the LSB

Count up/CPu: count up clock input

Count down/CP_D: count down clock input

LOAD: Asynchronous parallel load (active low)

CLEAR: Asynchronous master reset input (active High) MR

CARRY: Terminal count up output TCu

Borrow: Terminal count down output TCD

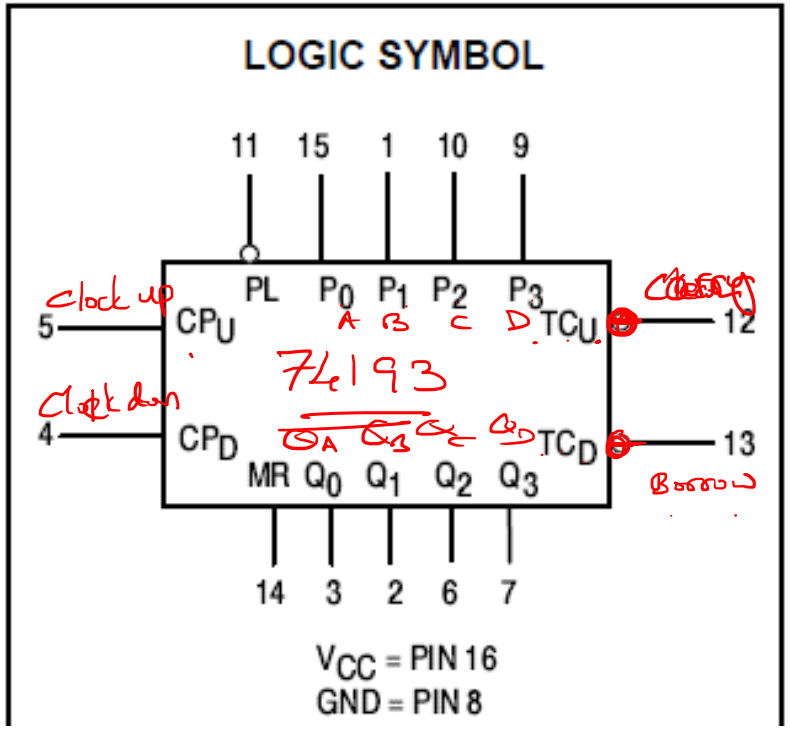
Data inputs: Parallel data inputs LSB A B C D MSB

MSB $Q_D Q_C Q_B Q_A$ LSB

Data I/p Asynchronous I/p

MR	D	C	B	A	Load	Q_D Q_C Q_B Q_A
L	1	0	1	1	1	x x x x
L	1	0	1	1	0	1 0 1 1
H	x	x	x	x	x	0 0 0 0

74193 IC: 4-bit up/down synchronous counter



MODE SELECT TABLE

MR	PL	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	⌐	H	Count Up
L	H	H	⌐	Count Down

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
⌐ = LOW-to-HIGH Clock Transition

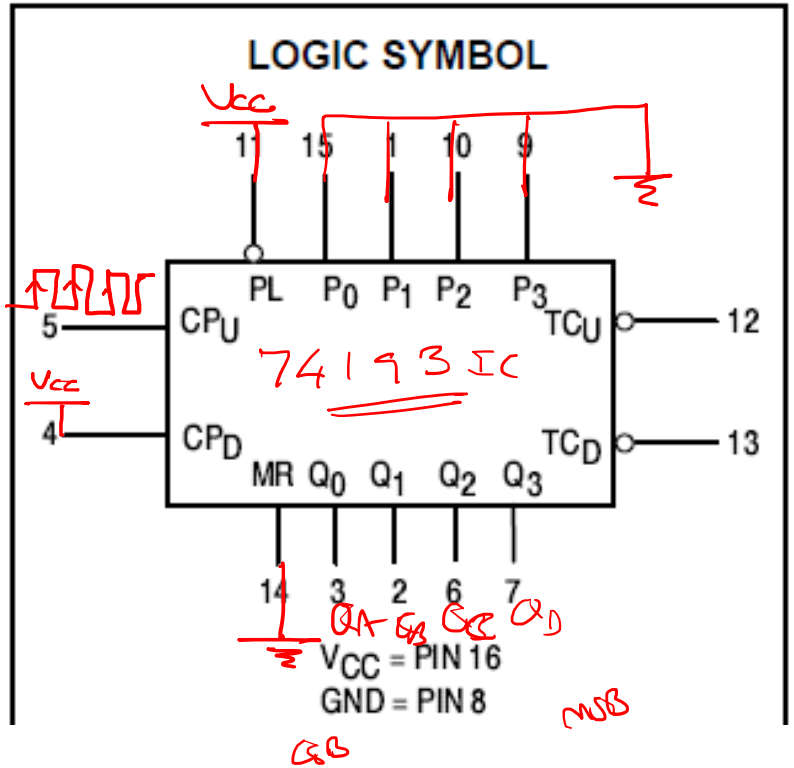
Design a MOD-16 binary UP counter using 74193 IC

4-bit binary UP

0000
0001
.
.
.
1111
0000

MR = HIGH/LOW

$\overline{PL}$ = HIGH/LOW



Design a MOD 16 binary DOWN counter using 74193 IC

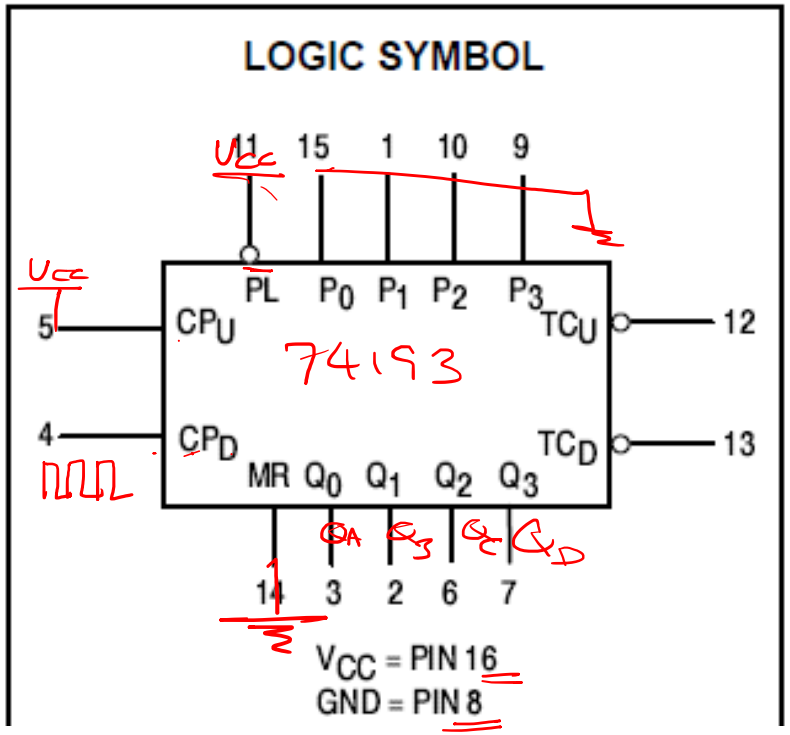
(4-bit binary down counting) Clock should be given CP_D

Please Note

A HIGH Level on MR Resets the output as $Q_D Q_C Q_B Q_A$ = 0 0 0 0

So for Normal Counting

Set MR to low

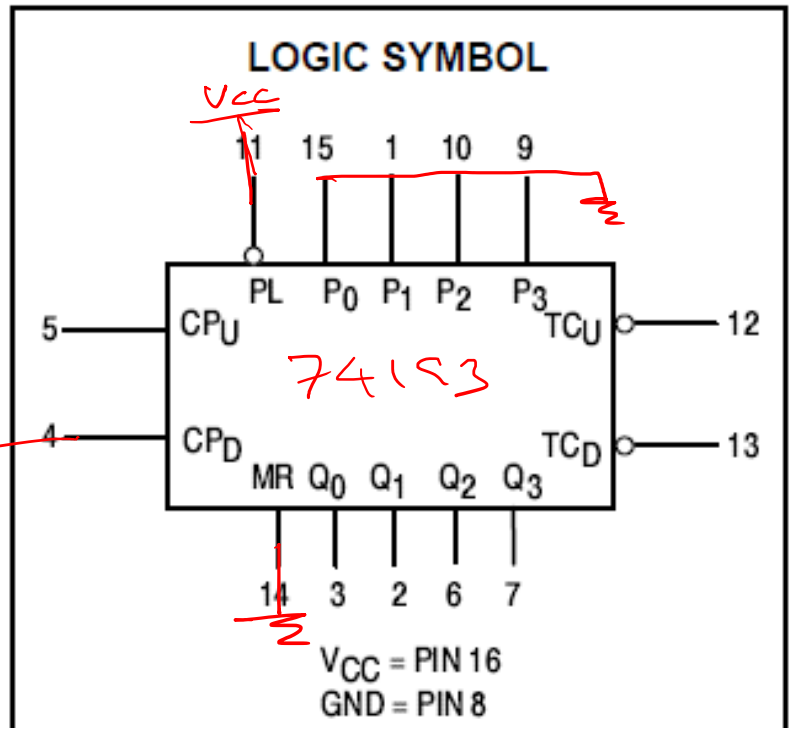


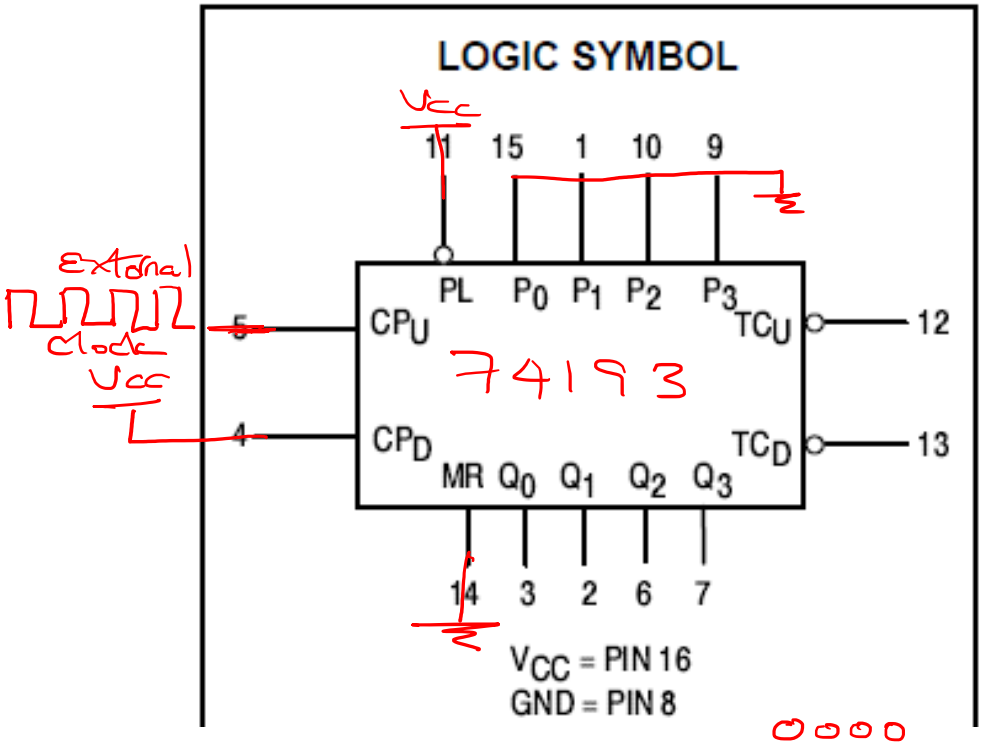
down counting: 1111 → 1110 → 1101 → ... → 0000

$\overline{PL}$ → HIGH

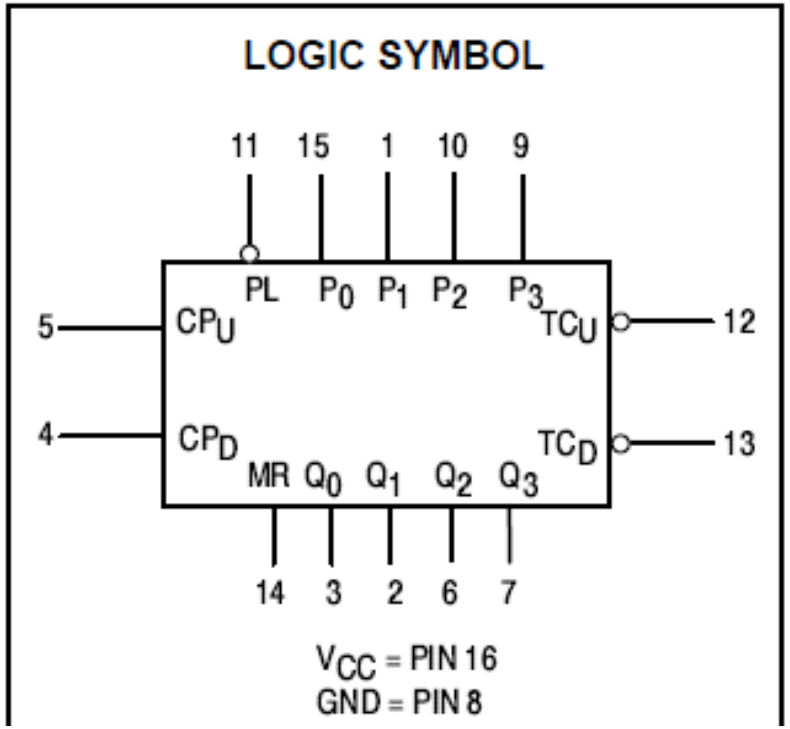
T_D

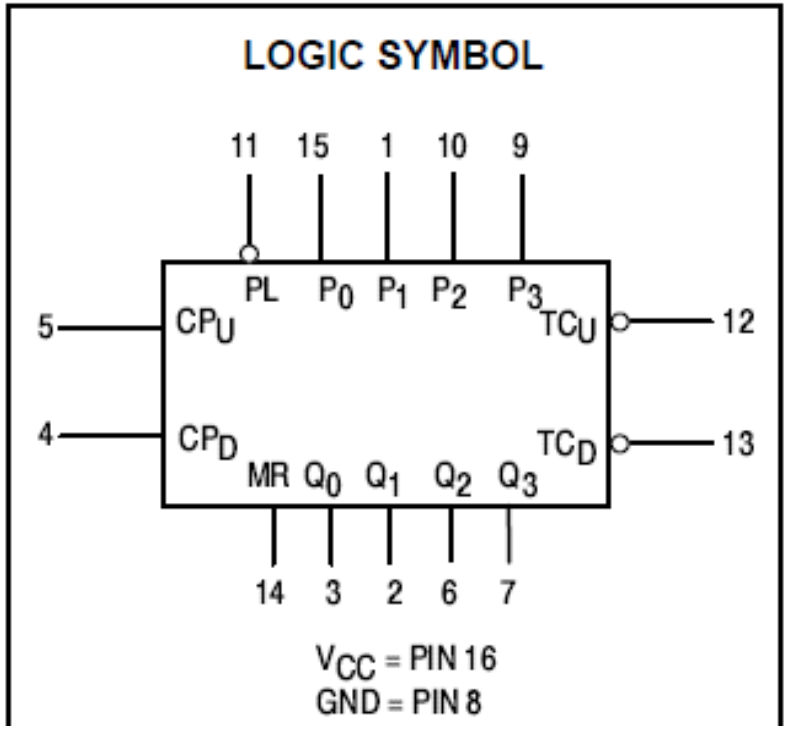
Design a 2-digit hexadecimal UP counter (00-FF H) using 74193 IC



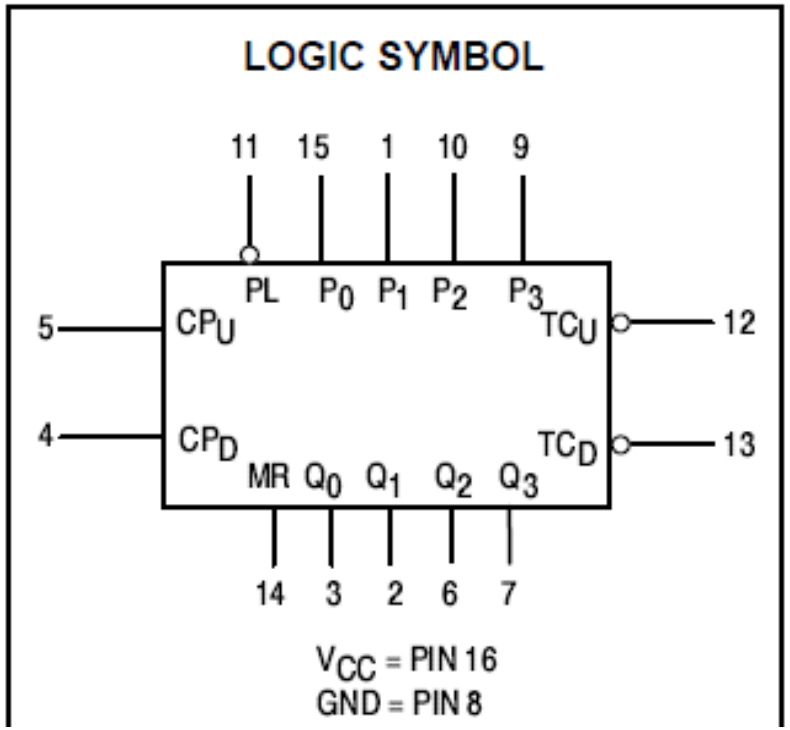


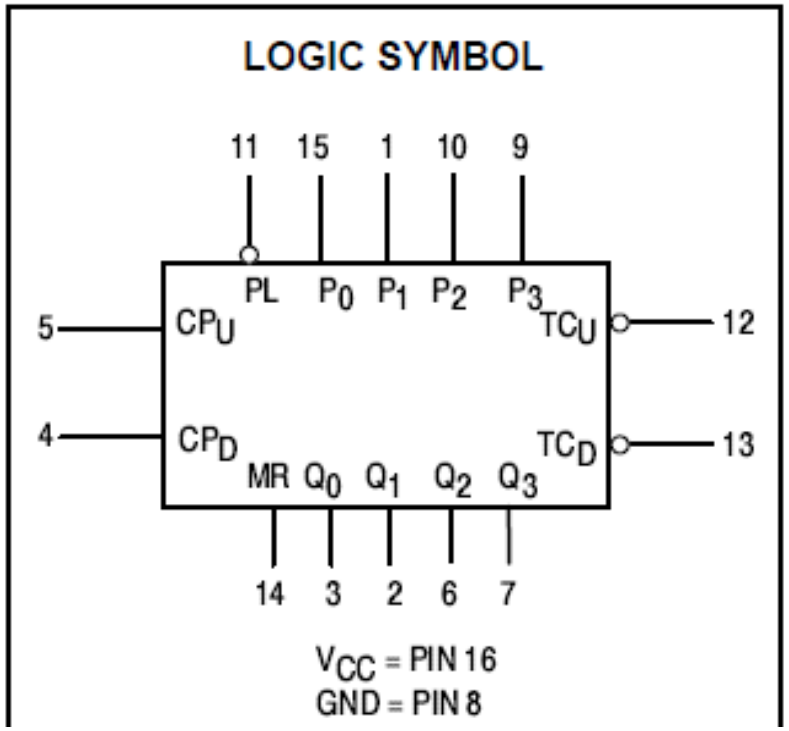
Design a 2-digit hexadecimal UP counter (00-FF H) using 74193 IC



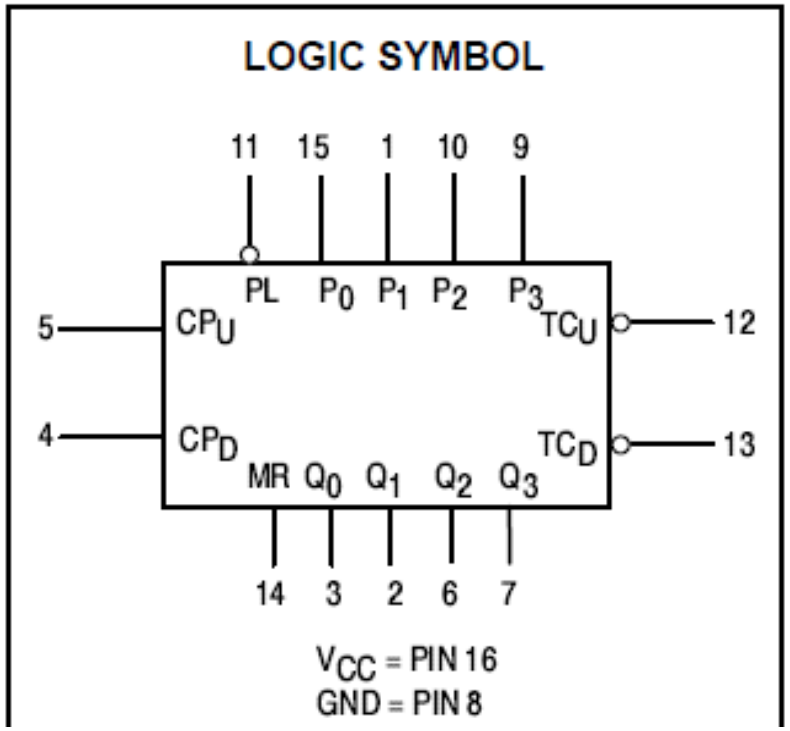


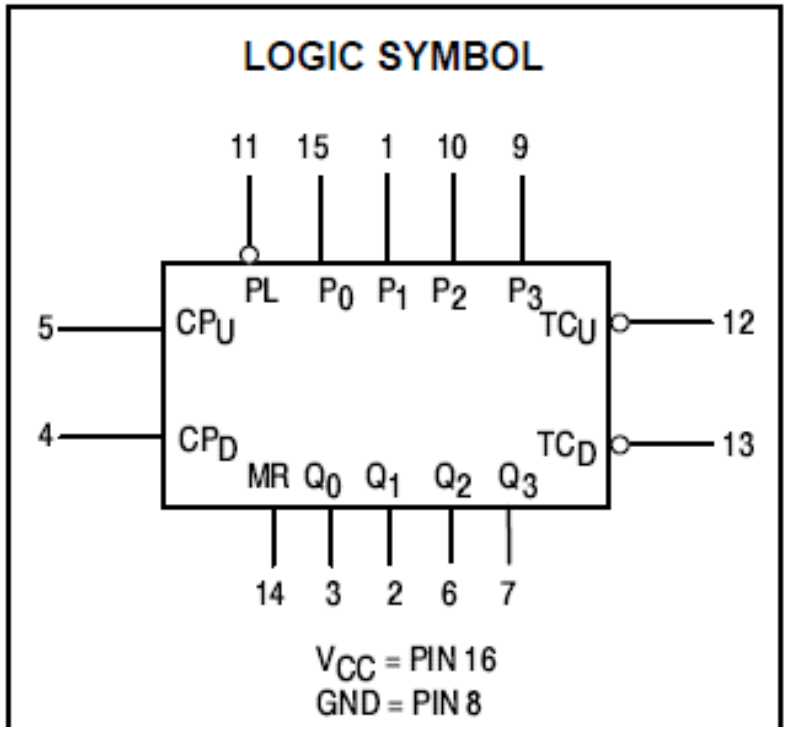
Design a 2-digit hexadecimal UP counter (18H-99 H) using 74193 IC





Design a 2-digit hexadecimal DOWN counter (A1H-23 H) using 74193 IC





Counters with parallel load(Presettable)

- Flip flops will have an additional asynchronous input referred as ‘load’, which may be active high or low.

- For active low ‘load’ input, if load =0, flip flop should be loaded with external input bit P else output should change according to other synchronous/asynchronous inputs.

- This feature enables the counter to have parallel load capability for transferring an external input /data /count into the counter.

Flip flop with parallel load: design

Design an presettable asynchronous counter to count between the limits $(3)_{16}$ to $(B)_{16}$ **using T-ffs**

Design an presettable synchronous counter to count between the limits $(3)_{16}$ to $(B)_{16}$ **using T-ffs**

Design an asynchronous counter to count between the limits $(3)_{16}$ to $(N)_{16,}$ N is a single digit hexadecimal number with value > $(3)_{16}$. Using 7485 IC, 4-bit asynchronous counter (with parallel load) block diagram and external gates..

- Questions: ?