

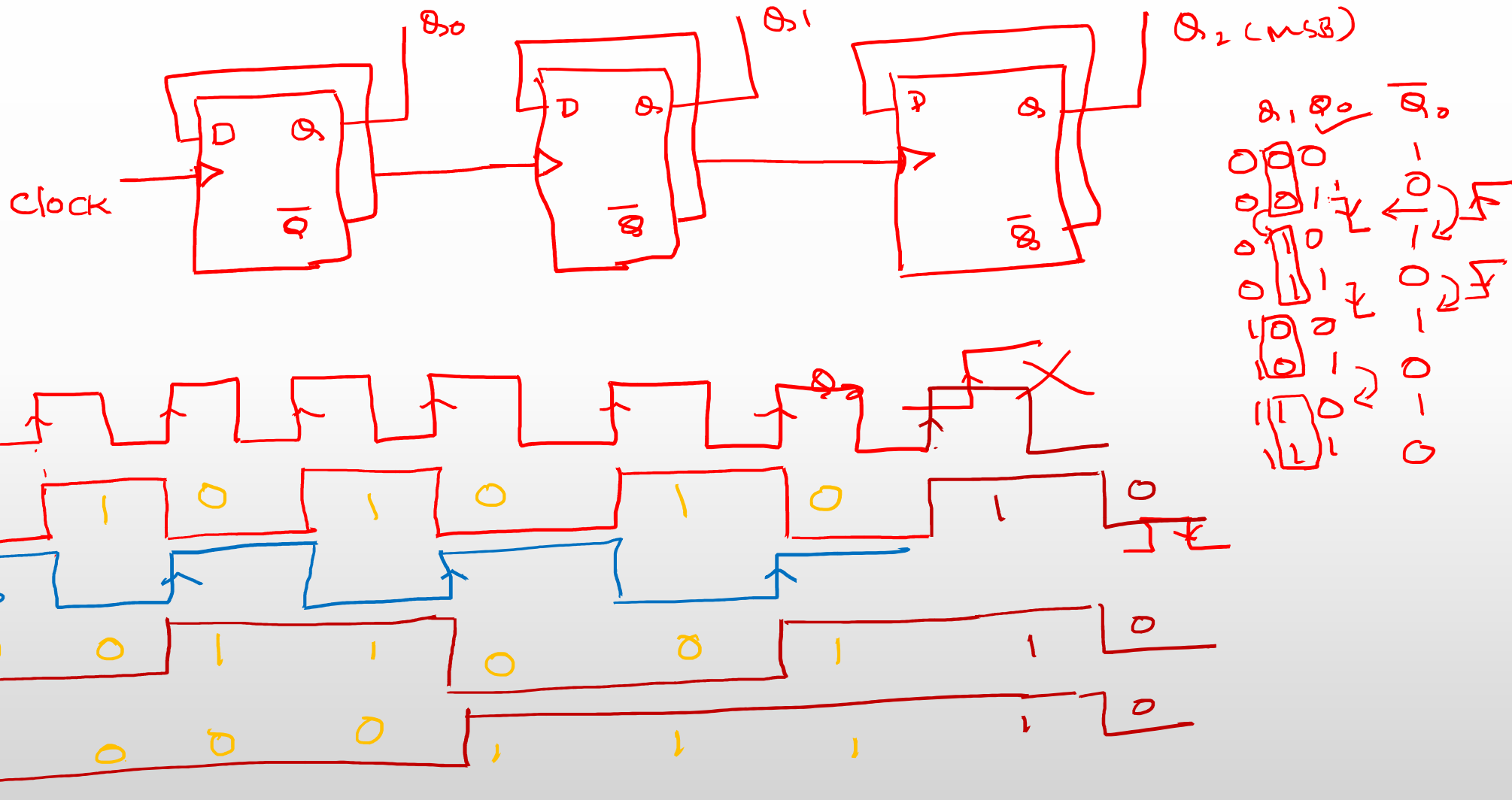


ASYNCHRONOUS COUNTER(RIPPLE COUNTER) CONTD..

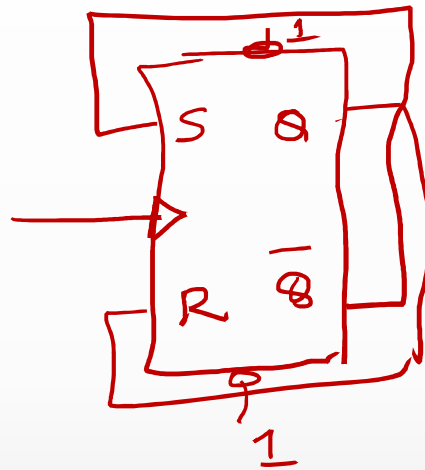
Counters:

- Register that goes through prescribed sequence of states upon the application of input pulses is called a counter.
- There are 2 types of counters:
 - *Asynchronous counters (Ripple counters)* : Clock inputs are triggered by transitions of other flipflop.
 - *Synchronous counters* : The clock inputs of all flip flops receive common clock.

- Design a 3 – bit Asynchronous UP counter using positive edge triggered D flip flops.



- Design a 4 – bit (MOD 16/ Divide by 16) Asynchronous UP counter using negative edge triggered SR flip flops.
- Design a 4 – bit Asynchronous UP counter using positive edge triggered SR flip flops.



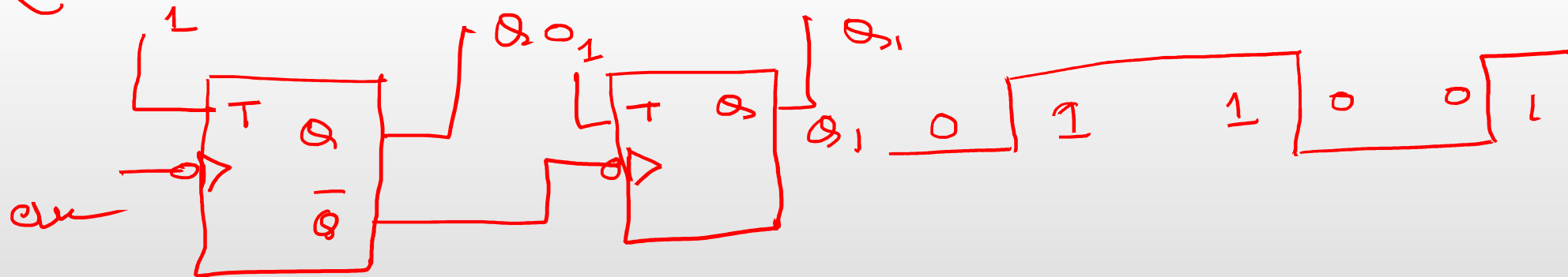
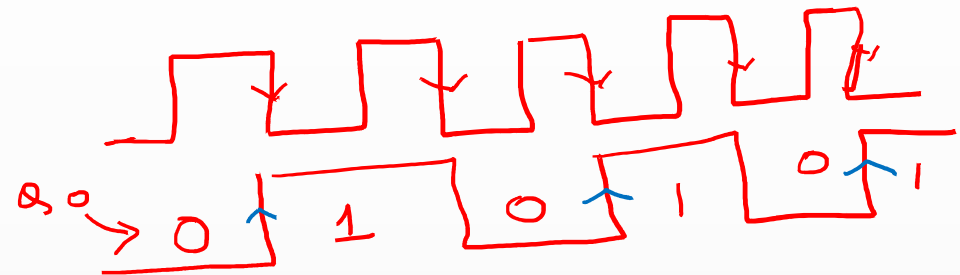
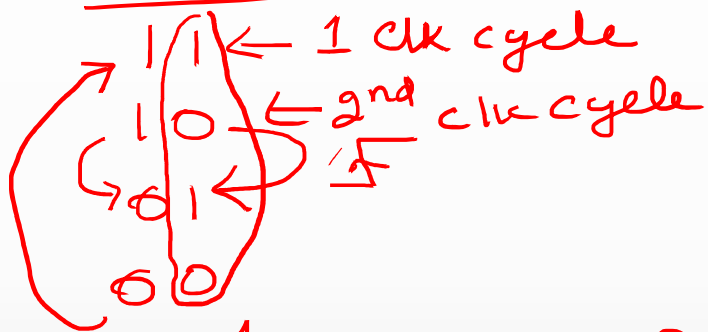


DOWN COUNTERS

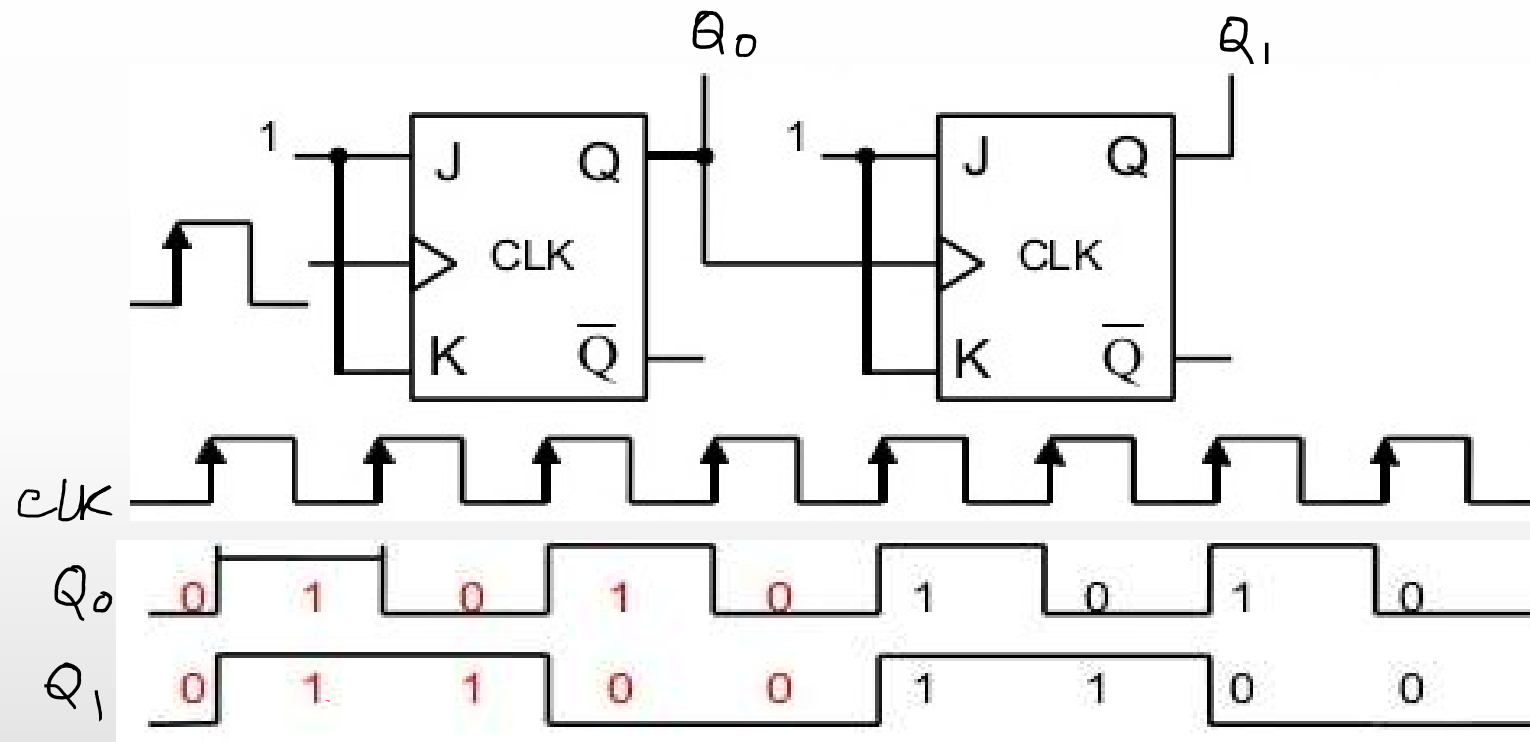
MOD4 down \Rightarrow 2-bit

-ve edge triggered (JK, T, SR, D)

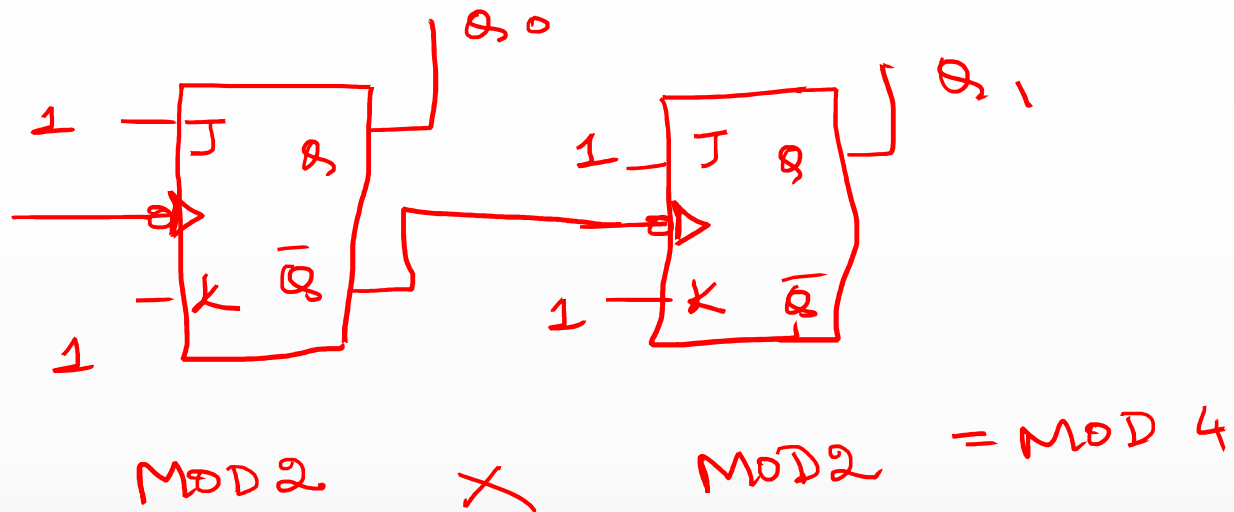
Q_1, Q_0



- Design a 2 – bit Asynchronous DOWN counter using positive edge triggered JK flip flops.



- Design a 2 – bit Asynchronous DOWN counter using negative edge triggered JK flip flops.



- Design a 2 – bit Asynchronous DOWN counter using negative edge triggered T flip flops.

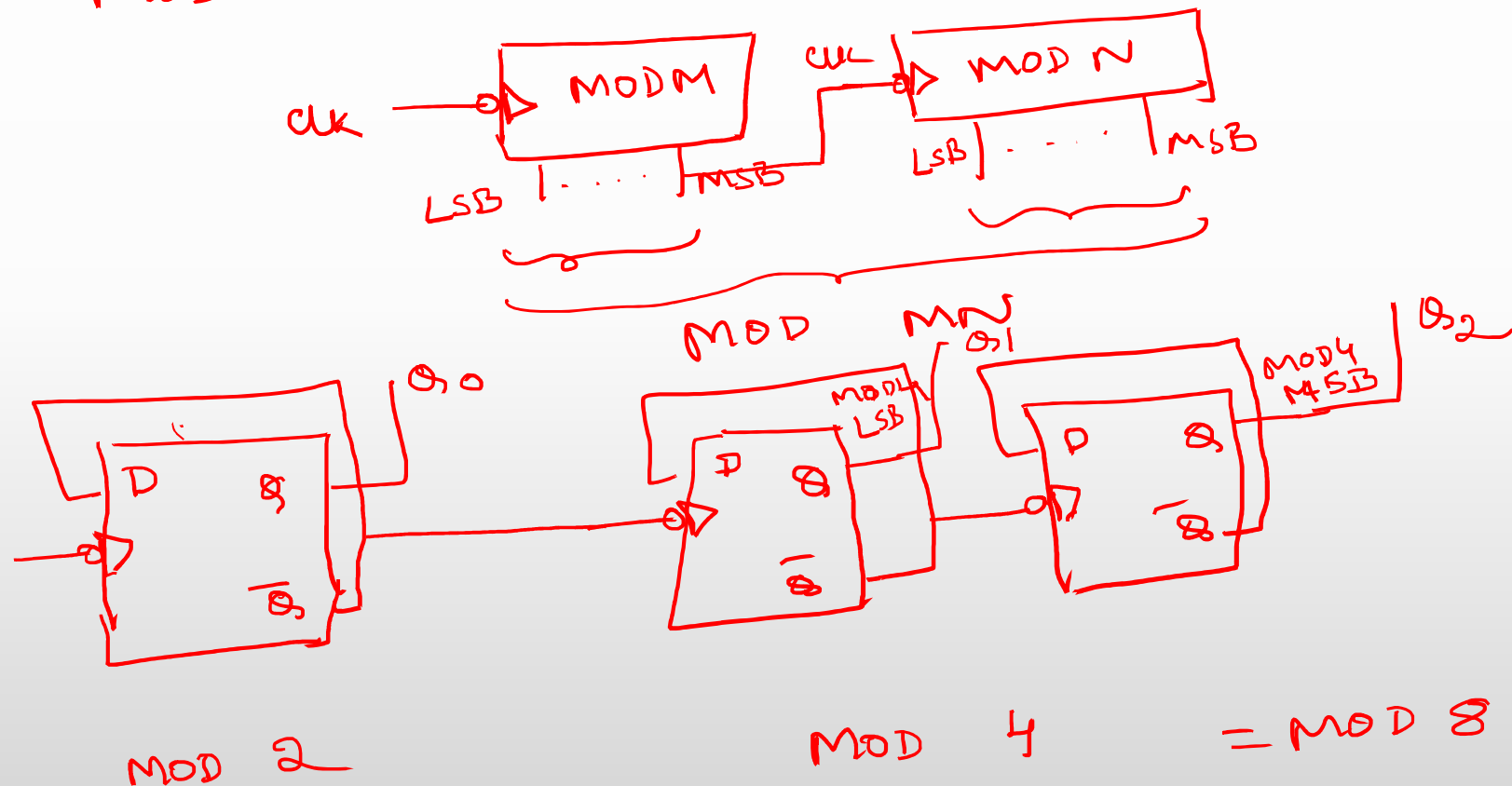
- Design a 2 – bit Asynchronous DOWN counter using positive edge triggered T flip flops.

Draw the circuit

- Design a 3 – bit Asynchronous DOWN counter using negative edge triggered D flip flops.

$$\text{MOD } 8 \Rightarrow \text{MOD } 4 \times \text{MOD } 2 = \underline{\text{MOD } 2 \times \text{MOD } 4} \quad \checkmark$$

$$\text{MOD } MN \Rightarrow \text{MOD } M \times \text{MOD } N$$



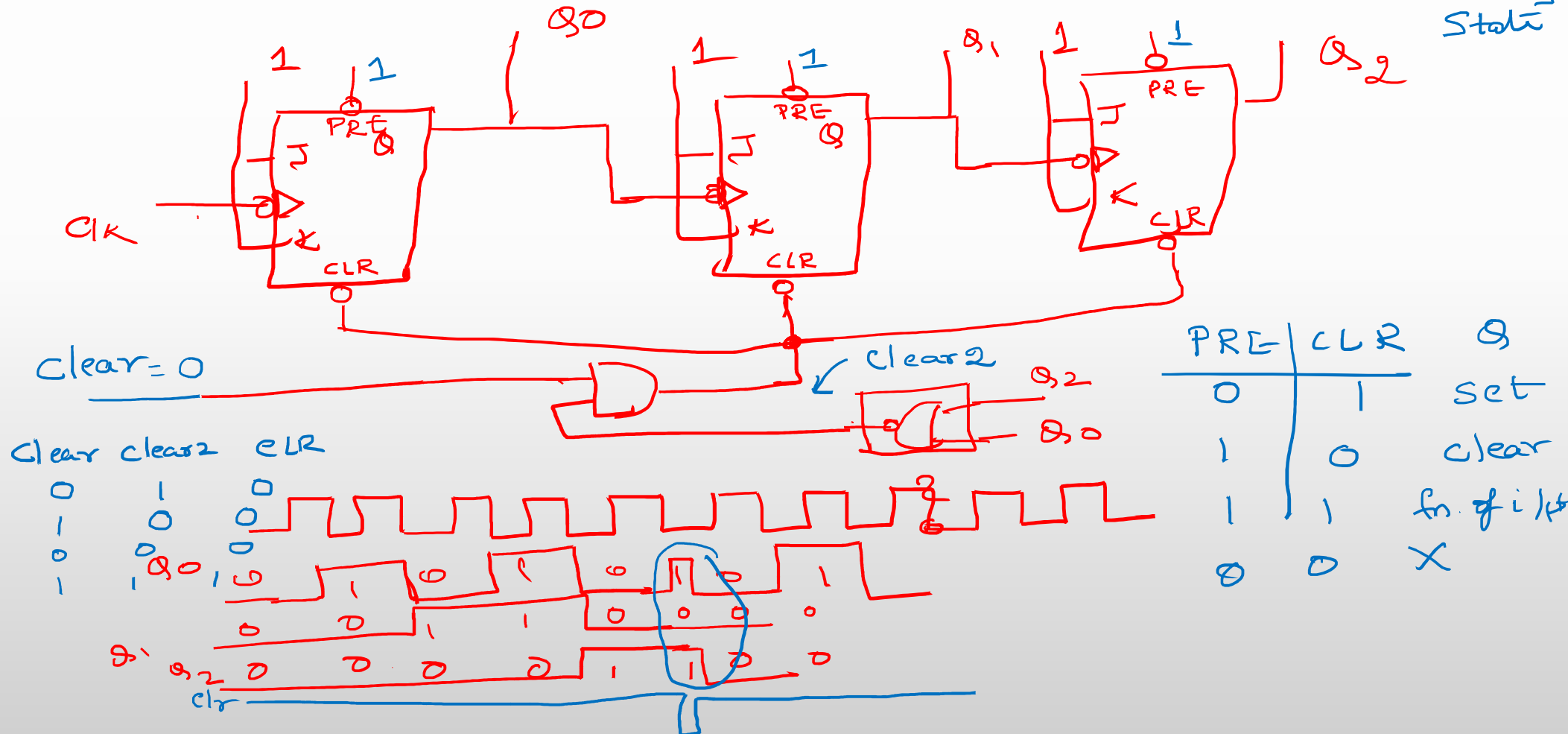
- Design a 3 – bit Asynchronous DOWN counter using positive edge triggered D flip flops.

- சுதிரி ரு

$0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 0$
 $\underbrace{\hspace{10em}}_{1 \ 2 \ 3 \ 4 \ 5 \ 6^{th}}$

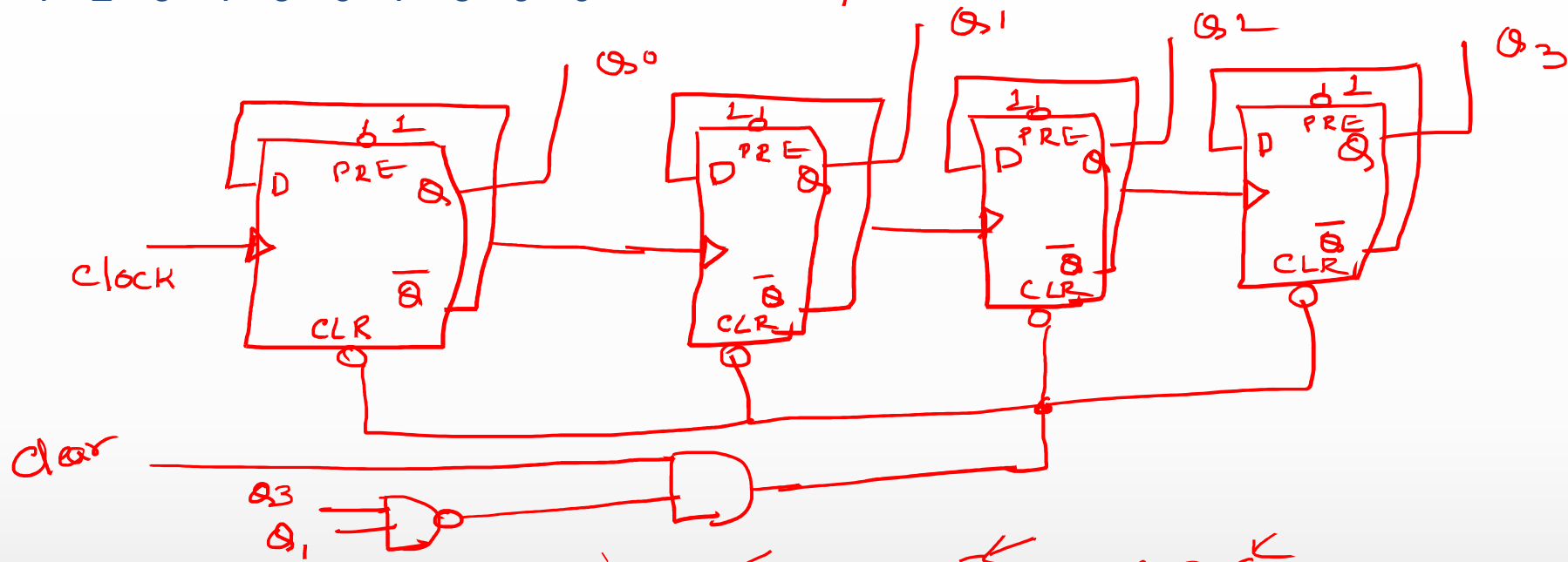
000 \rightarrow 001 \rightarrow 010 \rightarrow 011 \rightarrow 100 \rightarrow 101

decoding
State



- Design a MOD 10 Asynchronous UP counter using positive edge triggered D Flip Flops.

0-→1-→2-→3-→4-→5-→6-→7-→8-→9-→0 *Decade/Decimal*



decoding state } $Q_3 \quad Q_1$
1010

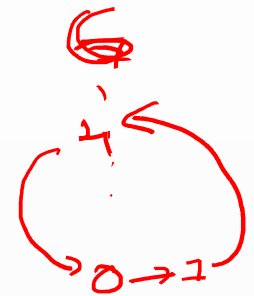
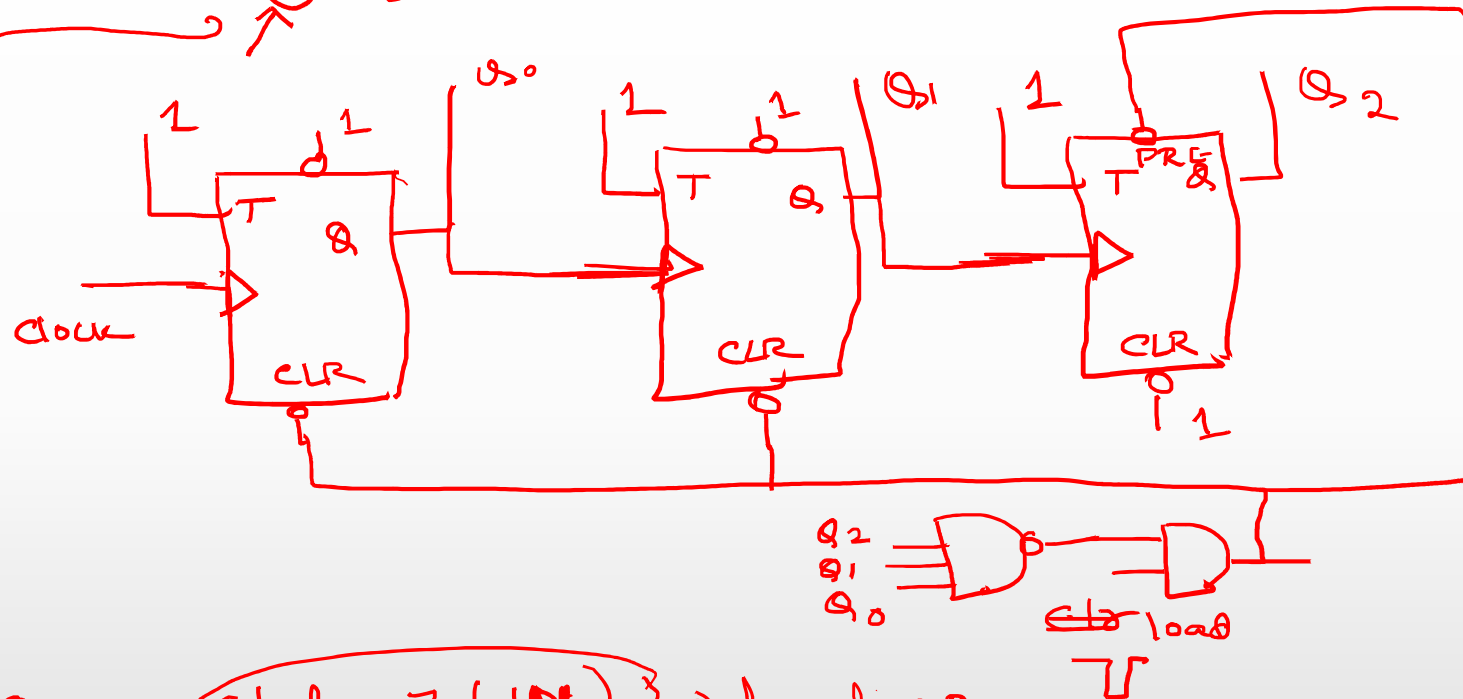
MOD 4
 $\begin{Bmatrix} 00 \\ 01 \\ 10 \\ 11 \end{Bmatrix}$
 =

MOD 5
 $\begin{Bmatrix} 000 \\ 001 \\ 010 \\ 011 \\ 100 \end{Bmatrix}$
 4
 1

MOD 6
 $\begin{Bmatrix} 000 \\ 001 \\ 010 \\ 011 \\ 100 \\ 101 \end{Bmatrix}$

Design a MOD 5 Asynchronous DOWN counter using positive edge triggered T Flip Flops.

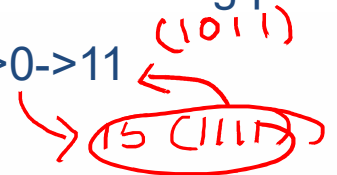
4 → 3 → 2 → 1 → 0 → 4 → 3 → 2 → 1 → 0 → ...



State 0 → State 7 (111) → decoding state
 ↓
 State 4 (100)
 Q₂ Q₁ Q₀

- Design a MOD 12 Asynchronous DOWN counter using positive edge triggered T Flip Flops.

11->10->9->8->7->6->5->4->3->2->1->0->11



(1011)

15 (1111)

- Design a MOD 18 Asynchronous DOWN counter using positive edge triggered JK Flip Flops.

- Design a 3 bit Asynchronous UP/DOWN counter using negative edge triggered JK Flip Flops.

Design a counter to obtain a 1KHz clock signal from a 10KHz clock signal with 50% duty cycle using negative edge triggered JK Flip Flops. UP counter

Square

$$\text{MOD } 10 = \text{MOD } 5 \times \text{MOD } 2, \quad 4 \text{ ffs.}$$

Dec. count	Q_3	Q_2	Q_1	Q_0	clk cycle
0	0	0	0	0	1
1	0	0	0	1	2
2	0	0	1	0	3
3	0	0	1	1	4
4	0	1	0	0	5
8	1	0	0	0	6
9	1	0	0	1	7
10	1	0	1	0	8
11	1	0	1	1	9
12	1	1	0	0	10
	0	0	0	0	
		0	0	1	

Design a MOD 6 Asynchronous counter with 50% duty cycle using negative edge triggered D Flip Flops.

$$f_{\text{output}} = \frac{f_{\text{clk}}}{6}$$

$$\text{MOD } MN = \text{MOD } M \times \text{MOD } N \rightarrow = 2^{\text{power}}$$

$$MN \neq 2^{\text{power}}$$

$$\text{MOD } 6 = \text{MOD } 3 \times \text{MOD } 2 \rightarrow 50\%$$

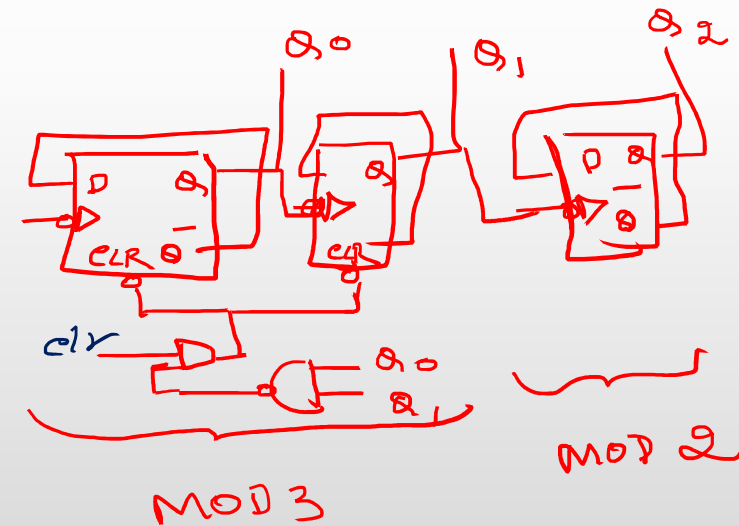
$$\text{MOD } 2 \times \text{MOD } 3$$

$$Q_2, Q_1, Q_0$$

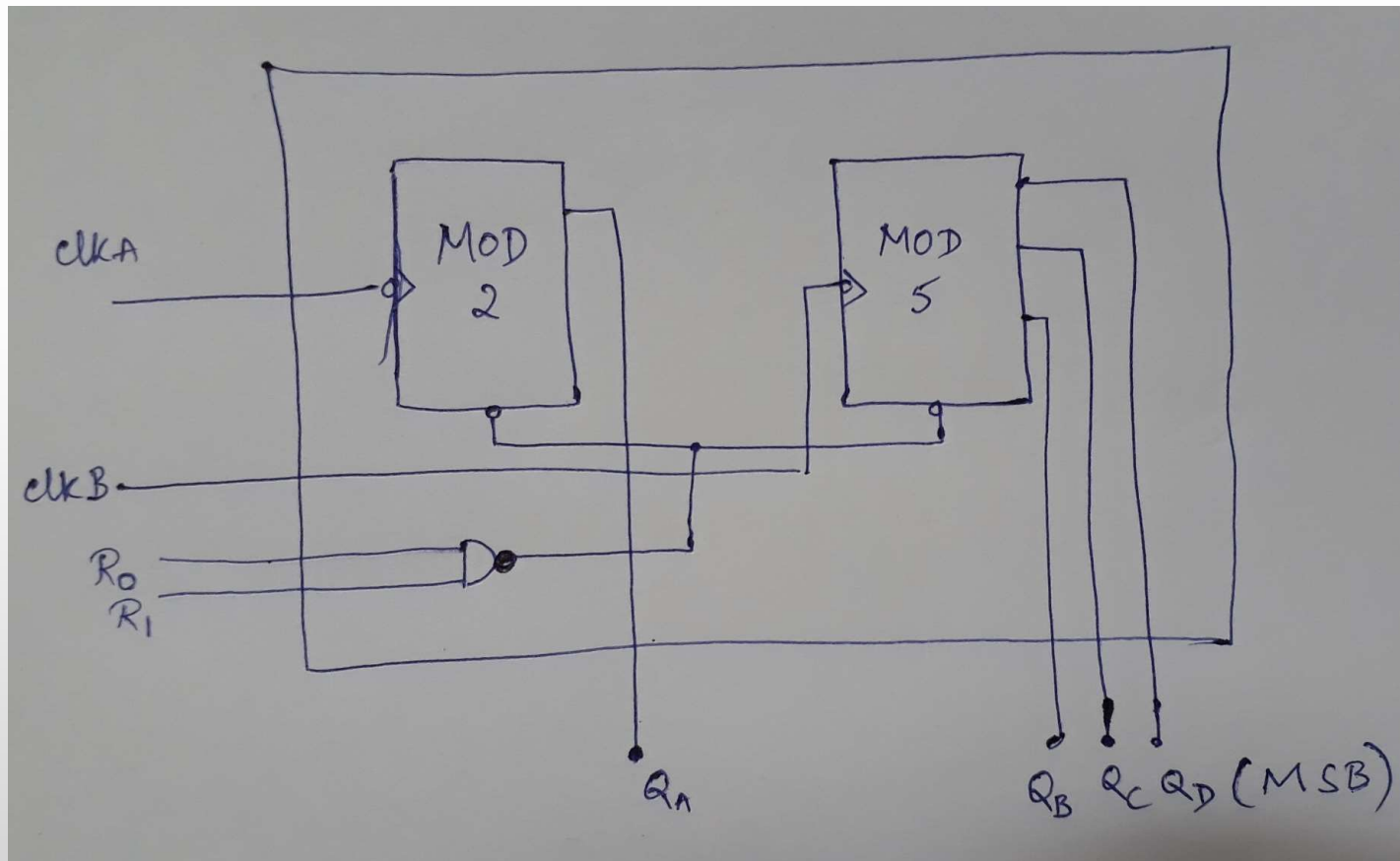
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	0	0	0

MOD 6

MOD 3			MOD 2		MOD 3	
Q_2, Q_1	Q_0		Q_1	Q_0		
0	0	0	0	0	0	0
0	0	1	0	1	0	1
0	1	0	1	0	1	0
0	1	1	1	1	1	1
1	0	0	0	0	0	0
1	0	1	0	1	0	1
1	1	0	1	0	1	0
1	1	1	1	1	1	1



7490 IC (MOD 10 Asynchronous UP Counter)



CKB	1	14	CKA
R0(1)	2	13	NC
R0(2)	3	12	Q _A
NC	4	11	Q _D
V _{CC}	5	10	GND
R9(1)	6	9	Q _B
R9(2)	7	8	Q _C

Note: Connect pin number 6 & 7 to GND

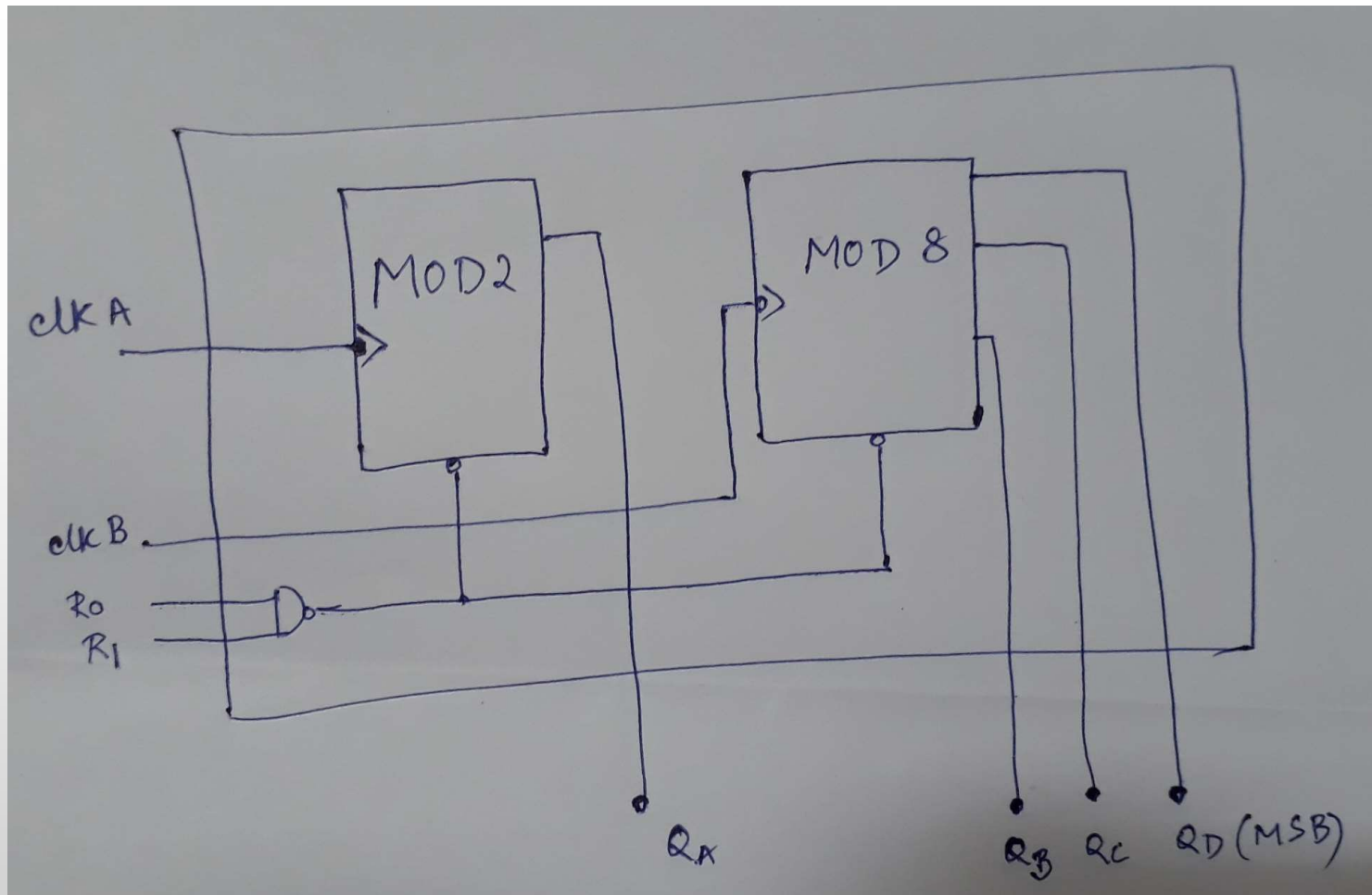
- Design MOD 10 counter using 7490IC

- Design MOD 6 counter using 7490IC and external gate

- Design a counter that performs UP count from 00 to 99 using 7490ICs

- Design a counter to perform a count from 00 to 24 using 7490ICs and external gate if required.

7493 IC (MOD 16 Asynchronous UP Counter)



1	B	A	14
2	R1	NC	13
3	R2	QA	12
4	NC	QD	11
5	VCC	GND	10
6	NC	QB	9
7	NC	QC	8

- Design MOD 16 counter using 7493IC

- Design MOD 12 counter using 7493 IC and external gate if required

- Design a counter that performs UP count from 00H to FFH using 7493ICs

- Design a counter to perform a count from 00 to 65H using 7493ICs and external gate if required.