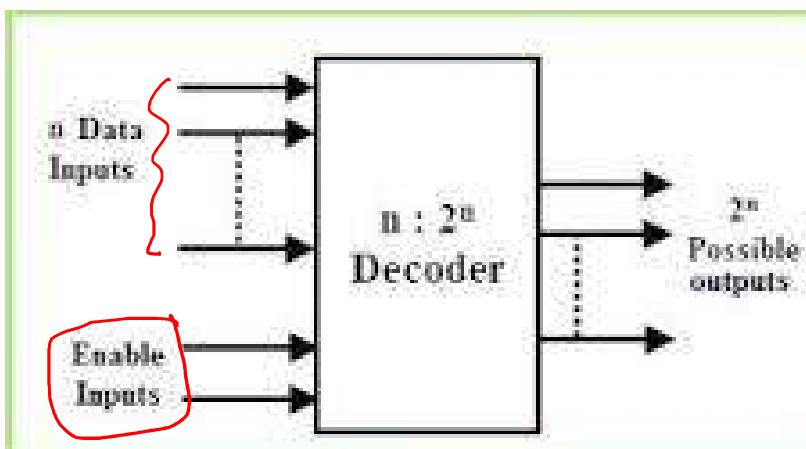


# DECODERS AND ENCODERS

Students are advised to write down the notes for every lecture

# Decoder:

- Decoder is a combinational circuit
- Converts a binary information from n-input lines to a maximum of  $2^n$  unique output lines ( n-to-  $2^n$  line decoder) and one or more enable inputs.Ex: 2-to-4 line, 3-to-8 line..etc
- In standard decoders, only one output line will be active at a time corresponding to the input binary combination.



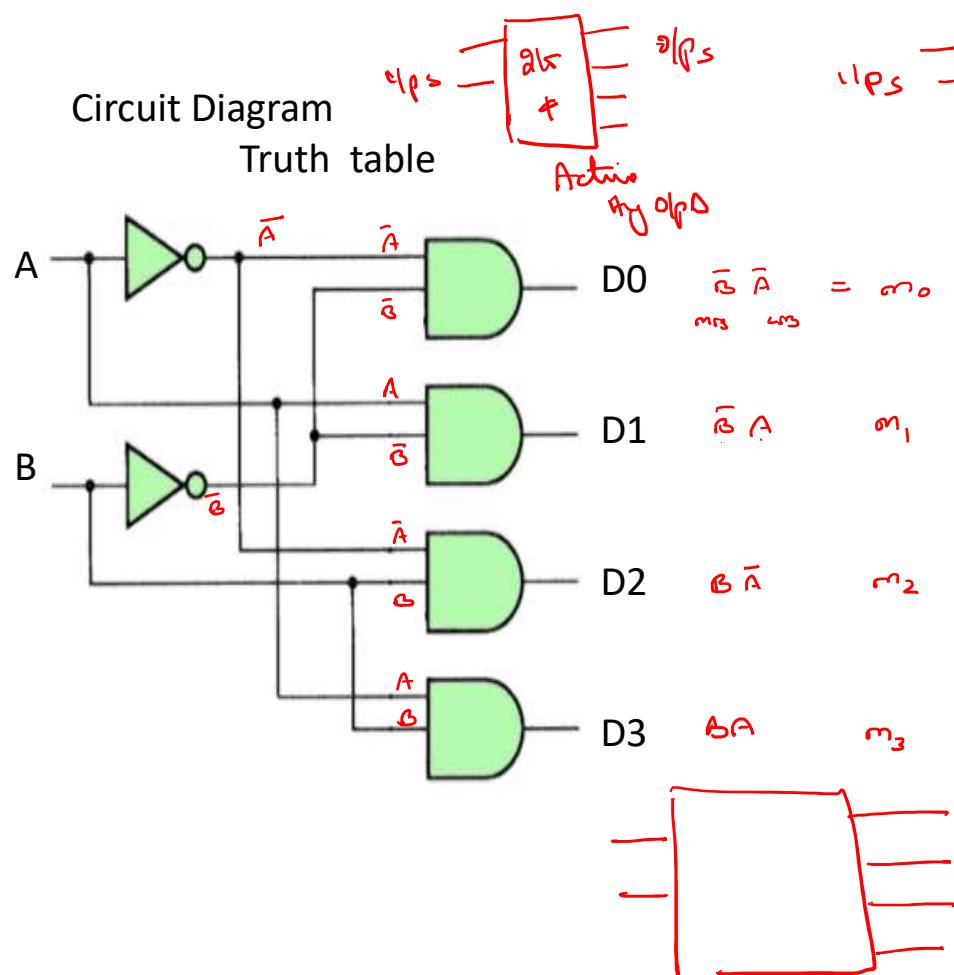
2<sup>n</sup>

E.g. 2-61  
2: a decoder

	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>
00	x	x	x	✓
01	x	x	✓	x
10	x	✓	x	x
11	✓	x	x	x

1 : 2 line  
2 : 4 line  
3 . 8  
4 : 16 decoder  
⋮  
 $bil = 2^n$  lines decoder

# 2-to-4 line decoder



NAND Gates at output array

S	A	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	1	1	1	0
0	1	0	1	0	1
1	0	1	0	1	1
1	1	0	1	1	1

M<sub>3</sub> M<sub>2</sub> M<sub>1</sub> M<sub>0</sub>

Active low o/p

Truth table for Active HIGH o/p

$\bar{A}\bar{B}$	$\bar{A}B$	$A\bar{B}$	$AB$	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	0	0	0	0	0	1
0	1	0	0	0	0	1	0
1	0	0	1	0	1	0	0
1	1	1	0	1	0	0	0

m<sub>3</sub> m<sub>2</sub> m<sub>1</sub> m<sub>0</sub>

Active HIGH Outputs

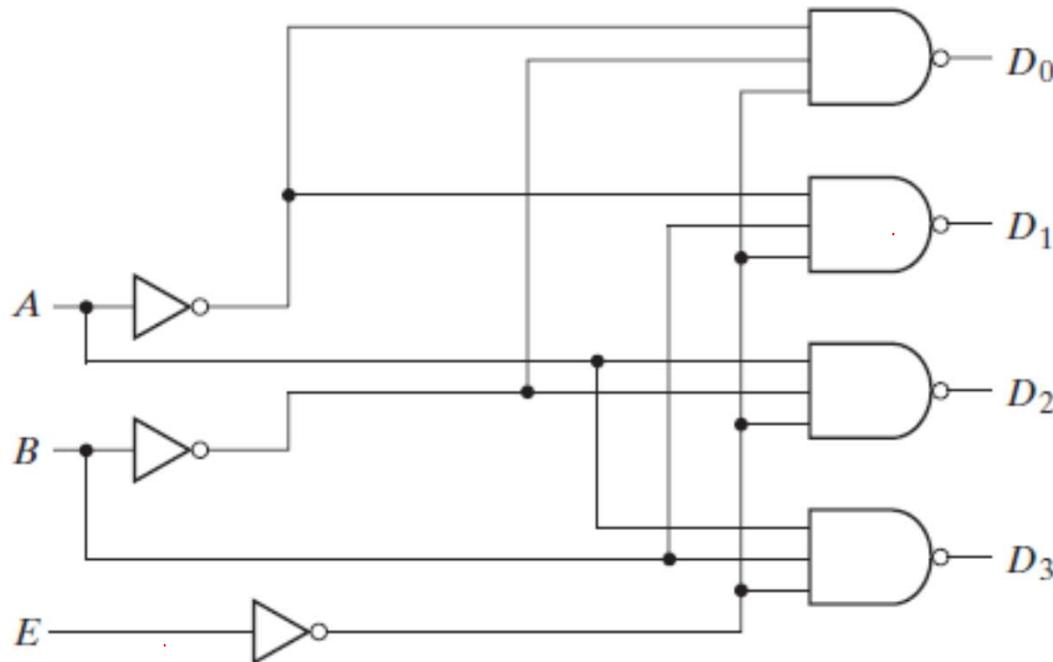
with outputs HIGH

Active HIGH output

with NAND Gates at outputs → Active LOW o/p

Note: m<sub>2</sub> = m<sub>3</sub>

2-to-4 line decoder with active low output &  
 enable <sup>input</sup> active low



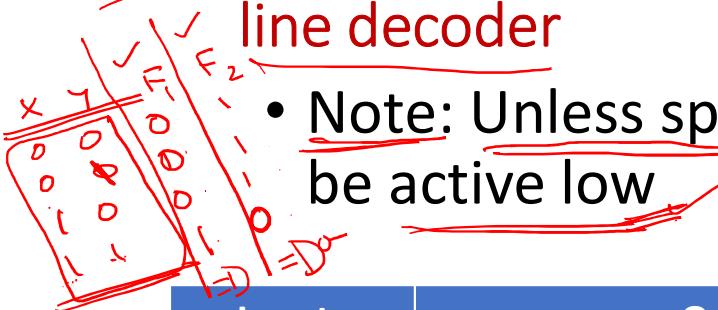
(a) Logic diagram

$E$	$A$	$B$	$D_0$	$D_1$	$D_2$	$D_3$
1	$X$	$X$	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

(b) Truth table



Ques: Write the truth table, logic diagram and block diagram of 3-to-8 line decoder



- Note: Unless specified, assume the output and enable input to be active low

Inputs			Outputs								
E	A	B	C	D0	D1	D2	D3	D4	D5	D6	D7
1	x	xx		*	*	*	*	*	*	*	*
0	0	0	0	0	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	1	1	1	1	1	1
0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1
0	1	1	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	0

Expressions for o/p variables

Question should arise and are

- Q1. Are there any enable inputs? E =
- Q2. If enables are there, then are they active low / active HIGH?

- Q3. Whether o/p lines are active low/high?

$$D_0 = \overline{E} \overline{A} \overline{B} \overline{C}$$

$$D_1 = \overline{E} \overline{A} \overline{B} C$$

$$D_2 = \overline{E} \overline{A} B \overline{C}$$

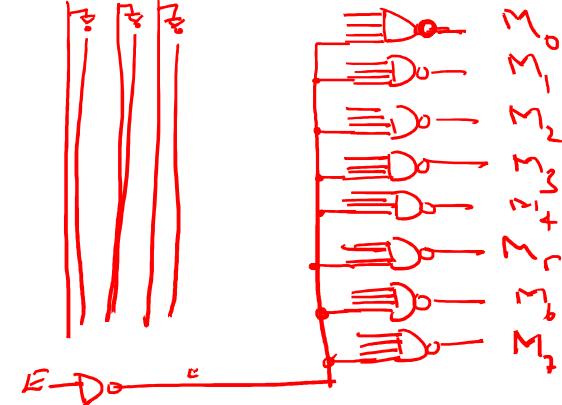
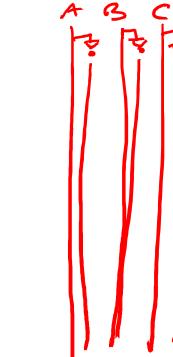
$$D_3 = \overline{E} \overline{A} B C$$

$$D_4 = \overline{E} A \overline{B} \overline{C}$$

$$D_5 =$$

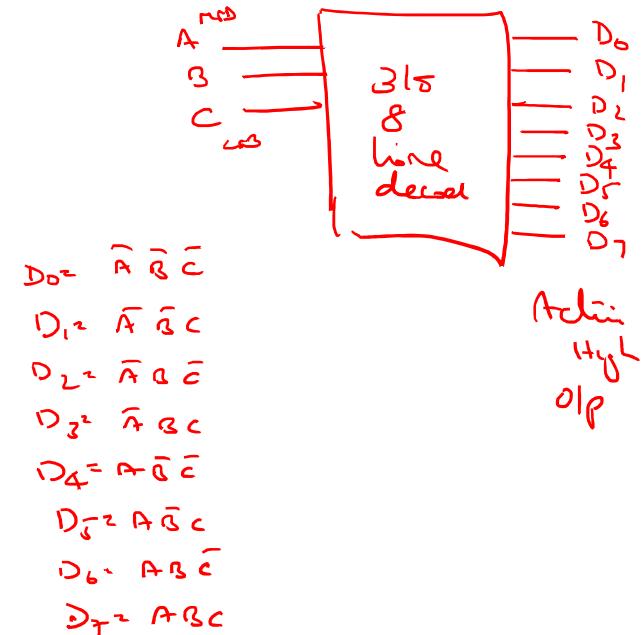
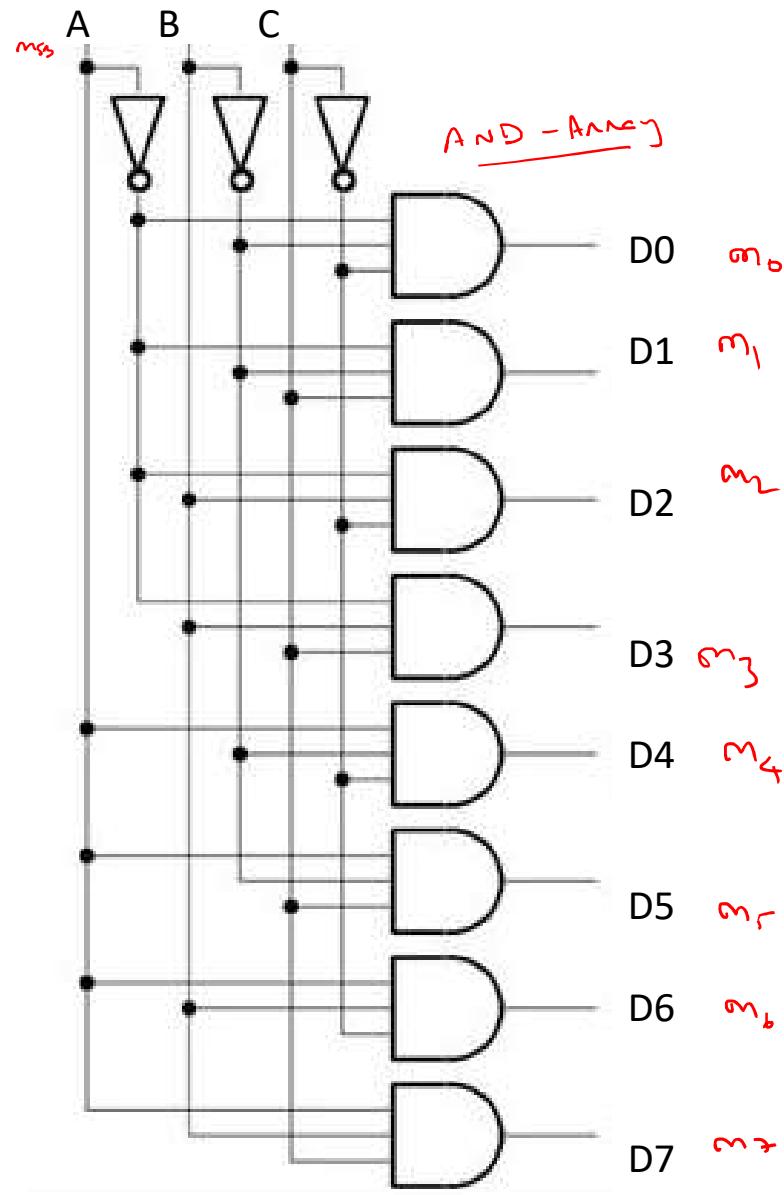
$$D_6 =$$

$$D_7 =$$

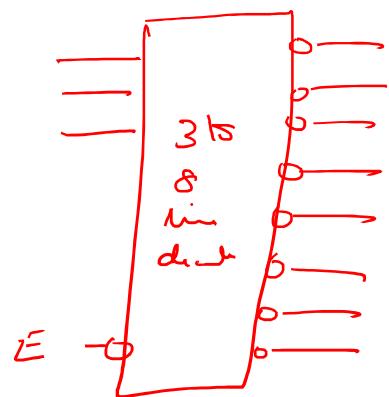
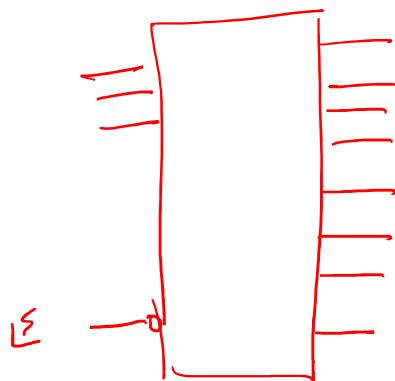
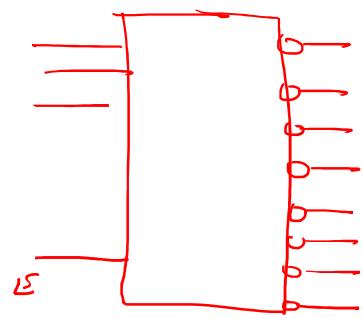
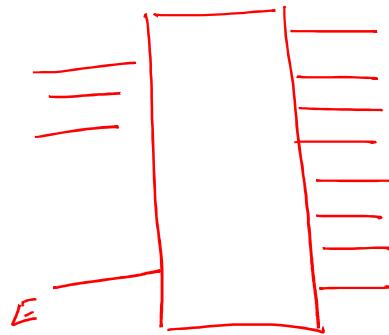


Action High O/P's

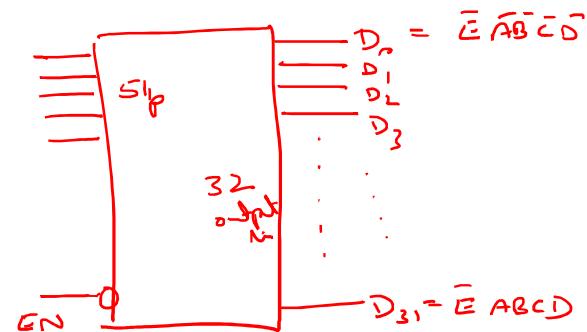
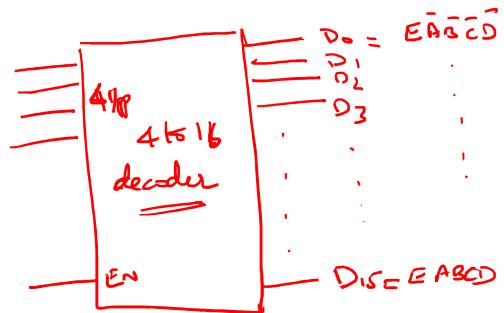
How do you input enable E  
to the circuit?



## Block diagram of 3-to-8 line decoder



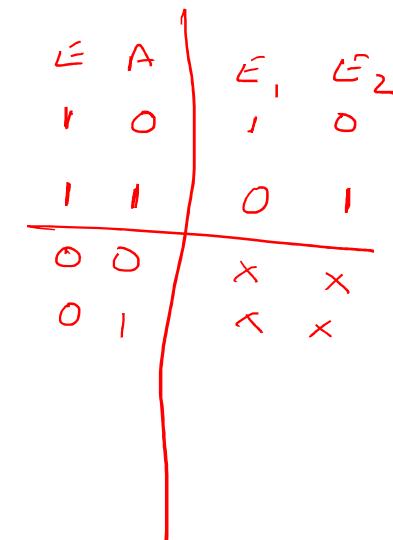
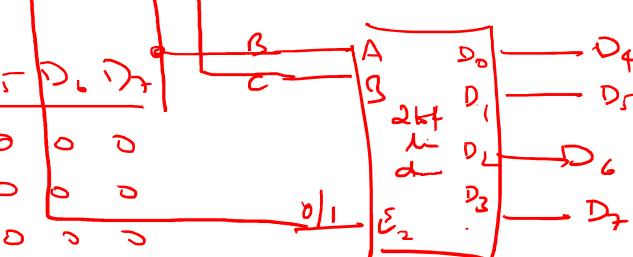
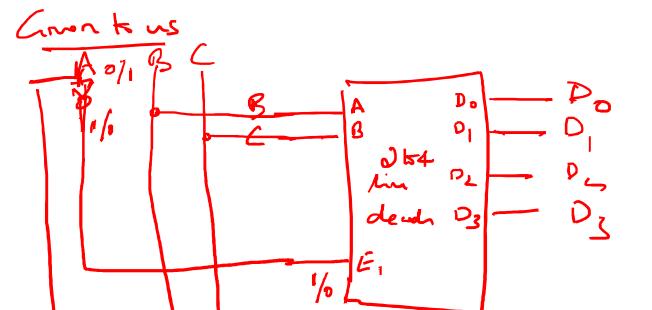
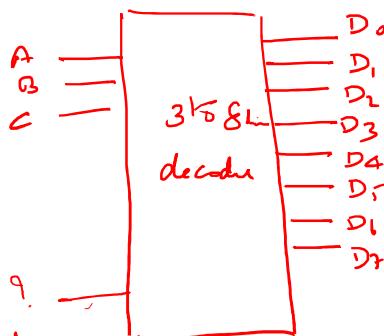
# Discussion of 4-to-16 and 5-to-32 line decoders



Design 3-to-8 line decoder using minimum number of:

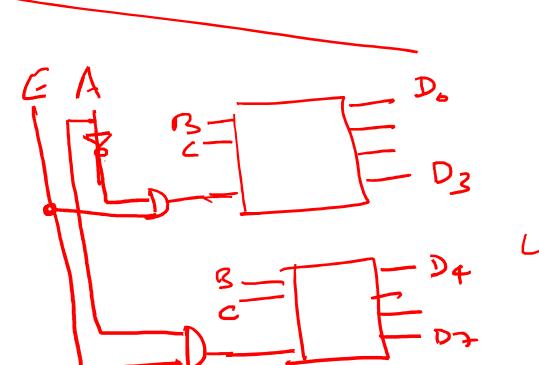
1. 2-to-4 decoders with enable input and one external gate
2. 2-to-4 decoders with enable inputs only

Design 3-to-8 line decoder using minimum number of:  
2-to-4 decoders with enable input and one external gate ✓

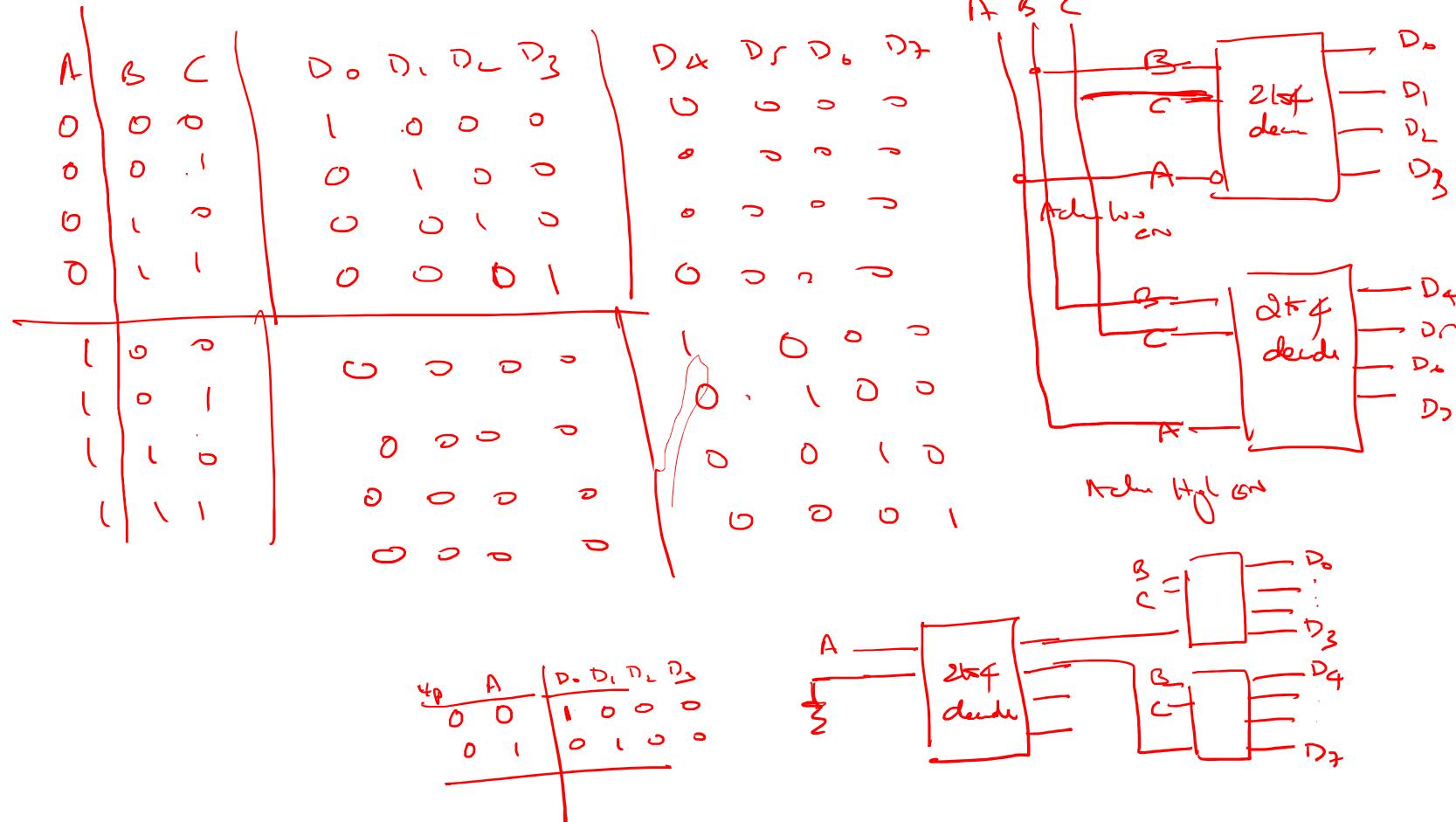


$$E_1 = E|_{\bar{A}}$$

$$\underline{E_2} = \underline{E A}$$



# Design 3-to-8 line decoder using minimum number of 2-to-4 decoders only

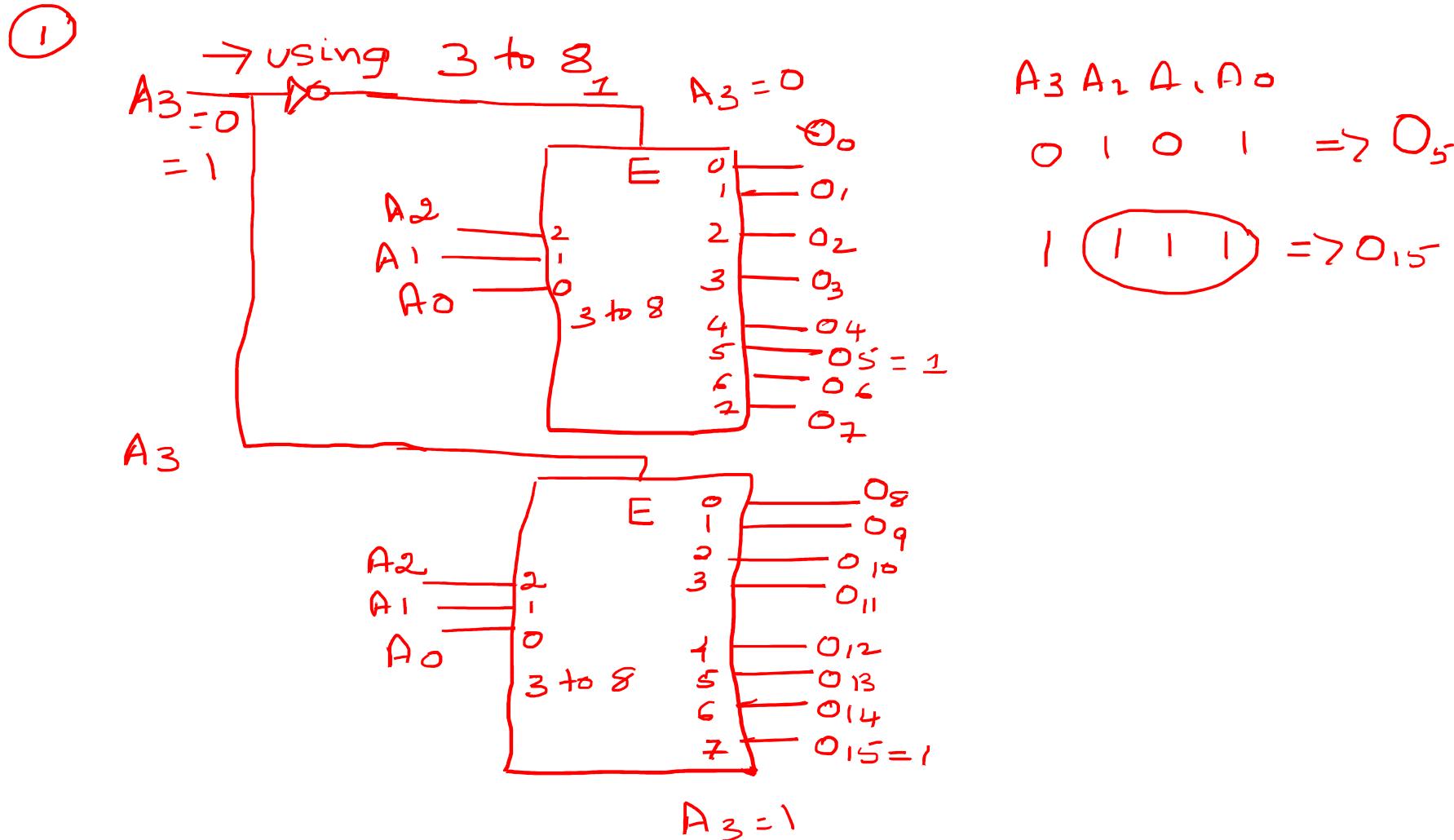


Design 4-to-16 line decoder using minimum number of

- 1. 3-to-8 decoders with enable input and one external gate
- 2. Only 3-to-8 and 2-to-4 line decoders with enable inputs
- 3. Only 2-to-4 line decoders with enable inputs

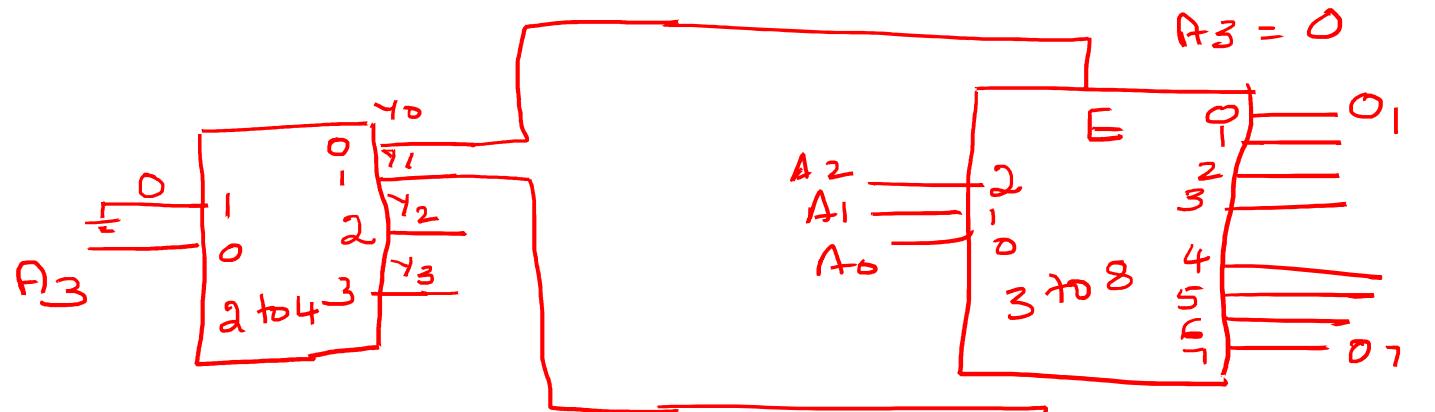
# Design 4-to-16 line decoder

# Design 4-to-16 line decoder



# Design 4-to-16 line decoder

(2) 3-to-8 decoder & 2-to-4 decoder



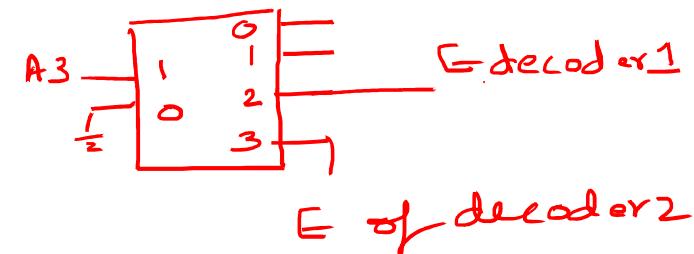
$$\begin{array}{c} 0 \ A_3 \\ \hline 0 \ 0 - y_0 \\ 0 \ 1 - y_1 \end{array}$$

$1 \ 0 \times$   
 $1 \ 1 \times$

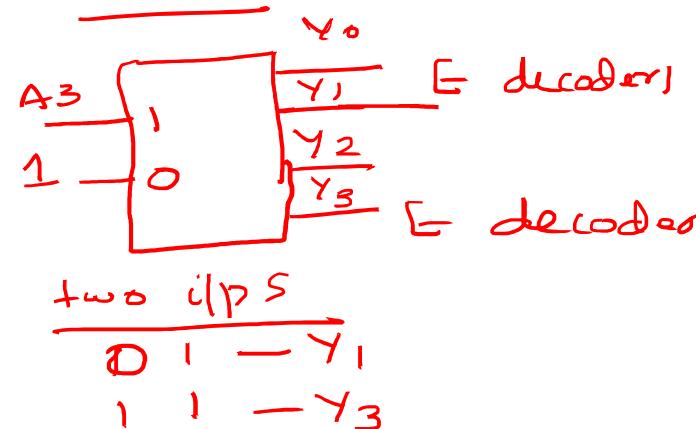
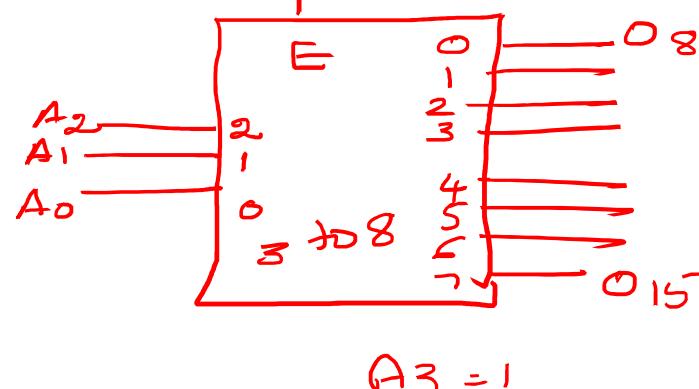
will never occur

$$y_2 = y_3 = 0$$

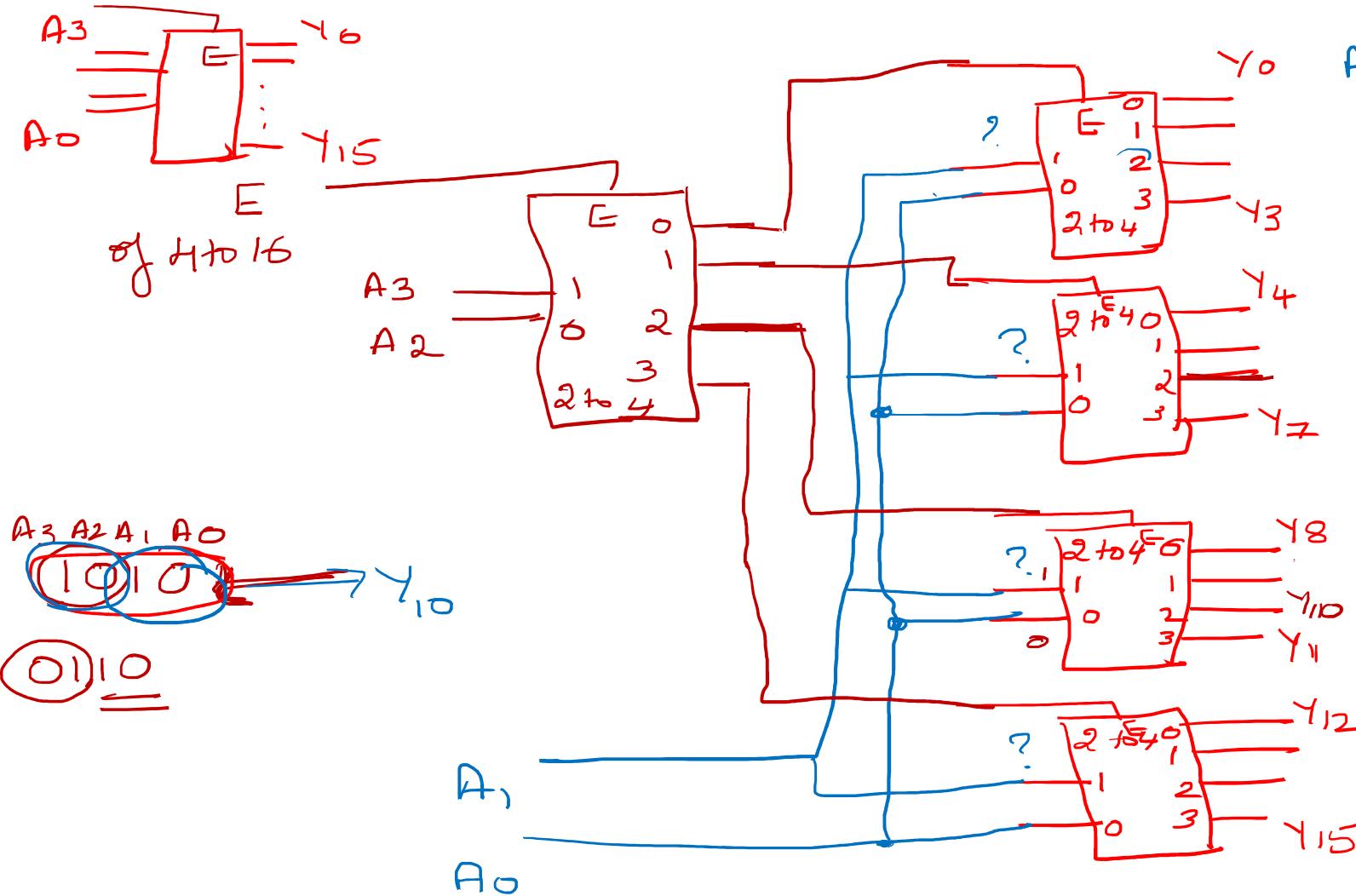
Soln 2



Soln 3



4 to 16 using only 2 to 4 decoders



$$A_3A_2 = 00$$

$$\textcircled{0} \textcircled{0} \textcircled{0} \textcircled{0} \rightarrow \textcircled{0} \textcircled{0} \textcircled{1} \textcircled{1}$$

$$A_3A_2 = 01$$

$$\textcircled{0} \textcircled{1} \textcircled{0} \textcircled{0} - \textcircled{0} \textcircled{1} \textcircled{1} \textcircled{1}$$

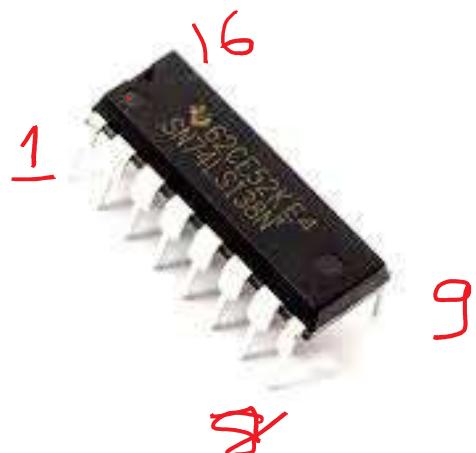
$$A_3A_2 = 10$$

$$\textcircled{1} \textcircled{0} \textcircled{0} \textcircled{0} - \textcircled{1} \textcircled{0} \textcircled{1} \textcircled{1}$$

$$A_3A_2 = 11$$

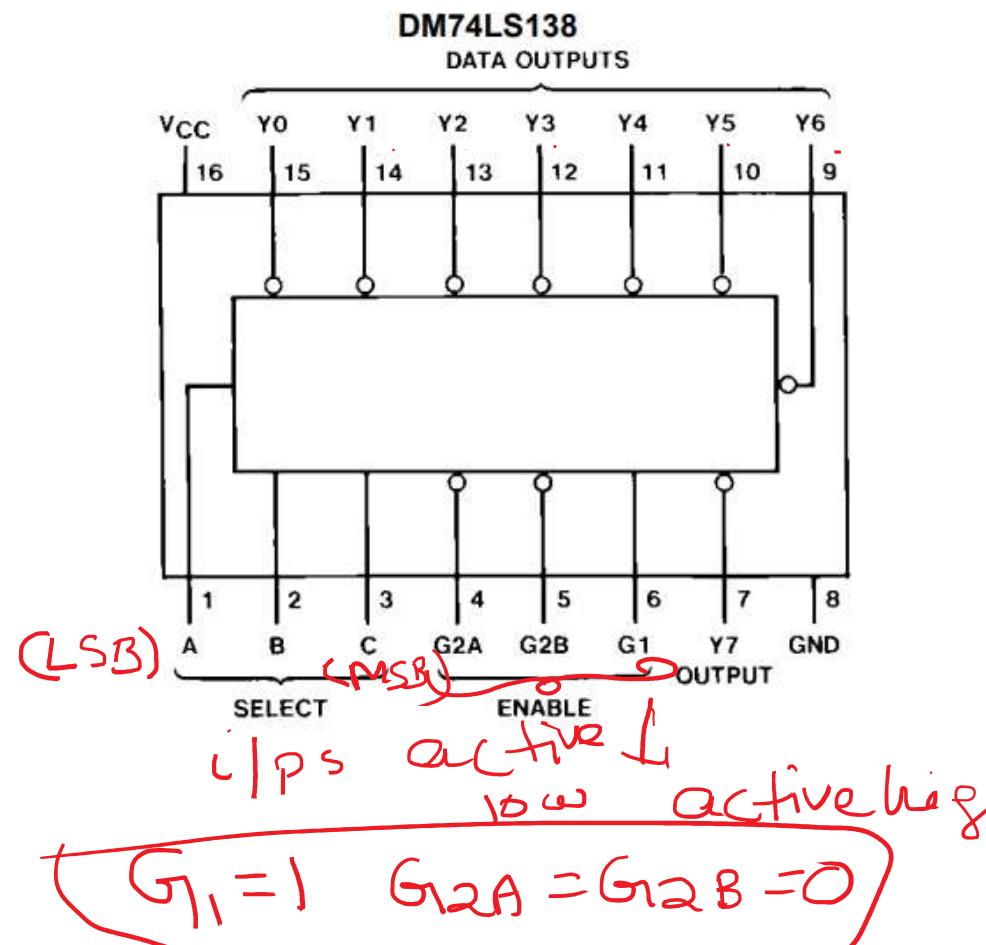
$$\textcircled{1} \textcircled{1} \textcircled{0} \textcircled{0} - \textcircled{1} \textcircled{1} \textcircled{1} \textcircled{1}$$

# 74138 IC: 3-to-8 line decoder with active low output

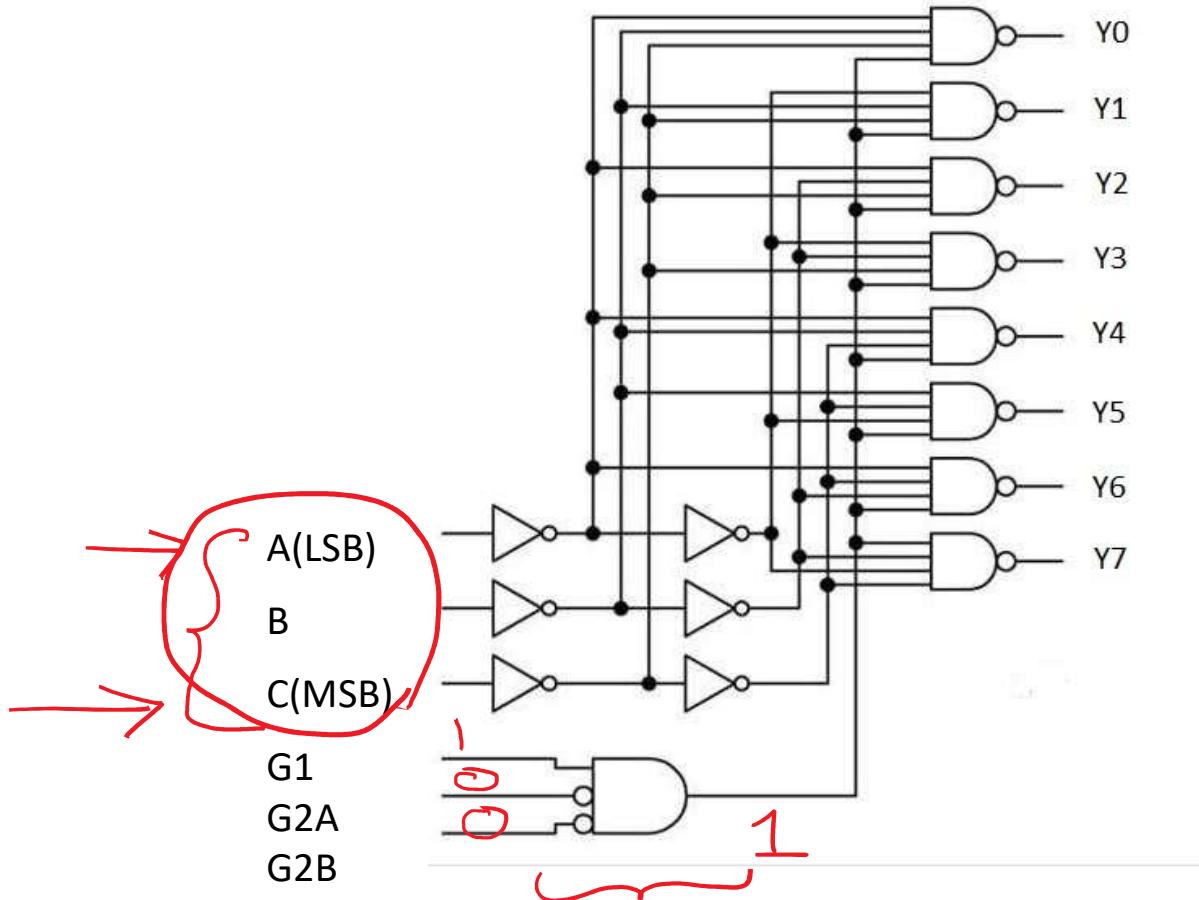


$$000 \Rightarrow Y_0 = 0$$

$$Y_1 \text{ to } Y_7 = 1$$

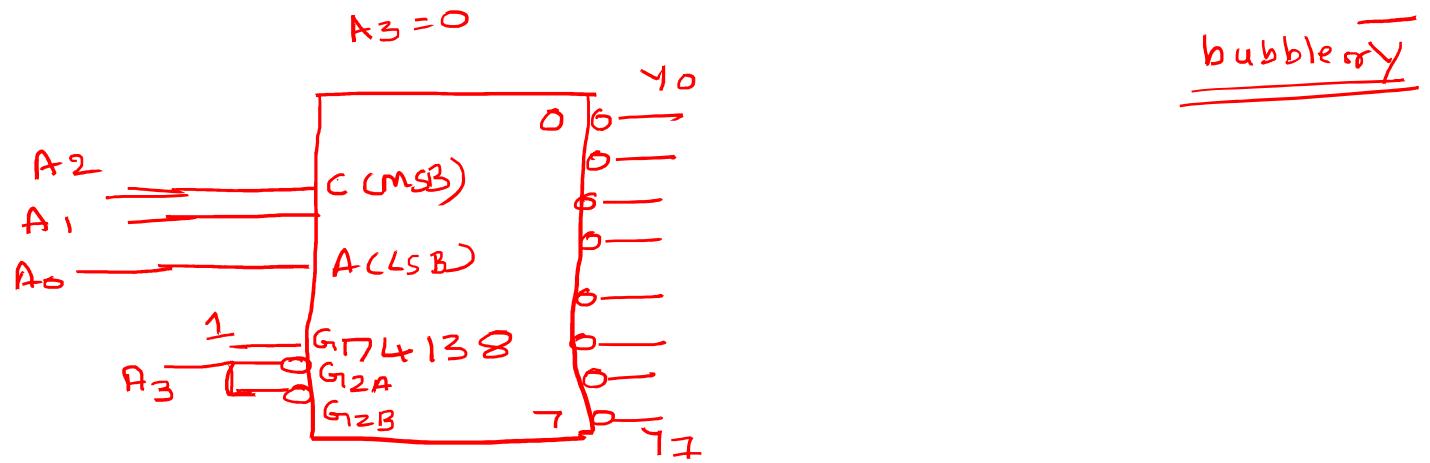


# 74138 IC internal diagram

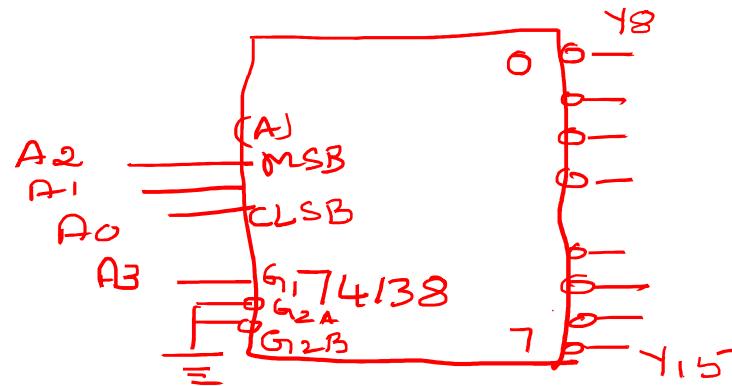


# Design 4-to-16 decoder using minimum of 74138 ICs ONLY

$A_3 A_2 A_1 A_0$



bubble or Y

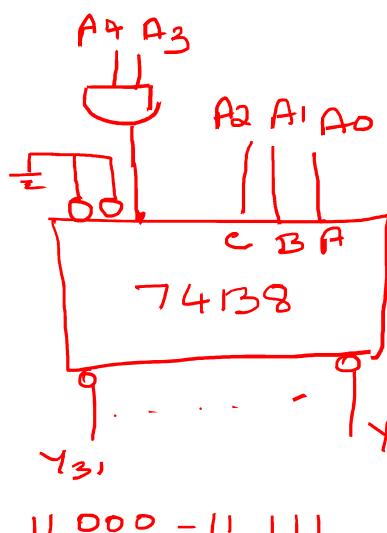


$A_3 = 1$

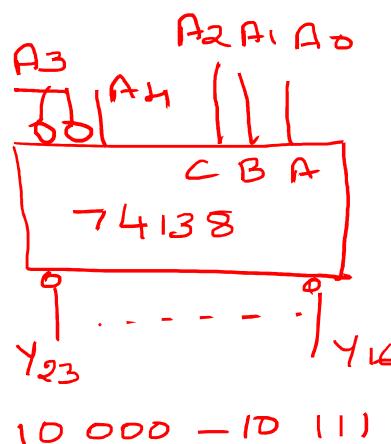
Design 5-to-32 decoder with active low output  
 using minimum of 74138 ICs and one external gate  
**ONLY**

$$\underline{A_4 A_3 A_2 A_1 A_0 \Rightarrow Y_0 \text{ to } Y_{31}}$$

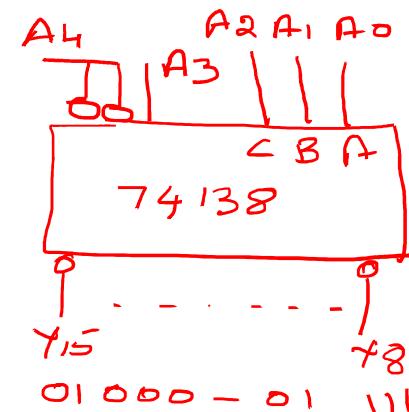
$$A_4 A_3 = 11$$



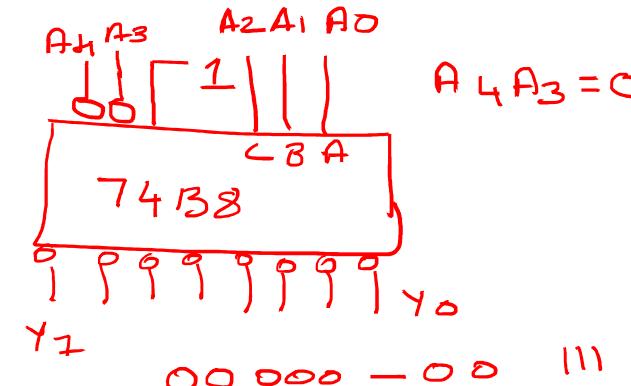
$$A_4 A_3 = 10$$



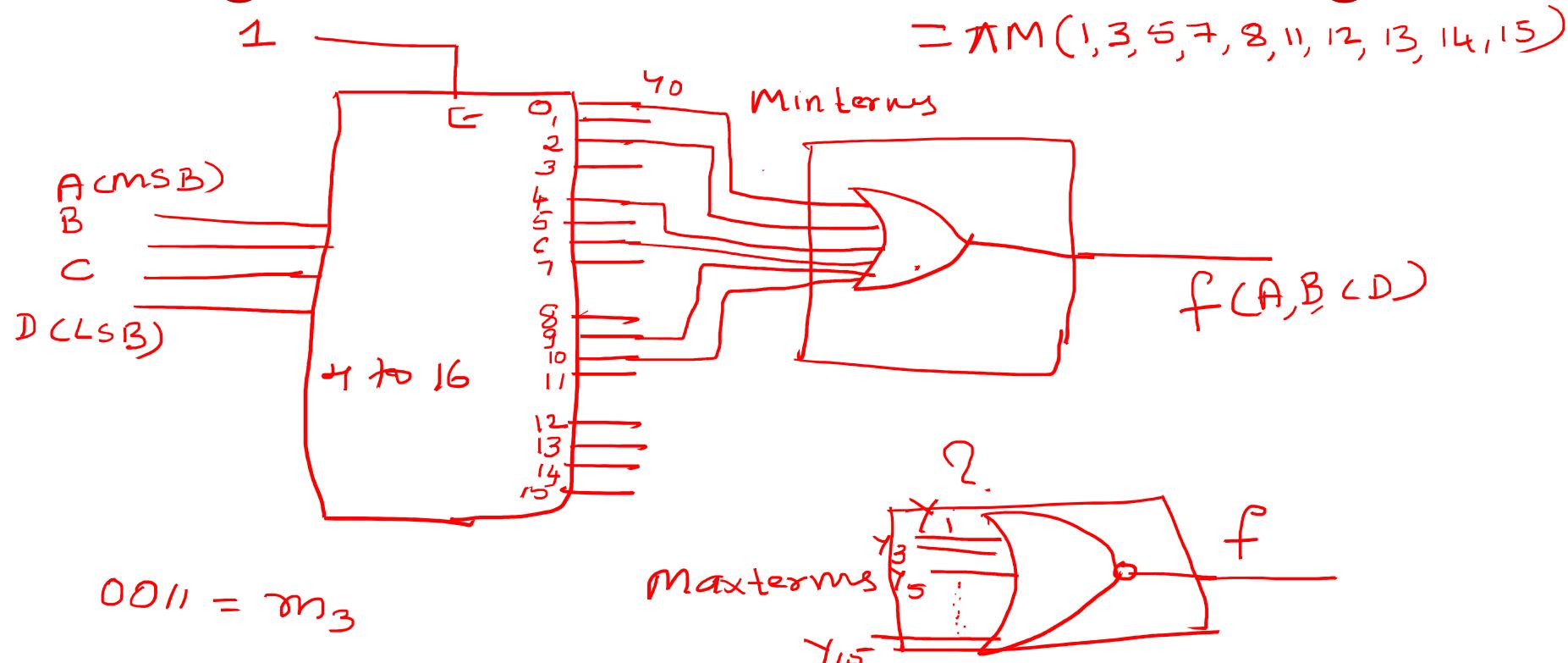
$$A_4 A_3 = 01$$



$$A_4 A_3 = 00$$



Implement  $f(A, B, C, D) = \sum m(0, 2, 4, 6, 9, 10)$  ✓  
 using suitable decoder and external gates



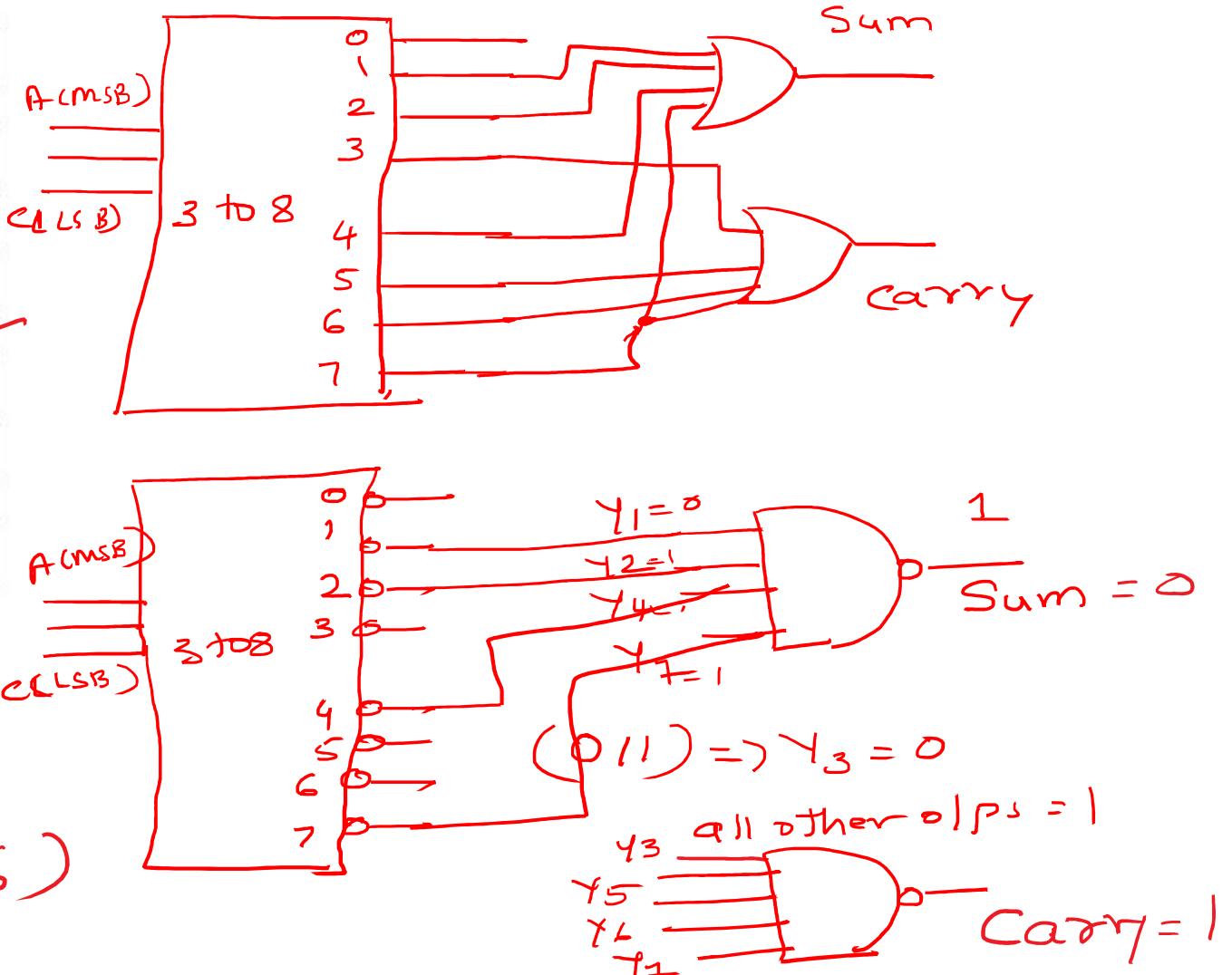
Design a full adder using 3-to-8 line decoder and external gates

Inputs			Outputs	
A	B	C <sub>in</sub>	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

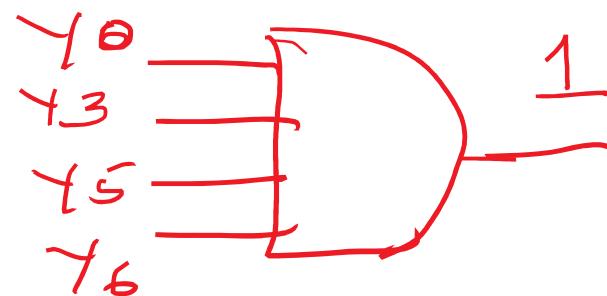
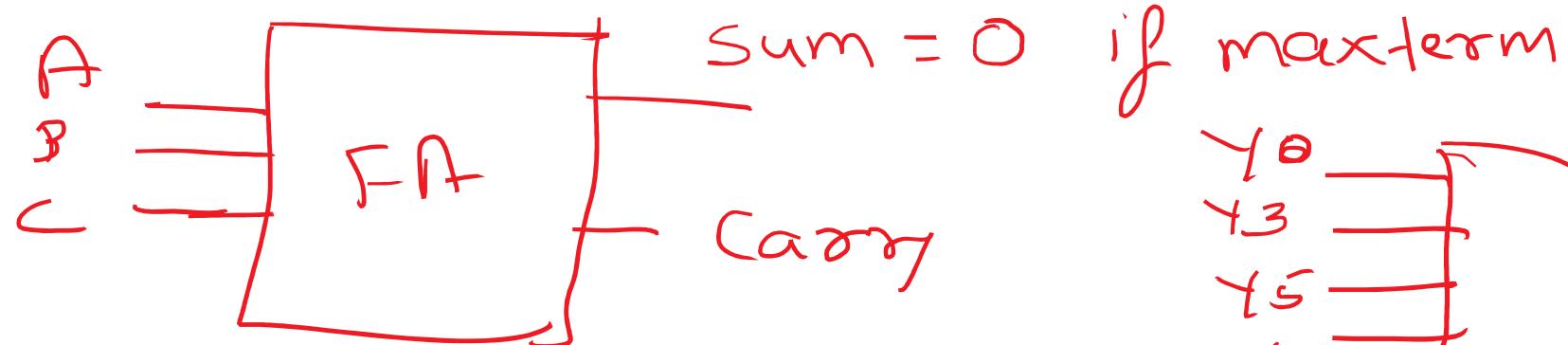
$$\text{Sum} = \sum m(1, 2, 4, 7)$$

$$\text{Carry} = \sum m(3, 5, 6, 7)$$

$$\text{Sum} = \pi m(0, 3, 5, 6)$$



$\text{Sum} = \text{AM}(0, 3, 5, 6) \quad Y_0 \quad Y_3 \quad Y_5 \quad Y_6$



Decoder	$\Sigma_m$	$\pi_M$
Active-high	OR	NOR
Active-low	NAND	AND

Realize  $f_1(x,y,z) = \prod M(1,3,6,7)$  using

- a. 3-to-8 line decoder with active high output and suitable gates
- b. 74138 decoder and suitable gates

•

Design a code converter to convert a decimal digit represented in 84-2-1 code to a decimal digit represented in excess-3 code using 74138 decoder and external gates..

Code converter design....

Code converter design...

Design  $f(x,y,z) = x' + y'z$  using 3-to-8 line decoder and external gates.

## Encoder:

- Combinational circuit that performs inverse operation of a decoder.
- Encoder has  $2^n$  (or fewer) input lines and n output lines. Ex: 4-to-2 line, 8-to-3 line...etc
- 4-to-2 encoder is given below:

Truth table

Inputs				Outputs	
$D_0$	$D_1$	$D_2$	$D_3$	x	y
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1

Circuit

Write the truth table and circuit for 8-to-3 line encoder

Design a 4 –to-2 line priority encoder

4-to-2 line priority encoder contd...

- Any questions?