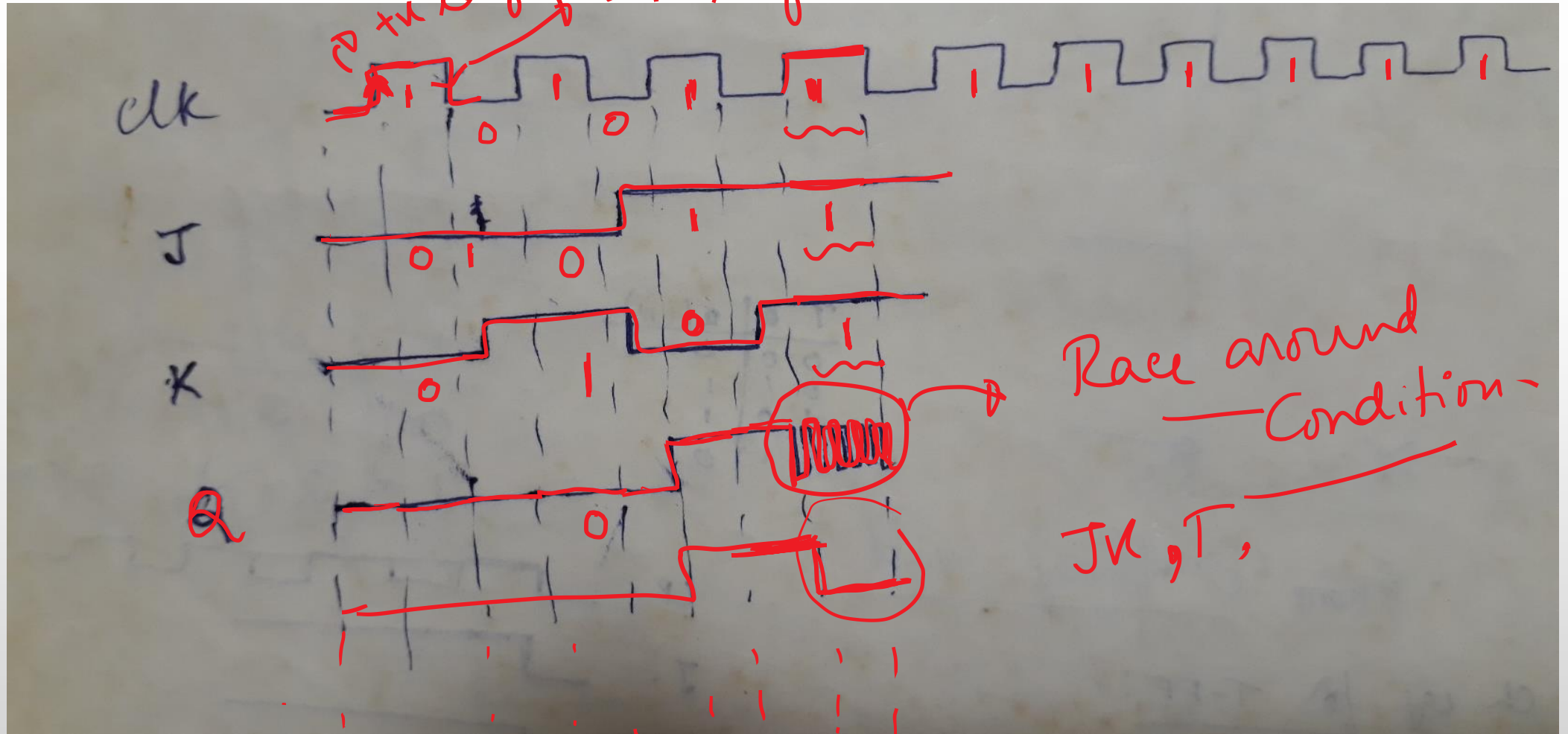


SEQUENTIAL CIRCUITS

- Race around condition
- Master slave model
- Flip flop conversion

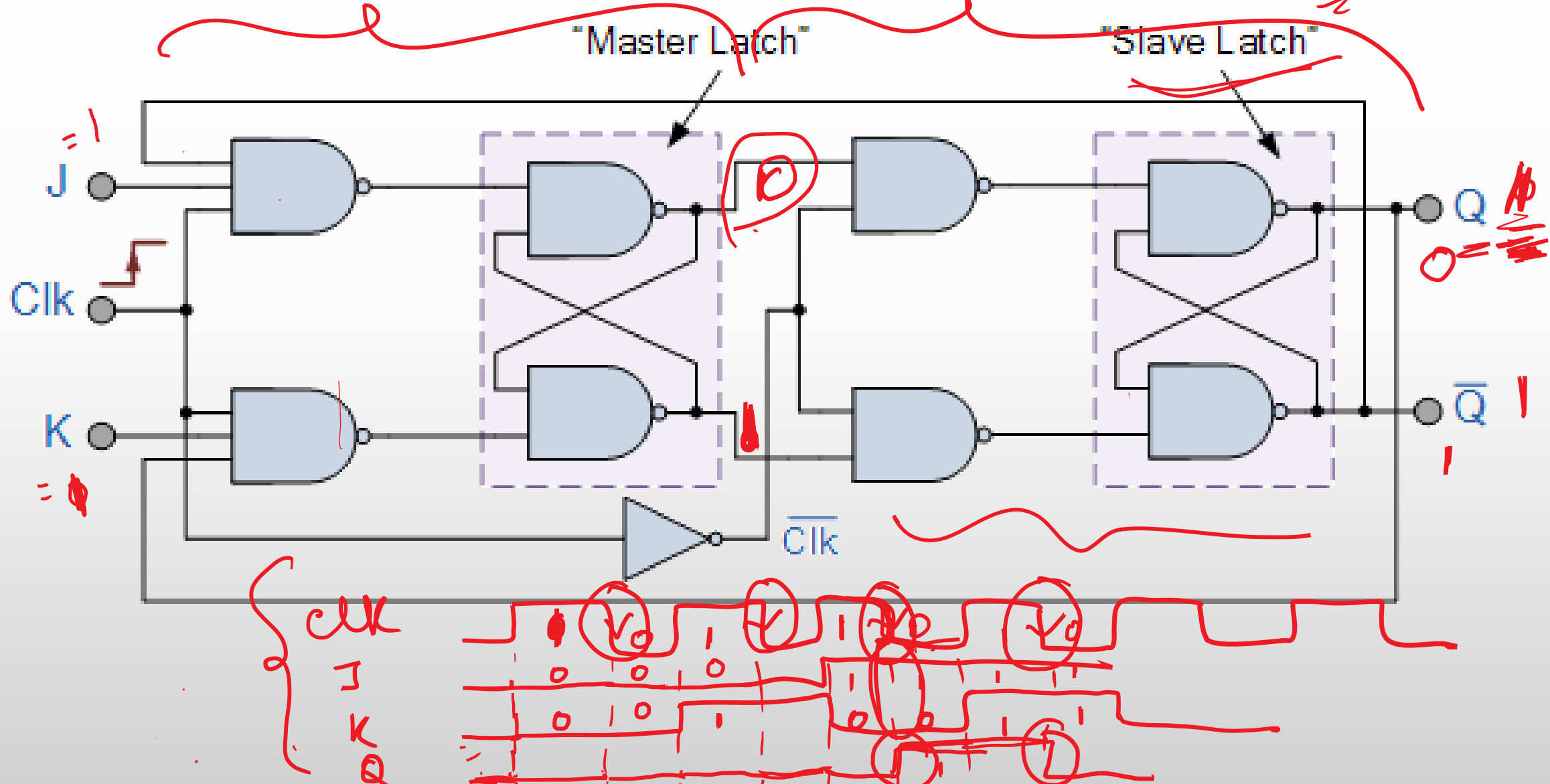
Race Around Condition

- For JK flip flop if J, K and Clock are equal to 1 the state of flip-flop keeps on toggling which leads to uncertainty in determining the output of the flip-flop. This problem is called **Race around the condition**.

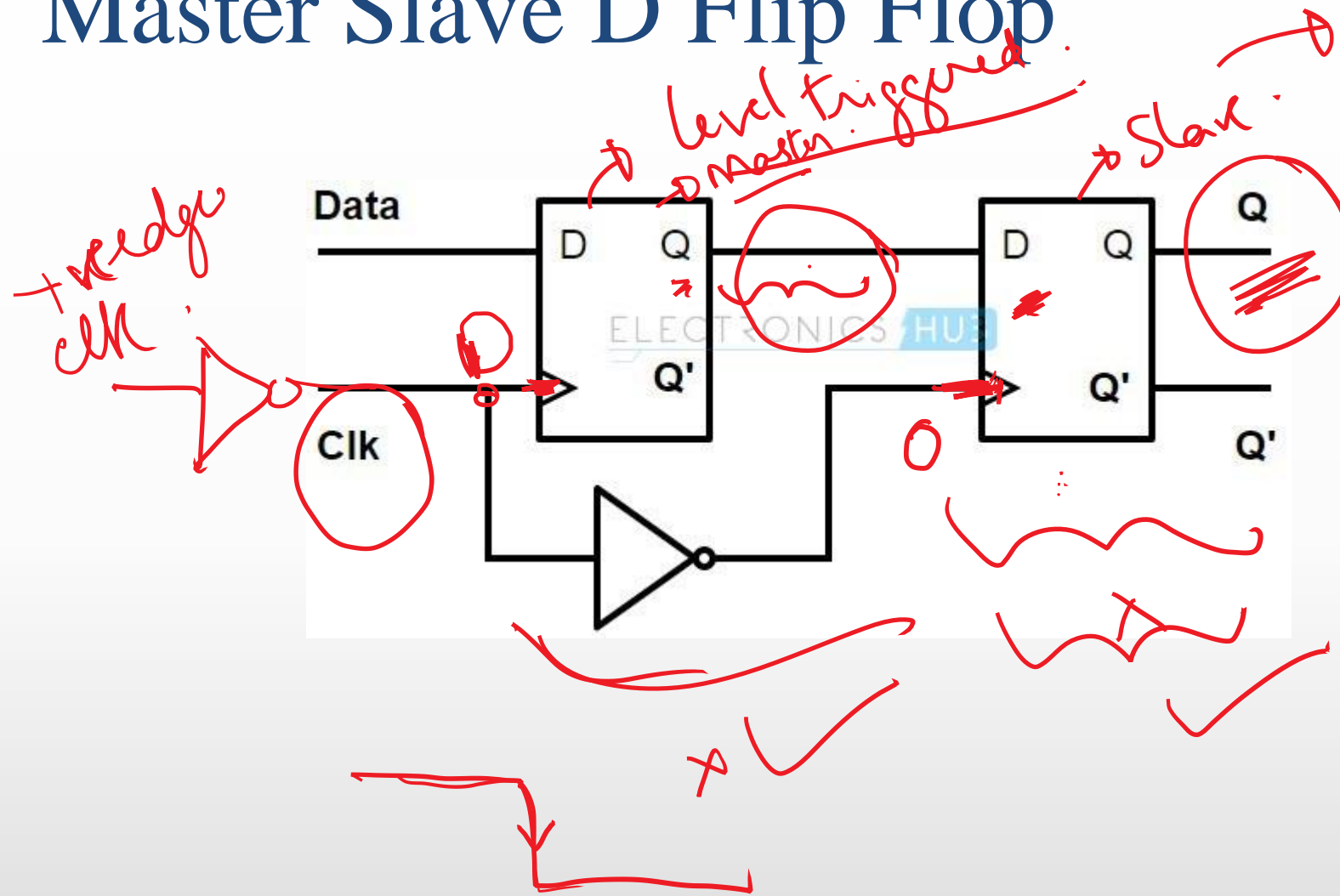


Master Slave JK Flip Flop

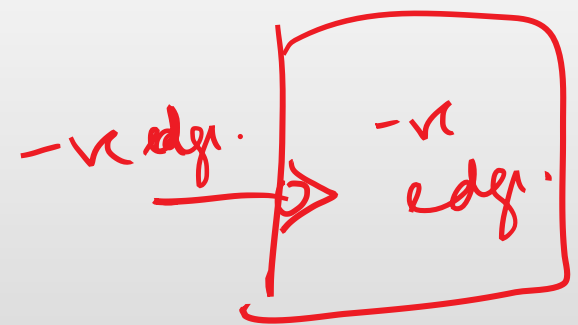
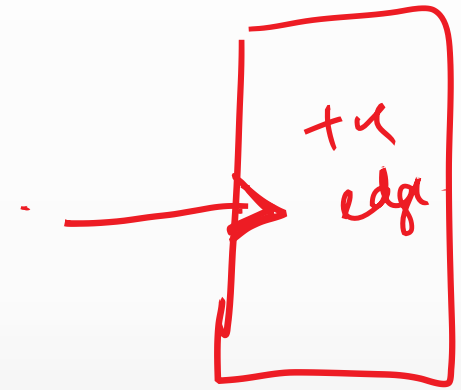
JK-FF - with edge trigger



Master Slave D Flip Flop



-ve edge.



Flip Flop Conversion

1. Design a T Flip Flop using D Flip Flop

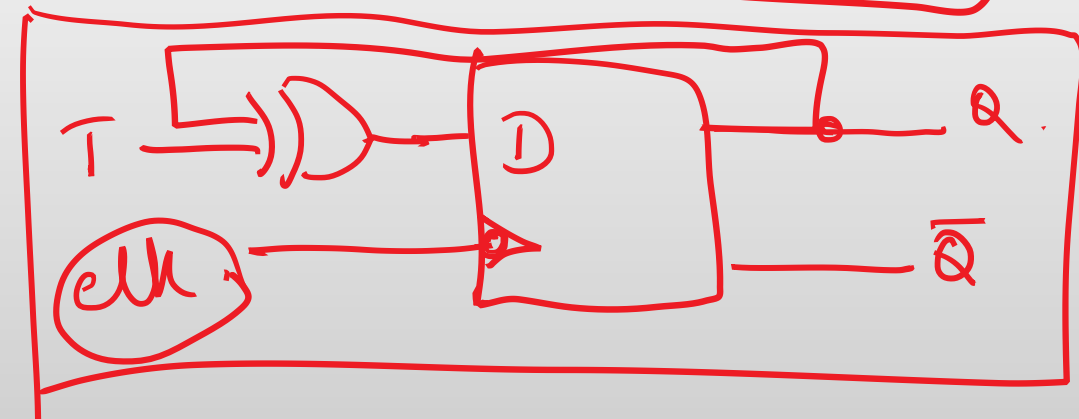


D:-

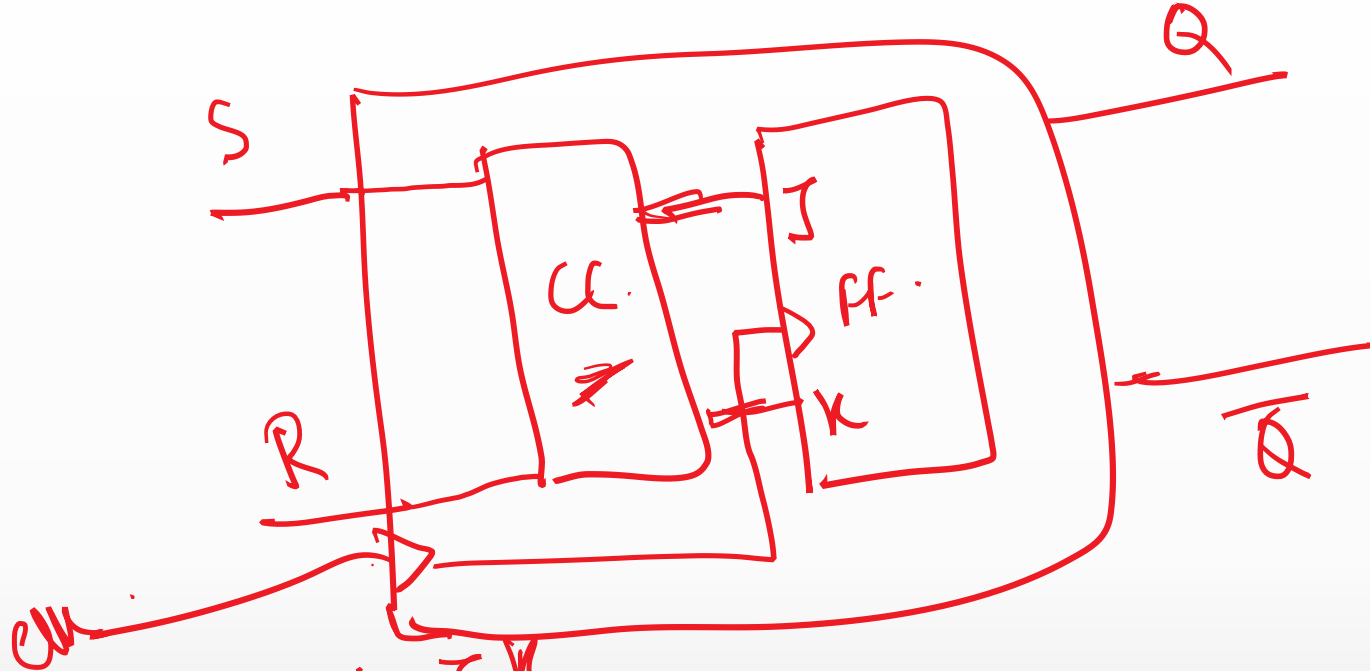
T \ Q	0	1
0	0	1
1	1	0

$$D = T \oplus Q(t)$$

T	$Q(t)$	$Q(t+1)$	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0



2. Convert a given JK flip flop to work as SR flip flop



	J	K	Q(t)	Q(t+1)
0 → 0	0	0	0	0
	0	1	0	0
	1	0	0	1
	1	1	0	0
0 → 1	0	0	1	1
	0	1	1	1
	1	0	1	0
	1	1	1	1

S	R	Q(t)	Q(t+1)	J	K
0	0	0	0	0	x
0	0	1	1	x	0
0	1	0	0	0	x
0	1	1	0	x	1
1	0	0	1	x	0
1	0	1	1	x	0
1	1	0	x	x	x
1	1	1	x	x	x

PTQ SR
JK
FF

$S=R=1 \Rightarrow$ doesn't occur

S \ R(Q)	00	01	10	11
0	0	X	X	0
1	1	X	X	X

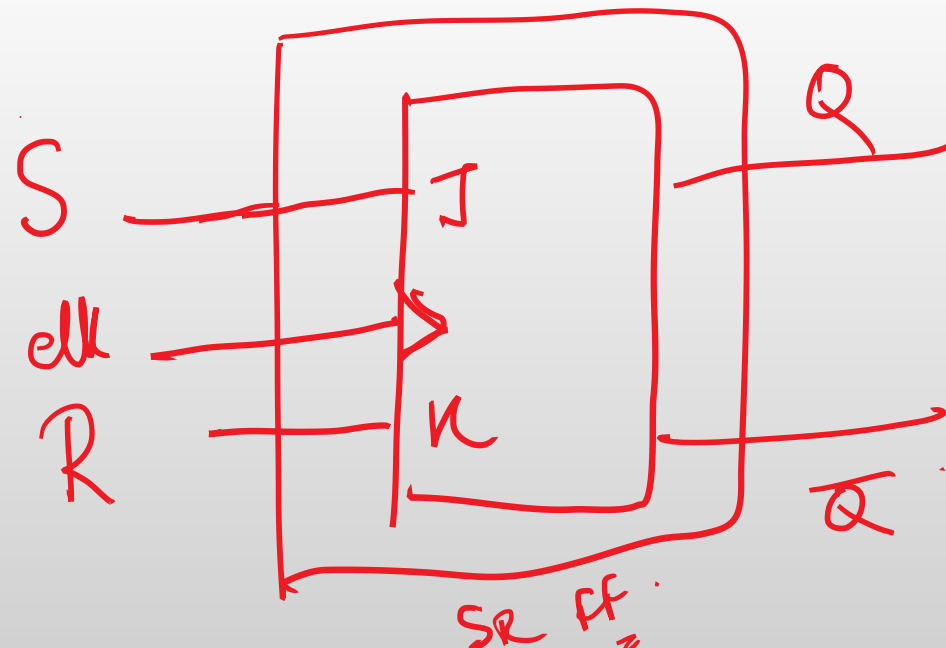
Diagram showing a Karnaugh map for the SR flip-flop. The map is a 2x4 grid. The top row is labeled 0 and the bottom row is labeled 1. The columns are labeled 00, 01, 10, and 11. The cells contain 0, X, X, 0 for the top row and 1, X, X, X for the bottom row. A circle is drawn around the bottom row (S=1), indicating that Q = S.

$Q = S$

S \ R(Q)	00	01	11	10
0	X	0	1	X
1	X	0	X	X

Diagram showing a Karnaugh map for the SR flip-flop. The map is a 2x4 grid. The top row is labeled 0 and the bottom row is labeled 1. The columns are labeled 00, 01, 11, and 10. The cells contain X, 0, 1, X for the top row and X, 0, X, X for the bottom row. A circle is drawn around the top-right 2x2 area (R=1), indicating that Q = R.

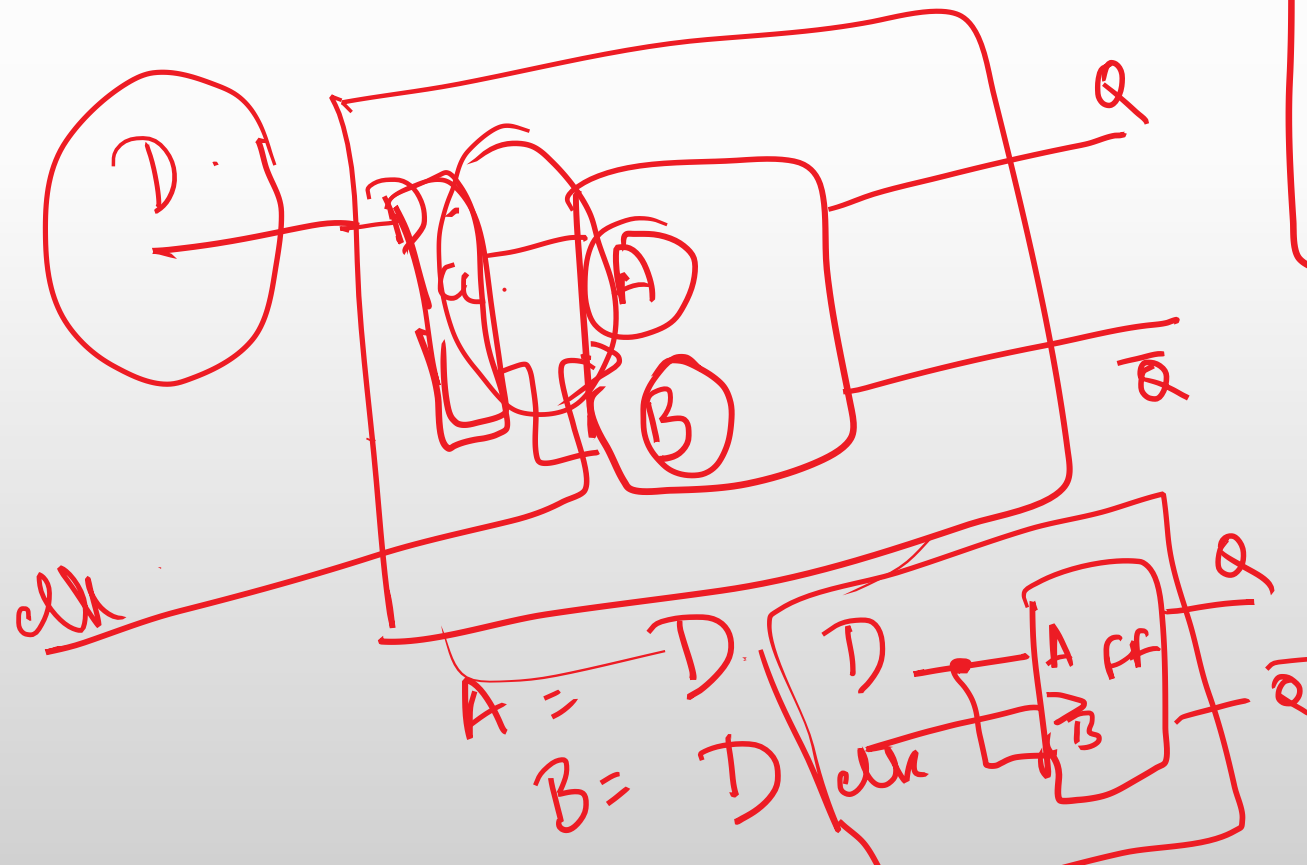
$Q = R$



3. Design a D flip flop using an AB flip flop whose function table is given below.

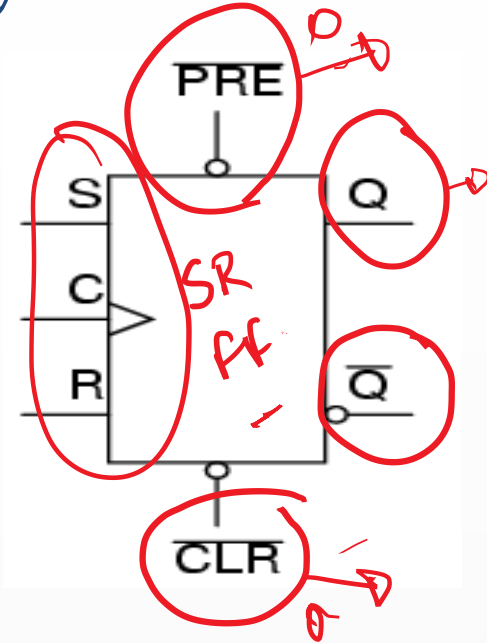
A	B	Output
0	0	RESET
0	1	No Change
1	0	Toggle
1	1	SET

D	Q(t)	Q(t+1)	A	B
0	0	0	0	x
0	1	0	x	0
1	0	1	1	x
1	1	1	x	1



	A	B	
0 → 0	0	0	0x
	0	1	
0 → 0	0	0	x0
	1	0	
0 → 1	1	0	1x
	1	1	

Asynchronous Inputs:



2 - Asyn inputs

PRE (SET)

CLR (RESET)

PRESET	CLEAR	FF Response
0	0	Indeterminate
0 ✓	1 ✓	SET ✓ $Q = 1$
1	0 ✓	CLEAR ✓ $Q = 0$
1 ✓	1 ✓	Clocked operation

