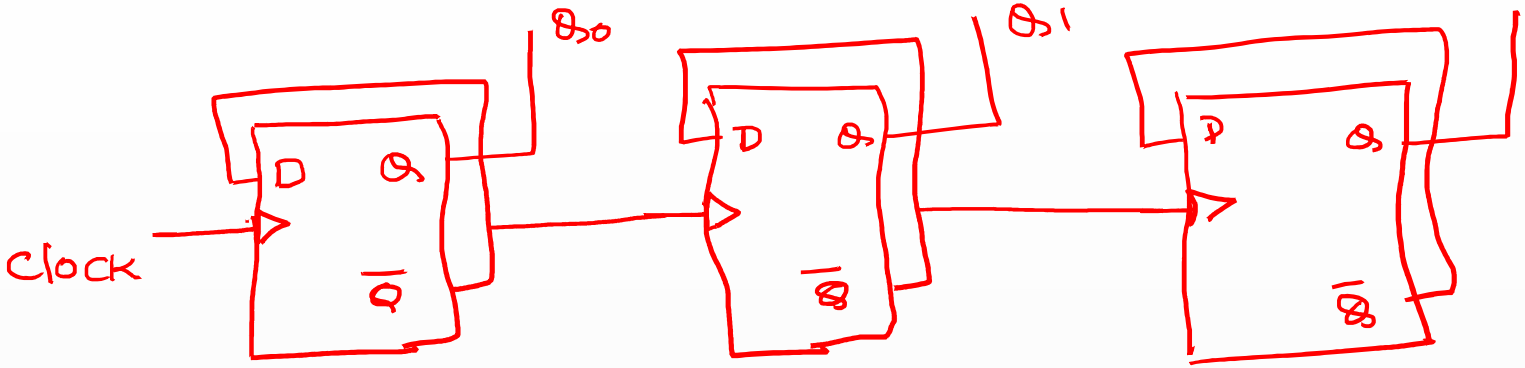
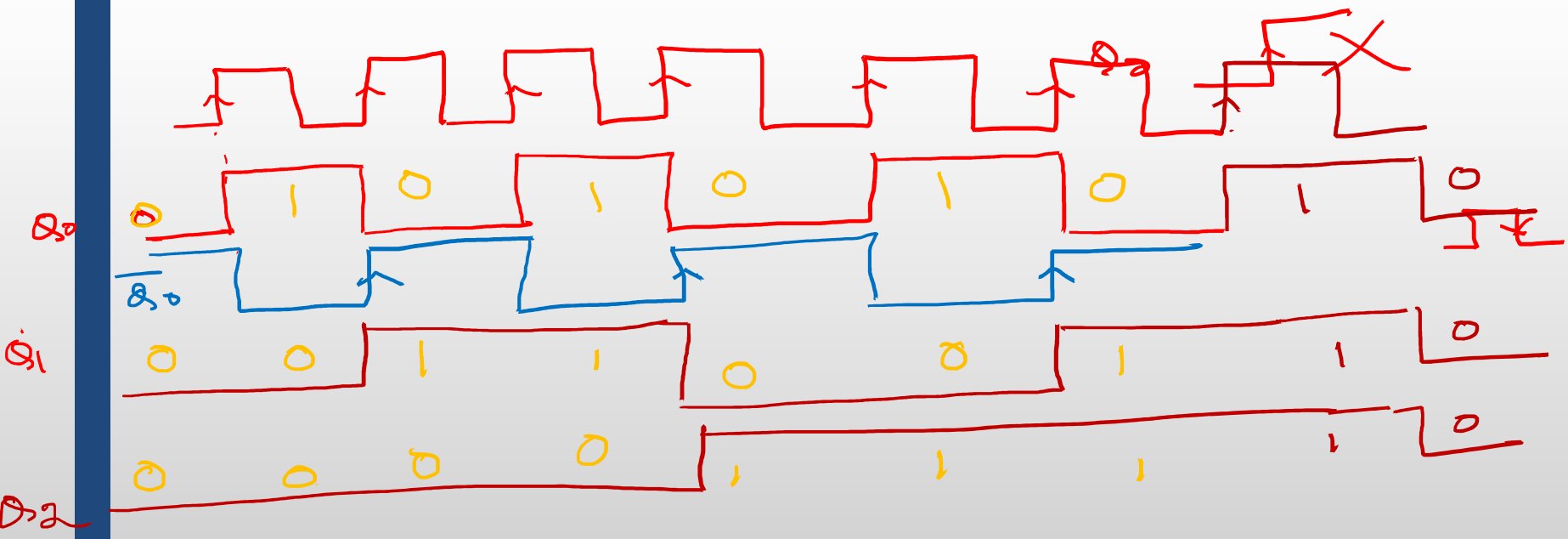
ASYNCHRONOUS COUNTER(RIPPLE COUNTER)

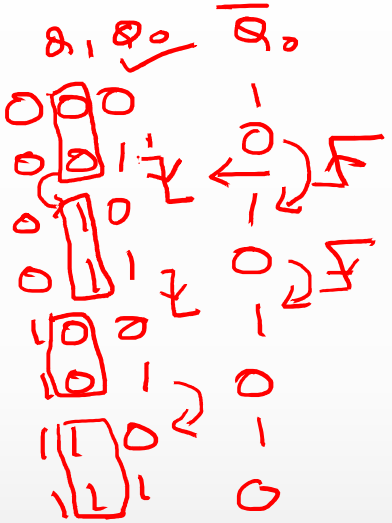
Counters:

- Register that goes through prescribed sequence of states upon the application of input pulses is called a counter.
- There are 2 types of counters:
  - *Asynchronous counters (Ripple counters) :* Clock inputs are triggered by transitions of other flipflop.
  - *Synchronous counters :* The clock inputs of all flip flops receive common clock.

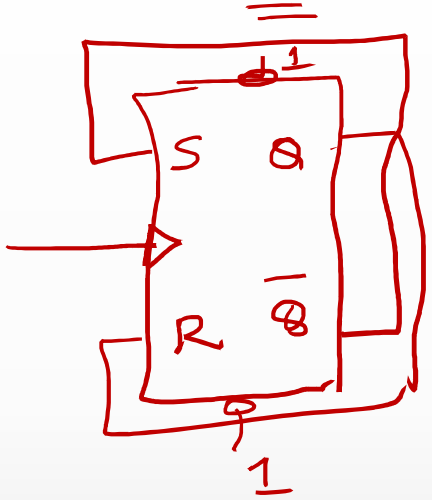
- Design a 3 – bit Asynchronous UP counter using positive edge triggered D flip flops.







- Design a 4 – bit (MOD 16/ Divide by 16) Asynchronous UP counter using negative edge triggered SR flip flops.
- Design a 4 – bit Asynchronous UP counter using positive edge triggered SR flip flops.

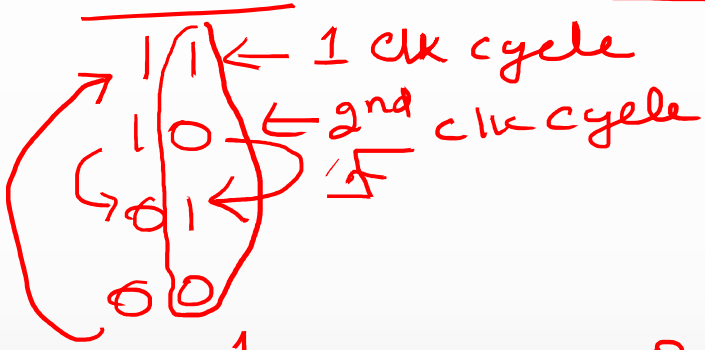


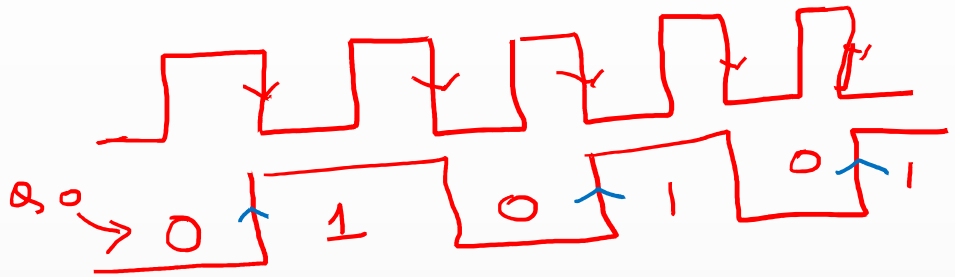
DOWN COUNTERS

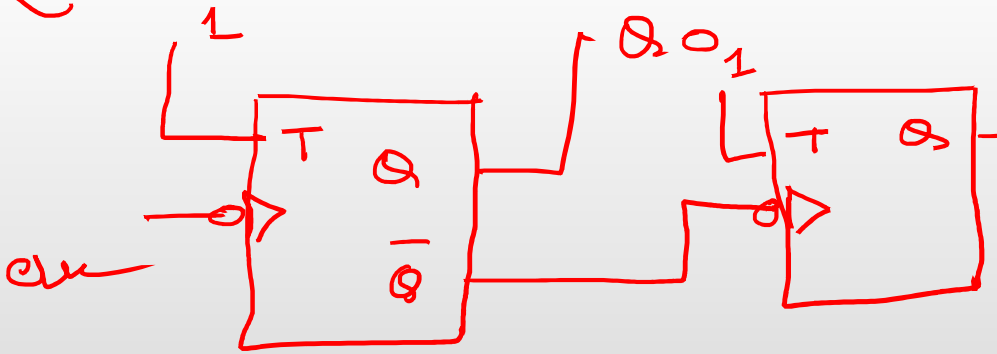
MOD 4 down ⇒ 2-bit

−ve edge triggered (JK, T, SR, D)

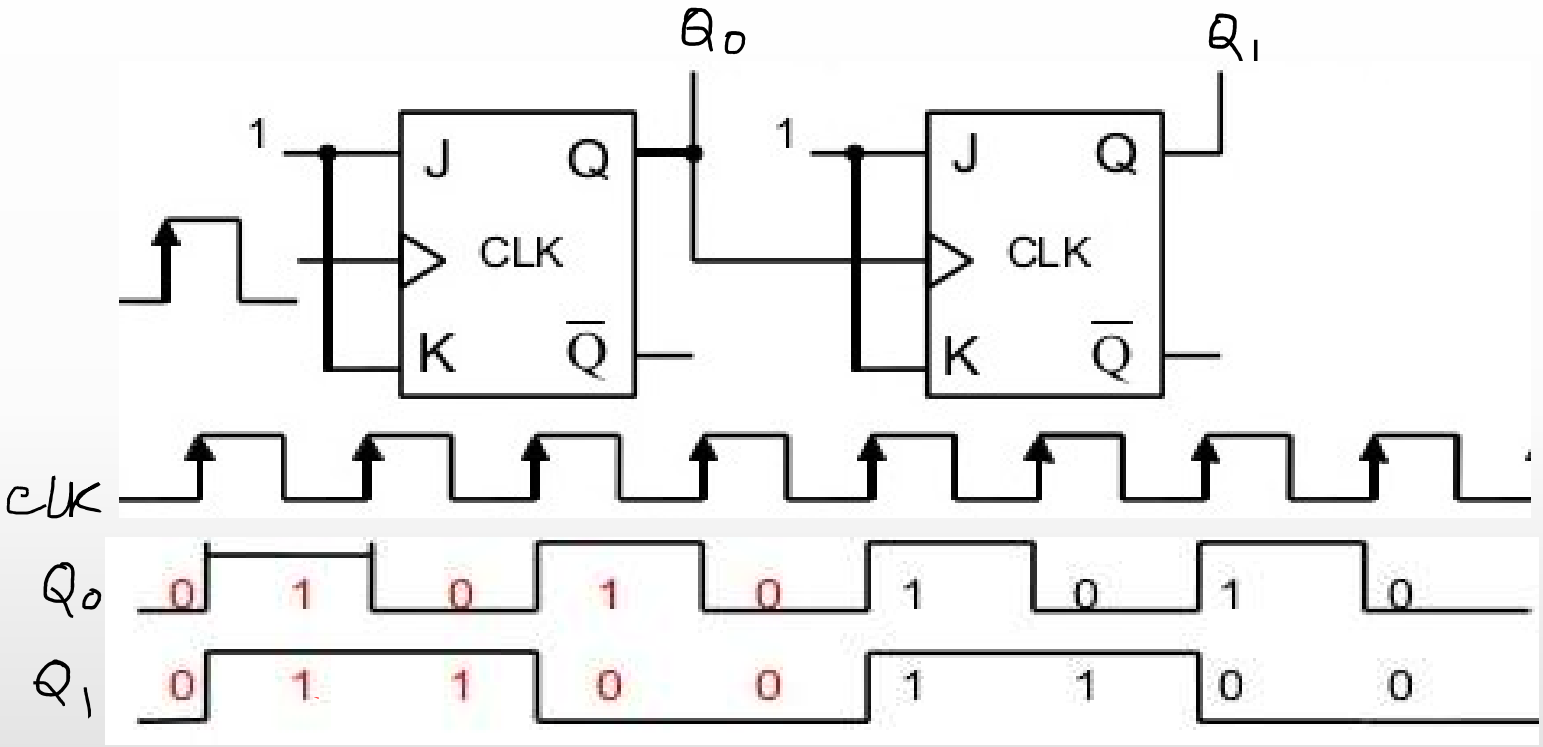
$Q_1\ Q_0$



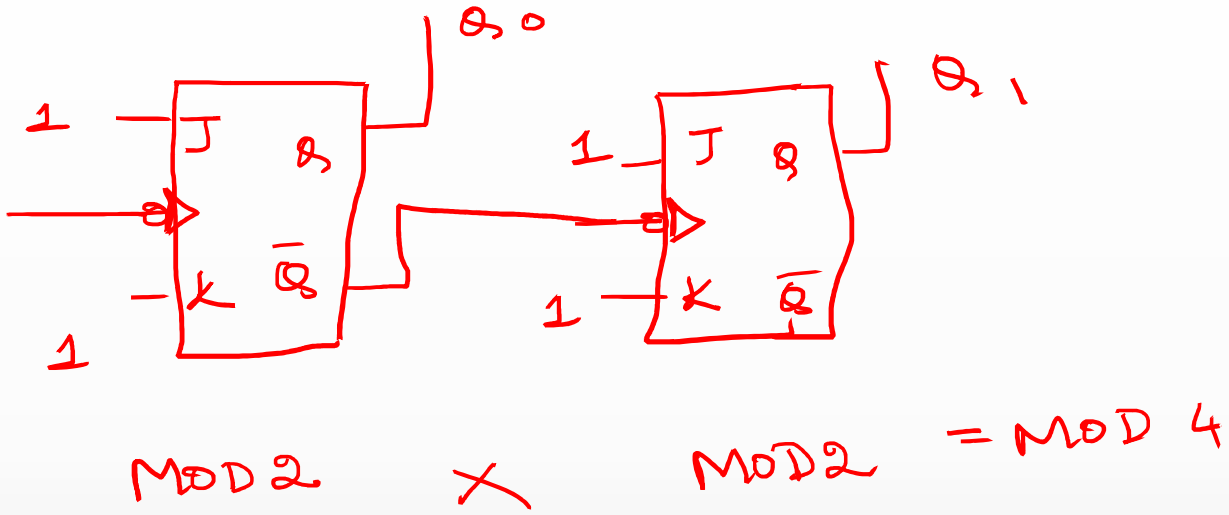




- Design a 2 – bit Asynchronous DOWN counter using positive edge triggered JK flip flops.



- Design a 2 – bit Asynchronous DOWN counter using negative edge triggered JK flip flops.

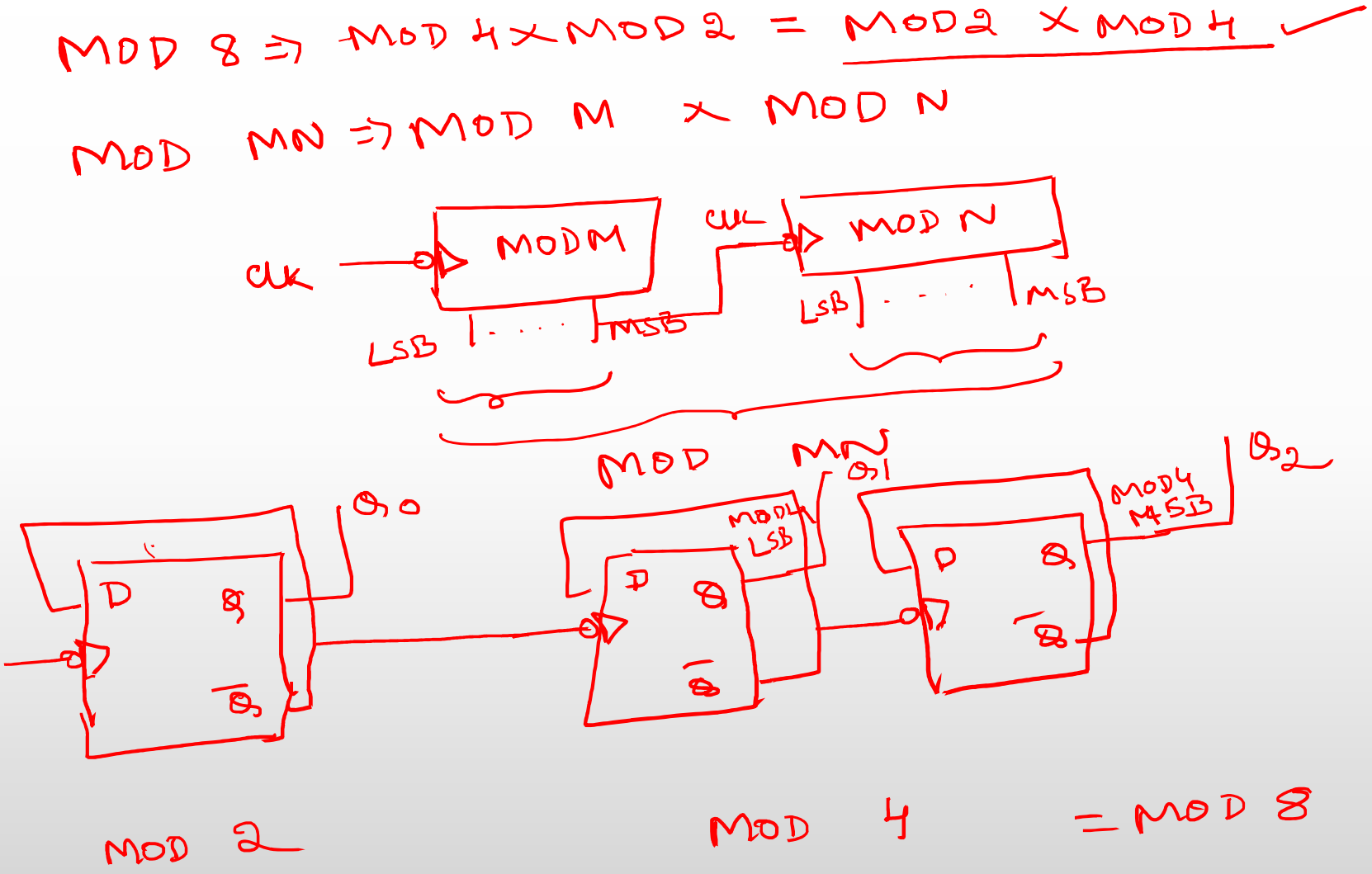


- Design a 2 – bit Asynchronous DOWN counter using negative edge triggered T flip flops.

- Design a 2 – bit Asynchronous DOWN counter using positive edge triggered T flip flops.

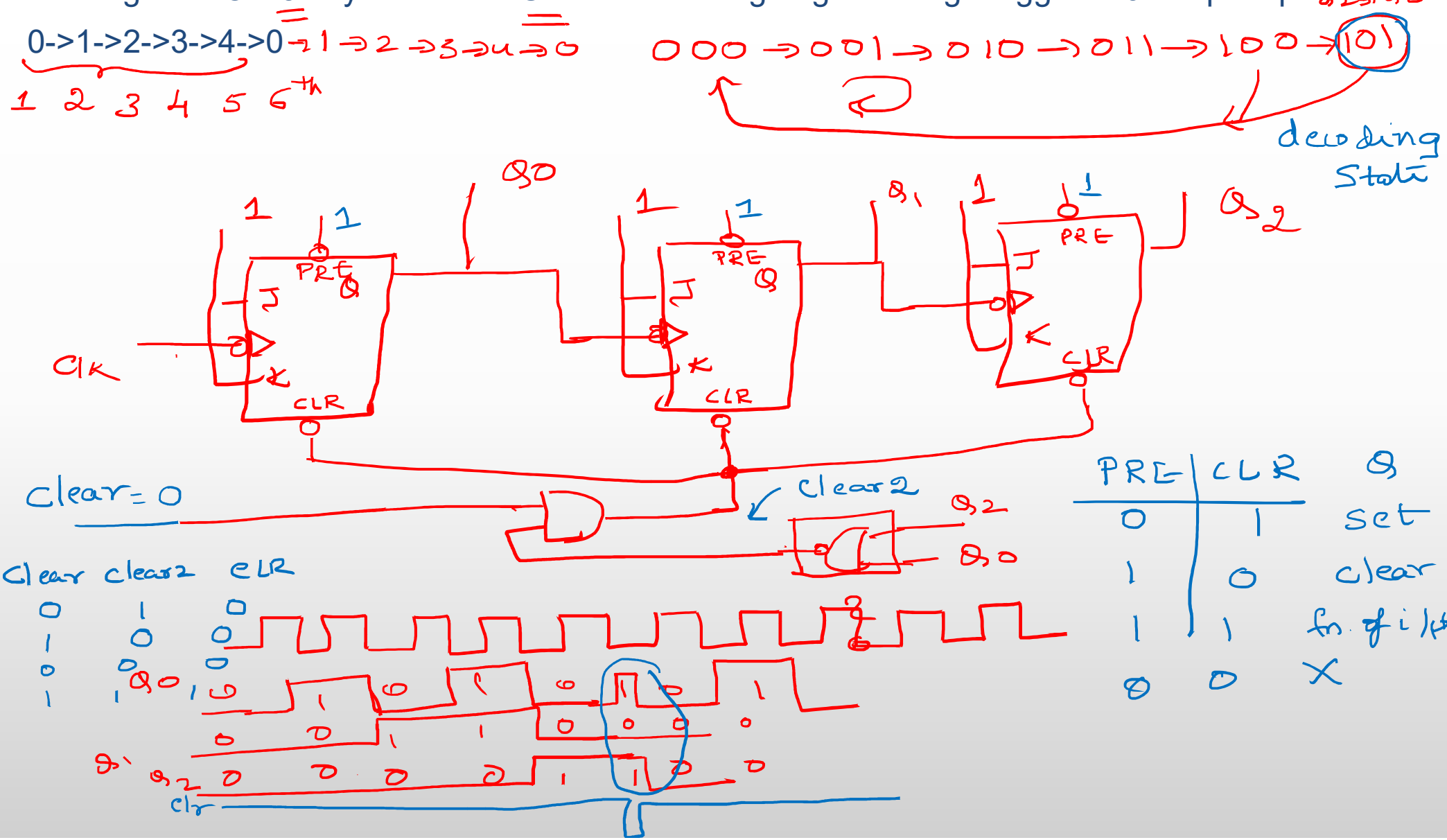
Draw the circuit

- Design a 3 – bit Asynchronous DOWN counter using negative edge triggered D flip flops.



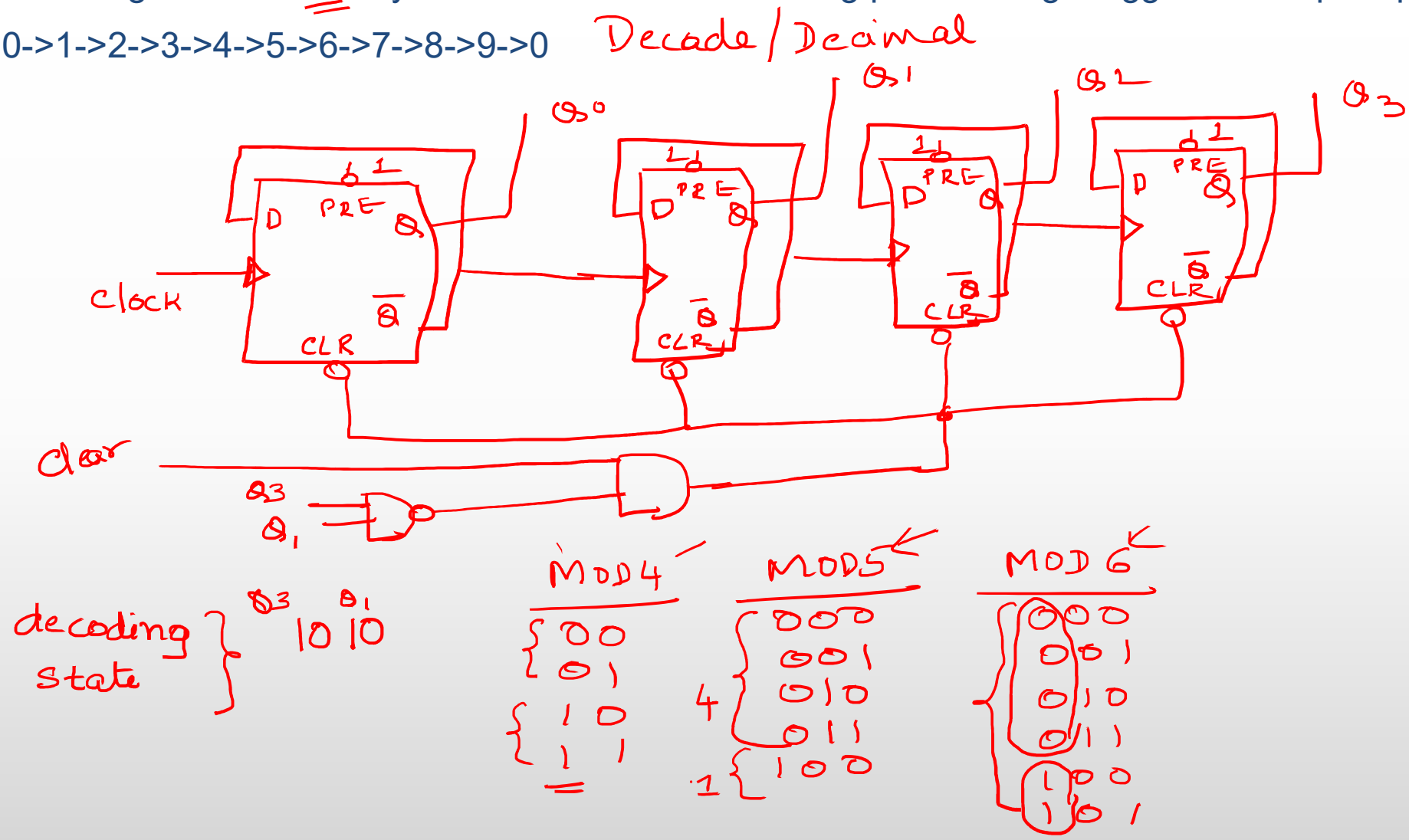
- Design a 3 – bit Asynchronous DOWN counter using positive edge triggered D flip flops.

- Design a MOD 5 Asynchronous UP counter using negative edge triggered JK Flip Flops



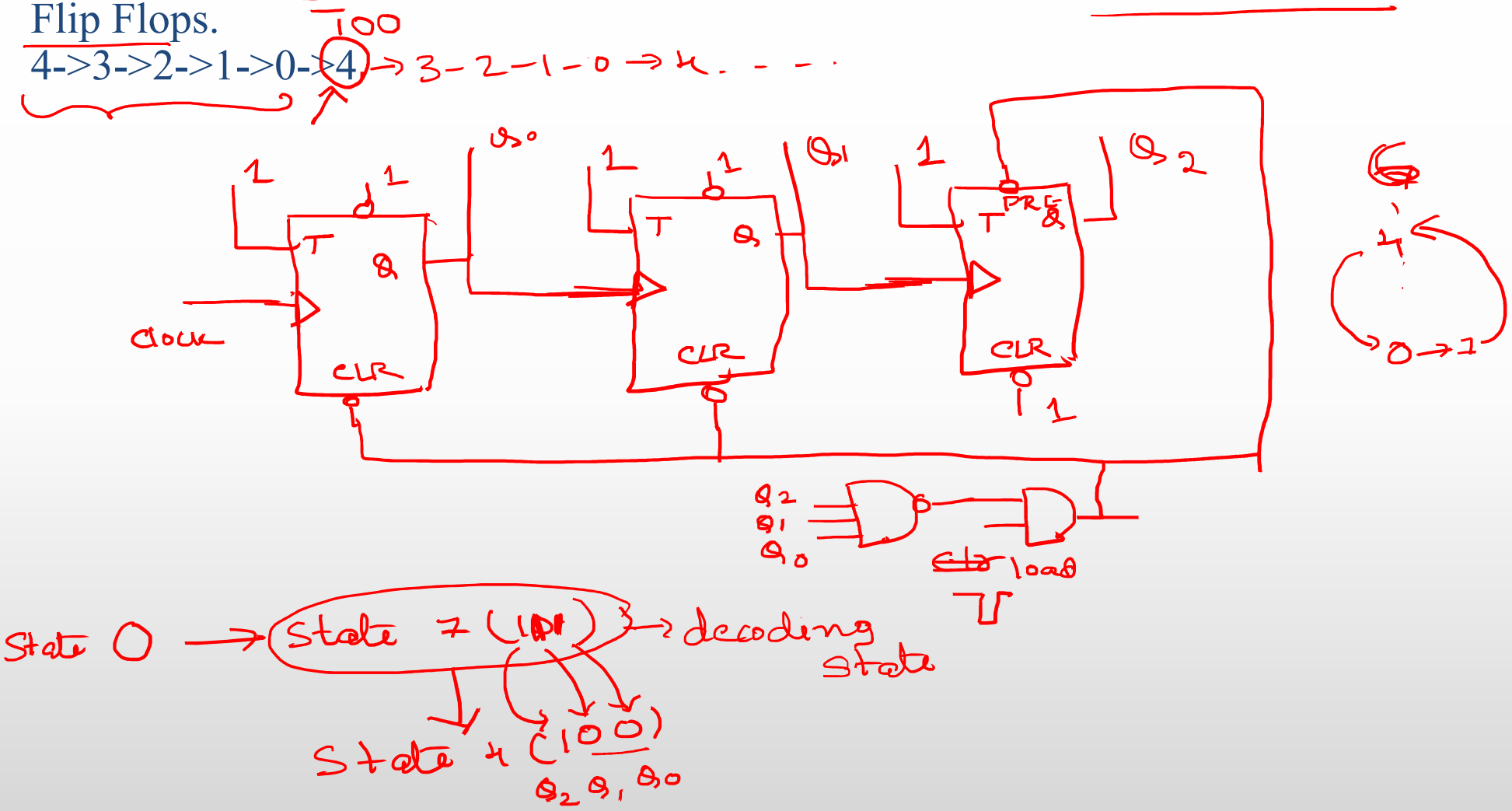
- Design a MOD 10 Asynchronous UP counter using positive edge triggered D Flip Flops.

0->1->2->3->4->5->6->7->8->9->0



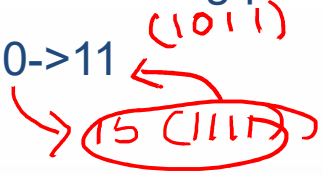
Design a MOD 5 Asynchronous DOWN counter using positive edge triggered T Flip Flops.

4->3->2->1->0->4



- Design a MOD 12 Asynchronous DOWN counter using positive edge triggered T Flip Flops.

  11->10->9->8->7->6->5->4->3->2->1->0->11



- Design a MOD 18 Asynchronous DOWN counter using positive edge triggered JK Flip Flops.

- Design a 3 bit Asynchronous UP/DOWN counter using negative edge triggered JK Flip Flops.

Design a counter to obtain a 1KHz clock signal from a 10KHz clock signal with 50% duty cycle using negative edge triggered JK Flip Flops.

UP counter

Square

$Q_2 Q_1 Q_0$ Q_3

MOD 10 = MOD 5 × MOD 2 , 4 ffs.

Dec. count	Q_3 Q_2 Q_1 Q_0	clk cycle
0	0 000	1
1	0 001	2
2	0 010	3
3	0 011	4
4	0 100	5
8	1 000	6
9	1 001	7
10	1 010	8
11	1 011	9
12	1 100	10

0 000

001

⋮

Design a MOD 6 Asynchronous counter with 50% duty cycle using negative edge triggered D Flip Flops.

$$f_{output} = \frac{f_{clk}}{6}$$

MOD MN = MOD M x MOD N → $= 2^{power}$

$MN \neq 2^{power}$ $Q_1 Q_0$ Q_2

MOD6 = MOD 3 x MOD 2 → 50 %.

MOD 2 x MOD 3

$Q_2 Q_1 Q_0$

0	0	0	0
1	0	0	1
2	0	1	0
4	1	0	0
5	1	0	1
6	1	1	0
	0	0	0

MOD 6

MOD3 MOD 2

$Q_2 Q_1$ Q_0

0	0	0 – 0
0	1	1 – 1
1	0	2 – 2
0	0	3 – 3
0	1	4 – 4
1	0	5 – 5
1	0	

MOD 3

0 0
0 1
1 0