SEQUENTIAL CIRCUITS

- Race around condition
- Mater slave model
- Flip flop conversion

Race Around Condition

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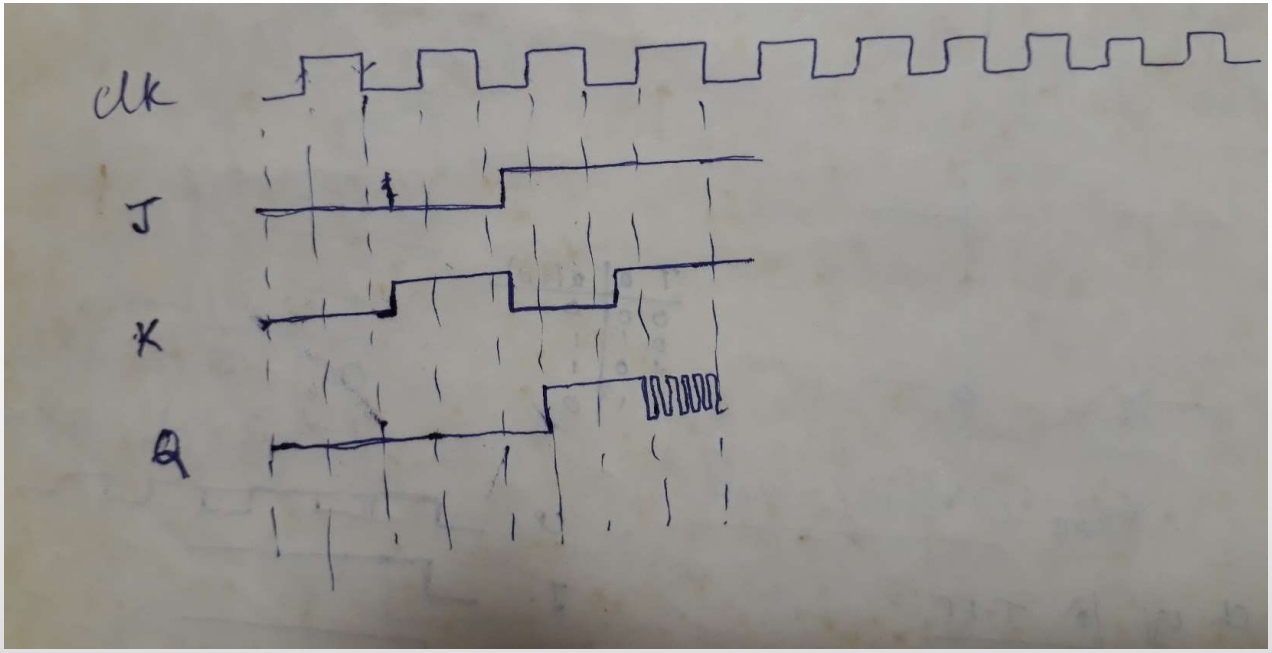
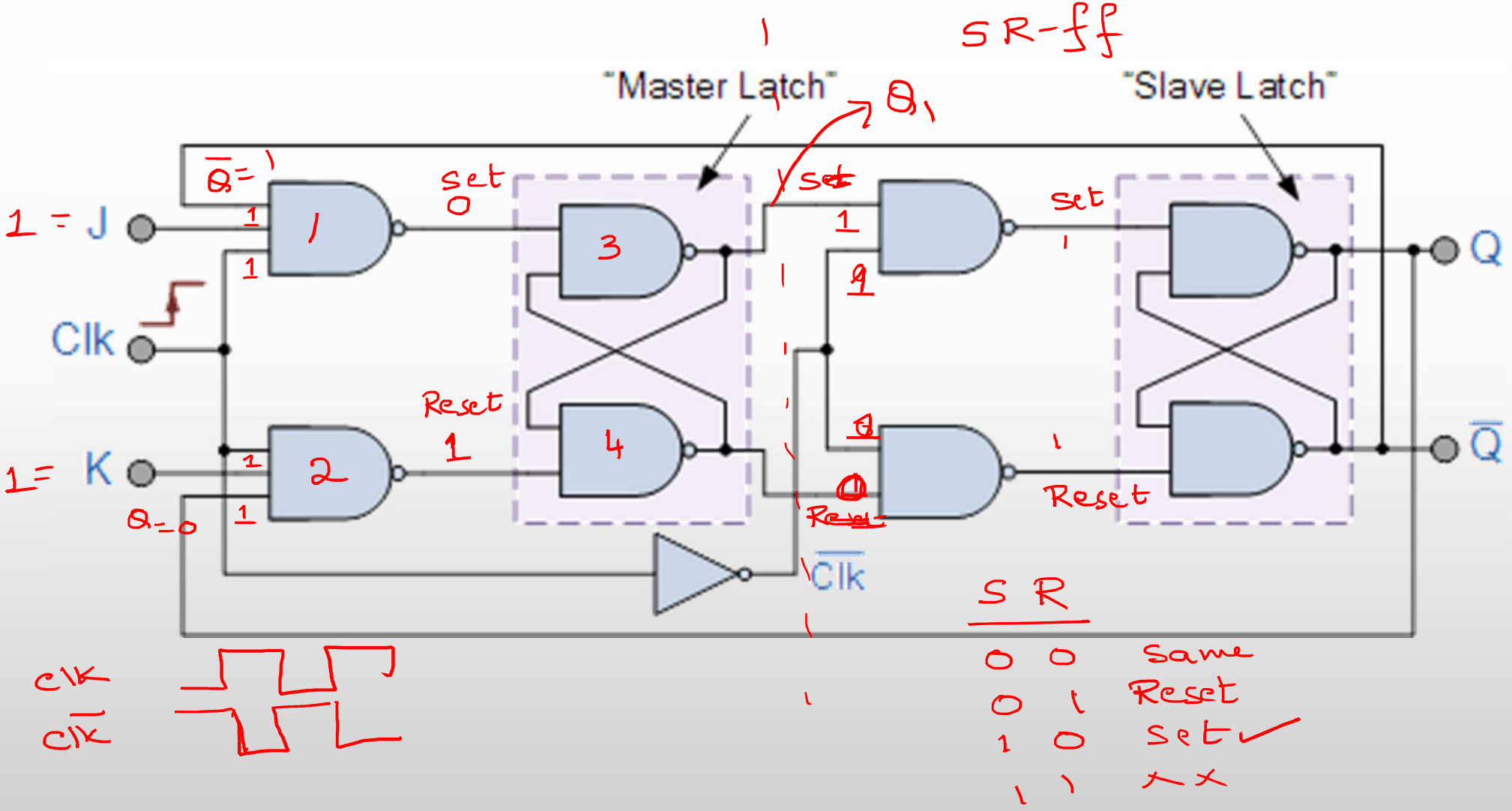


Master Slave JK Flip Flop



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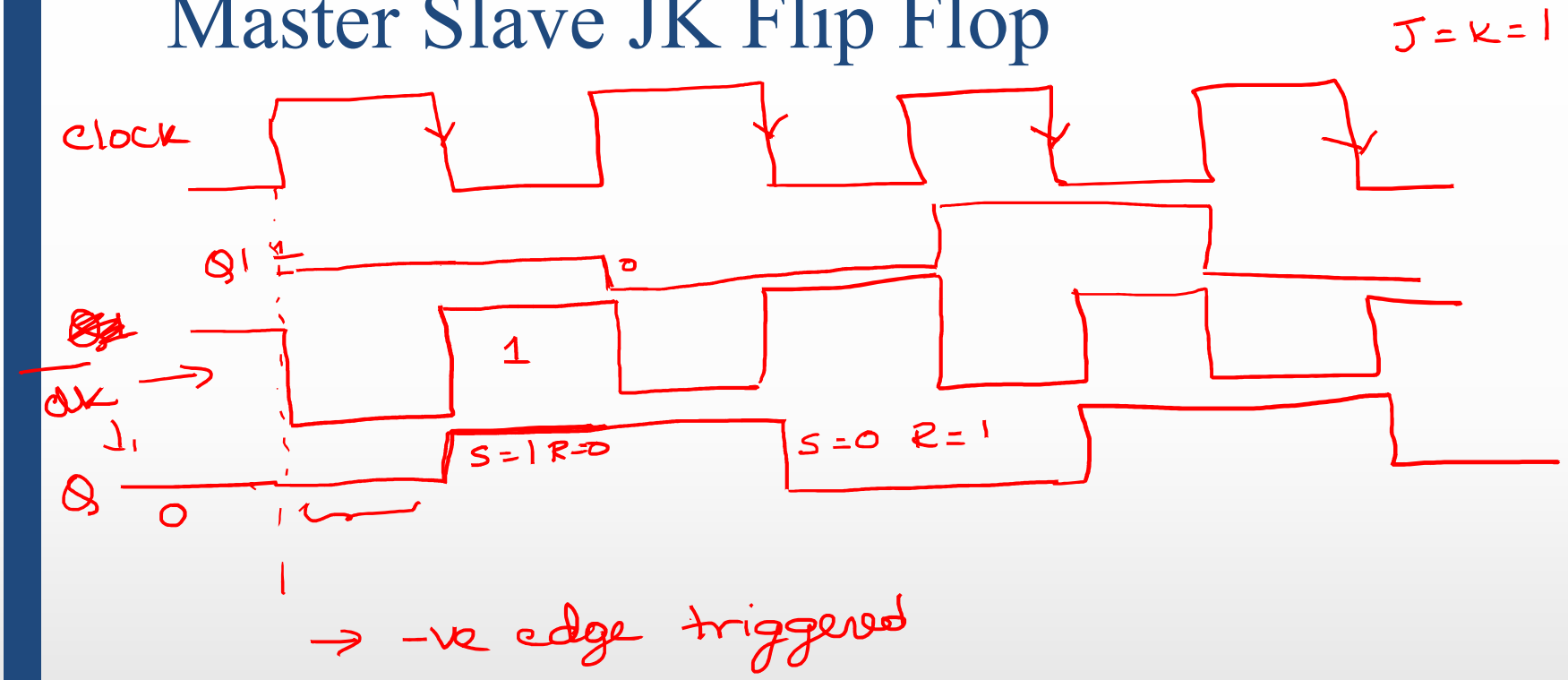
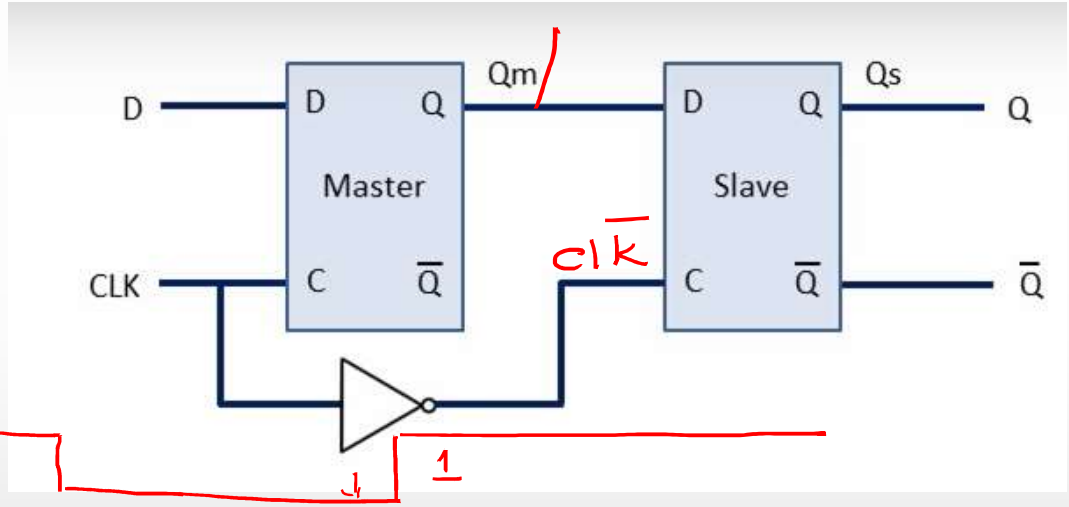
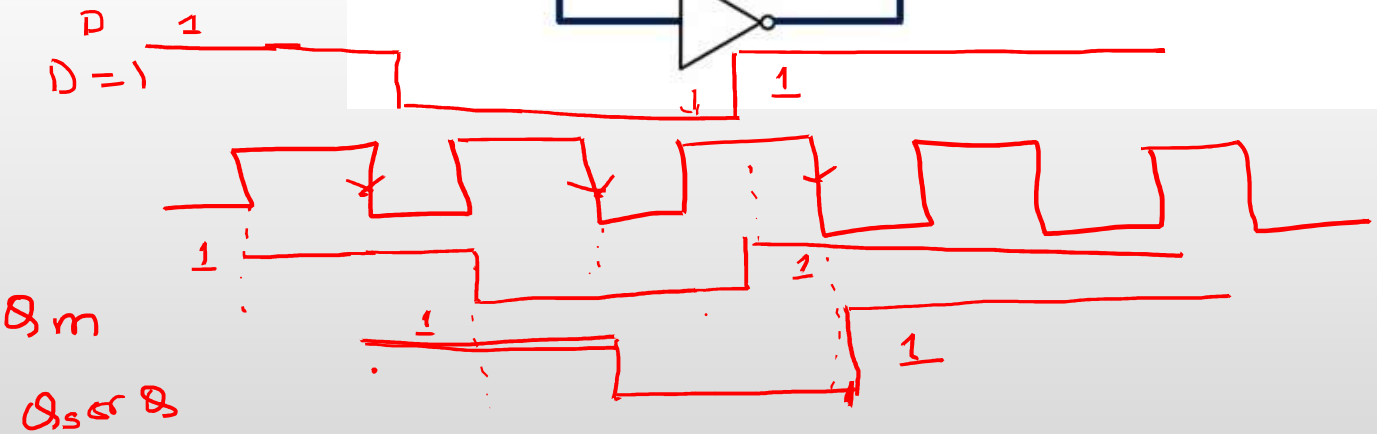


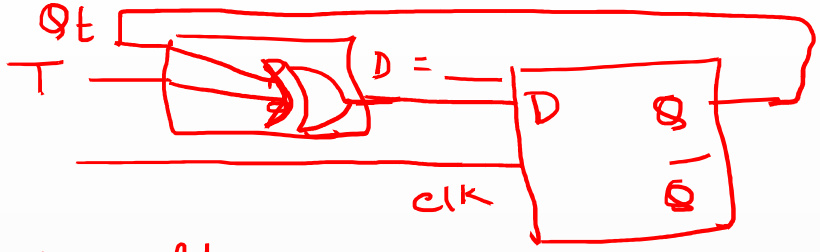
Master Slave D Flip Flop

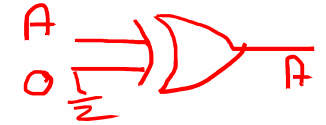


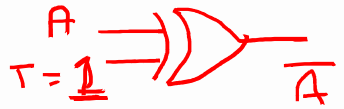


Flip Flop Conversion

1. Design a T Flip Flop using D Flip Flop







TT of T-ff.

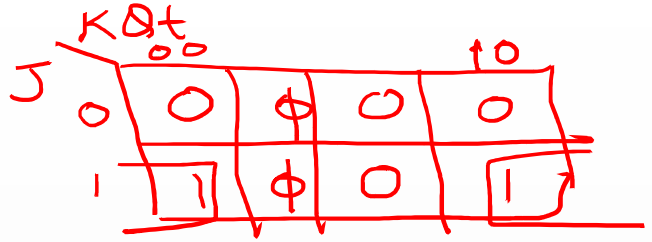
T	Q_t	Q_{t+1}	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

← Refer to excitation table of D-ff

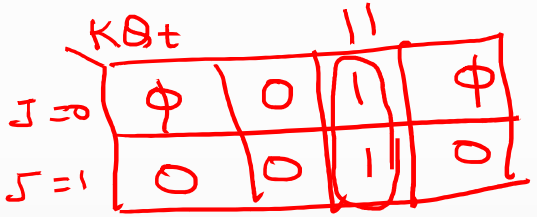
$D(T, Q_t) = T \oplus Q_t$

2. Convert a given SR flip flop to work as a JK flip flop

J	K	Q_t	Q_{t+1}	S	R
0	0	0	0	0	ϕ
0	0	1	1	ϕ	0
0	1	0	0	0	ϕ
0	1	1	0	ϕ	1
1	0	0	1	1	0
1	0	1	1	ϕ	0
1	1	0	1	1	0
1	1	1	0	0	1

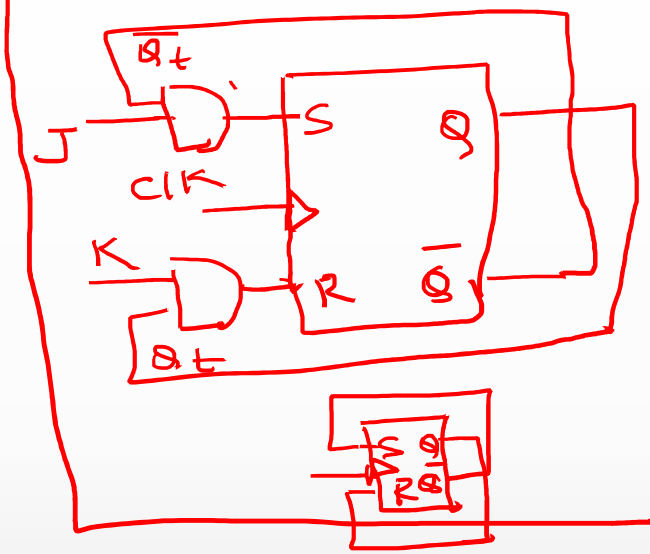


$S = J\overline{Q_t}$



$R = KQ_t$

Final ckt



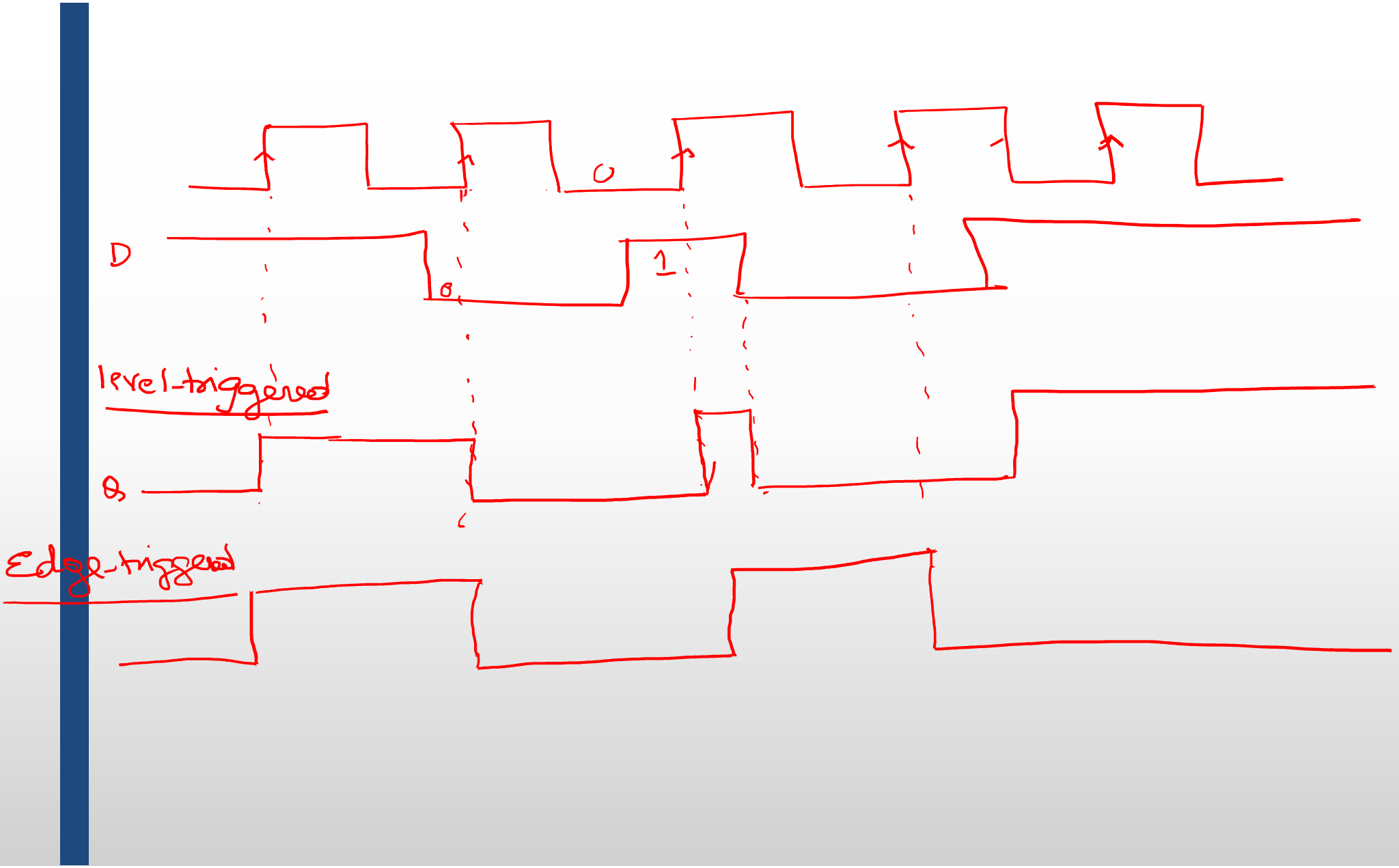
Toggle for every clk cycle

J	K	
0	0	No change
0	1	Reset
1	0	Set
1	1	Toggles

Excitation table of SR

Q_t	Q_{t+1}	S	R
0	0	0	ϕ
0	1	1	0
1	0	0	1
1	1	ϕ	0

S=0 R=0 / S=0 R=1
(No change/Reset)
Set S=1 R=0
S=0 R:0
(No change/set)

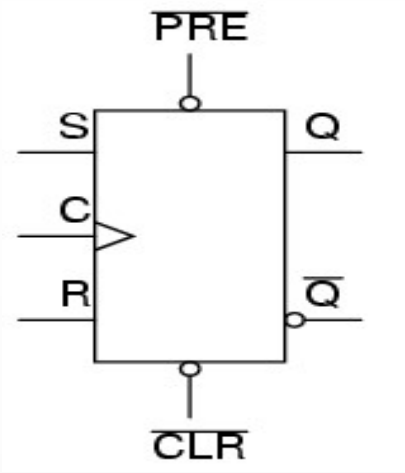

C
D
0
1
level-triggered
Q
Edge-triggered

3. Design a D flip flop using an AB flip flop whose function table is given below.

A	B	Output
0	0	RESET
0	1	No Change
1	0	Toggle
1	1	SET

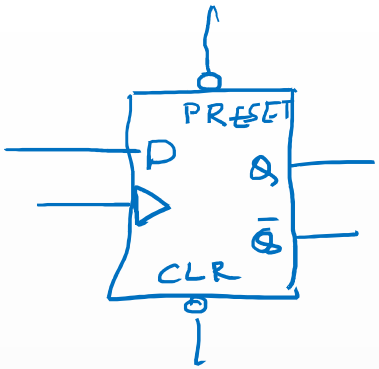
3. Design a D flip flop using an AB flip flop CONTD.

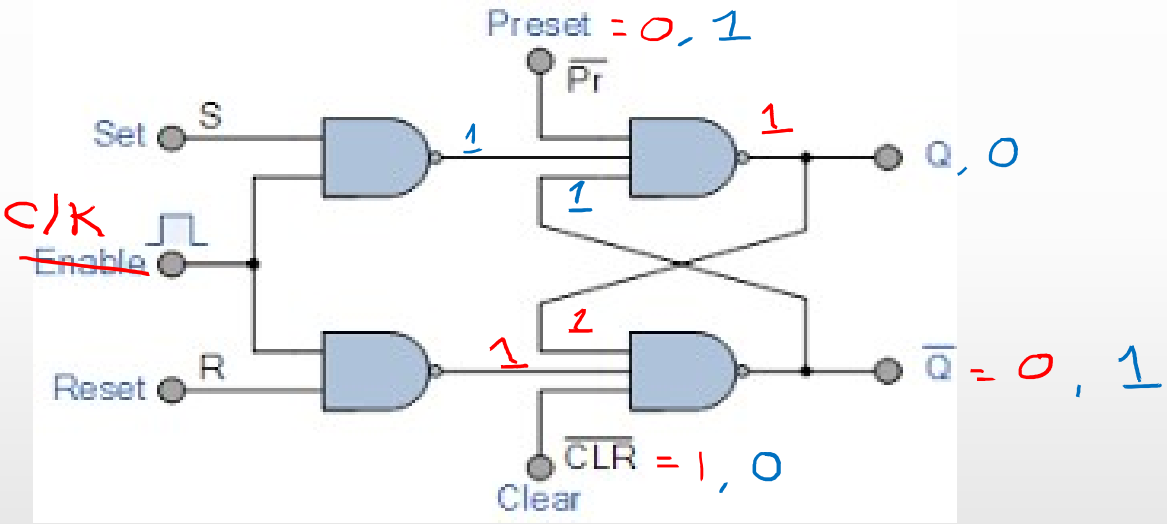
Asynchronous Inputs:



PRESET	CLEAR	FF Response
0	0	Indeterminate
0	1	SET
1	0	CLEAR
1	1	Clocked operation

Asynchronous Inputs:





- Any Questions?