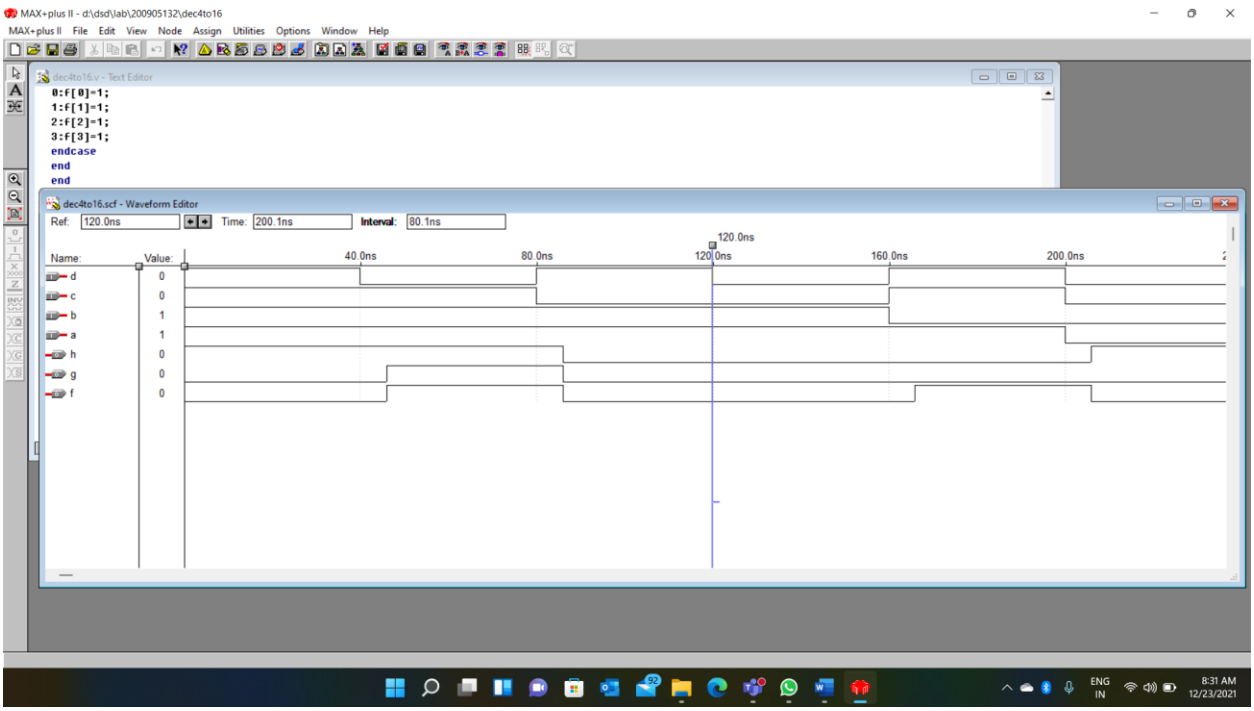
DSD LAB 5

1. Design and simulate a combinational circuit with external gates and a 4 to 16 decoder built using a decoder tree of 2 to 4 decoders to implement the functions below. F= ab'c + a'cd + bcd' , G=acd' + a'b'c and H=a'b'c' + abc + a'cd

   Solution:

```
module dec2to4(x,y,e,f);
input x,y,e;
output [3:0]f;
reg [3:0]f;
always@ (x or y)
begin
f=0;
if(e==1)
begin
case({x,y})
0:f[0]=1;
1:f[1]=1;
2:f[2]=1;
3:f[3]=1;
endcase
end
end
endmodule

module dec4to16(a,b,c,d,f,g,h);
input a,b,c,d;
output f,g,h;
wire [3:0]x;
wire [15:0]y;
dec2to4 stage0(a,b,1,x);
dec2to4 stage1(c,d,x[0],y[3:0]);
dec2to4 stage2(c,d,x[1],y[7:4]);
```

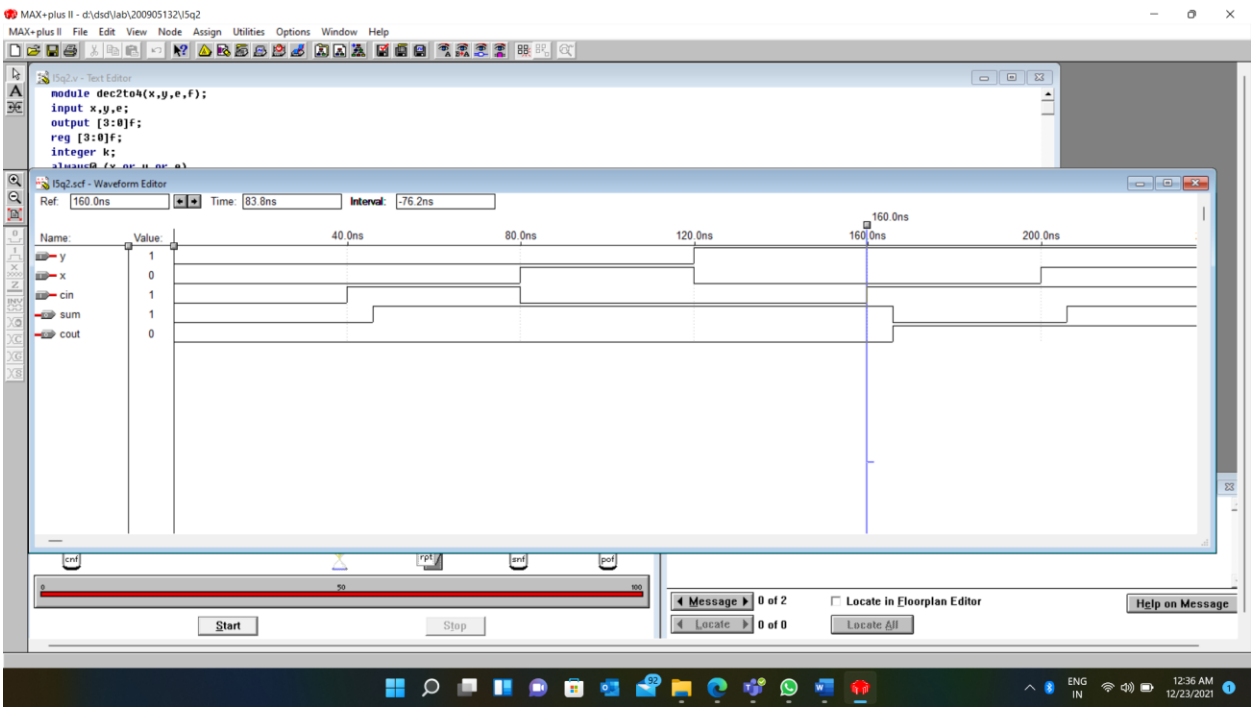
```
dec2to4 stage3(c,d,x[2],y[11:8]);
dec2to4 stage4(c,d,x[3],y[15:12]);
assign f=y[3]|y[6]|y[7]|y[10]|y[11]|y[14];
assign g=y[2]|y[3]|y[10]|y[14];
assign h=y[0]|y[1]|y[3]|y[7]|y[14]|y[15];
endmodule
```



2. Design and implement a full adder using 2 to 4 decoder(s) and other gates.

```
module dec2to4(x,y,e,f);
input x,y,e;
output [3:0]f;
reg [3:0]f;
integer k;
always@ (x or y or e)
begin
f=0;
if(e==1)
```

```
for(k=0;k<4;k=k+1)
if(k=={x,y})
f[k]=1;
end
endmodule

module l5q2(x,y,cin,cout,sum);
input x,y,cin;
output cout,sum;
wire [7:0]z;
dec2to4 stage0(y,cin,~x,z[3:0]);
dec2to4 stage1(y,cin,x,z[7:4]);
assign cout=z[3]|z[5]|z[6]|z[7];
assign sum=z[1]|z[2]|z[4]|z[7];
endmodule
```



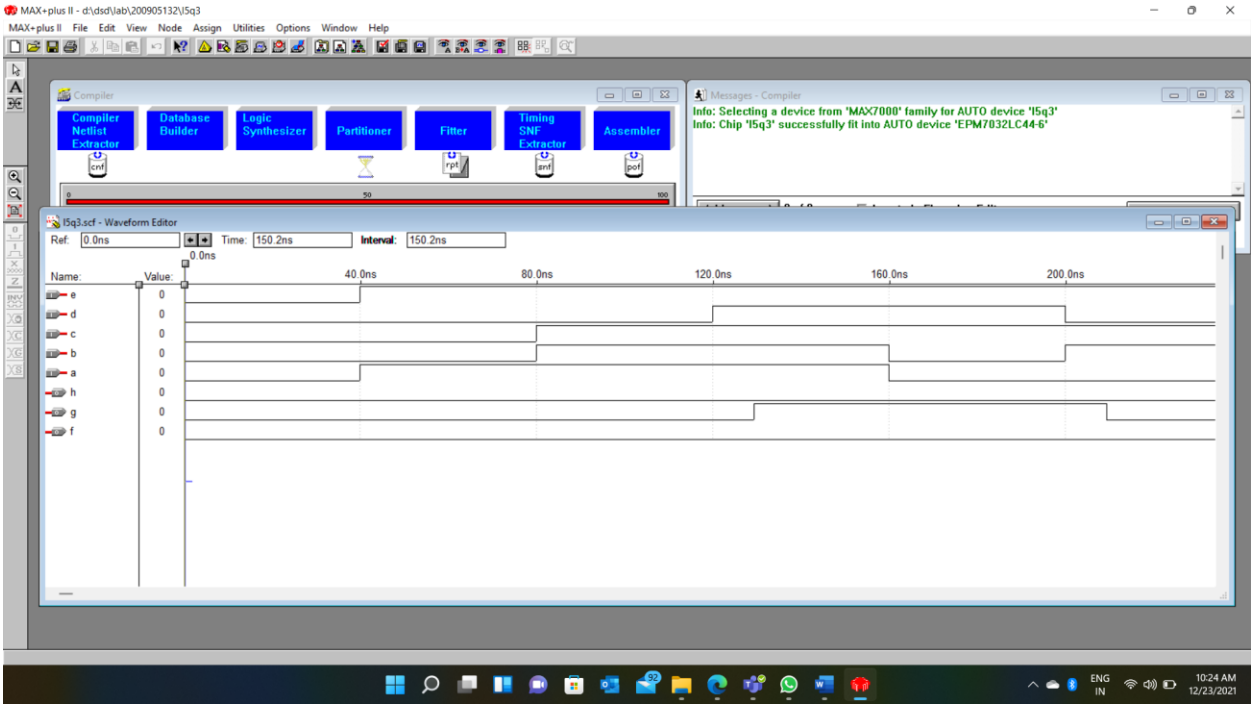
3. Design and simulate the circuit with 3 to 8 decoder(s) and external gates to implement the functions below.
F(a, b, c, d)= Σm(2,4,7,9) G (a, b, c, d)= Σm (0,3,15) H(a, b, c, d)= Σm(0,2,10,12)

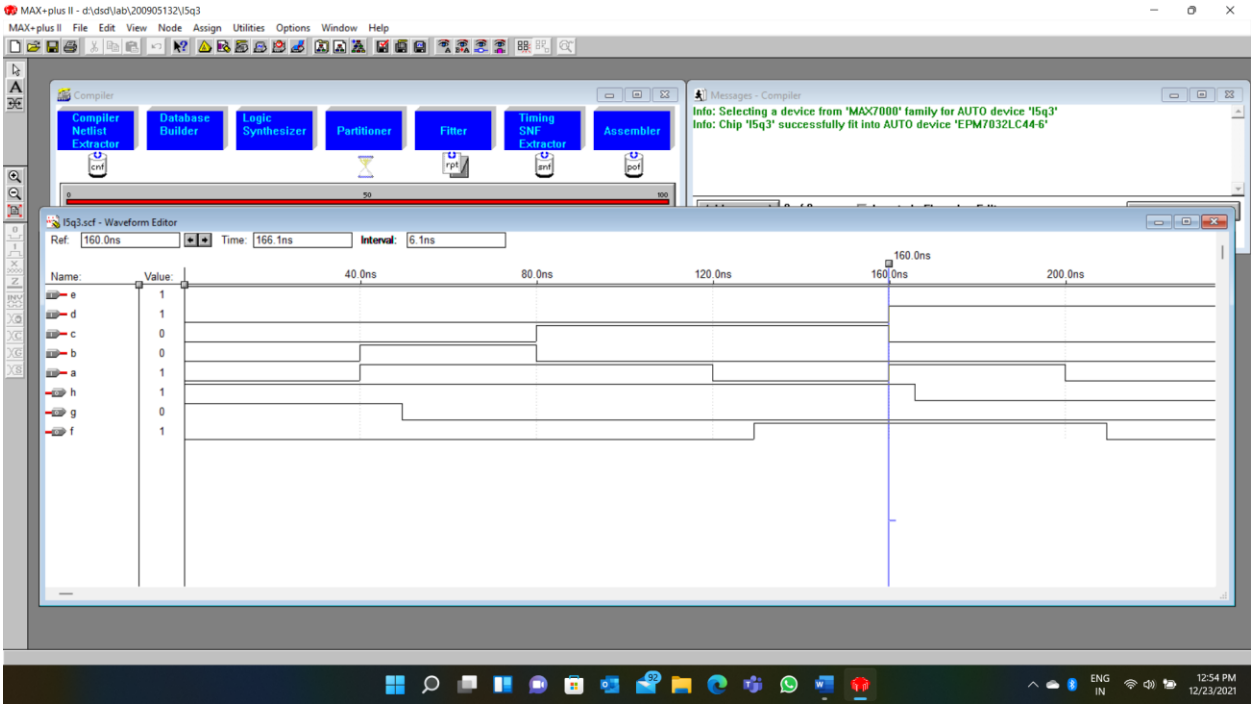
Solution:

```
module dec3to8(w,e,f);

input [2:0]w;

input e;

output [7:0]f;

integer k;

reg [7:0]f;

always@ (w or e)

begin
```

```
f=0;
if(e==1)
for(k=0;k<8;k=k+1)
if(w==k)
f[k]=1;
end
endmodule

module l5q3(a,b,c,d,e,f,g,h);
input a,b,c,d,e;
output f,g,h;
wire [15:0]y;
wire [2:0]q;
assign q={b,c,d};
dec3to8 stage0(q,a&e,y[15:8]);
dec3to8 stage1(q,~a&e,y[7:0]);
assign f=y[2]|y[4]|y[7]|y[9];
assign g=y[0]|y[3]|y[15];
assign h=y[0]|y[2]|y[10]|y[12];
```

endmodule


MAX+plus II - d:\dsd\lab\20090132\l5q3
MAX+plus II File Edit View Node Assign Utilities Options Window Help
Compiler
Compiler Netlist Extractor
Database Builder
Logic Synthesizer
Partitioner
Fitter
Timing SNF Extractor
Assembler
Messages - Compiler
Info: Selecting a device from 'MAX7000' family for AUTO device 'l5q3'
Info: Chip 'l5q3' successfully fit into AUTO device 'EPM7032LC44-6'
l5q3.scf - Waveform Editor
Ref: 0.0ns
Time: 150.2ns
Interval: 150.2ns
Name:
Value:
40.0ns
80.0ns
120.0ns
160.0ns
200.0ns
e 0
d 0
c 0
b 0
a 0
h 0
g 0
f 0
ENG IN
10:24 AM 12/23/2021


MAX+plus II - d:\dsd\lab\20090132\l5q3
MAX+plus II File Edit View Node Assign Utilities Options Window Help
Compiler
Compiler Netlist Extractor
Database Builder
Logic Synthesizer
Partitioner
Fitter
Timing SNF Extractor
Assembler
Messages - Compiler
Info: Selecting a device from 'MAX7000' family for AUTO device 'l5q3'
Info: Chip 'l5q3' successfully fit into AUTO device 'EPM7032LC44-6'
l5q3.scf - Waveform Editor
Ref: 160.0ns
Time: 166.1ns
Interval: 6.1ns
160.0ns
Name:
Value:
40.0ns
80.0ns
120.0ns
160.0ns
200.0ns
e 1
d 1
c 0
b 0
a 1
h 1
g 0
f 1
ENG IN
12:54 PM 12/23/2021