PART A : ICT 2171 Digital Systems and Computer Organization 22 JAN 2022

Answer All Questions

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4

Binary equivalent of the gray code number 101110 is:
(1 Point)

- 111001

110010

110100

101000

5

A Boolean expression F is defined with the following minterms. Find the minimum number of two input NOR gates required to realize the simplified expression of F .
(1 Point)

$F = \sum (3, 7, 11, 12, 13, 14, 15)$

8

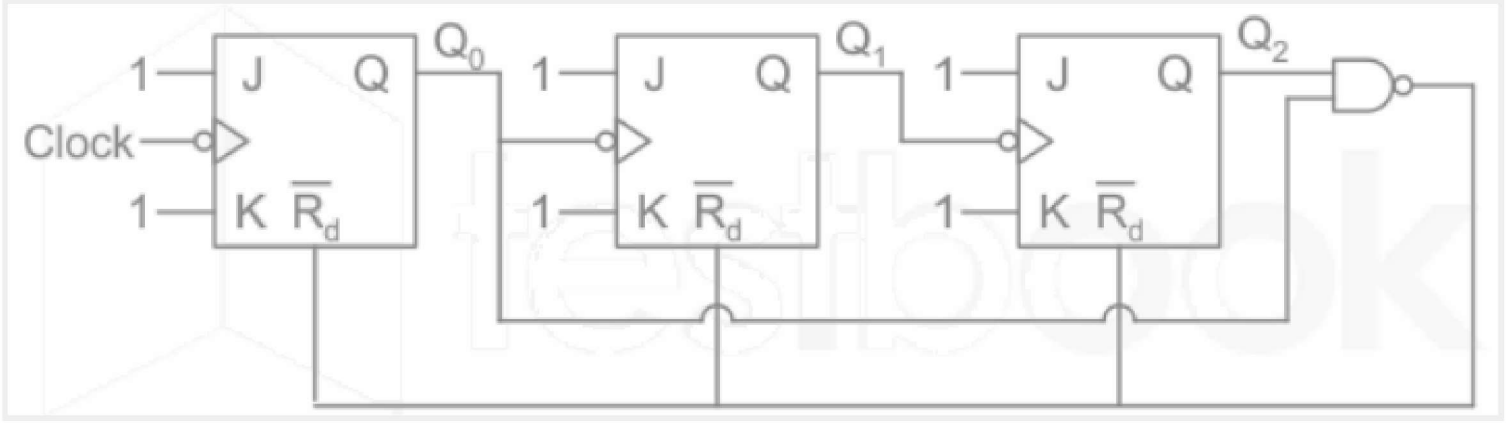
6

7

9

6

The circuit has JK flip flops with active low asynchronous reset inputs. Which of the following correctly defines the function of this circuit?
(1 Point)



- It is a MOD-6 binary down counter
- It is a MOD-6 binary up counter
- It is a MOD-5 binary up counter
- It is a MOD-5 binary down counter

7

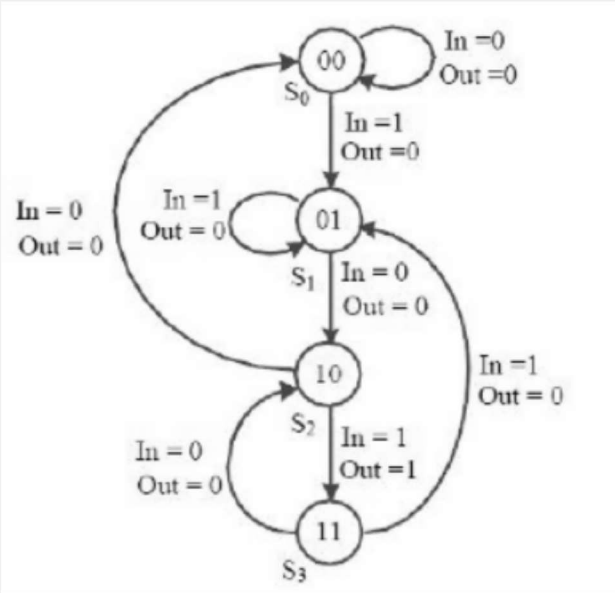
An initially cleared JK flip flop is used with input J = 1 and K = Q. What will be the reading on output Q for next 6 clock pulses ?
(1 Point)

- 1 0 1 0 1 0
- 1 0 1 1 0 1

100110

110110

8



An input sequence 10101101001101 is applied to the state machine with S0 being the initial state. Which of the following correctly defines the given circuit ?
(1 Point)

It is a overlapping sequence detector and 3 times 'Out' will be 1.

It is a non-overlapping sequence detector and 4 times 'Out' will be 1.

It is a overlapping sequence detector and 4 times 'Out' will be 1.

- ◯ It is a non-overlapping sequence detector and 3 times 'Out' will be 1.

9

Which of the following are weighted as well as self complementary codes?
(1 Point)

- ◯ 8 4 -2 -1 only
- ◯ Excess-3 code only
- ◯ 8 4 -2 -1 and Excess-3 code
- ◯ 8 4 -2 -1 and 7 4 2 1

10

The simplified expression for the most significant output Y1 of 4:2 priority encoder is._____.
The input priority is A<B<C<D, A is the most significant and D is the leas significant input.
(1 Point)

- ◯ C +D
- ◯ A + B
- ◯ A C'D' +B'C'D'

- A +B 'C

11

A binary multiplier needs to be designed to multiply a 4-bit binary number by (1010). What is the minimum number of AND gate and 4-bit parallel adders required for the design?
(1 Point)

- 8 AND gates and 2, 4-bit parallel adder
- 16 AND gates and 3, 4-bit parallel adder
- 4 AND gates and 2, 4-bit parallel adder
- Zero AND gates and one 4-bit parallel adder

12

Perform (01101)base2 – (00111)base2 using 1's complement method.

(1 Point)

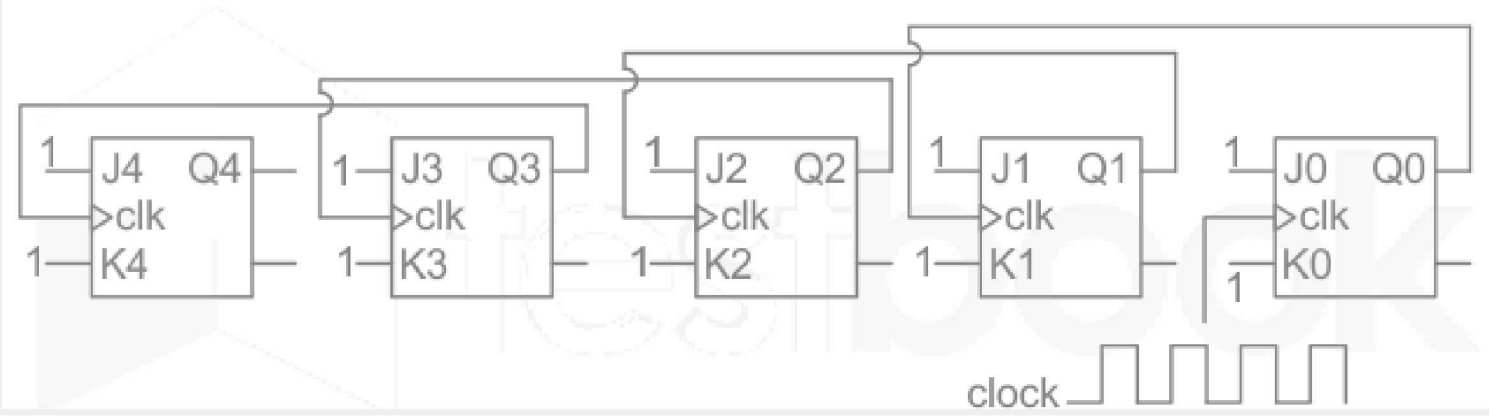
- 01101
- 00110

○ 00101

○ 10100

13

For the Circuit shown in the figure, a clock frequency of 2 MHz is applied. The frequency of output measured at Q3 is _____.
(1 Point)



○ 250 kHz

○ 256 kHz

○ 125 kHz

○ 62.5 kHz

14

In booth's multiplication, how many subtraction operations are performed for the multiplier (011101011)base 2.

(1 Point)

- 1
- 3
- 2
- 4

15

In which of the following circuit the flipflop's output transition serves as an input source to trigger other flipflops?
(1 Point)

- Ripple counter Circuits
- Serial Adder Circuits
- Parallel adder circuits

Shift Register Cicuits

16

If the function F (A, B, C) = ∑(0, 3, 4, 6, 7) is implemented using only 74153 IC, how many 74153 ICs are used?
(1 Point)

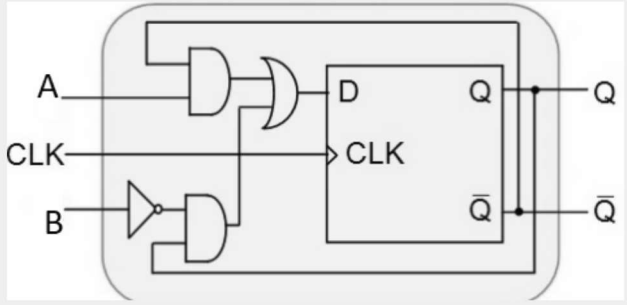
2

4

3

1

17



An A-B flipflop is constructed using D flipflop and is shown here in the figure. Which of the following option correctly defines the function of A-B flipflop ?
(1 Point)

- It is a JK flip flop with A = J and B = K
- It is a JK flip flop with A = K and B = J
- It is a SR flip flop with A = R and B = S
- It is a SR flip flop with A = S and B = R

18

Assume a system's memory has 128M words. Blocks are 64 words in length and the cache consists of 32K blocks. What are the sizes of the tag, set, and word fields assuming a set associative cache mapping scheme with 4 blocks/set?
(1 Point)

- 10, 4, 6
- 17, 4, 6
- 14, 2, 6
- 5, 2, 6

19

A logic function F(x, y, z) = x' + y'z is realized using 3-to-8 line decoder with active high output and external NOR gate. Write the output lines that need to be tapped to connect to the NOR gate?
(1 Point)

- 4, 7
- 4, 6, 7
- 0, 2, 4, 7
- 0, 1, 2, 3, 5

20

The minterms for the output E(equal) of 2-bit magnitude comparator are_____. Inputs are in the order A1 A0 B1 B0.
(1 Point)

- 2, 4, 6, 8, 10, 12, 14
- 0,2

0, 5, 10, 15

1, 2, 4, 8

21

The control unit design using hardwired approach consists of

a. Decoder
b. Multiplexer
c. Mod counter
d. Sequence controller

(1 Point)

b, c, d options are correct

a, b, c options are correct

a, b, d options are correct

a, c, d options are correct

22

Which signal is used to obtain control over the system bus for one clock cycle?

(1 Point)

- DMA request
- INHIBIT'
- HOLD
- HLDA

23

Which of the following statement is incorrect with respect to asynchronous counters ?
(1 Point)

- A n-bit Johnson ring counter has (2n - 1) distinct states and it is also a MOD (2n - 1) counter
- For a ripple counter, if the number of flipflops are 'n' then the total states involved is (2^n). It is called as MOD (2^n) counter
- A n-bit Johnson ring counter has (2n) distinct states and it is also a MOD (2n) counter

For a ripple counter, if the number of flipflops are 'n' then the total states involved is (2^n - 1). It is called as MOI (2^n - 1) counter

24

A bit sequence of length 15 requires _____ flip flops in a sequence generator
(1 Point)

5

4

16

15

25

What are the different parts in Control Memory Data Buffer register in microprogrammed approach for control unit design?

a. Control Signals
b. Condition Select
c. MUX
d. Branch Address
e. Micro Program Counter

(1 Point)

- a, c,d options are correct
- b,c,e options are correct
- a, b,d options are correct
- b,d,e options are correct

26

Two 1-bit magnitude comparator blocks with cascading inputs are cascaded to form a 2-bit magnitude comparator to compare A1A0=10 with B1B0=01. A1 and B1 are given as input to the least significant comparator block, and A0 and B0 are given as inputs to most significant block. The output at the most significant blocks are;
(1 Point)

- L=1, G = 0, E =0
- L=1, G=1, E=0
- L=0, G=1, E=0
- L=0, G=0, E=1

27

Which of the following statement correctly defines Master-Slave Flipflop characteristic?
(1 Point)

- Change in the output occurs when the state of the Slave is affected
- Change in the output occurs when the state of the Master is affected
- At a same time both the Master and the slave states are affected
- Any changes in the input lines immediately reflects on the output lines

28

Total Number of 2 input & 3 input NAND gates required to realize the function F= ((C'.B.A)'(D'.C.A)'(C.B'.A)') is _____
(1 Point)

- 7
- 8
- 6
- 9

29

A Full Adder can be designed using _____ half adders only.
(1 Point)

- 5
- 2
- 3
- 4

30

The present output Qn = 0 and the next output Qn+1 = 1. Which of the following inputs correctly defines this situation from the excitation table of edge triggered JK flipflop?
(1 Point)

- J = Don' Care and K = 0
- J = 0 and K = Don' Care
- J = 1 and K = Don' Care
- J = Don' Care and K = 1

31

Which of the following statement is wrong with respect to Mealy model ?
(1 Point)

- Output depends on input and present state
- Output depends on only present state of the circuit
- State transitions are also the part of output computation
- State transitions reflects its effect on output

32

Simplest realization of Ex-NOR logic using two input NAND/NOR only requires _____ gates.
(1 Point)

- 5
- 3
- 6
- 4

33

Minimum number of half adders required to implement 3 input NOR gate using ONLY half adders are :
(1 Point)

- 5
- 6
- 9
- 7

Submit