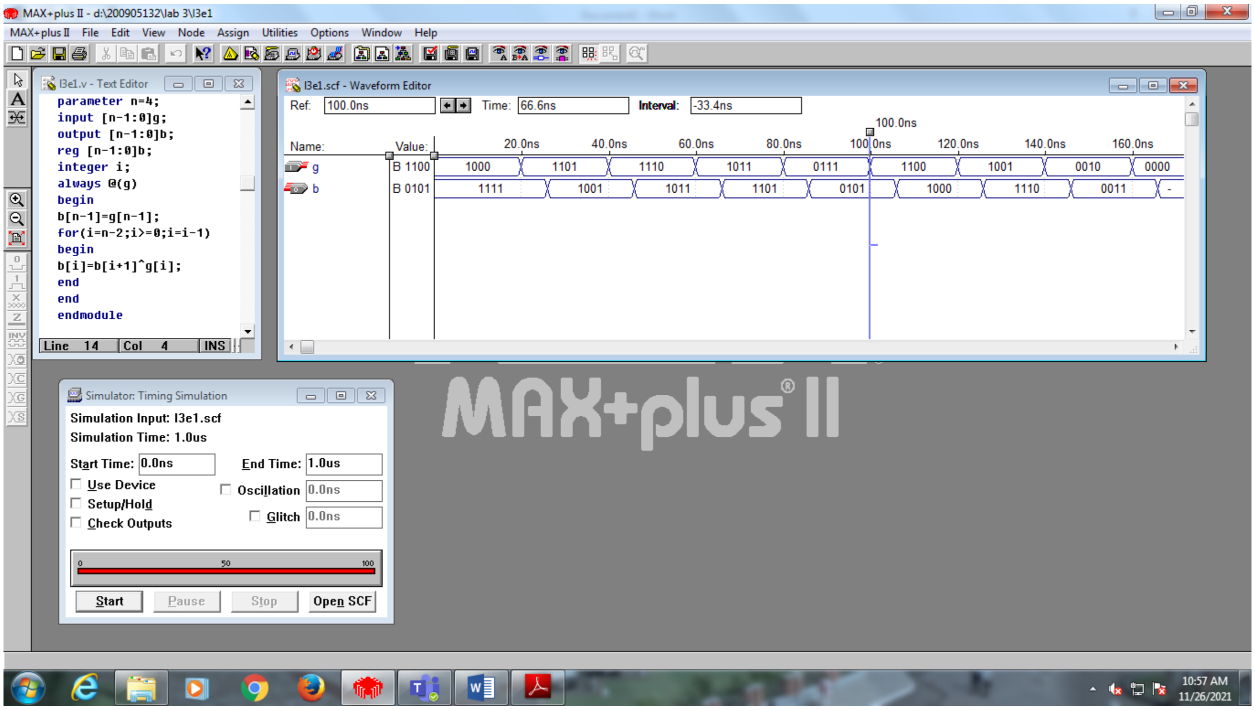
DSD Lab 3

1. Using **for** loop, write behavioral Verilog code to convert an N bit grey code into equivalent binary code.

```
module l3e1(g,b);
parameter n=4;
input [n-1:0]g;
output [n-1:0]b;
reg [n-1:0]b;
integer i;
always @(g)
begin
b[n-1]=g[n-1];
for(i=n-2;i>=0;i=i-1)
begin
b[i]=b[i+1]^g[i];
end
end
endmodule
```


MAX+plus II - d:\200905132\lab 3\l3e1
MAX+plus II File Edit View Node Assign Utilities Options Window Help
l3e1.v - Text Editor
l3e1.scf - Waveform Editor
Simulator: Timing Simulation
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11/26/2021

```
parameter n=4;
input [n-1:0]g;
output [n-1:0]b;
reg [n-1:0]b;
integer i;
always @(g)
begin
b[n-1]=g[n-1];
for(i=n-2;i>=0;i=i-1)
begin
b[i]=b[i+1]^g[i];
end
end
endmodule
```

Line 14 Col 4 INS

Ref: 100.0ns Time: 66.6ns Interval: -33.4ns

Name:	Value:	20.0ns	40.0ns	60.0ns	80.0ns	100.0ns	120.0ns	140.0ns	160.0ns	
g	B 1100	1000	1101	1110	1011	0111	1100	1001	0010	0000
b	B 0101	1111	1001	1011	1101	0101	1000	1110	0011	-

Simulation Input: l3e1.scf
Simulation Time: 1.0us

Start Time: 0.0ns End Time: 1.0us

□ Use Device □ Oscillation 0.0ns
□ Setup/Hold □ Glitch 0.0ns
□ Check Outputs

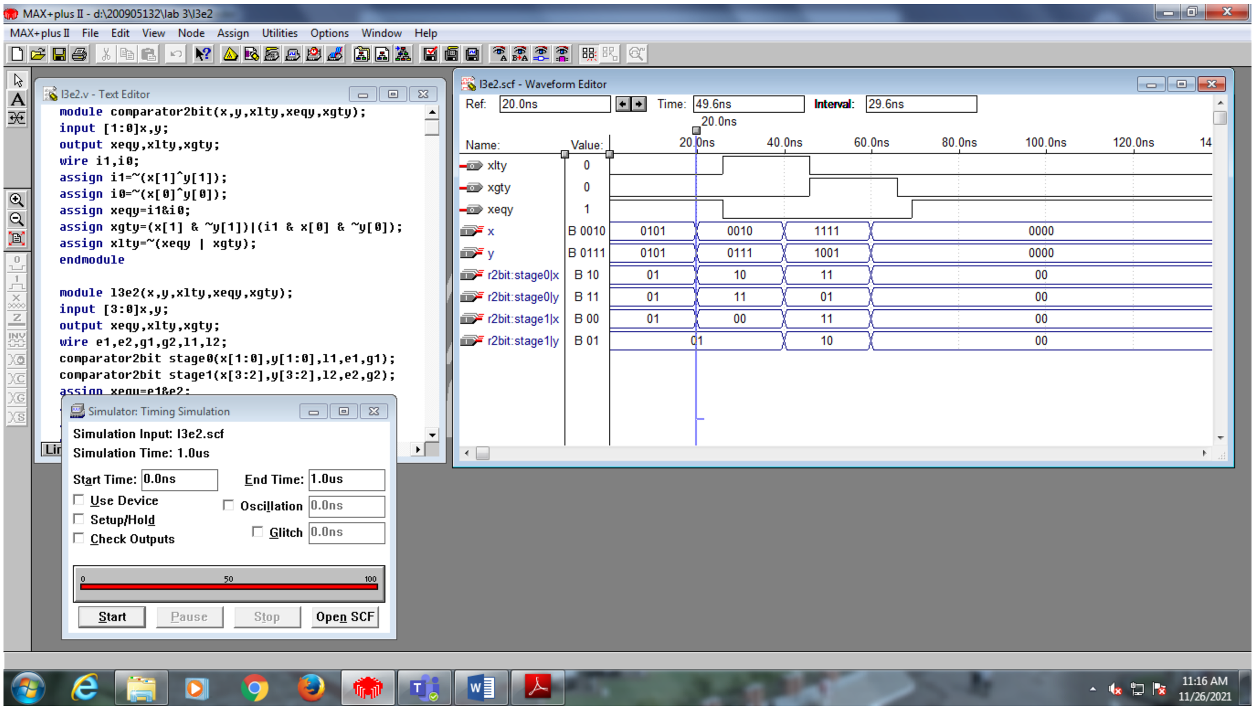
0 50 100

Start Pause Stop Open SCF

2. Write and simulate the Verilog code for a 4-bit comparator using 2-bit comparators.

```
module comparator2bit(x,y,xlty,xeqy,xgty);
input [1:0]x,y;
```

```
output xeqy,xlty,xgty;
wire i1,i0;
assign i1=~(x[1]^y[1]);
assign i0=~(x[0]^y[0]);
assign xeqy=i1&i0;
assign xgty=(x[1] & ~y[1])|(i1 & x[0] & ~y[0]);
assign xlty=~(xeqy | xgty);
endmodule

module l3e2(x,y,xlty,xeqy,xgty);
input [3:0]x,y;
output xeqy,xlty,xgty;
wire e1,e2,g1,g2,l1,l2;
comparator2bit stage0(x[1:0],y[1:0],l1,e1,g1);
comparator2bit stage1(x[3:2],y[3:2],l2,e2,g2);
assign xeqy=e1&e2;
assign xgty=g1 | (e1 & g2);
assign xlty=l1 | (e1 & l2);
endmodule
```



```
module comparator2bit(x,y,xlty,xeqy,xgty);
input [1:0]x,y;
output xeqy,xlty,xgty;
wire i1,i0;
assign i1=~(x[1]^y[1]);
assign i0=~(x[0]^y[0]);
assign xeqy=i1&i0;
assign xgty=(x[1] & ~y[1])|(i1 & x[0] & ~y[0]);
assign xlty=~(xeqy | xgty);
endmodule

module l3e2(x,y,xlty,xeqy,xgty);
input [3:0]x,y;
output xeqy,xlty,xgty;
wire e1,e2,g1,g2,l1,l2;
comparator2bit stage0(x[1:0],y[1:0],l1,e1,g1);
comparator2bit stage1(x[3:2],y[3:2],l2,e2,g2);
assign xeqy=e1&e2;
```

l3e2.scf - Waveform Editor

Ref: 20.0ns Time: 49.6ns **Interval:** 29.6ns

```
                         20.0ns
Name:            Value:  20.0ns    40.0ns    60.0ns    80.0ns    100.0ns    120.0ns    14
xlty             0
xgty             0
xeqy             1
x                B 0010   0101  | 0010  | 1111  |            0000
y                B 0111   0101  | 0111  | 1001  |            0000
r2bit:stage0|x   B 10     01    | 10    | 11    |            00
r2bit:stage0|y   B 11     01    | 11    | 01    |            00
r2bit:stage1|x   B 00     01    | 00    | 11    |            00
r2bit:stage1|y   B 01         01        | 10    |            00
```

Simulator: Timing Simulation

Simulation Input: l3e2.scf
Simulation Time: 1.0us

Start Time: 0.0ns   End Time: 1.0us

□ Use Device   □ Oscillation 0.0ns
□ Setup/Hold   □ Glitch 0.0ns
□ Check Outputs

0 50 100

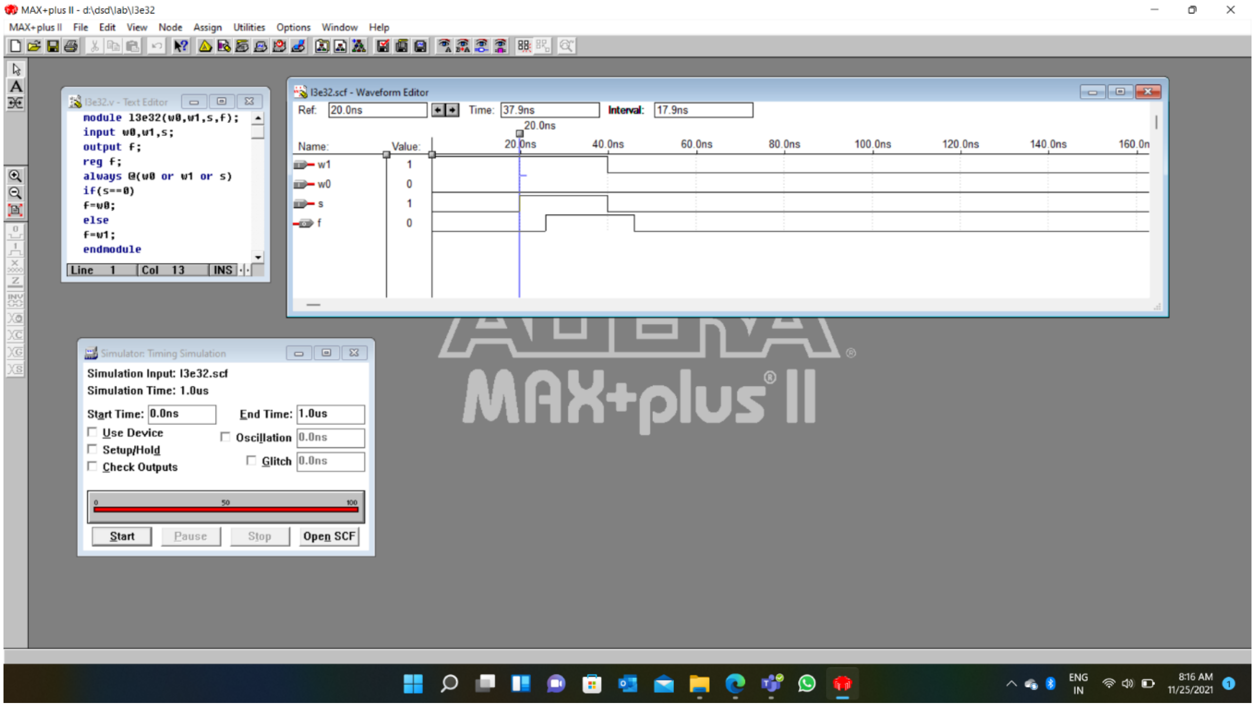
Start Pause Stop Open SCF

3. Write behavioral Verilog code for

- an 8 to 1 multiplexer using **case** statement
- a 2 to 1 multiplexer using the **if-else** statement.

Using the above modules write the hierarchical code for a 16 to 1 multiplexer.

```
module mux2to1 (w0, w1, s, f);

input w0, w1, s;

output f;

reg f;

always @(w0 or w1 or s)

if (s == 0)

f = w0;

else

f = w1;

endmodule
```



MAX+plus II - d:\dsd\lab\l3e32

l3e32.v - Text Editor

```
module l3e32(w0,w1,s,f);
input w0,w1,s;
output f;
reg f;
always @(w0 or w1 or s)
if(s==0)
f=w0;
else
f=w1;
endmodule
```

Line 1 Col 13 INS

l3e32.scf - Waveform Editor

Ref: 20.0ns Time: 37.9ns Interval: 17.9ns

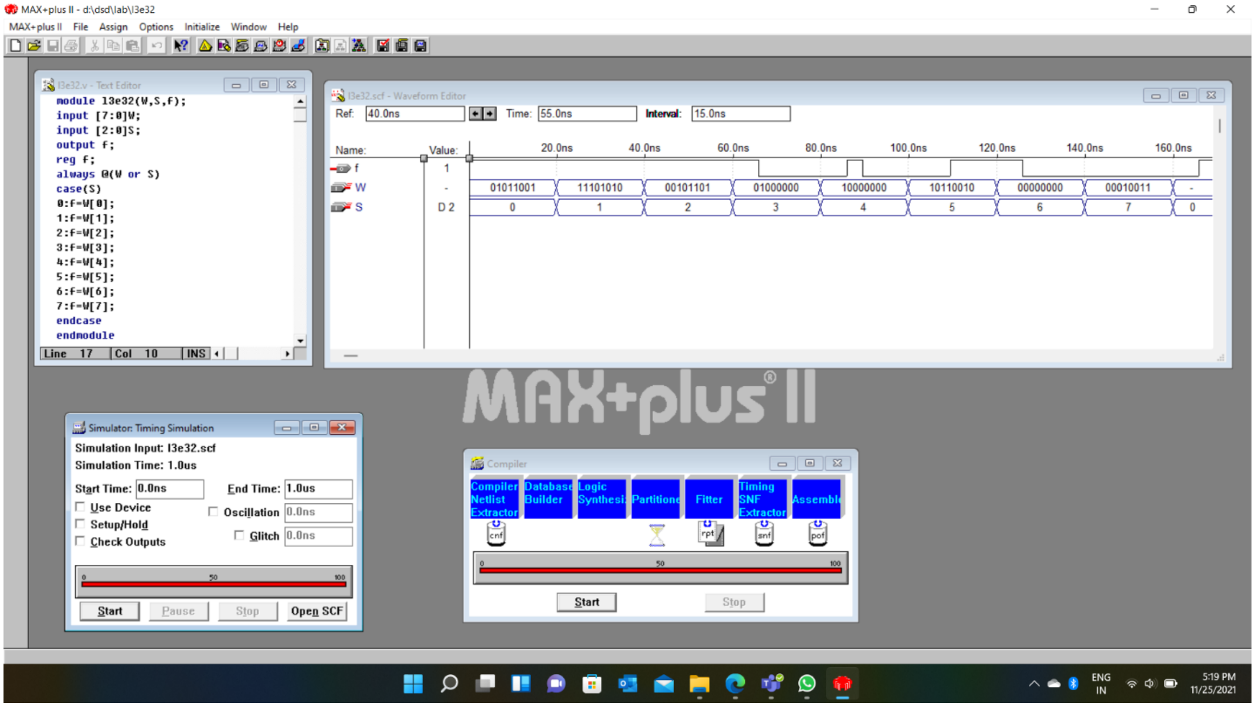
Simulator: Timing Simulation

Simulation Input: l3e32.scf
Simulation Time: 1.0us

Start Time: 0.0ns End Time: 1.0us
□ Use Device □ Oscillation 0.0ns
□ Setup/Hold □ Glitch 0.0ns
□ Check Outputs

```
module l3e32(W,S,f);
input [7:0]W;
input [2:0]S;
```

```
output f;
reg f;
always @(W or S)
case(S)
0:f=W[0];
1:f=W[1];
2:f=W[2];
3:f=W[3];
4:f=W[4];
5:f=W[5];
6:f=W[6];
7:f=W[7];
endcase
endmodule
```



```
module l3e32(W,S,f);
input [7:0]W;
input [2:0]S;
output f;
reg f;
always @(W or S)
case(S)
0:f=W[0];
1:f=W[1];
2:f=W[2];
3:f=W[3];
4:f=W[4];
5:f=W[5];
6:f=W[6];
7:f=W[7];
endcase
endmodule
```

Ref: 40.0ns Time: 55.0ns Interval: 15.0ns

```
Name:   Value:  20.0ns    40.0ns    60.0ns    80.0ns    100.0ns   120.0ns   140.0ns   160.0ns
f       1
W       -       01011001  11101010  00101101  01000000  10000000  10110010  00000000  00010011  -
S       D 2     0         1         2         3         4         5         6         7         0
```

Simulator: Timing Simulation

Simulation Input: l3e32.scf

Simulation Time: 1.0us

Start Time: 0.0ns End Time: 1.0us

□ Use Device □ Oscillation 0.0ns

□ Setup/Hold □ Glitch 0.0ns

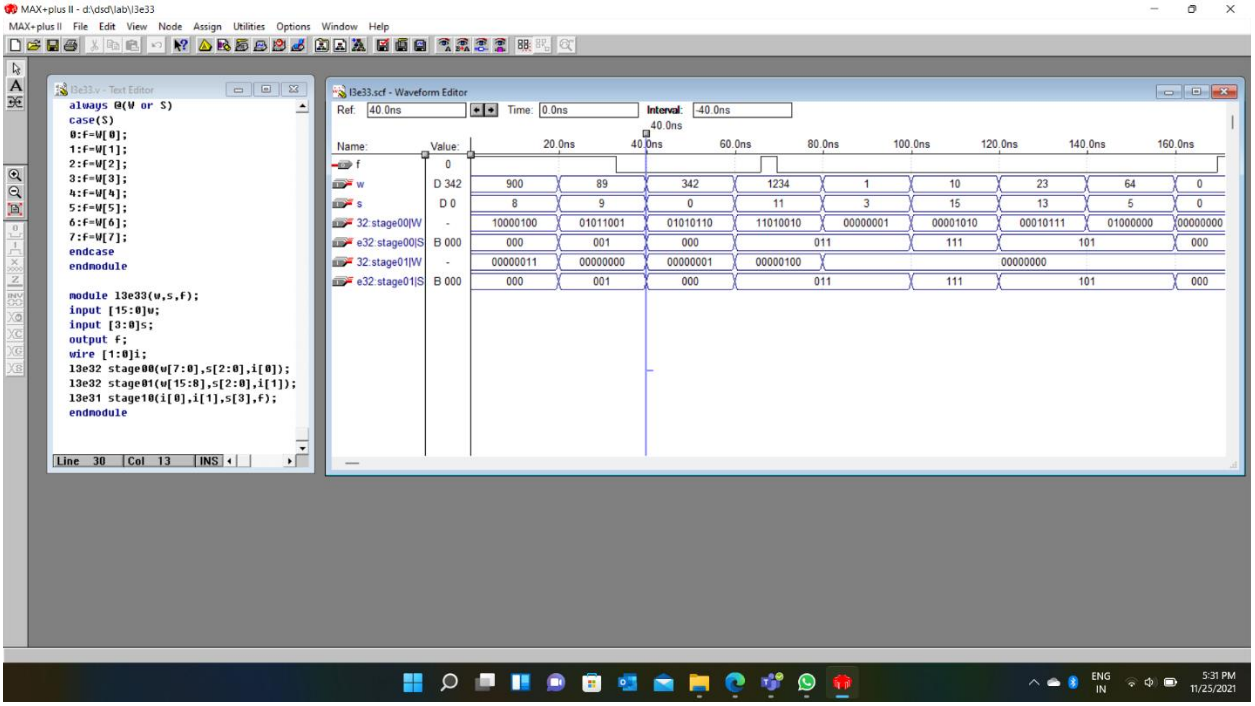
□ Check Outputs

0 50 100

Start Pause Stop Open SCF

```
module l3e31(w0, w1, s, f);
input w0,w1,s;
output f;
reg f;
always @(w0 or w1 or s)
if (s == 0)
f = w0;
else
```

```
f = w1;
endmodule
module l3e32(W,S,f);
input [7:0]W;
input [2:0]S;
output f;
reg f;
always @(W or S)
case(S)
0:f=W[0];
1:f=W[1];
2:f=W[2];
3:f=W[3];
4:f=W[4];
5:f=W[5];
6:f=W[6];
7:f=W[7];
endcase
endmodule
module l3e33(w,s,f);
input [15:0]w;
input [3:0]s;
output f;
wire [1:0]i;
l3e32 stage00(w[7:0],s[2:0],i[0]);
l3e32 stage01(w[15:8],s[2:0],i[1]);
l3e31 stage10(i[0],i[1],s[3],f);
endmodule
```



MAX+plus II - d:\dsd\lab\l3e33
MAX+plus II File Edit View Node Assign Utilities Options Window Help
l3e33.v - Text Editor
l3e33.scf - Waveform Editor
5:31 PM
11/25/2021
ENG
IN

```
always @(W or S)
case(S)
0:f=W[0];
1:f=W[1];
2:f=W[2];
3:f=W[3];
4:f=W[4];
5:f=W[5];
6:f=W[6];
7:f=W[7];
endcase
endmodule

module l3e33(w,s,f);
input [15:0]w;
input [3:0]s;
output f;
wire [1:0]i;
l3e32 stage00(w[7:0],s[2:0],i[0]);
l3e32 stage01(w[15:8],s[2:0],i[1]);
l3e31 stage10(i[0],i[1],s[3],f);
endmodule
```

Line 30 Col 13 INS

```
Ref: 40.0ns   Time: 0.0ns   Interval: -40.0ns
                                                40.0ns
Name:            Value:       20.0ns      40.0ns      60.0ns      80.0ns      100.0ns     120.0ns     140.0ns     160.0ns
f                0
w                D 342    900        89         342        1234       1          10         23         64         0
s                D 0      8          9          0          11         3          15         13         5          0
32:stage00|W     -        10000100   01011001   01010110   11010010   00000001   00001010   00010111   01000000   00000000
e32:stage00|S    B 000    000        001        000               011            111                   101        000
32:stage01|W     -        00000011   00000000   00000001   00000100                        00000000
e32:stage01|S    B 000    000        001        000               011            111                   101        000
```