Department of Information & Communication Technology
MIT, Manipal

III Sem B. Tech (IT/CCE),
ICT 2154 Digital Systems / ICT 2171 Digital Systems and Computer Organization
In-sem Examination

Date: 15/12/2021 **Max. Marks: 20**

Write-upTime: 10.30 to 11.50am **Upload time: 11.50am to 12.00pm**

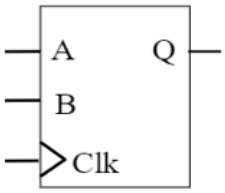
Note to Students: Answer ALL Questions

<table>
<tr><td>Q1.</td><td>Design the following combinational circuit using single 7485IC, 7483IC and minimum number of full adder blocks.

If A>B, F= A+4B

Else F= 4A-B

Where A and B are 2-bit binary numbers.</td><td>3
Marks</td></tr>
<tr><td>Q2.</td><td>Construct a hexadecimal up counter to count from 0 to 79H using minimum asynchronous ICs and external gates. Draw the logic diagram.</td><td>3
Marks</td></tr>
<tr><td>Q3.</td><td>Design a 2-bit binary adder using 74151 ICs and minimum external gates.</td><td>3
Marks</td></tr>
<tr><td>Q4.</td><td>Function table defines the working of a fictious AB flip flop. Design the AB flip flop using D flip flop and external gates.

<table>
<tr><th>A</th><th>B</th><th>Q(t+1)</th></tr>
<tr><td>0</td><td>0</td><td>Q</td></tr>
<tr><td>0</td><td>1</td><td>Q’</td></tr>
<tr><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td></tr>
</table>

</td><td>3
Marks</td></tr>
<tr><td>Q5.</td><td>Design a JK flip flop using a basic NAND latch and gates.</td><td>4
Marks</td></tr>
<tr><td>Q6.</td><td>Design a code converter to convert a decimal digit represented in 5 4 2 1 code to a decimal digit represented in self-complementary 8 4 -2 -1 code using minimum number of 3 to 8 decoders with active low output and active high enable input, and external gates.</td><td>4
Marks</td></tr>
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