Synchronous counters

- Limitations of asynchronous counters
- Synchronous counter design
- Synchronous counter ICs

Synchronous counter design

- All the flip flops are clocked simultaneously using same clock.
- Suitable for high frequency applications
- Designed using sequential circuit design process which can be used for any synchronous circuit designs

8. Design 3-bit gray code counter using JK ffs

Next State table

Decimal Number	3-bit Binary	3-bit Gray Code
0	000	000
1	001	001
2	010	011
3	011	010
4	100	110
5	101	111
6	110	101
7	111	100
8		
9		

cannot be represented using only 3 bits

Binary → Gray

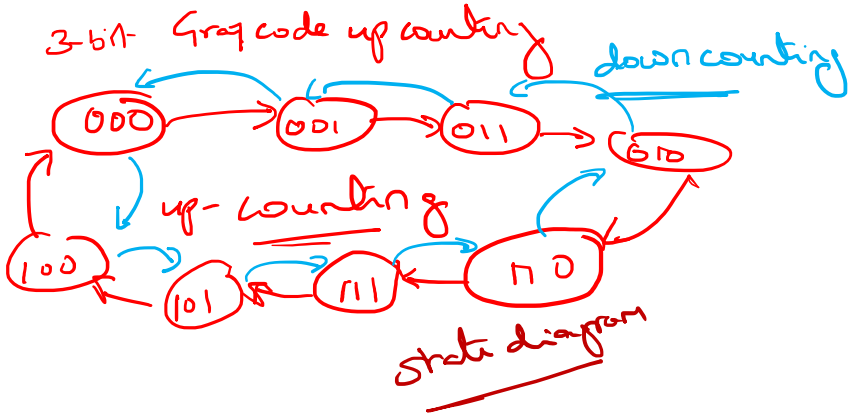
first bit → first bit

second bit → second bit

third bit → third bit

1. up counting
2. down counting

3 bit → 3 JK flipflops



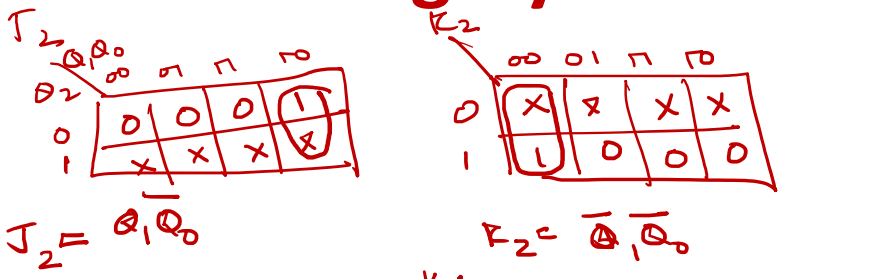
	present state $Q_2 Q_1 Q_0$	Next state $Q_2 Q_1 Q_0$	MSB J_2 K_2	J_1 K_1	LSB J_0 K_0
m_0	0 0 0	0 0 1	0 X	0 X	1 X
m_1	0 0 1	0 1 1	0 X	1 X	X 0
m_3	0 1 1	0 1 0	0 X	X 0	X 1
m_2	0 1 0	1 1 0	1 X	X 0	0 X
m_6	1 1 0	1 1 1	X 0	X 0	1 X
m_7	1 1 1	1 0 1	X 0	X 1	X 0
m_5	1 0 1	1 0 0	X 0	0 X	X 1
m_4	1 0 0	0 0 0	X 1	0 X	0 X

Pr	Next	J	K	
0	0	0	X	
0	1	1	X	Set / Toggle
1	0	X	1	Reset / Toggle
1	1	X	0	no change / Set

from function table of JK

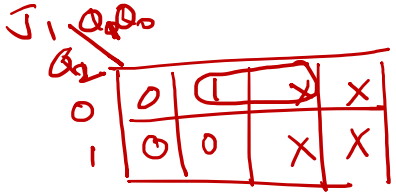
present state	Next state	J_2 K_2	J_1 K_1	J_0 K_0
m_0 000	001	0 X	0 X	1 X
m_1 001	011	0 X	1 X	X 0
m_2 010	110	1 X	X 0	0 X
m_3 011	010	0 X	X 0	X 1
m_4 100	000	X 1	0 X	0 X
m_5 101	100	X 0	0 X	X 1
m_6 110	111	X 0	X 0	1 X
m_7 111	101	X 0	X 1	X 0

3-bit gray code counter using JK ffs

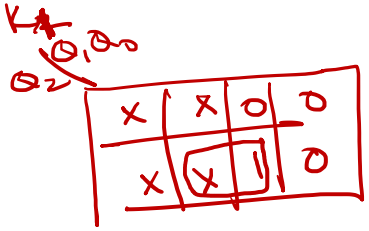


$J_2 = Q_1\bar{Q}_0$

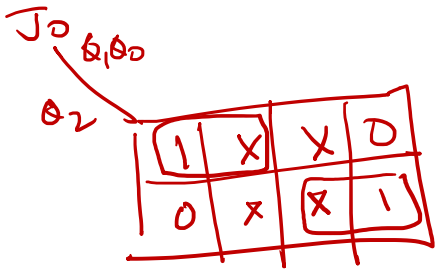
$K_2 = \bar{Q}_1\bar{Q}_0$



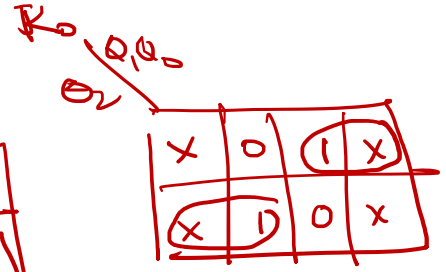
$J_1 = \bar{Q}_2 Q_0$



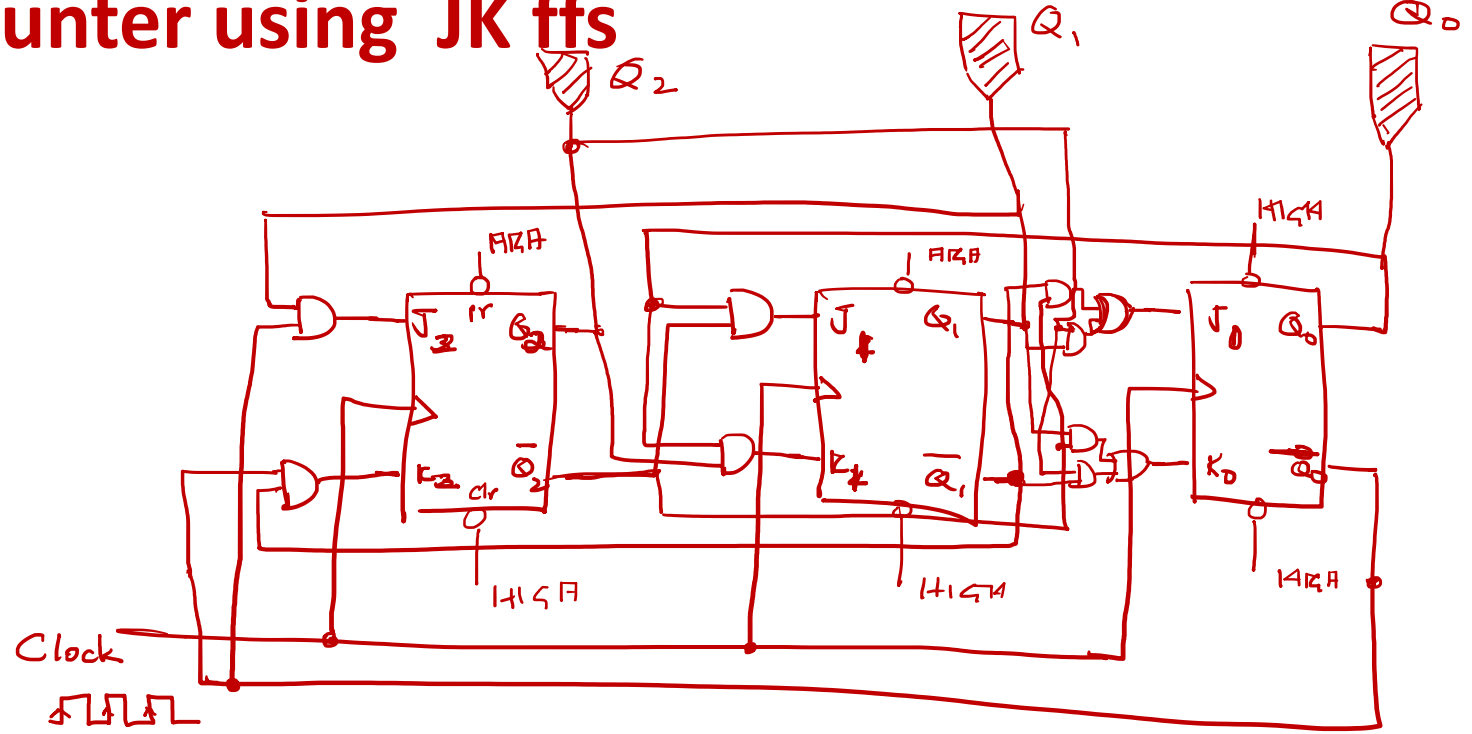
$K_1 = Q_2 Q_0$



$J_0 = \bar{Q}_2\bar{Q}_1 + Q_2 Q_1$



$K_0 = \bar{Q}_2 Q_1 + Q_2\bar{Q}_1$



Tutorial or Work-out question for you

Design 3-bit Gray code down counter using JK flipflop

9. Design a 3-bit up/down synchronous binary counter using T ffs

- If control input up/down = 0, counter should count upwards from the present count or else it has to count downwards from the present count.

Extend control signal

if the question is rewritten as, "design a 3bit up/down counter using T FF"

up/down ⇒ 0/1 PS NS

Design

Y	$Q_2Q_1Q_0$ (PS)	$Q_2Q_1Q_0$ (NS)	T_2	T_1	T_0
0	000	001	0	0	1
0	001	010	0	1	1
0	010	011	0	0	1
0	011	100	1	1	1
0	100	101	0	0	1
0	101	110	0	1	1
0	110	111	0	0	1
0	111	000	1	1	1
1	000	111	1	0	1
1	001	000	0	1	1
1	010	001	0	0	1
1	011	010	0	1	1
1	100	011	0	0	1
1	101	100	0	1	1
1	110	101	0	0	1
1	111	110	1	0	1

extend up

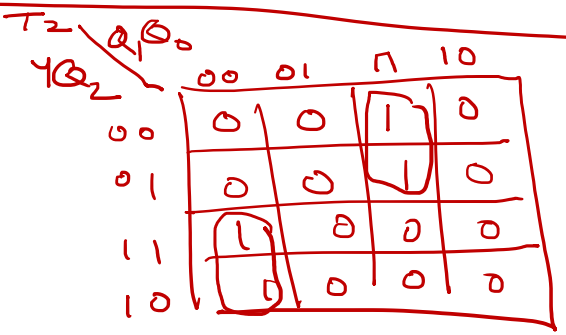
up counts

down counts

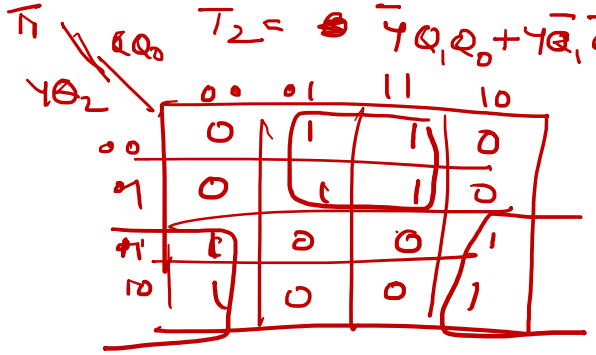
$T_0 = 1$

$T_1 = \bar{Y}Q_0 + Y\bar{Q}_0$

$T_2 = \bar{Y}Q_1Q_0 + Y\bar{Q}_1\bar{Q}_0$

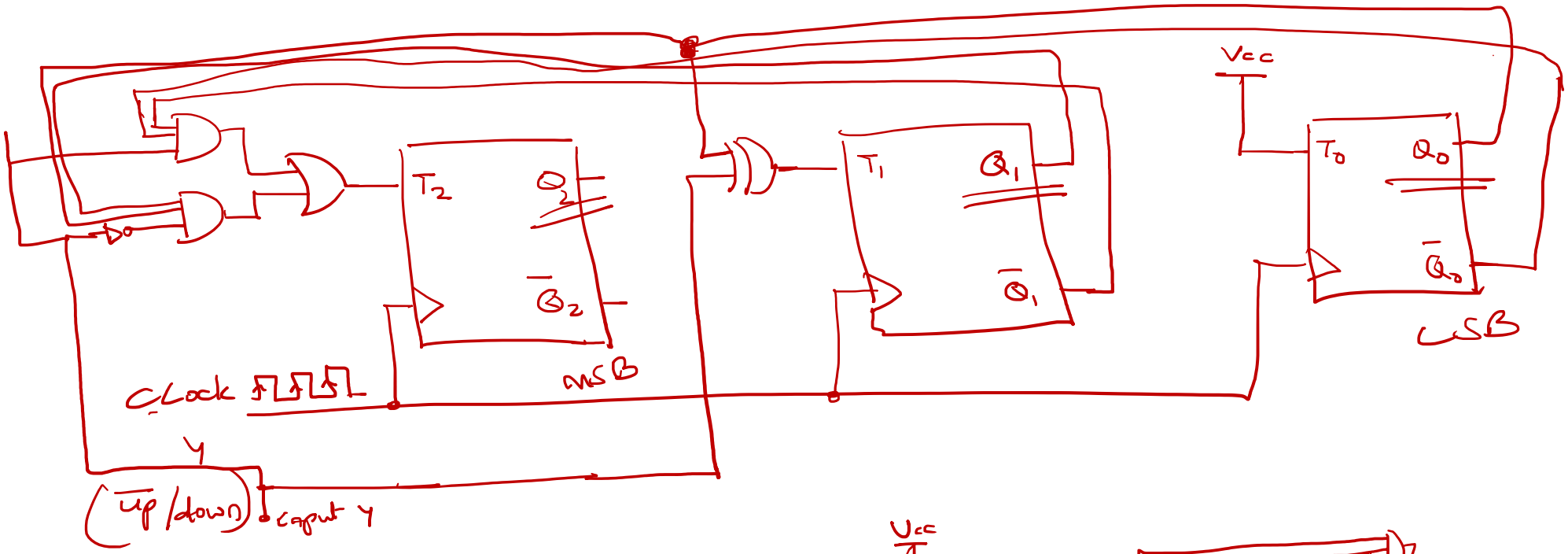


$T_2 = \bar{Y}Q_1Q_0 + YQ_1\bar{Q}_0$



$T_1 = \bar{Y}Q_0 + Y\bar{Q}_0$

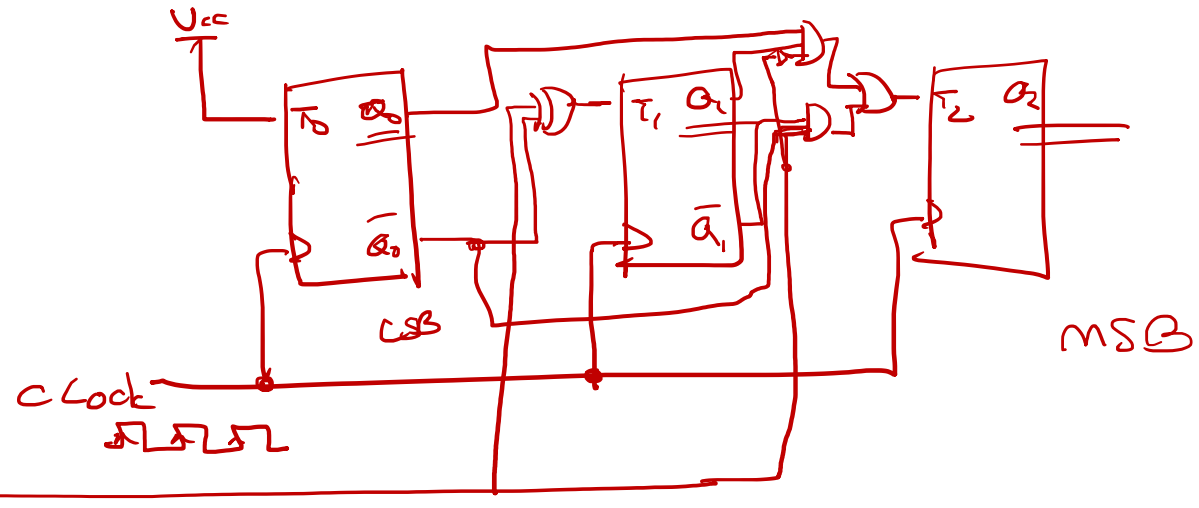
3-bit up/down synchronous binary counter using T ffs



$T_2 = \bar{Y} Q_1 Q_0 + Y \bar{Q}_1 \bar{Q}_0$

$T_1 = \bar{Y} Q_0 + Y \bar{Q}_0$

$T_0 = 1$

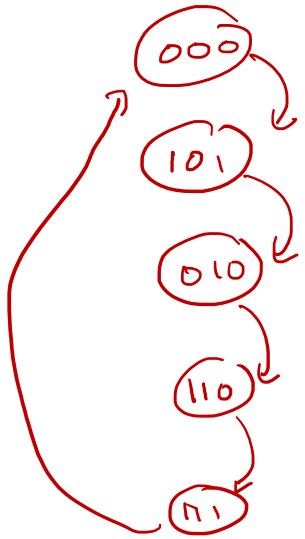


Design 3-bit synchronous counter to count according to the given sequence using D ffs.

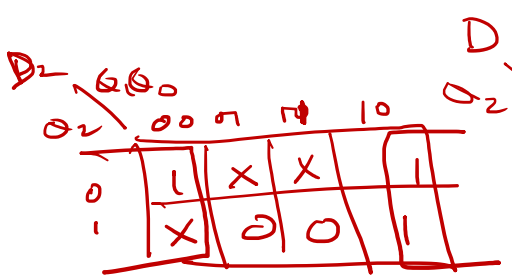
used states & counting

- 0→5→2→6→7→0

unused states states: 1, 3, 4,



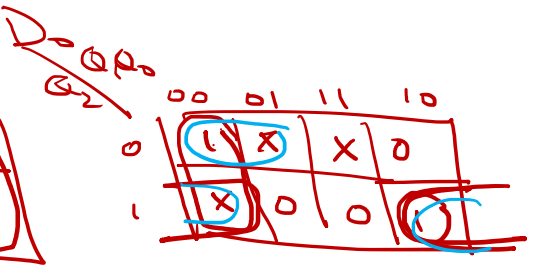
	PS $Q_2Q_1Q_0$	NS $Q_2Q_1Q_0$	D_2 D_1 D_0
m_0	0 0 0	1 0 1	1 0 1
m_1	0 0 1	X X X	X X X
m_2	0 1 0	1 1 0	1 1 0
m_3	0 1 1	X X X	X X X
m_4	1 0 0	X X X	X X X
m_5	1 0 1	0 1 0	0 1 0
m_6	1 1 0	1 1 1	1 1 1
m_7	1 1 1	0 0 0	0 0 0



$D_2 = \bar{Q}_0$

$D_1 = Q_1\bar{Q}_0 + \bar{Q}_1Q_0$

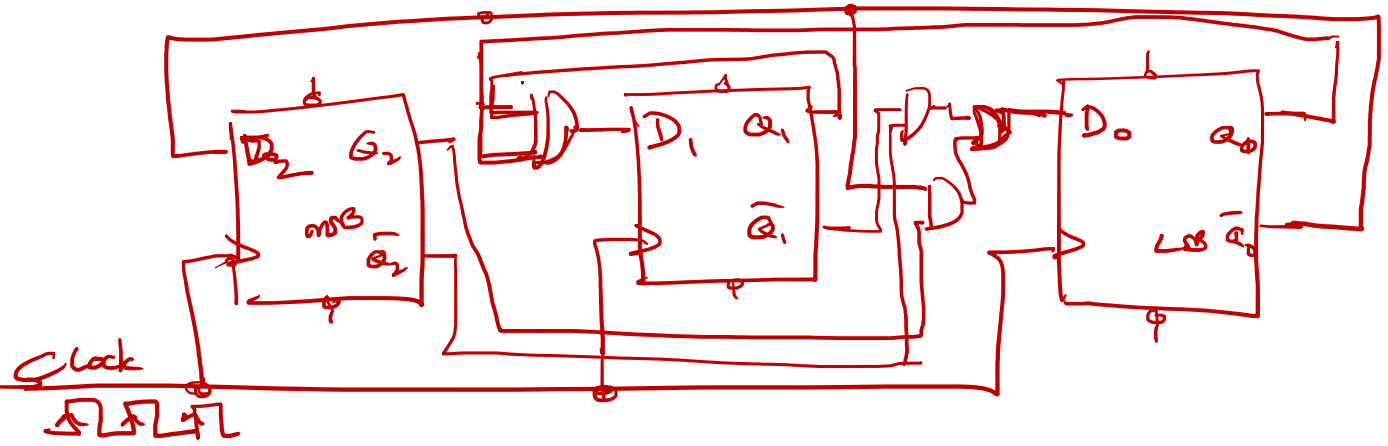
$D_1 = Q_1 \oplus Q_0$



$D_0 = \bar{Q}_1\bar{Q}_0 + Q_2\bar{Q}_0$

or

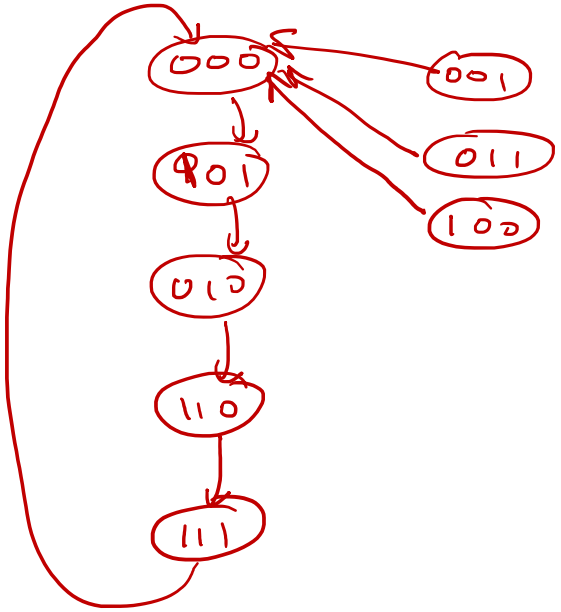
$D_0 = \bar{Q}_2\bar{Q}_1 + Q_2\bar{Q}_0$



Eg:

Design 3-bit synchronous counter to count according to the given sequence using D ffs. All the undefined states should go to state 0.---Self correcting counters.

- 0→5→2→6→7→0



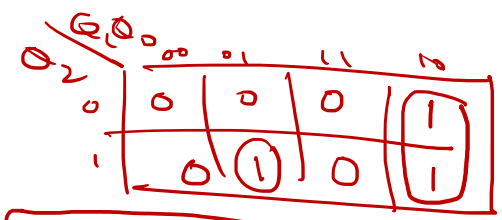
PS $Q_2Q_1Q_0$	NS $Q_2Q_1Q_0$
000	101
001	000
010	110
011	000
100	000
101	010
110	111
111	000

Correction

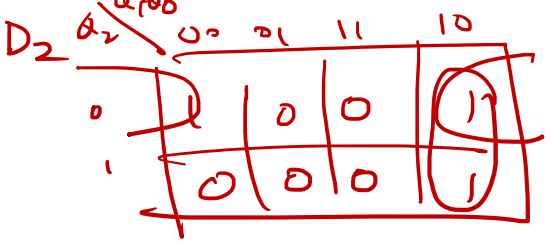
D_2	D_1	D_0
1	0	1
0	0	0
1	1	0
0	0	0
0	0	0
0	1	0
0	1	0
0	0	0

$D_0 = \bar{Q}_2\bar{Q}_1\bar{Q}_0$

$D_1 = m_2 + m_5 + m_6$



$D_1 = Q_1\bar{Q}_0 + Q_2\bar{Q}_1Q_0$



$D_2 = Q_1\bar{Q}_0 + \bar{Q}_2Q_0$

please Draw the circuit

$$D_0 = \bar{Q}_2 \bar{Q}_1 \bar{Q}_0$$

$$D_1 = Q_1 \bar{Q}_0 + Q_2 \bar{Q}_1 Q_0$$

$$D_2 = Q_1 \bar{Q}_0 + \bar{Q}_2 \bar{Q}_0$$

Design 3-bit synchronous counter to count according to the given sequence using D ffs. All the undefined states should go to next valid/defined state.

- 0→5→2→6→7→0

Next Valid code for unused code:

Next Valid code

001 → 010

011 → 101

100 → 101

Assuming we are going upwards

Downwards

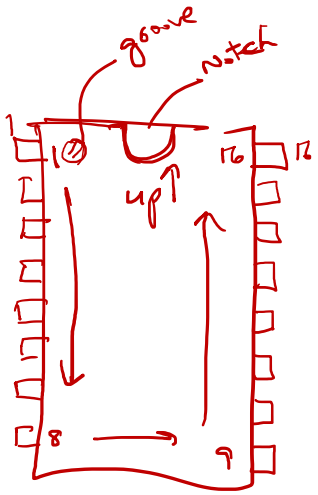
000

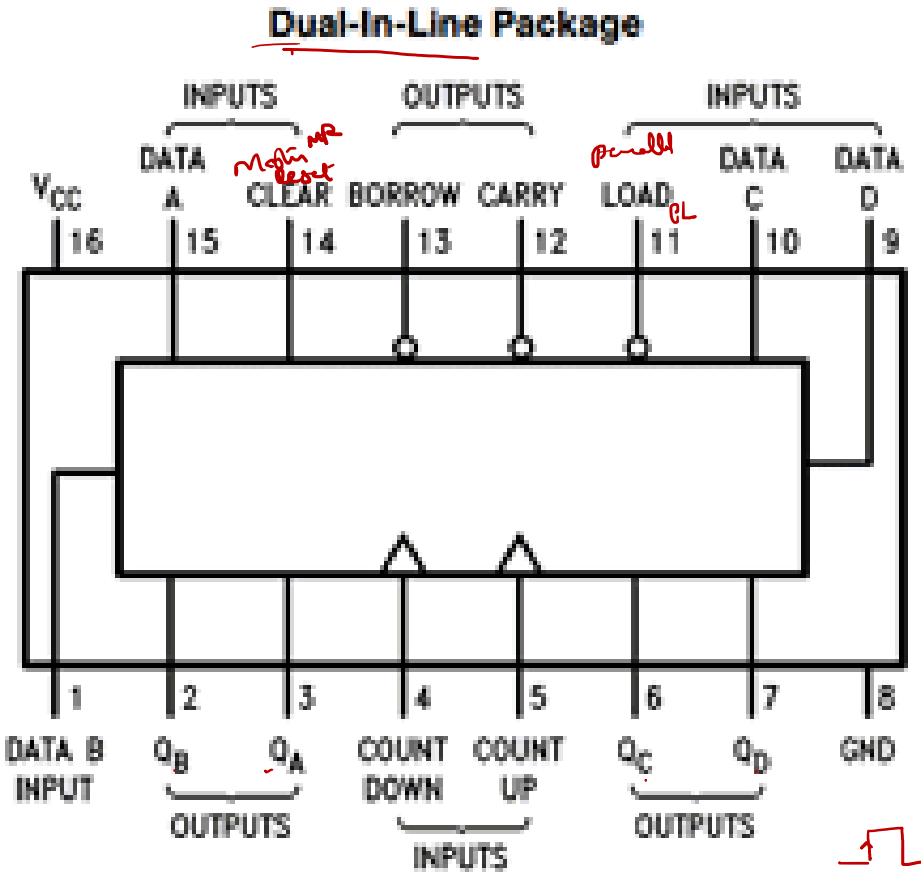
010

010

What is Defined state Ex. all unused codes go to Valid code say 110

74193 IC: 4-bit up/down synchronous counter





Q_D is the MSB and Q_A is the LSB

Count up/CPu: count up clock input

Count down/CP_D: count down clock input

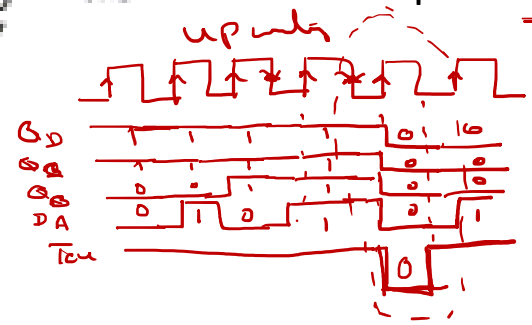
LOAD: Asynchronous parallel load (active low)

CLEAR: Asynchronous master reset input

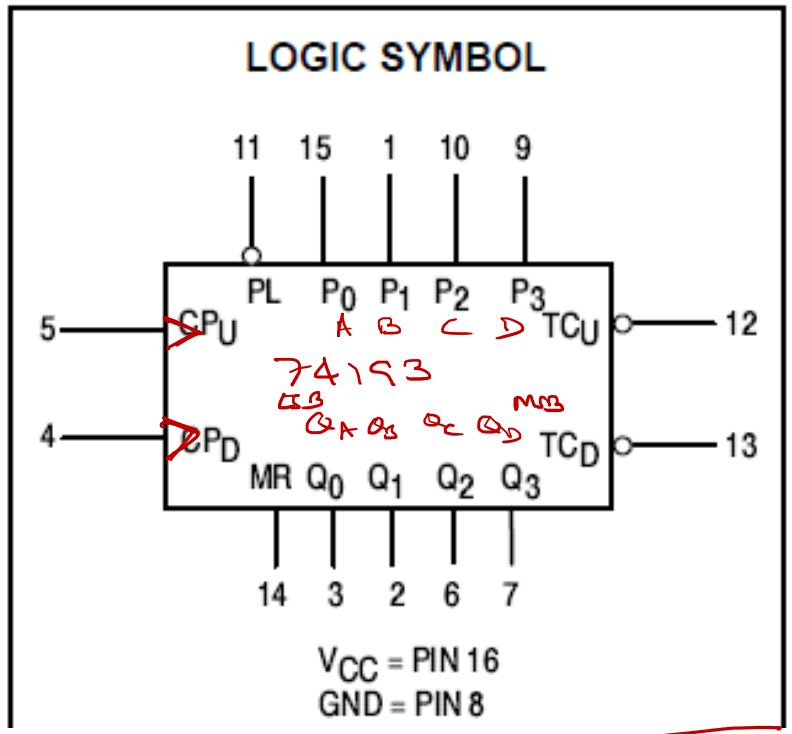
CARRY: Terminal count up output

Borrow: Terminal count down

Data inputs: Parallel data inputs



74193 IC: 4-bit up/down synchronous counter



MODE SELECT TABLE

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	⌐	H	Count Up
L	H	H	⌐	Count Down

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
⌐ = LOW-to-HIGH Clock Transition

Design a MOD 16 binary UP counter using 74193 IC