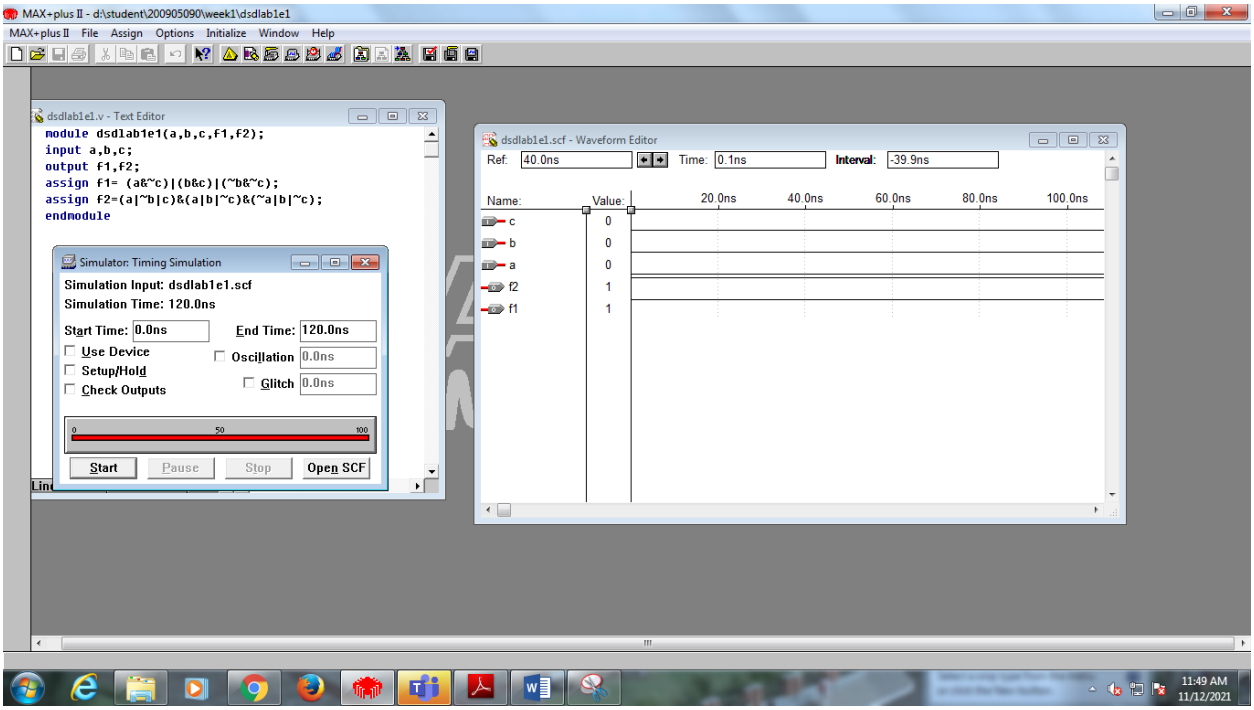
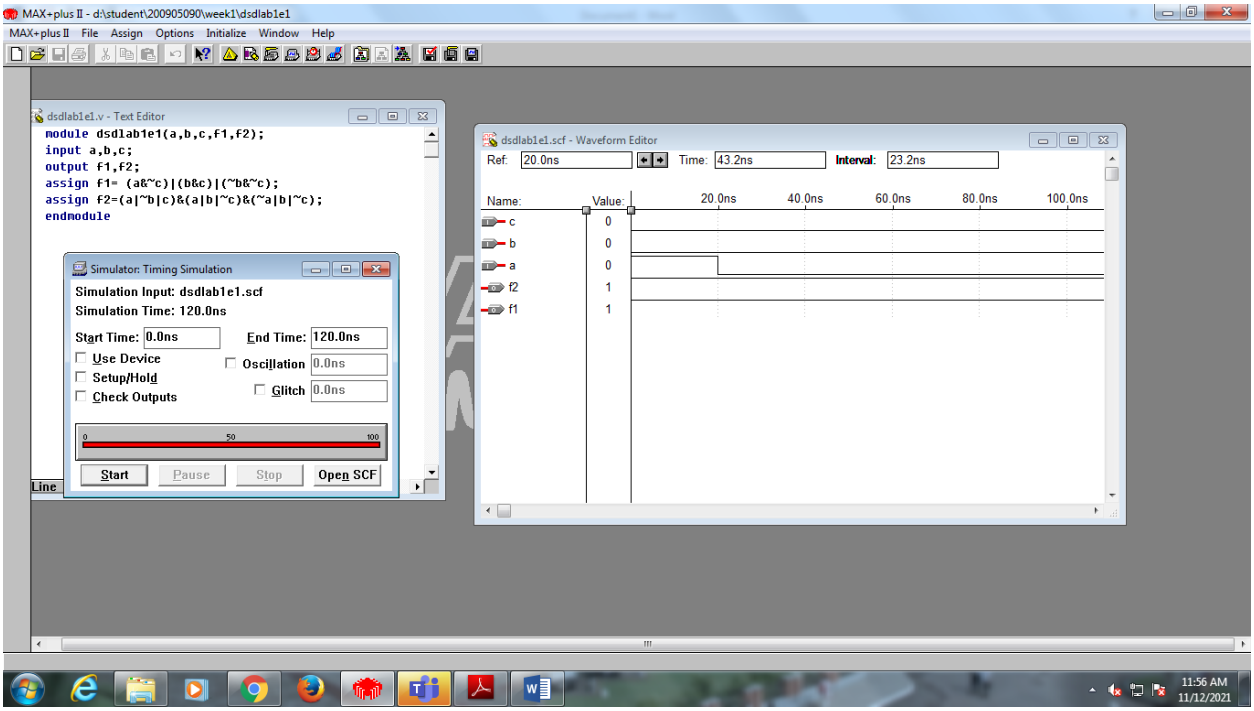
DSD LAB 1

1. Write Verilog code to describe the following functions
f1 =ac'+bc+b'c'
f2 = (a+b'+c)(a+b+c')(a'+b+c')
Check whether f1 and f2 in question 1 are functionally equivalent or not.

Solution:

```
module dsdlab1e1(a,b,c,f1,f2);

input a,b,c;

output f1,f2;

assign f1= (a&~c)|(b&c)|(~b&~c);

assign f2=(a|~b|c)&(a|b|~c)&(~a|b|~c);

endmodule
```

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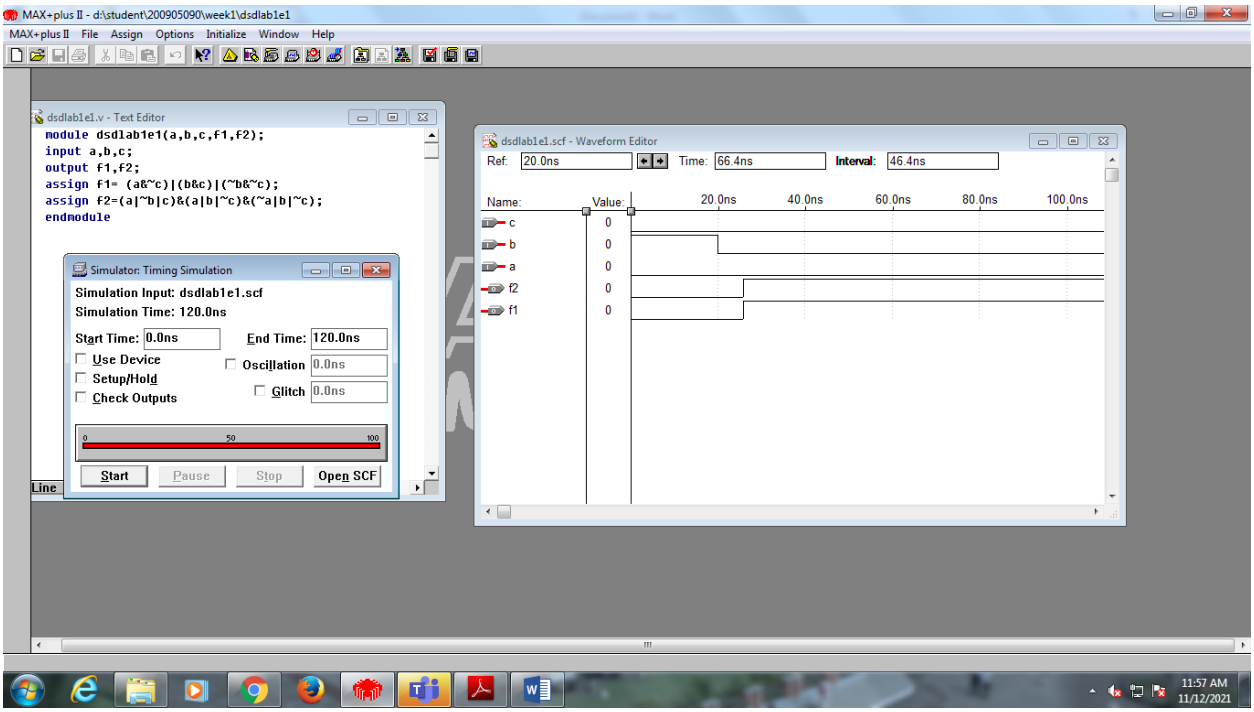
MAX+plus II File Assign Options Initialize Window Help
dsdlab1e1.v - Text Editor
module dsdlab1e1(a,b,c,f1,f2);
input a,b,c;
output f1,f2;
assign f1= (a&~c)|(b&c)|(~b&~c);
assign f2=(a|~b|c)&(a|b|~c)&(~a|b|~c);
endmodule
Simulator: Timing Simulation
Simulation Input: dsdlab1e1.scf
Simulation Time: 120.0ns
Start Time: 0.0ns
End Time: 120.0ns
Use Device
Setup/Hold
Check Outputs
Oscillation 0.0ns
Glitch 0.0ns
Start
Pause
Stop
Open SCF
Line
dsdlab1e1.scf - Waveform Editor
Ref: 20.0ns
Time: 43.2ns
Interval: 23.2ns
Name:
Value:
20.0ns
40.0ns
60.0ns
80.0ns
100.0ns
c 0
b 0
a 0
f2 1
f1 1
11:56 AM
11/12/2021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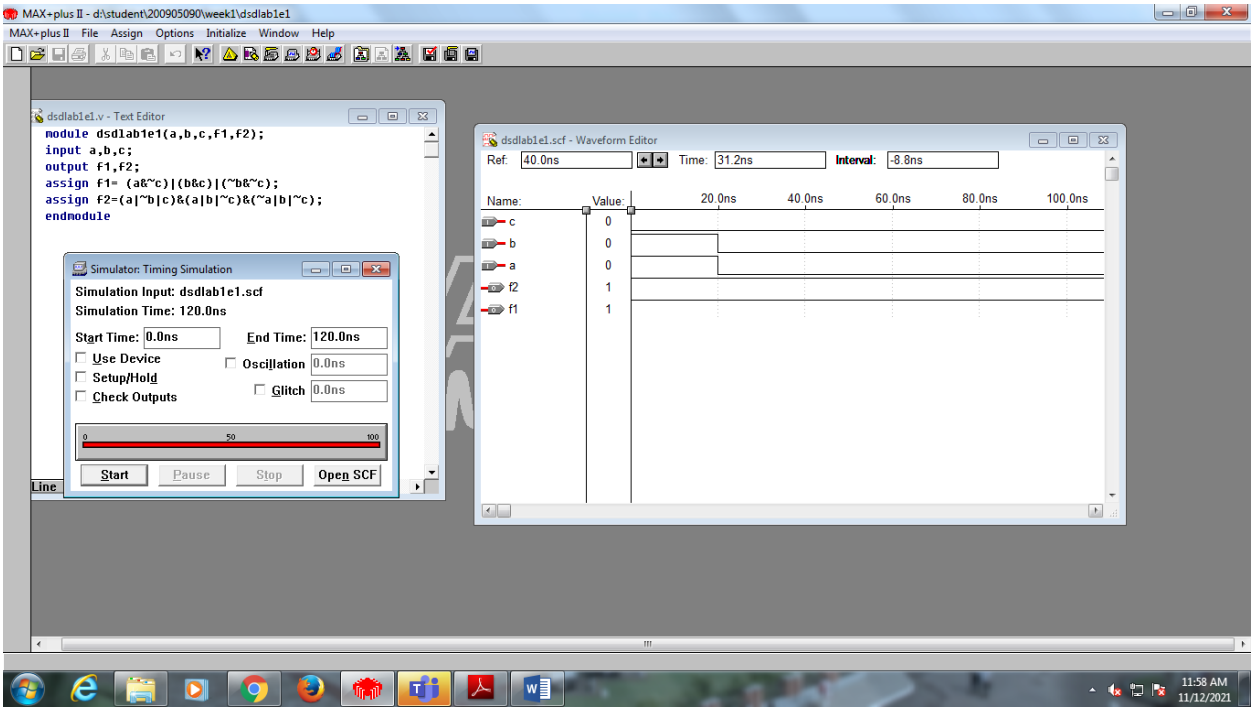
MAX+plus II File Assign Options Initialize Window Help
dsdlab1e1.v - Text Editor
module dsdlab1e1(a,b,c,f1,f2);
input a,b,c;
output f1,f2;
assign f1= (a&~c)|(b&c)|(~b&~c);
assign f2=(a|~b|c)&(a|b|~c)&(~a|b|~c);
endmodule
Simulator: Timing Simulation
Simulation Input: dsdlab1e1.scf
Simulation Time: 120.0ns
Start Time: 0.0ns
End Time: 120.0ns
Use Device
Setup/Hold
Check Outputs
Oscillation 0.0ns
Glitch 0.0ns
Start
Pause
Stop
Open SCF
Line
dsdlab1e1.scf - Waveform Editor
Ref: 20.0ns
Time: 66.4ns
Interval: 46.4ns
Name:
Value:
20.0ns
40.0ns
60.0ns
80.0ns
100.0ns
c 0
b 0
a 0
f2 0
f1 0
11:57 AM
11/12/2021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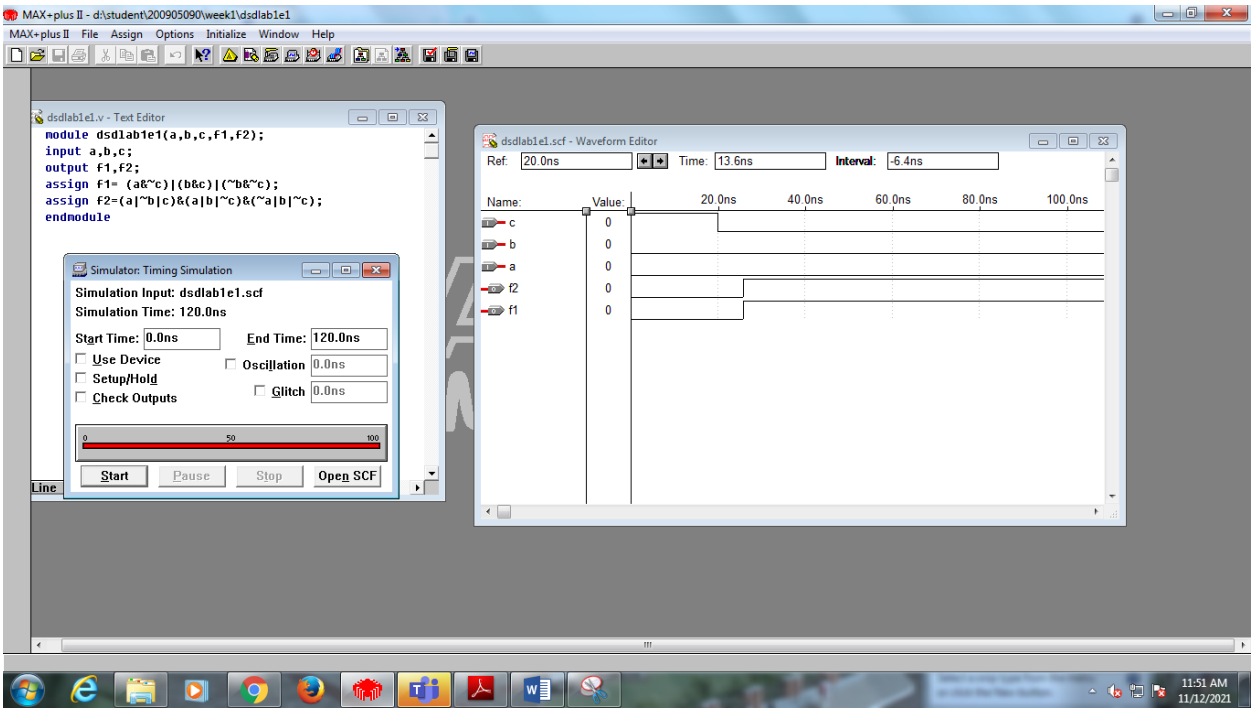
MAX+plus II File Assign Options Initialize Window Help
dsdlab1e1.v - Text Editor
module dsdlab1e1(a,b,c,f1,f2);
input a,b,c;
output f1,f2;
assign f1= (a&~c)|(b&c)|(~b&~c);
assign f2=(a|~b|c)&(a|b|~c)&(~a|b|~c);
endmodule
Simulator: Timing Simulation
Simulation Input: dsdlab1e1.scf
Simulation Time: 120.0ns
Start Time: 0.0ns
End Time: 120.0ns
Use Device
Setup/Hold
Check Outputs
Oscillation 0.0ns
Glitch 0.0ns
Start
Pause
Stop
Open SCF
Line
dsdlab1e1.scf - Waveform Editor
Ref: 40.0ns
Time: 31.2ns
Interval: -8.8ns
Name:
Value:
20.0ns
40.0ns
60.0ns
80.0ns
100.0ns
c 0
b 0
a 0
f2 1
f1 1
11:58 AM
11/12/2021


MAX+plus II - d:\student\200905090\week1\dsdlab1e1
MAX+plus II File Assign Options Initialize Window Help
dsdlab1e1.v - Text Editor
module dsdlab1e1(a,b,c,f1,f2);
input a,b,c;
output f1,f2;
assign f1= (a&~c)|(b&c)|(~b&~c);
assign f2=(a|~b|c)&(a|b|~c)&(~a|b|~c);
endmodule
Simulator: Timing Simulation
Simulation Input: dsdlab1e1.scf
Simulation Time: 120.0ns
Start Time: 0.0ns
End Time: 120.0ns
Use Device
Setup/Hold
Check Outputs
Oscillation 0.0ns
Glitch 0.0ns
Start
Pause
Stop
Open SCF
Line
dsdlab1e1.scf - Waveform Editor
Ref: 20.0ns
Time: 13.6ns
Interval: -6.4ns
Name:
Value:
20.0ns
40.0ns
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80.0ns
100.0ns
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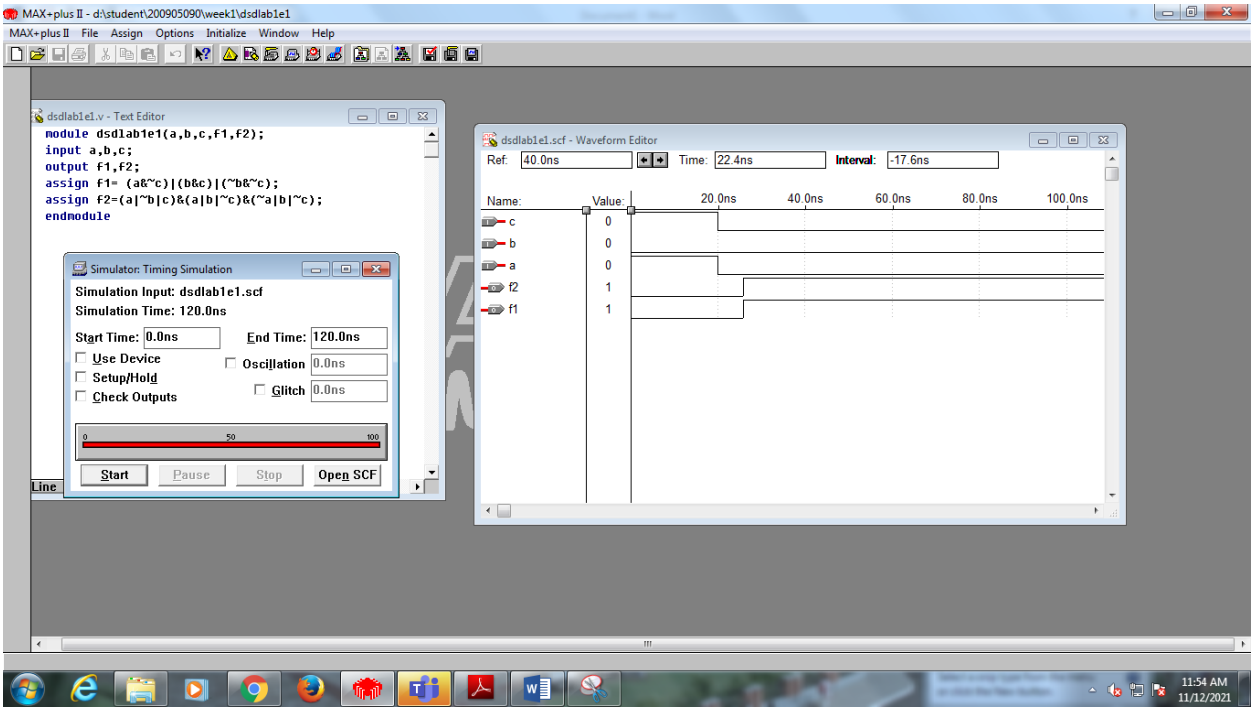
b 0
a 0
f2 0
f1 0
11:51 AM
11/12/2021


MAX+plus II - d:\student\200905090\week1\dsdlab1e1
MAX+plus II File Assign Options Initialize Window Help
dsdlab1e1.v - Text Editor
module dsdlab1e1(a,b,c,f1,f2);
input a,b,c;
output f1,f2;
assign f1= (a&~c)|(b&c)|(~b&~c);
assign f2=(a|~b|c)&(a|b|~c)&(~a|b|~c);
endmodule
Simulator: Timing Simulation
Simulation Input: dsdlab1e1.scf
Simulation Time: 120.0ns
Start Time: 0.0ns
End Time: 120.0ns
Use Device
Setup/Hold
Check Outputs
Oscillation 0.0ns
Glitch 0.0ns
Start
Pause
Stop
Open SCF
dsdlab1e1.scf - Waveform Editor
Ref: 40.0ns
Time: 22.4ns
Interval: -17.6ns
Name:
Value:
20.0ns
40.0ns
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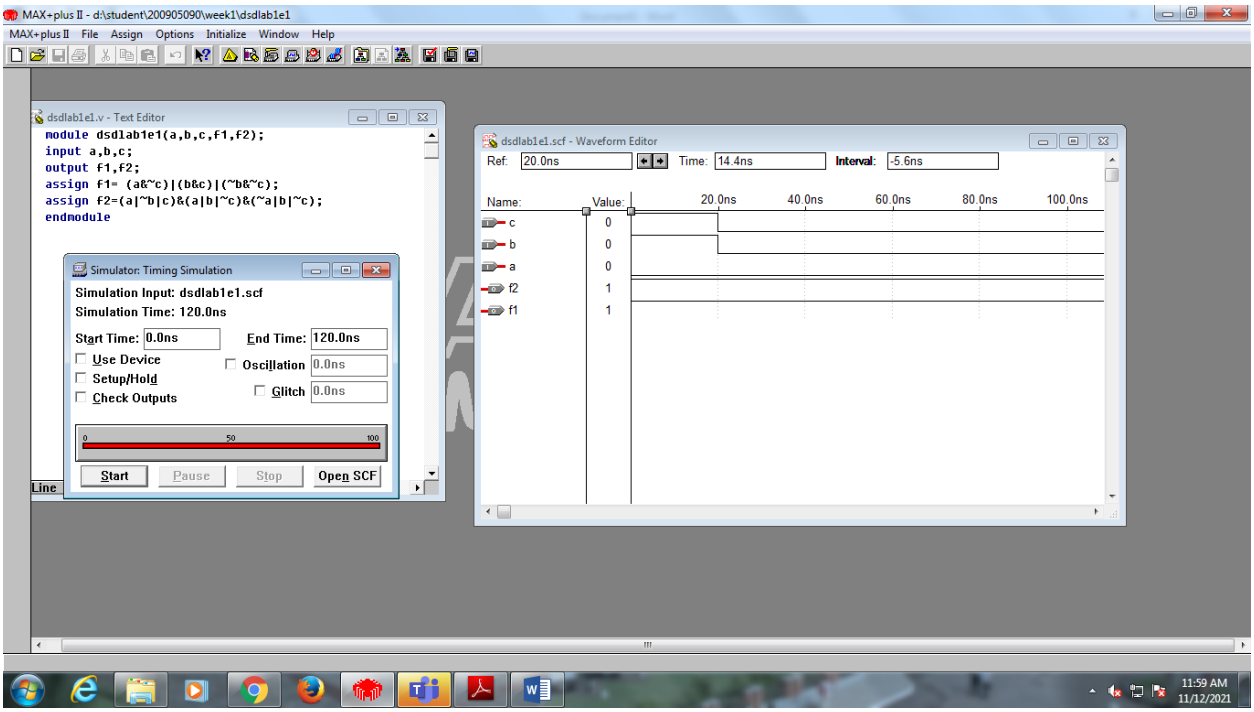
b 0
a 0
f2 1
f1 1
11:54 AM
11/12/2021


MAX+plus II - d:\student\200905090\week1\dsdlab1e1
MAX+plus II File Assign Options Initialize Window Help
dsdlab1e1.v - Text Editor
module dsdlab1e1(a,b,c,f1,f2);
input a,b,c;
output f1,f2;
assign f1= (a&~c)|(b&c)|(~b&~c);
assign f2=(a|~b|c)&(a|b|~c)&(~a|b|~c);
endmodule
Simulator: Timing Simulation
Simulation Input: dsdlab1e1.scf
Simulation Time: 120.0ns
Start Time: 0.0ns
End Time: 120.0ns
Use Device
Setup/Hold
Check Outputs
Oscillation 0.0ns
Glitch 0.0ns
Start
Pause
Stop
Open SCF
dsdlab1e1.scf - Waveform Editor
Ref: 20.0ns
Time: 14.4ns
Interval: -5.6ns
Name:
Value:
20.0ns
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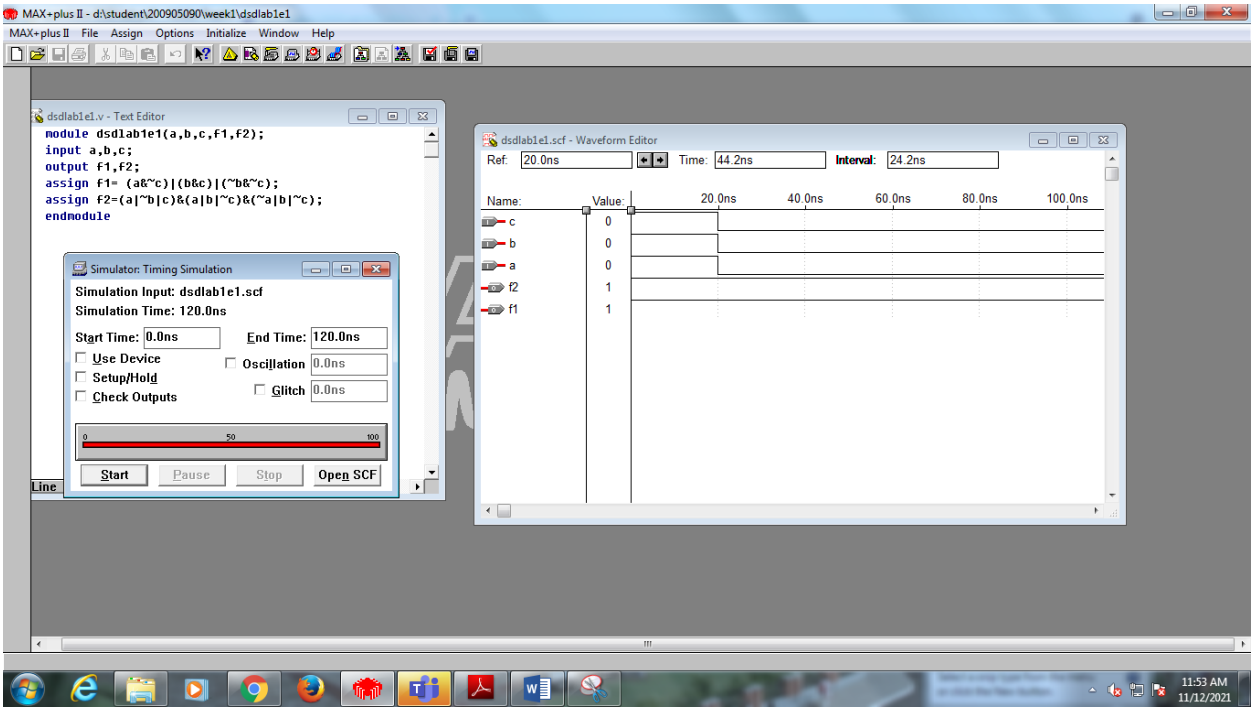
a 0
f2 1
f1 1
11:59 AM
11/12/2021



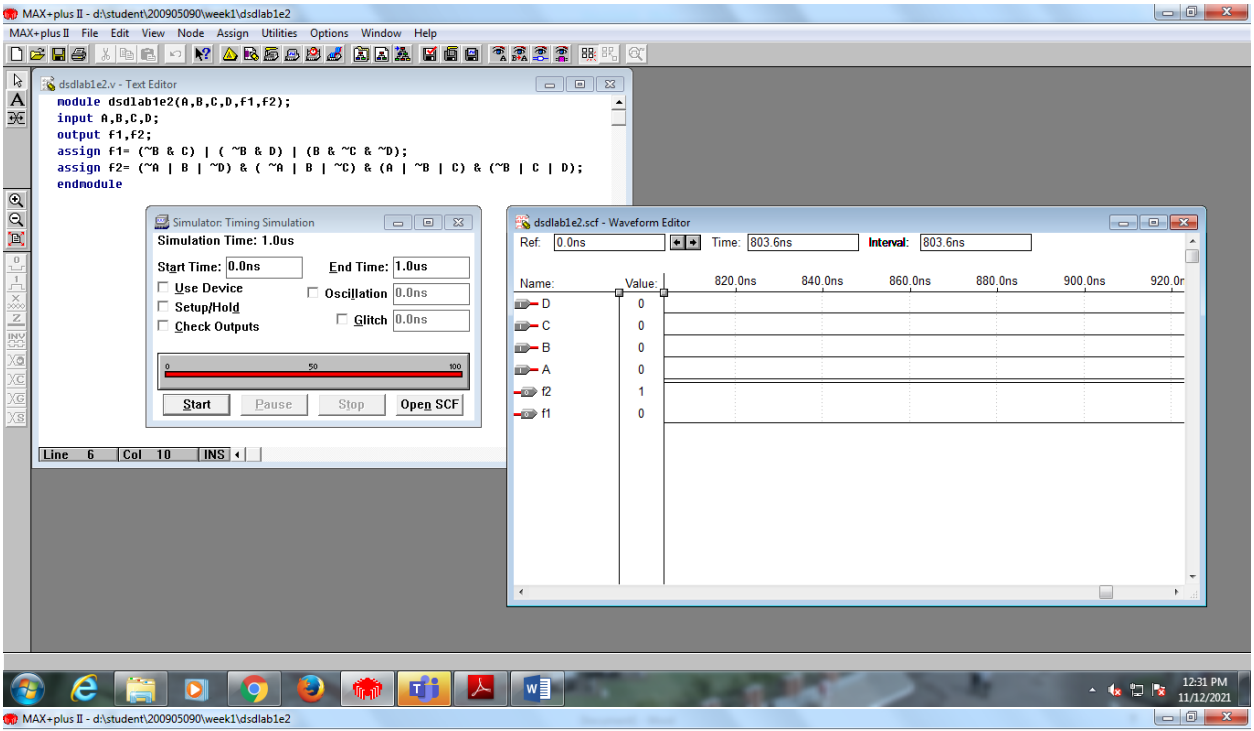
Thus the 2 functions are functionally equivalent.

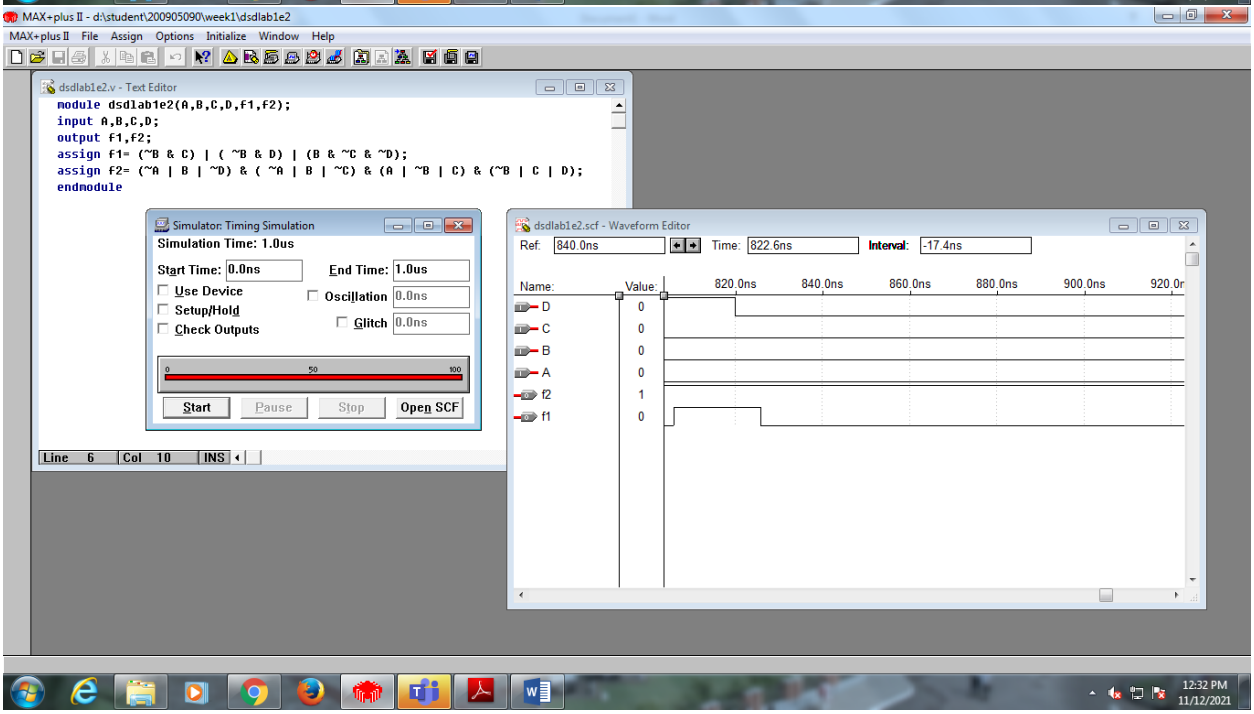
2. Simplify the following functions using K-map and implement the circuit using logic gates. Write
Verilog code and simulate the circuit
a) f(A,B,C,D) = Σm(1,3,4,9,10,12) + D(0,2,5,11)
b) f(A,B,C,D) = ΠM(6,9,10,11,12) + D(2,4,7,13)

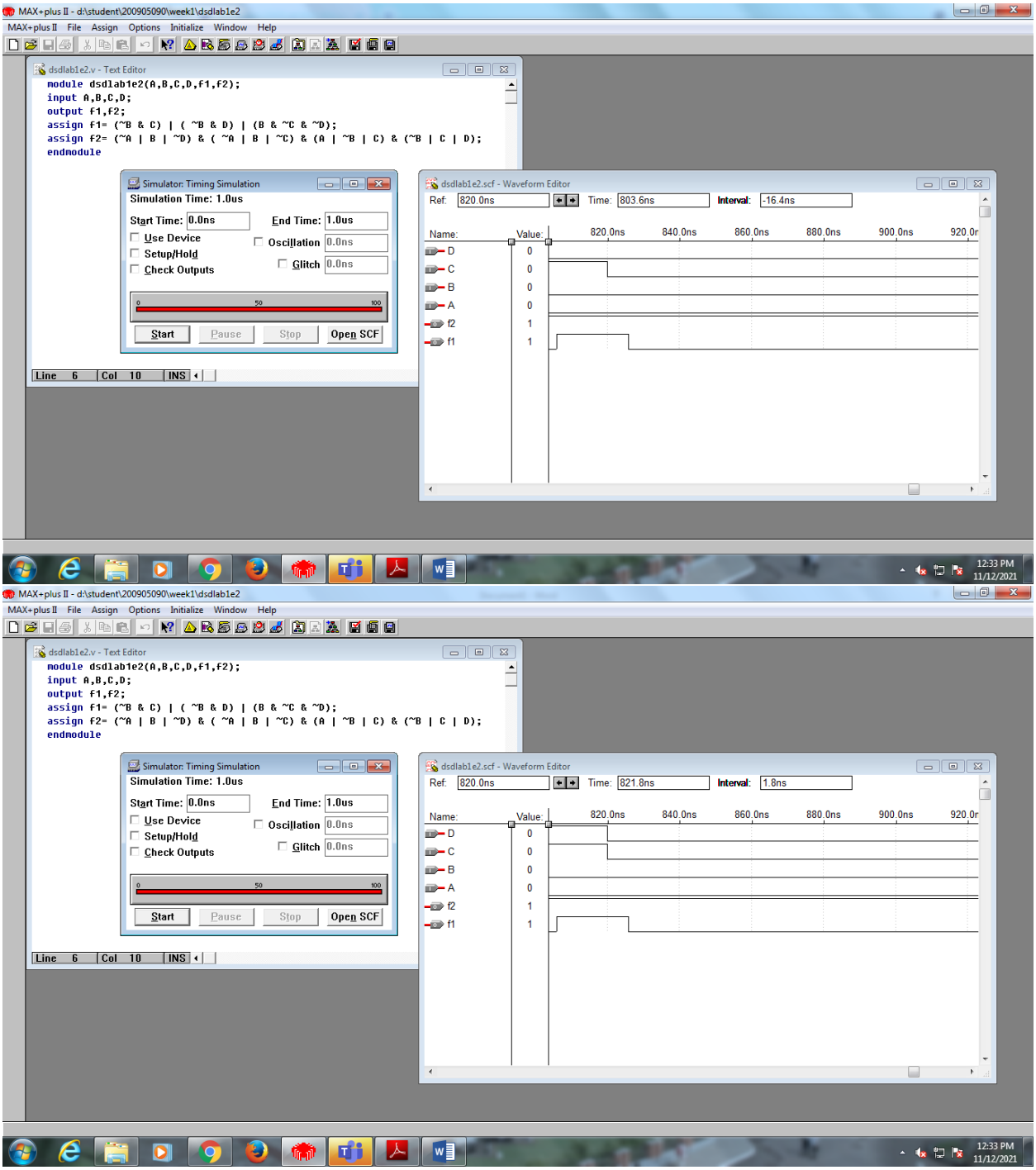
Solution:

a) f1=~BC+~BD+B~C~D
b) f2= (~A+B+~D)(~A+B+~C)(A+~B+C)(~B+C+D)

```
module dsdlab1e2(A,B,C,D,f1,f2);
input A,B,C,D;
output f1,f2;
assign f1= (~B & C) | ( ~B & D) | (B & ~C & ~D);
assign f2= (~A | B | ~D) & ( ~A | B | ~C) & (A | ~B | C) & (~B | C | D);
endmodule
```


MAX+plus II - d:\student\200905090\week1\dsdlab1e2
MAX+plus II File Edit View Node Assign Utilities Options Window Help
dsdlab1e2.v - Text Editor
module dsdlab1e2(A,B,C,D,f1,f2);
input A,B,C,D;
output f1,f2;
assign f1= (~B & C) | (~B & D) | (B & ~C & ~D);
assign f2= (~A | B | ~D) & (~A | B | ~C) & (A | ~B | C) & (~B | C | D);
endmodule
Simulator: Timing Simulation
Simulation Time: 1.0us
Start Time: 0.0ns
End Time: 1.0us
Use Device
Oscillation 0.0ns
Setup/Hold
Glitch 0.0ns
Check Outputs
Start Pause Stop Open SCF
Line 6 Col 10 INS
dsdlab1e2.scf - Waveform Editor
Ref: 0.0ns
Time: 803.6ns
Interval: 803.6ns
Name: Value: 820.0ns 840.0ns 860.0ns 880.0ns 900.0ns
D 0
C 0
B 0
A 0
f2 1
f1 0
12:31 PM
11/12/2021


MAX+plus II - d:\student\200905090\week1\dsdlab1e2
MAX+plus II File Assign Options Initialize Window Help
dsdlab1e2.v - Text Editor
module dsdlab1e2(A,B,C,D,f1,f2);
input A,B,C,D;
output f1,f2;
assign f1= (~B & C) | (~B & D) | (B & ~C & ~D);
assign f2= (~A | B | ~D) & (~A | B | ~C) & (A | ~B | C) & (~B | C | D);
endmodule
Simulator: Timing Simulation
Simulation Time: 1.0us
Start Time: 0.0ns
End Time: 1.0us
Use Device
Oscillation 0.0ns
Setup/Hold
Glitch 0.0ns
Check Outputs
Start Pause Stop Open SCF
Line 6 Col 10 INS
dsdlab1e2.scf - Waveform Editor
Ref: 840.0ns
Time: 822.6ns
Interval: -17.4ns
Name: Value: 820.0ns 840.0ns 860.0ns 880.0ns 900.0ns
D 0
C 0
B 0
A 0
f2 1
f1 0
12:32 PM
11/12/2021



3. Minimize the following expression using K-map and simulate using only NAND gates.
f(A,B,C,D)= πM(2,6,8,9,10,11,14)

```
module dsdlab1e3(A,B,C,D,f);
input A,B,C,D;
output f;
wire g;
assign g=~(~(A&~(B&B))&~(C&~(D&D)));
```

```
assign f=~(g&g);
endmodule
```