

**Department of Information & Communication Technology**  
**MIT, Manipal**

**III Sem B. Tech (IT/CCE),**  
**ICT 2154 Digital Systems / ICT 2171 Digital Systems and Computer Organization**  
**In-sem Examination**

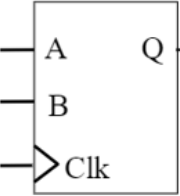
**Date: 15/12/2021**

**Max. Marks: 20**

**Write-up Time: 10.30 to 11.50am**

**Upload time: 11.50am to 12.00pm**

**Note to Students: Answer ALL Questions**

| <b>Q1.</b> | Design the following combinational circuit using single 7485IC, 7483IC and minimum number of half adder blocks.<br><br>If $A > B$ , $F = 2A + 3B$<br><br>Else $F = 3A - 2B$<br><br>Where A and B are 2-bit binary numbers.  | <b>3 Marks</b> |   |        |   |   |    |   |   |   |   |   |   |   |   |   |                |
|------------|---|----------------|---|--------|---|---|----|---|---|---|---|---|---|---|---|---|----------------|
| <b>Q2.</b> | Construct a hexadecimal up counter to count from 0 to 41H using only one 7490 IC and one 7493 IC. Draw the logic diagram.   | <b>3 Marks</b> |   |        |   |   |    |   |   |   |   |   |   |   |   |   |                |
| <b>Q3.</b> | Design a 2-bit magnitude comparator using 74151 ICs and minimum external gates.   | <b>3 Marks</b> |   |        |   |   |    |   |   |   |   |   |   |   |   |   |                |
| <b>Q4.</b> | Function table defines the working of a fictitious AB flip flop. Design the AB flip flop using D flip flop and external gates. <table border="1" style="display: inline-table; vertical-align: middle;"> <thead> <tr> <th>A</th><th>B</th><th>Q(t+1)</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>Q'</td></tr> <tr> <td>0</td><td>1</td><td>0</td></tr> <tr> <td>1</td><td>0</td><td>1</td></tr> <tr> <td>1</td><td>1</td><td>Q</td></tr> </tbody> </table>  | A              | B | Q(t+1) | 0 | 0 | Q' | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | Q | <b>3 Marks</b> |
| A          | B   | Q(t+1)         |   |        |   |   |    |   |   |   |   |   |   |   |   |   |                |
| 0          | 0   | Q'             |   |        |   |   |    |   |   |   |   |   |   |   |   |   |                |
| 0          | 1   | 0              |   |        |   |   |    |   |   |   |   |   |   |   |   |   |                |
| 1          | 0   | 1              |   |        |   |   |    |   |   |   |   |   |   |   |   |   |                |
| 1          | 1   | Q              |   |        |   |   |    |   |   |   |   |   |   |   |   |   |                |
| <b>Q5.</b> | Design a JK flip flop using a basic NOR latch and gates.  | <b>4 Marks</b> |   |        |   |   |    |   |   |   |   |   |   |   |   |   |                |
| <b>Q6.</b> | Design a code converter to convert a decimal digit represented in gray code to a decimal digit represented in self-complementary 4221 code using minimum number of 3 to 8 decoders with active high output and active high enable input, and external gates.  | <b>4 Marks</b> |   |        |   |   |    |   |   |   |   |   |   |   |   |   |                |