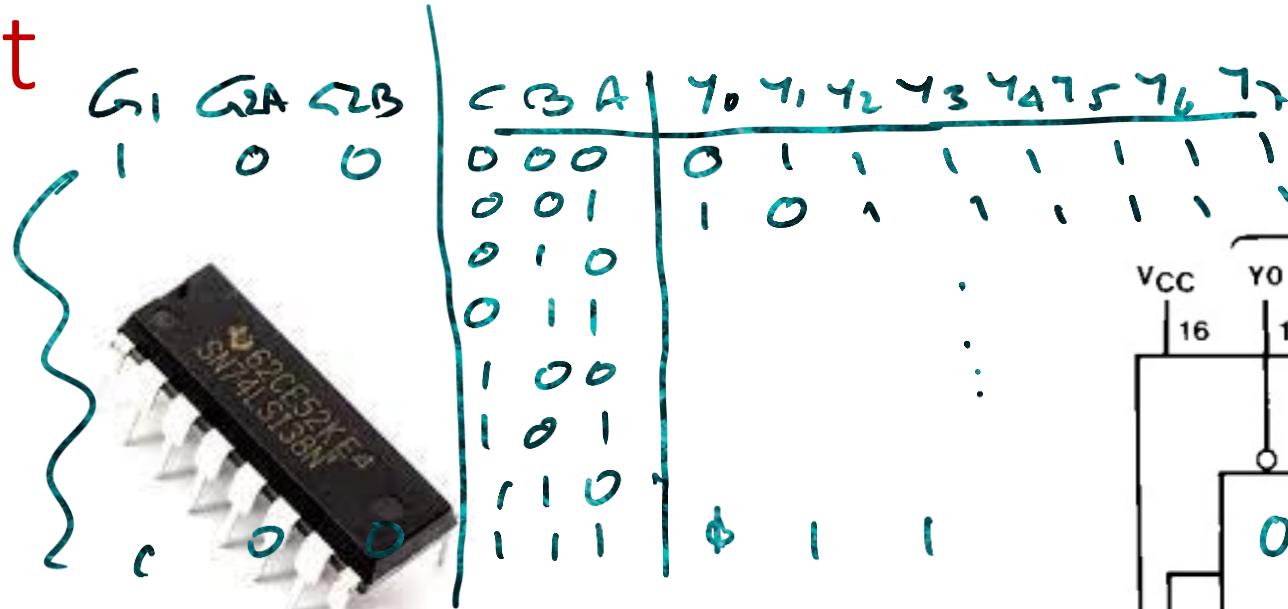


# **DECODERS AND ENCODERS**

Students are advised to write down the notes for every lecture

# 74138 IC: 3-to-8 line decoder with active low output



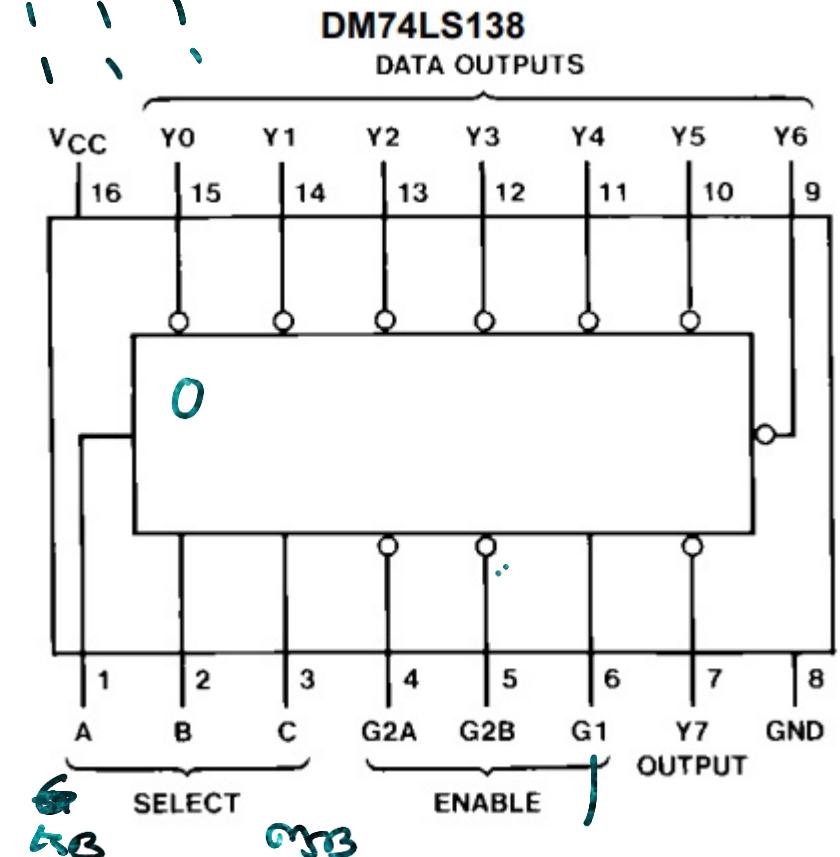
$G_1$  - Active high enable

$G_{2A}$  } Active low input enable

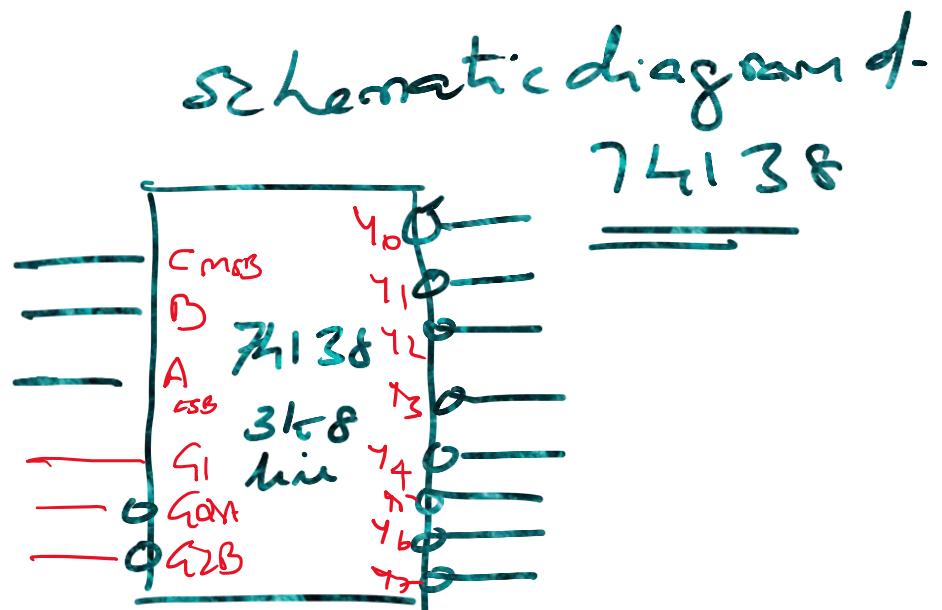
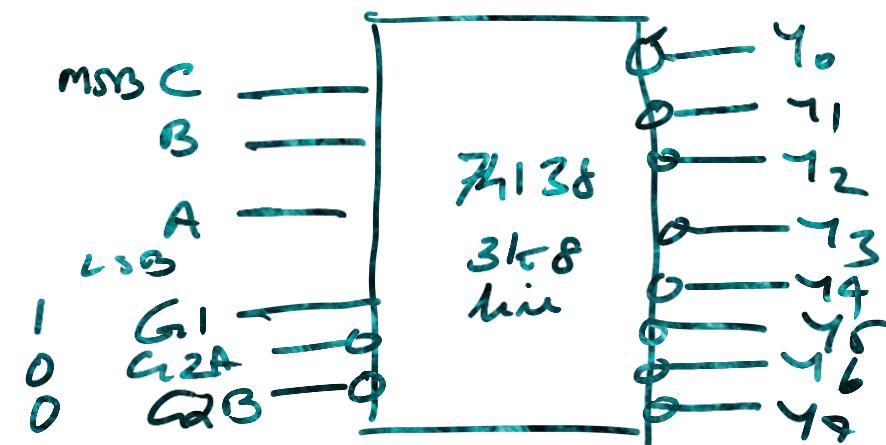
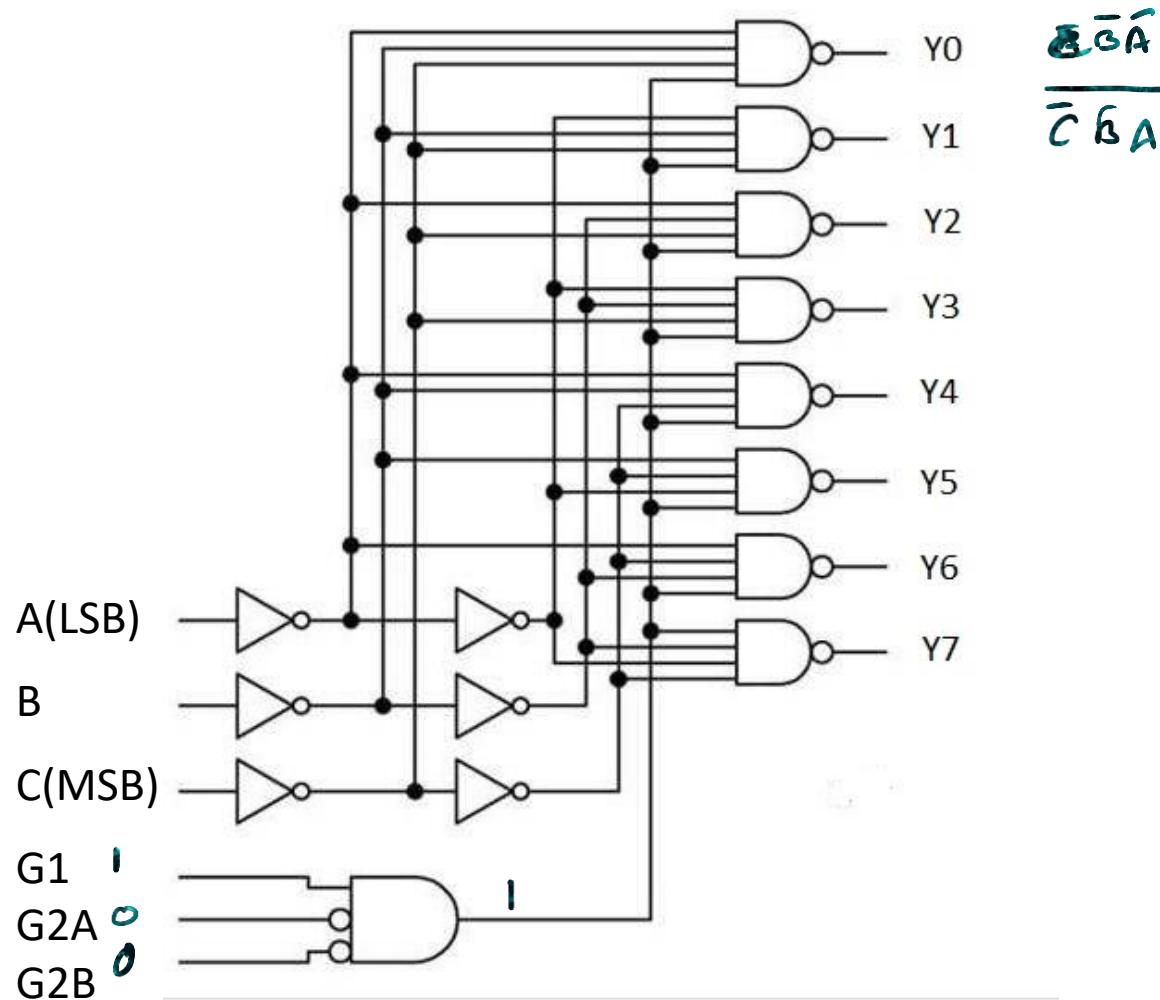
$G_{2B}$

3-select ip

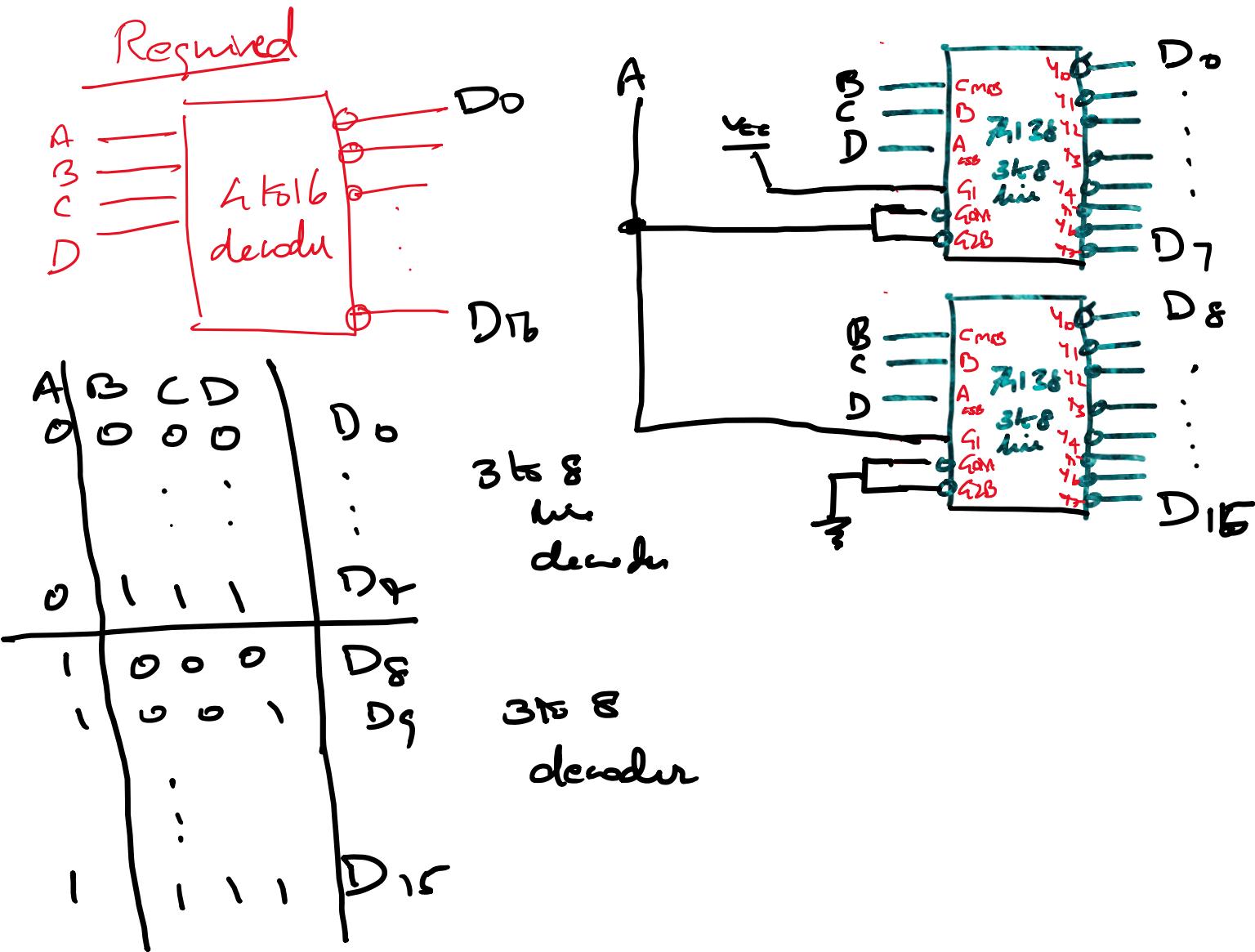
$c \beta A$   
msb      lsb



# 74138 IC internal diagram

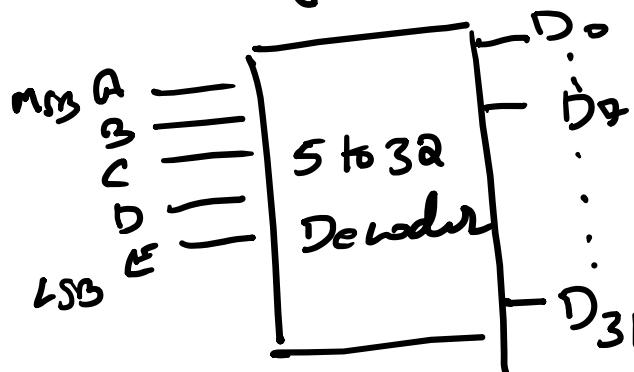


# Design 4-to-16 decoder using minimum of 74138 ICs ONLY

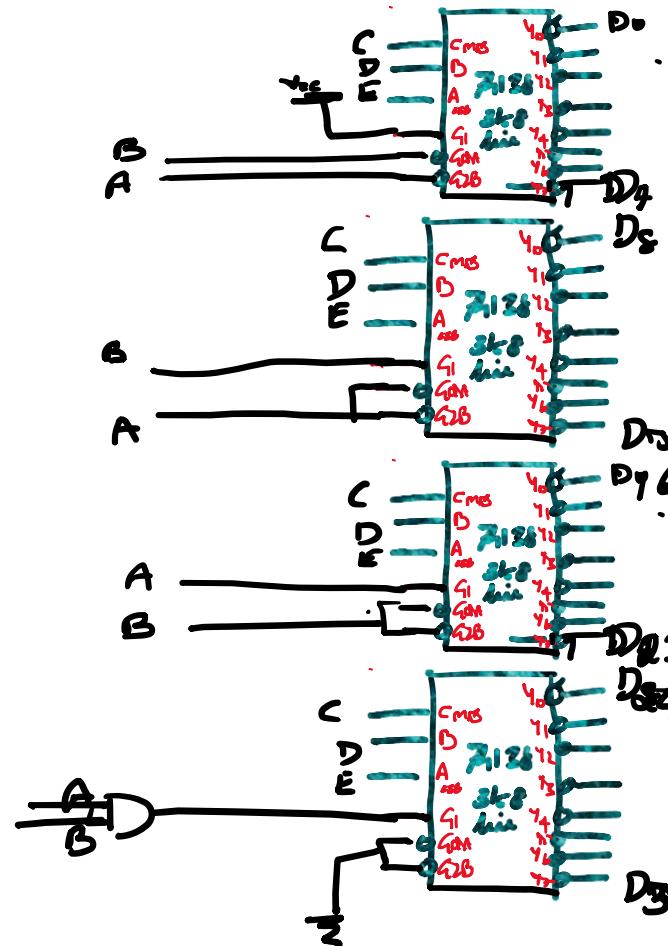


Design 5-to-32 decoder with active low output using minimum of 74138 ICs and one external gate ONLY

Required  
to design



A	B	C	D	E	D <sub>0</sub>	D <sub>31</sub>
0	0	0	0	0	1	1
0	0	0	0	1	0	1
0	0	0	1	0	1	0
0	0	0	1	1	0	0
0	0	1	0	0	0	1
0	0	1	0	1	1	0
0	0	1	1	0	0	1
0	0	1	1	1	1	0
0	1	0	0	0	0	0
0	1	0	0	1	1	0
0	1	0	1	0	0	1
0	1	0	1	1	1	0
0	1	1	0	0	0	0
0	1	1	0	1	1	0
0	1	1	1	0	0	1
0	1	1	1	1	1	0
1	0	0	0	0	0	0
1	0	0	0	1	1	0
1	0	0	1	0	0	1
1	0	0	1	1	1	0
1	0	1	0	0	0	0
1	0	1	0	1	1	0
1	0	1	1	0	0	1
1	0	1	1	1	1	0
1	1	0	0	0	0	0
1	1	0	0	1	1	0
1	1	0	1	0	0	1
1	1	0	1	1	1	0
1	1	1	0	0	0	0
1	1	1	0	1	1	0
1	1	1	1	0	0	1
1	1	1	1	1	1	0



A<sub>3</sub>  
0 0

A<sub>3</sub>  
0 1

A<sub>3</sub>  
1 0

A<sub>3</sub>  
1 1

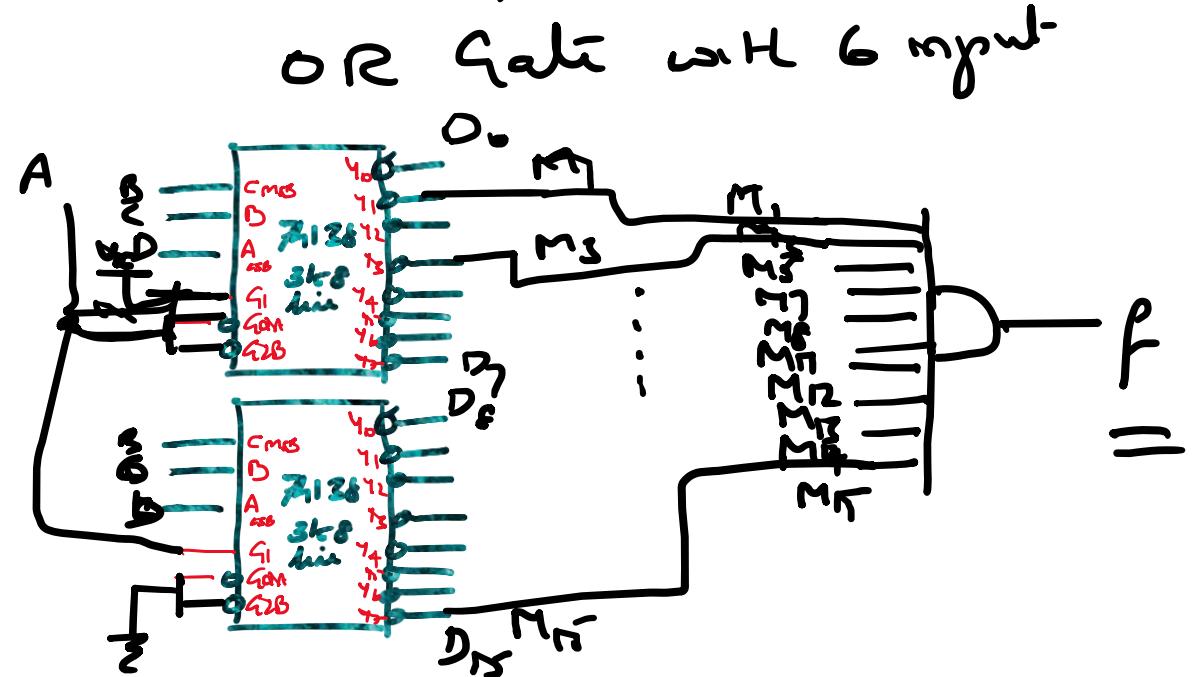
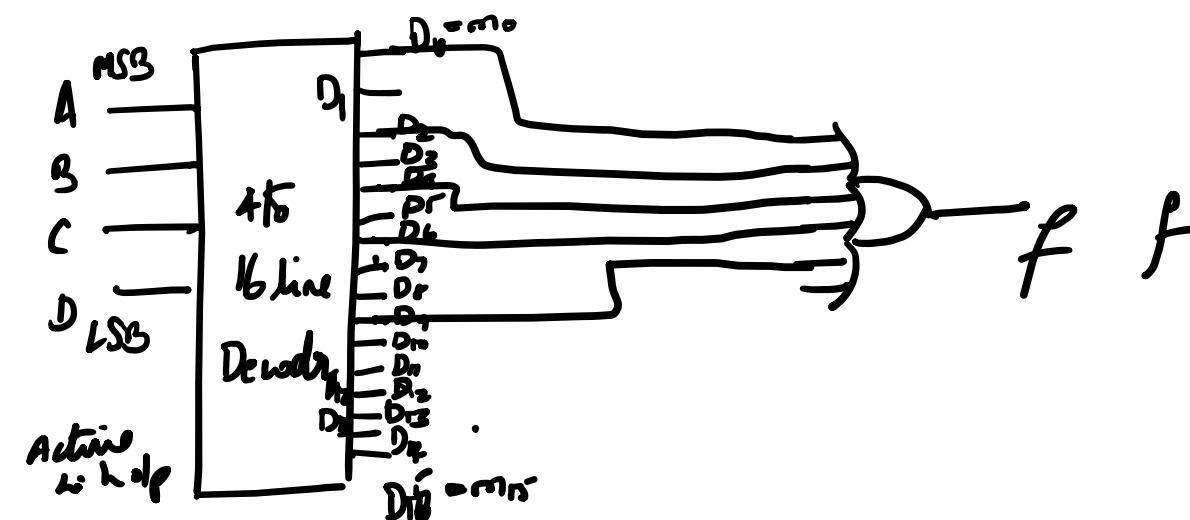
Implement  $f(A, B, C, D) = \sum m(0, 2, 4, 6, 9, 10)$  using suitable decoder and external gates

$$f(A, B, C, D) = \sum_{m=0, 2, 4, 6, 9, 10} \propto = \overline{\prod}_{m=1, 3, 5, 7, 8, 11, 12, 13, 14, 15} \rightarrow m_0 \cdot \overline{m}_3 \cdot \overline{m}_5 \cdot \overline{m}_1 \cdot \dots \cdot \overline{m}_{15}$$

use 4 to 16 decoders

$$= m_0 + m_2 + m_4 + m_6 + m_9 + m_{10}$$

OR Gate with 6 inputs



4 to 16 line  
Decoder with  
 $74138_A$

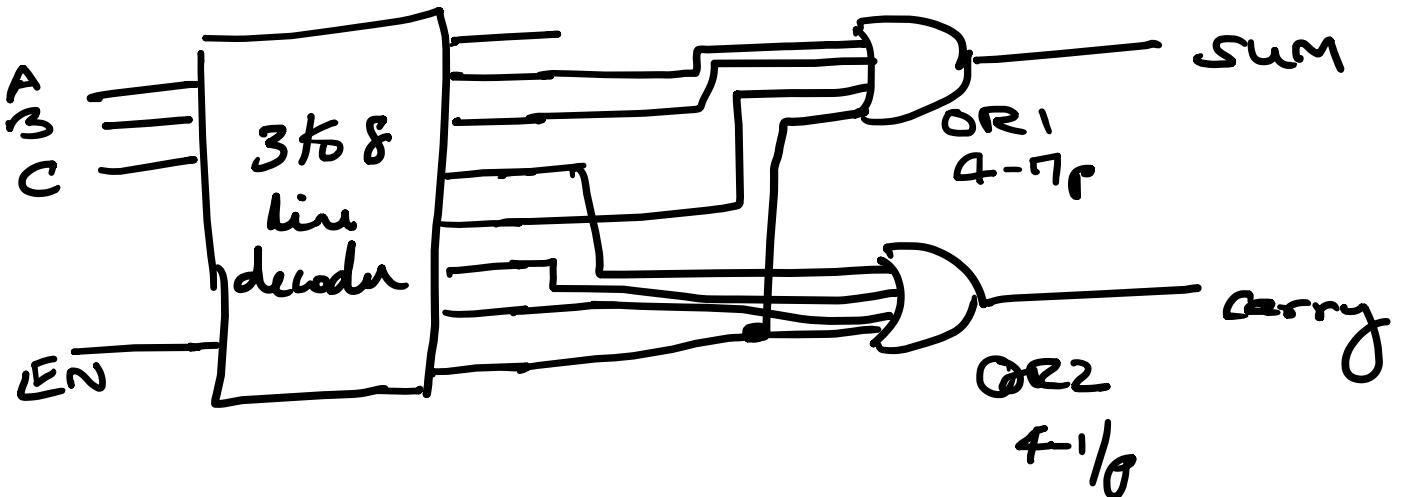
$\delta =$

Design a full adder using 3-to-8 line decoder and external gates

Inputs			Outputs	
A	B	C <sub>in</sub>	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$\text{Sum} = \sum_m 1, 2, 4, 7 = \prod_{\overline{m}} 0, 3, 5, 6$$

$$\text{Carry} = \sum_m \underline{\underline{3, 5, 6, 7}} = \prod_{\overline{m}} 0, 1, 2, 4,$$

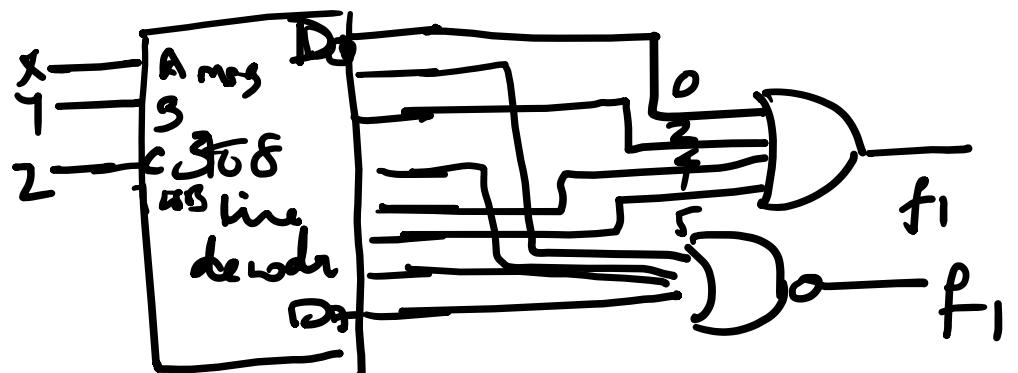


Realize  $f_1(x,y,z) = \prod M(1,3,6,7)$  using

- 3-to-8 line decoder with active high output and suitable gates
- 74138 decoder and suitable gates

$$f_1(x,y,z) = \prod_{M} 1, 3, 6, 7 = \sum_m 0, 2, 4, 5 \\ = M_1 \cdot \overline{M}_3 \cdot \overline{M}_6 \cdot M_7$$

Note: Active low o/p decoder  
& an (AND gate with 4-1 o/p)



Active HIGH o/p  
o/p  $\Rightarrow$  minterms

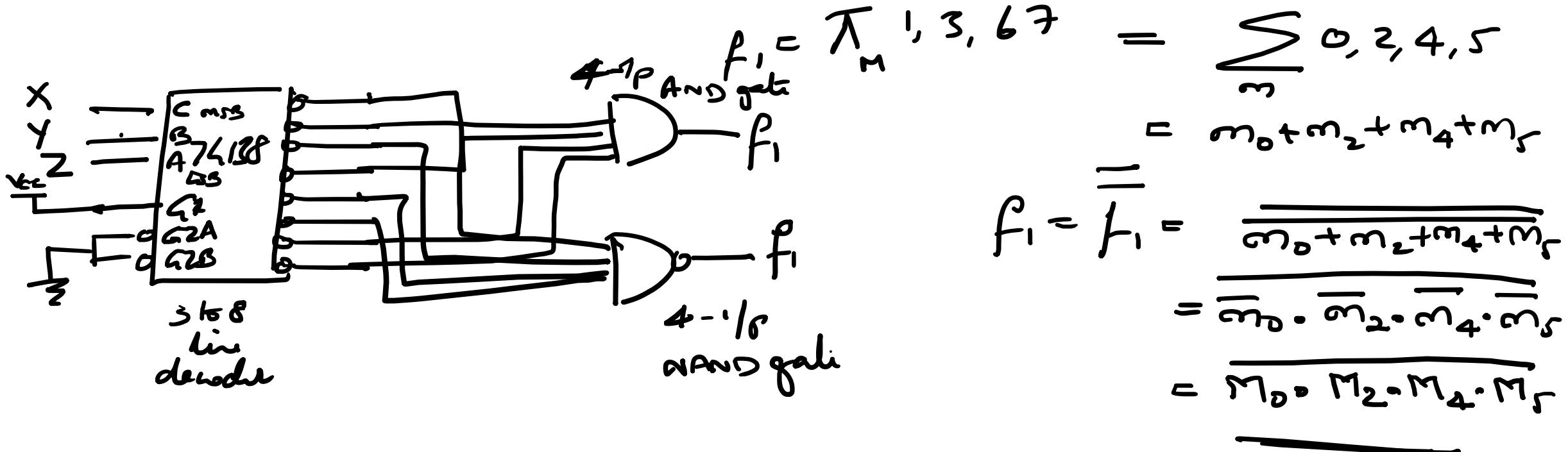
if we have active high o/p  
3 to 8 decoder then,  
using 4-1 o/p organi

$$f_1 = \overline{\overline{f_1}} = \overline{M_1 \cdot M_3 \cdot M_6 \cdot M_7} \\ = \overline{\overline{M_1} + \overline{M_3} + \overline{M_6} + \overline{M_7}} = \overline{m_1 + m_3 + m_6 + m_7}$$

Please Note: from MAX terms  
we can get the design  
implemented using NOR gates

Realize  $f_1(x,y,z) = \Pi M(1,3,6,7)$  using

- 3-to-8 line decoder with active high output and suitable gates
- 74138 decoder and suitable gates



Design a code converter to convert a decimal digit represented in 84-2-1 code to a decimal digit represented in excess-3 code using 74138 decoder and external gates..

	$\delta$	$\gamma$	-2	-1	$D_{\text{ess}}$	$E_3$	$E_2$	$E_1$	$E_0$
0	$m_0$	0	0	0	1	0	0	-1	-1
X	$m_1$	0	0	1	X	X	X	X	X
X	$m_2$	0	1	0	X	X	X	X	X
X	$m_3$	0	1	1	X	X	X	X	X
$\gamma$	$m_4$	1	0	0	1	0	-1	-1	-1
3	$m_5$	1	0	1	1	0	1	1	0
2	$m_6$	1	1	0	1	0	1	0	1
1	$m_7$	1	1	1	1	0	1	0	0
8	$m_8$	1	0	0	0	-1	0	1	1
7	$m_9$	C	0	0	1	-1	0	1	0
6	$m_{10}$	1	0	0	1	-1	0	0	1
5	$m_{11}$	1	0	1	1	-1	0	0	0
X	$m_{12}$	1	0	0	X	X	X	X	X
X	$m_{13}$	1	0	0	X	X	X	X	X
X	$m_{14}$	1	1	0	X	X	X	X	X
9	$m_{15}$	1	1	1	1	-1	1	0	0

$$E_3 = \sum_{\text{S}} 8, 9, 10, 11, 15 = \prod_{\text{M}} 0, 4, 5, 6, 7$$

$$\sum_{n=1}^{\infty} \frac{(-1)^{n+1}}{n} = \ln(2)$$

$$E_1 = \sum_m 0, 4, 5, 8, 9 = \prod_m 6, 7, 10, 11, 15$$

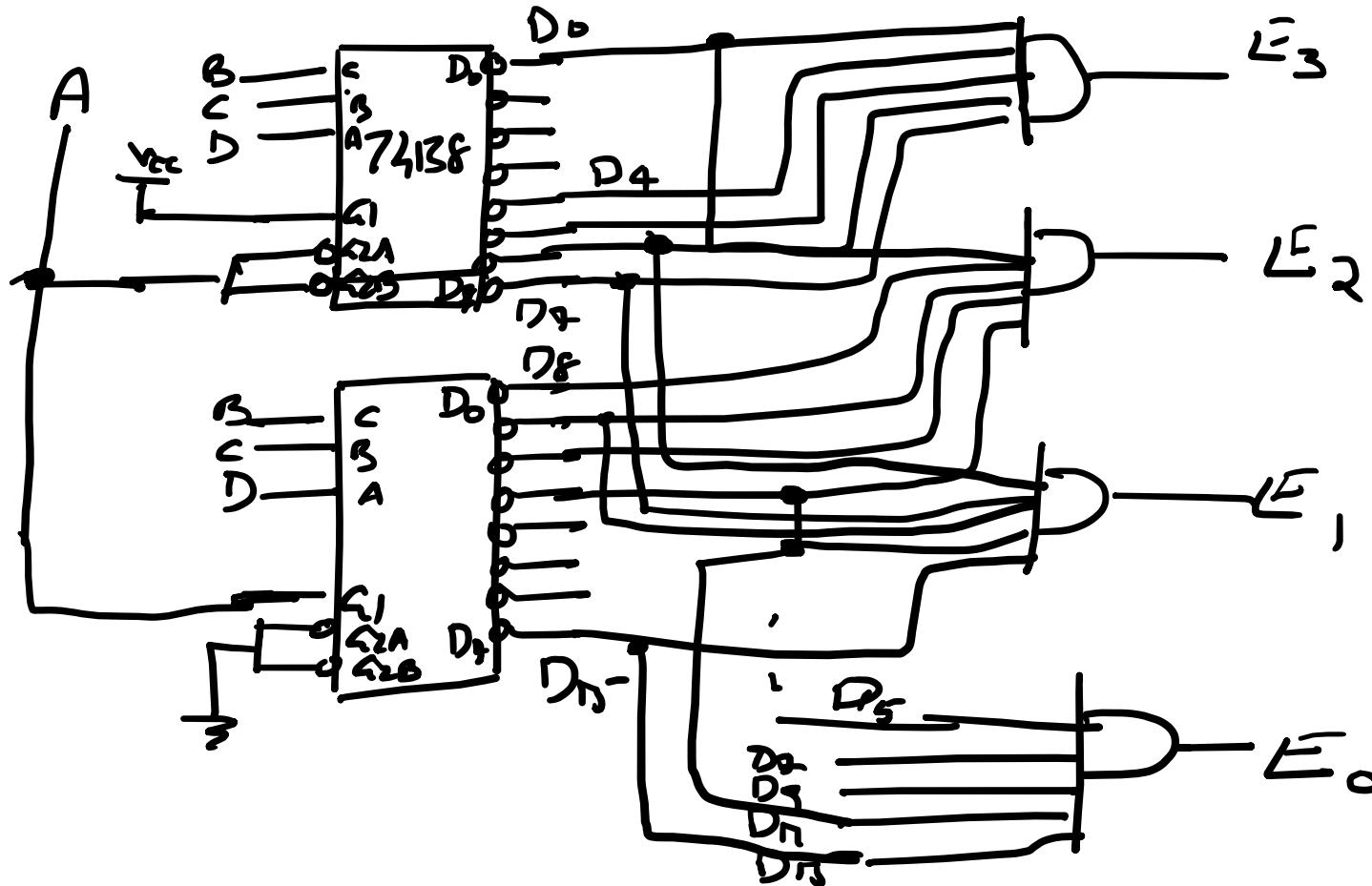
$$E_0 = \sum_{m=0}^{\infty} 0, 4, 6, 8, 10 = \prod_{m=1}^{\infty} 5, 7, 9, 11, 15$$

## Code converter design....

74138 & AND gates

using 74138: 3 to 8 line decoder w.tl active low o/p's.

Maxterms & AND Gates:



$$E_3 = \prod_M 0, 4, 5, 6, 7$$

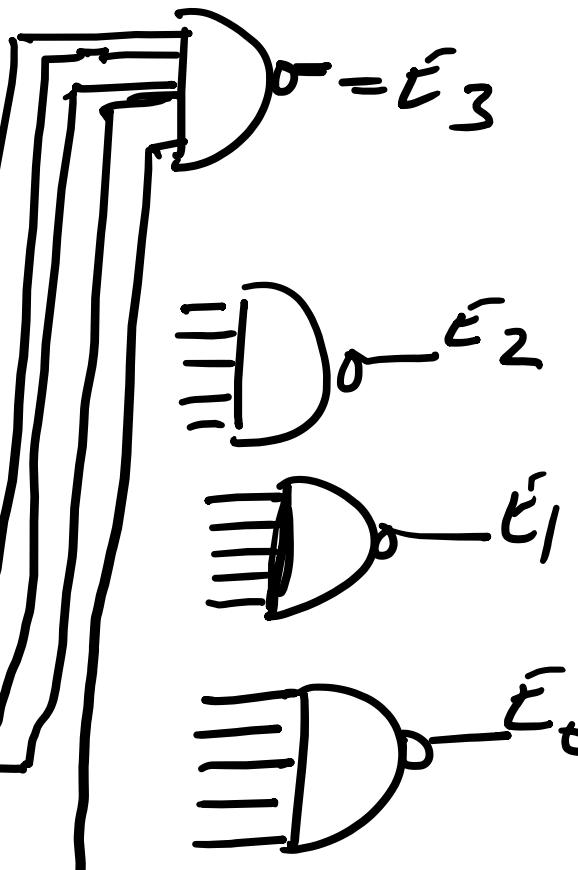
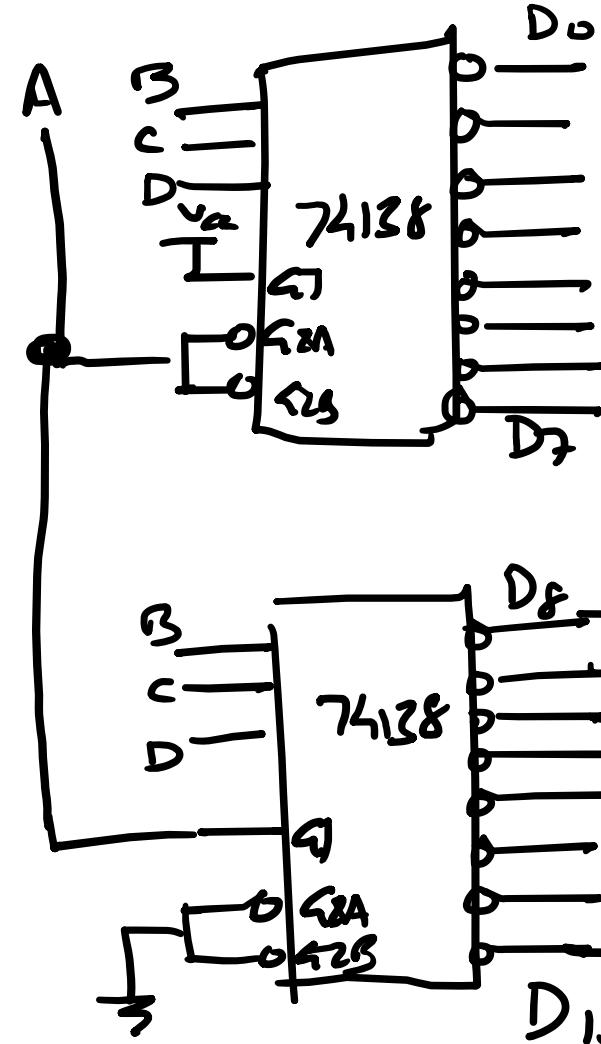
$$E_2 = \prod_M 0, 8, 9, 10, 11$$

$$E_1 = \prod_M 6, 7, 10, 11, 15$$

$$E_0 = \prod_M 5, 7, 9, 11, 15$$

Code converter design... using 74138 & NAND gates

4 to 16 decoder



$$E_3 = \sum_{3} 8, 9, 10, 11, 15$$

$$\bar{E}_2 = \sum_{3} 4, 5, 6, 7, 15$$

$$E_1 = \sum_{3} 0, 4, 5, 8, 9$$

$$\bar{E}_0 = \sum_{3} 0, 4, 6, 8, 10$$

$$\cdot E_3 \leftarrow \frac{m_8 + m_9 + m_{10} + m_{11} + m_{15}}{M_8 \cdot M_9 \cdot M_{10} \cdot M_{11} \cdot M_{15}}$$

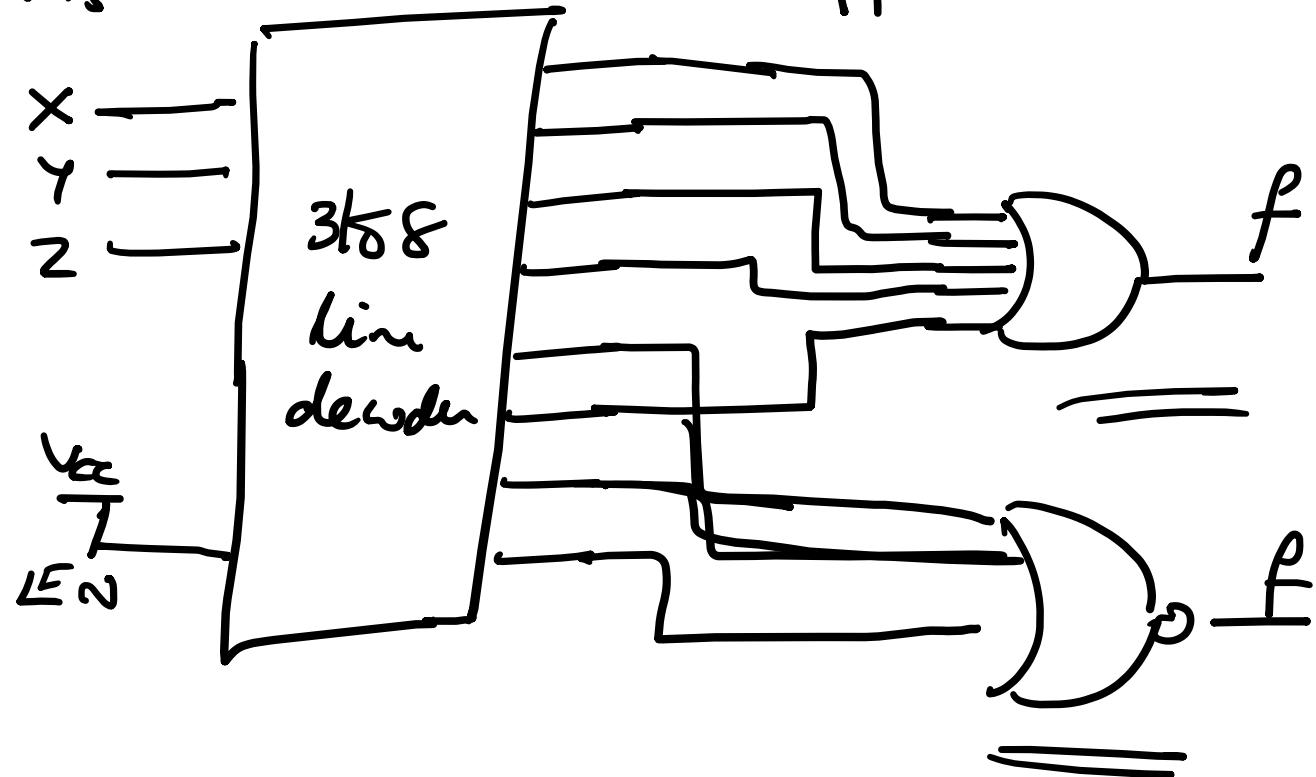
$$\leftarrow \frac{1}{M_8 \cdot M_9 \cdot M_{10} \cdot M_{11} \cdot M_{15}}$$

Example  $f = \bar{x} + \bar{y}z$

Design  $f(x,y,z) = x' + y'z$  using 3-to-8 line decoder and external gates.

$$\begin{aligned}
 f(x,y,z) &= \bar{x}(y+\bar{y})(z+\bar{z}) + (\bar{x}+x)\bar{y}z \\
 &= \bar{x}yz + \bar{x}\bar{y}z + \bar{x}\bar{y}\bar{z} + \bar{x}\bar{y}\bar{z} + \bar{x}\bar{y}z + x\bar{y}z \\
 &= m_3 + m_2 + m_4 + m_0 + m_1 + m_5
 \end{aligned}
 \quad \sum_{0,1,2,3,5} = \Rightarrow \prod_{4,6,7}$$

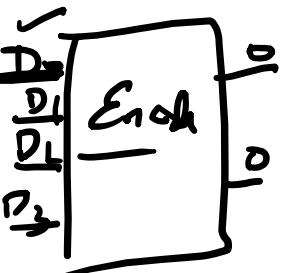
$x$	$y$	$z$	$f$
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0



# Encoder:

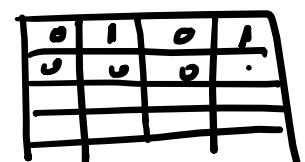
- Combinational circuit that performs inverse operation of a decoder.
- Encoder has  $2^n$  (or fewer) input lines and n output lines. Ex: 4-to-2 line, 8-to-3 line...etc
- 4-to-2 encoder is given below:

Truth table



$m_2$   
 $m_1$

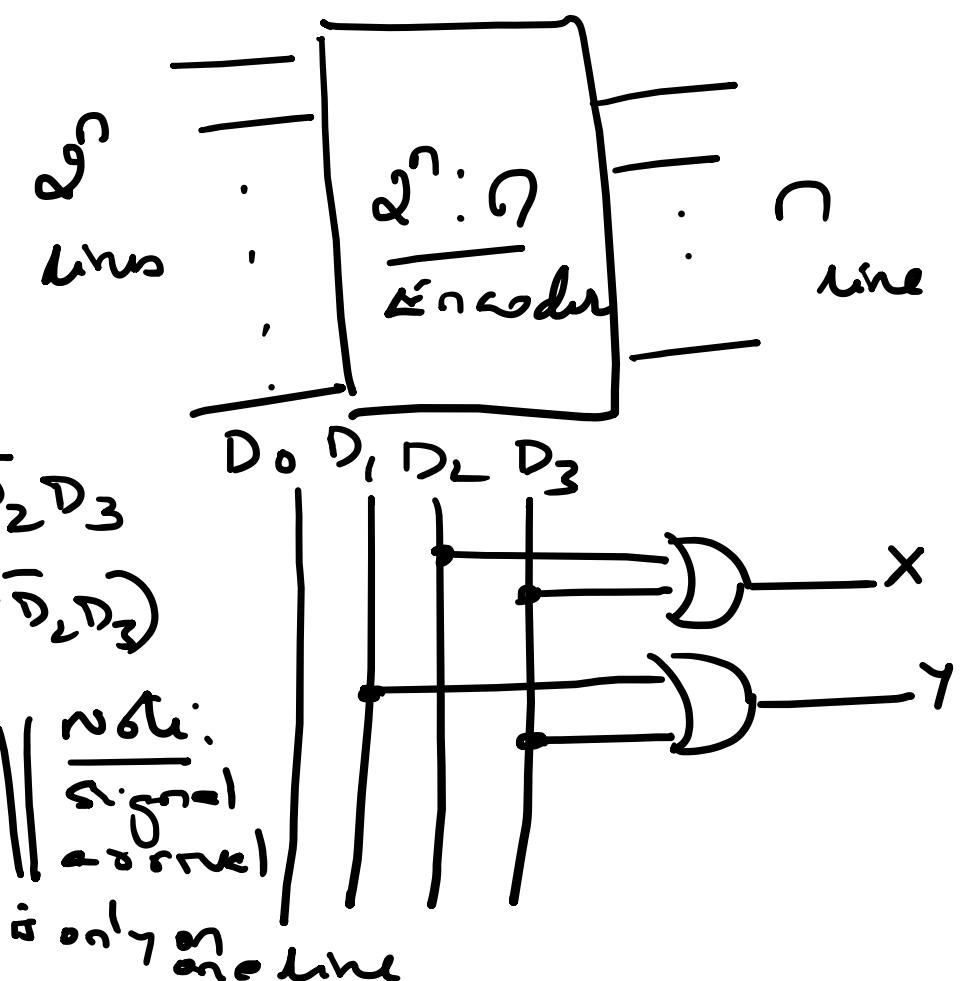
Inputs				Outputs	
D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	x	y
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1



Circuit

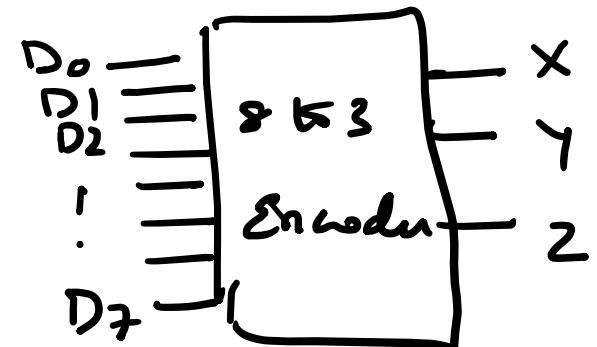
$$\begin{aligned} x &= \bar{D}_0 \bar{D}_1 D_2 \bar{D}_3 + \bar{D}_0 \bar{D}_1 \bar{D}_2 D_3 \\ &= \bar{D}_0 \bar{D}_1 (D_2 \bar{D}_3 + \bar{D}_2 D_3) \end{aligned}$$

$$\begin{aligned} x &= D_2 + D_3 \\ y &= D_1 + D_3 \end{aligned}$$



Write the truth table and circuit for 8-to-3 line encoder

$D_0$	$D_1$	$D_2$	$D_3$	$D_4$	$D_5$	$D_6$	$D_7$	$X$	$Y$	$Z$
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1



$$X = D_4 + D_5 + D_6 + D_7$$

$$Y = D_2 + D_3 + D_6 + D_7$$

$$Z = \underline{D_1 + D_3 + D_5 + D_7}$$

Design a 4-to-2 line priority encoder

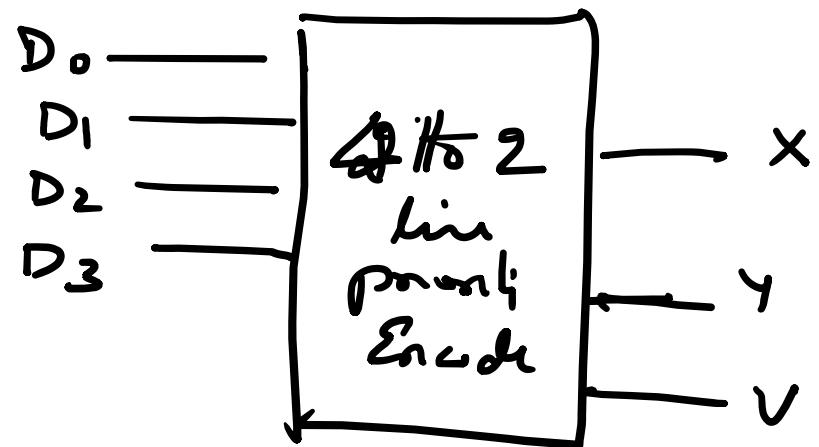
$D_0$	$D_1$	$D_2$	$D_3$	$x$	$y$	$v$
0	0	0	0	X	X	0
1	0	0	0	0	0	1
2	0	1	0	0	1	1
4	X	X	1	0	1	0
8	X	X	X	1	1	1

$$x = \underline{\underline{D_2 + D_3}} \text{ or } \underline{\underline{D_2 \bar{D}_3 + D_3}}$$

$$y = \underline{\underline{D_1 \bar{D}_2 + D_3}}$$

$$v = D_0 + D_1 + \underline{\underline{D_2 + D_3}}$$

0	1	1	1
1	1	1	1
1	1	1	1
1	1	1	1
1	1	1	1



$D_0$  has least priority

$D_3$  has priority over  $D_0$

$D_2$  ————— n —————  $D_0 \& D_1$

$D_3$  ————— n —————  $D_0, D_1 \& D_2$

$v$  for  $\rightarrow$  Valid

$$= \sum_m C_m \quad J = \prod_{n=0}^m (D_0 + D_1 + D_2 + D_3)$$

~~4 to 2~~

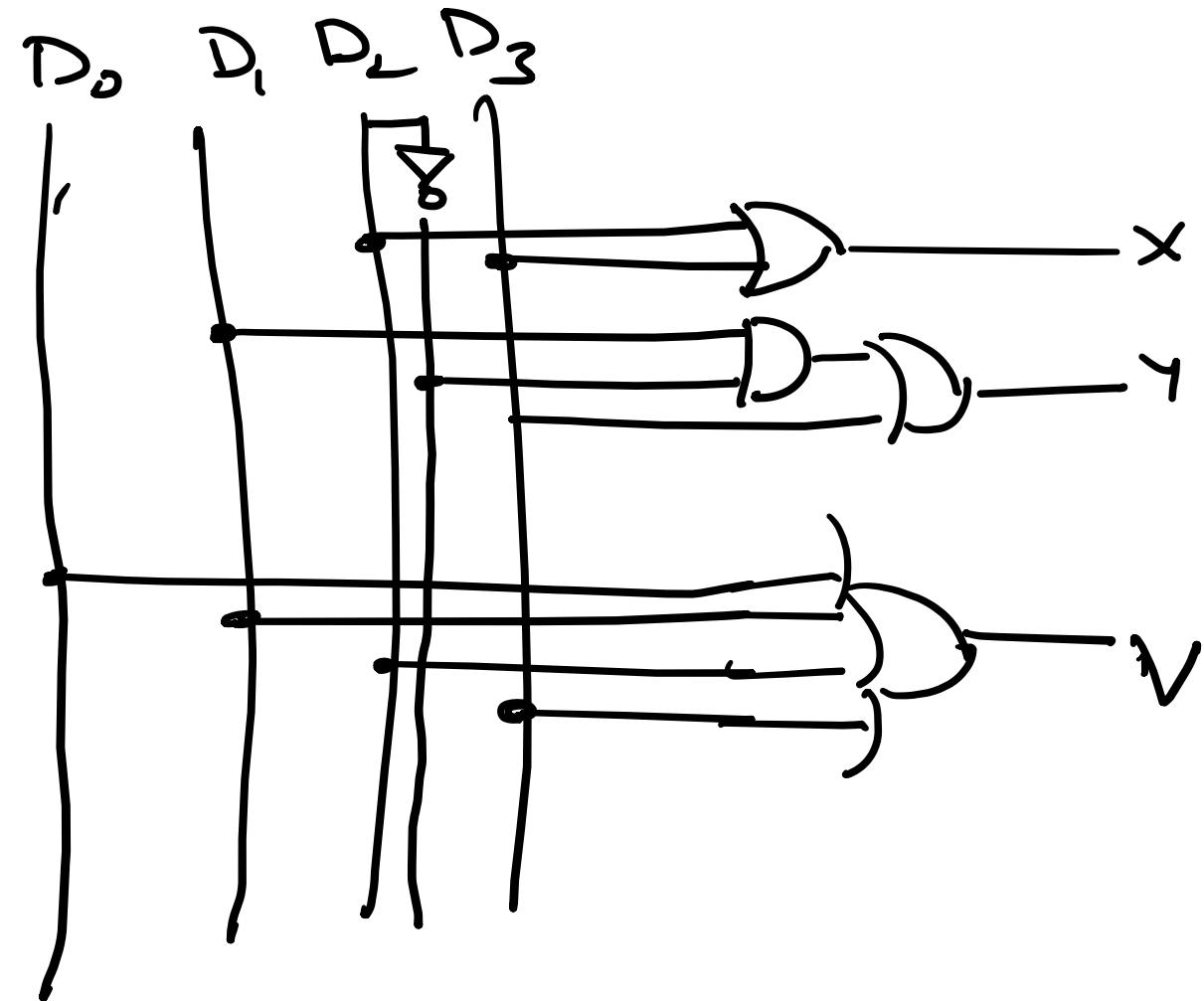
~~2 to 4~~ line priority encoder contd...

Draw the circuit

$$X = D_2 + D_3$$

$$Y = \overline{D_1} \overline{D_2} + D_3$$

$$Z = D_0 + D_1 + D_2 + D_3$$



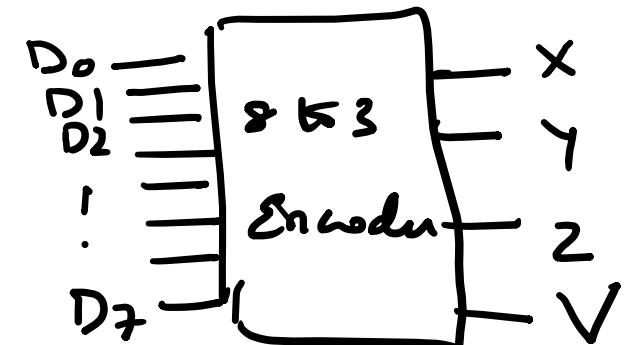
Write the truth table for 8-to-3 line encoder

priority

x

valid

$D_0$	$D_1$	$D_2$	$D_3$	$D_4$	$D_5$	$D_6$	$D_7$	X	Y	Z	V
0	0	0	0	0	0	0	0	X	X	X	0
-	0	0	0	0	0	0	0	0	0	0	-
X	-	0	0	0	0	0	0	0	0	-	-
X	X	-	0	0	0	0	0	0	-	0	-
X	X	X	-	0	0	0	0	0	-	1	-
X	X	X	X	-	0	0	0	-	0	0	1
X	X	X	X	X	-	0	0	-	0	1	1
X	X	X	X	X	X	-	0	-	1	1	1
X	X	X	X	X	X	X	-	-	-	-	-



- Any questions?