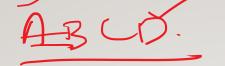
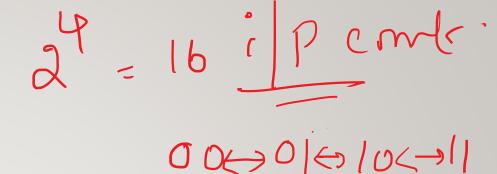
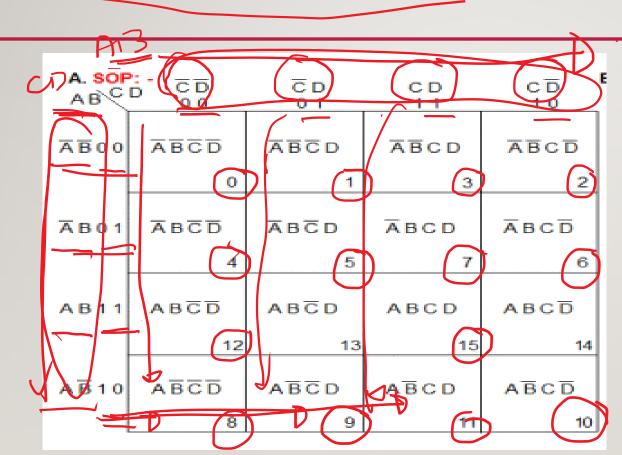
KARNAUGH MAP (K – MAP)

LECTURE 5 & 6

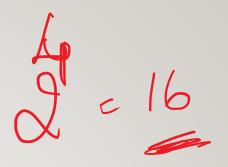


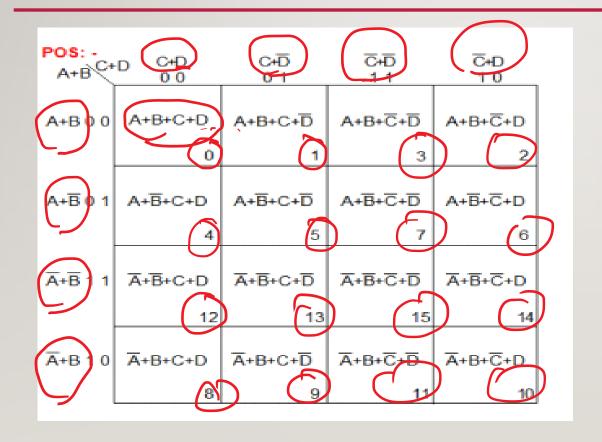
FOUR VARIABLE K - MAP

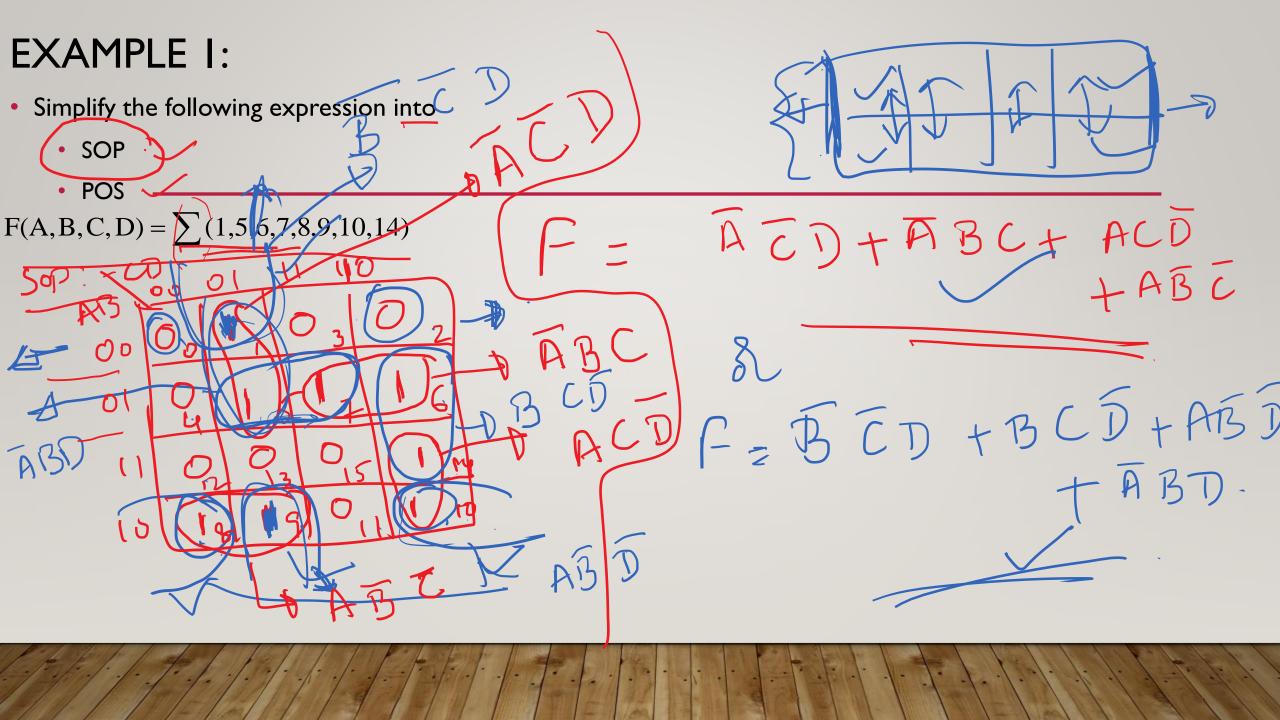




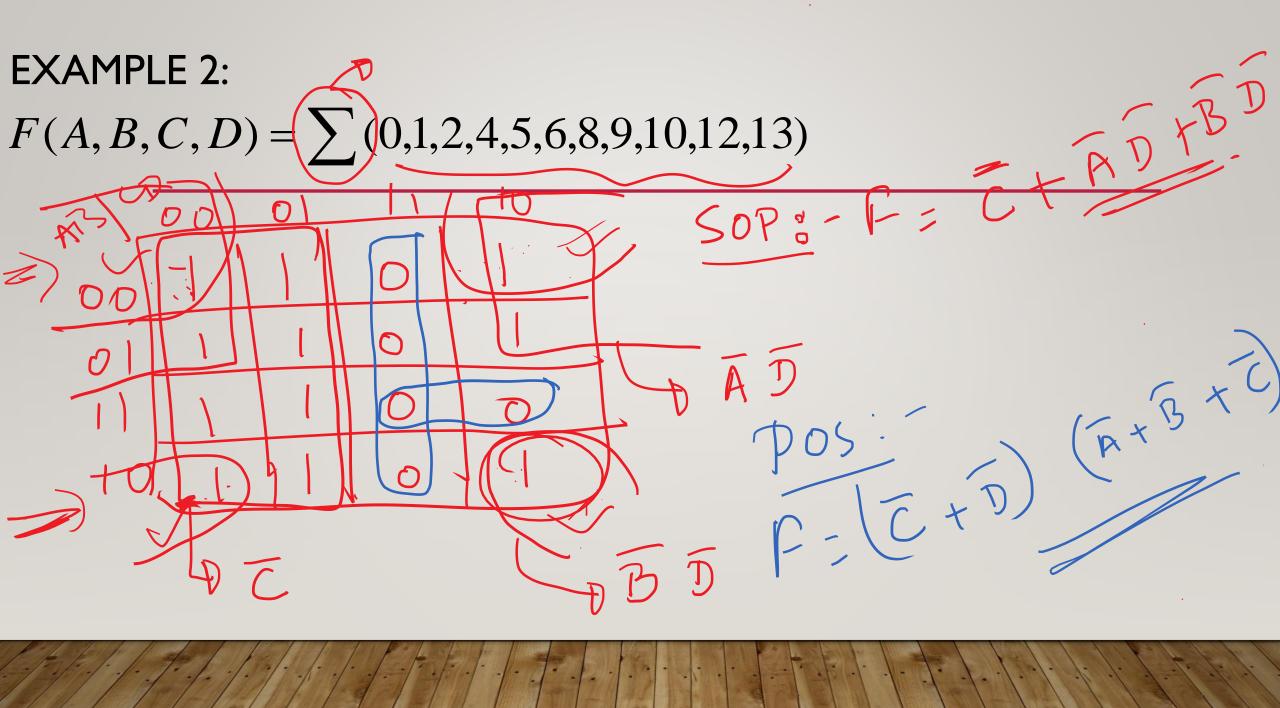
FOUR VARIABLE K - MAP





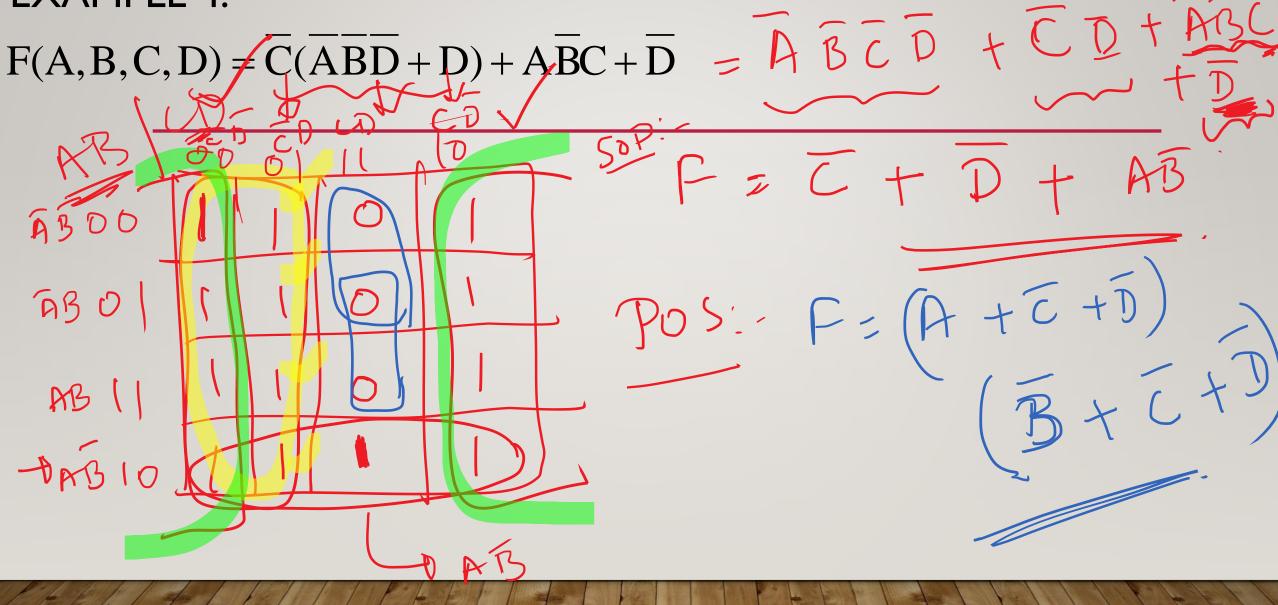


CONTINUED...



EXAMPLE 3: F(A,B,C,D)(0,2,3,4,8,9,10,14)

EXAMPLE 4:

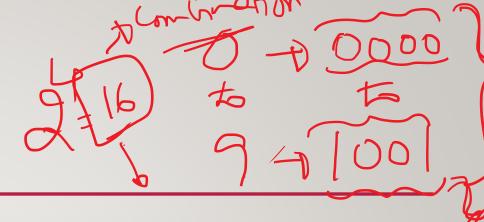


EXAMPLE 5:

$$F(A,B,C,D) = D(\overline{A}+B) + \overline{B}(C+AD) = \overline{A}D + \overline{B}D + \overline{B}C + \overline{A}BD$$

$$SOP = \overline{C}$$

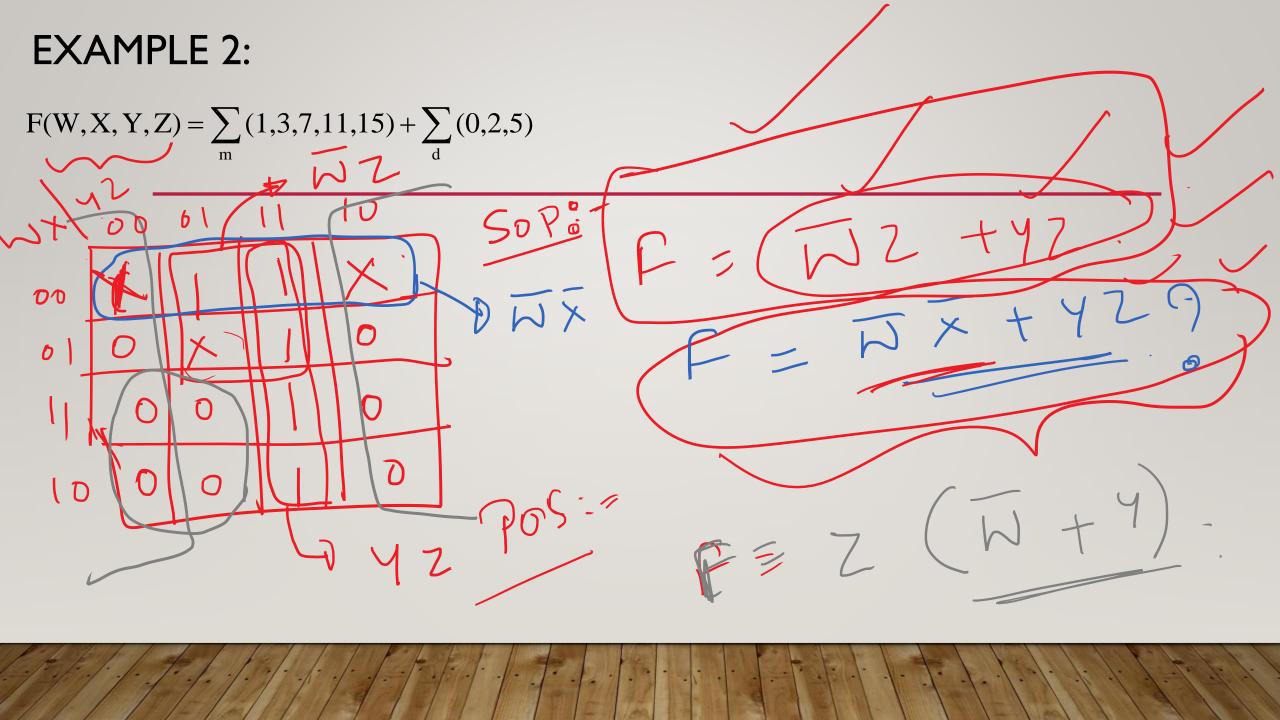
DON'T CARE CONDITION



- The "Don't Care" conditions indicate the input combinations which are invalid for a particular circuit.
- While forming groups of cells, we can consider a "Don't Care" cell as either I or 0 or we can simply ignore that cell.
- Therefore, "Don't Care" condition are used to form a larger group of cells.

EXAMPLE I:

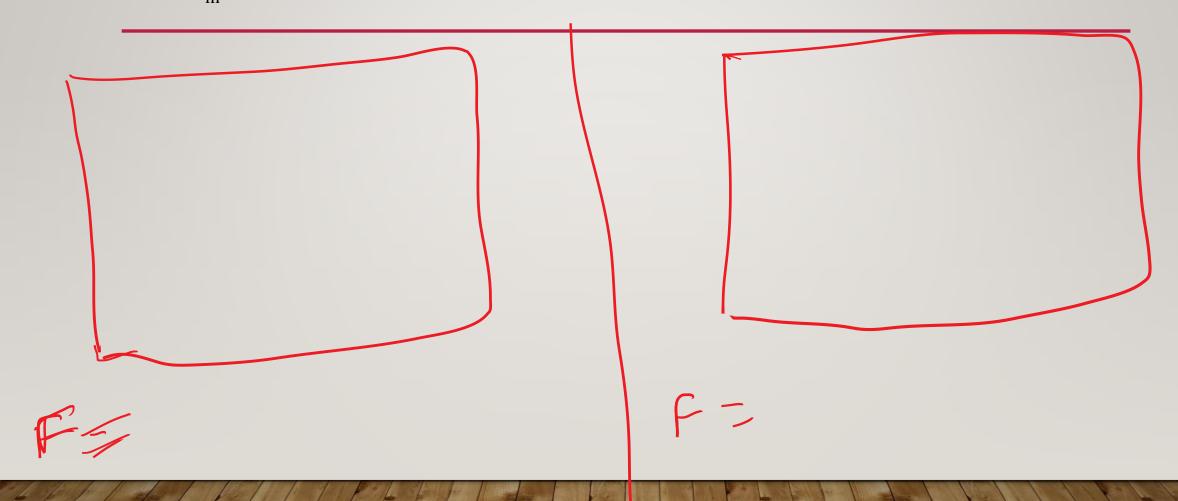
EXAMPLE 1:
$$F(A,B,C) = \sum_{(1,3,5,7)} (1,3,5,7) + \sum_{(0,2)} (0,2) \qquad Z \qquad M(1,3,5,7) + \sum_{(0,1)} (0,2) \qquad Z \qquad M(1,2) \qquad Z \qquad M(1$$



EXAMPLE 3: $F(W, X, Y, Z) = \prod (0,1,3,5,8,9,14). \prod (2,6,10)$ 01

EXAMPLE 4:

$$F(W,X,Y,Z) = \sum_{m} (1,4,5,7,9,10,11) + D(14,15)$$



and XNOR

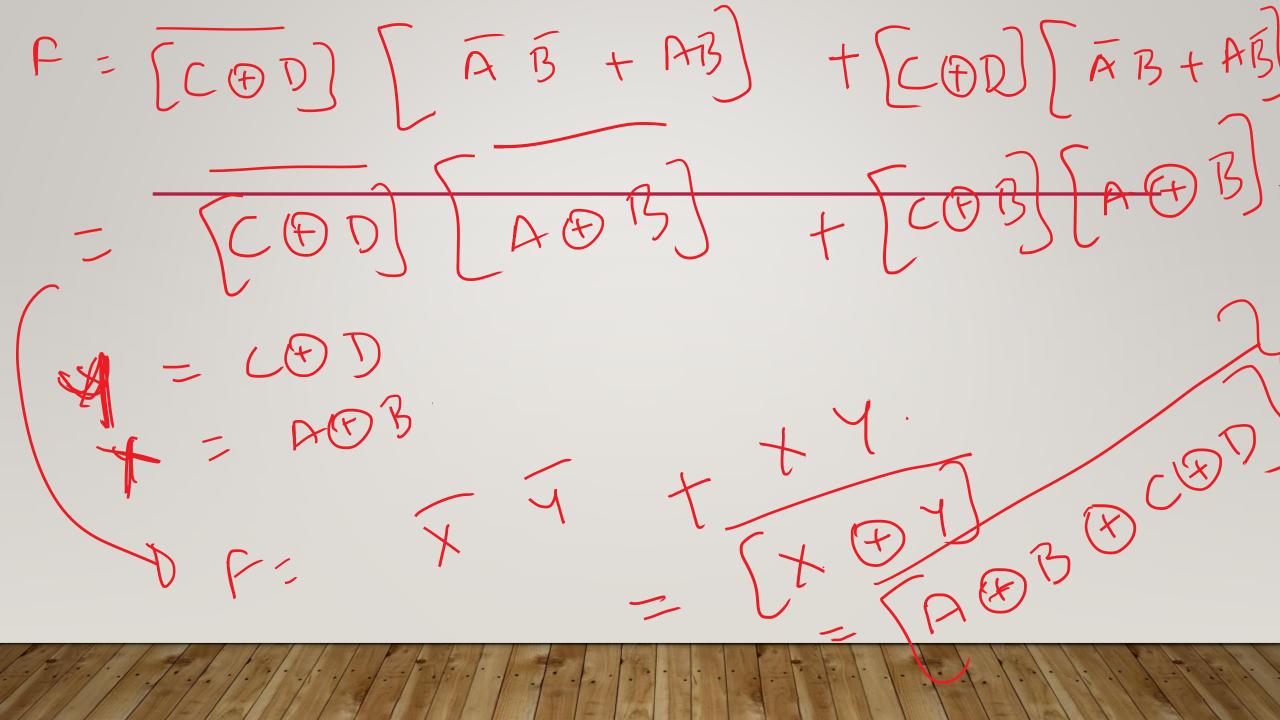
even Devening **EXAMPLE 5:** Design a combinational circuit to check for even parity of 4 bits. A logic 'I' output is required when the 4 bits constitute an even parity. 00 00

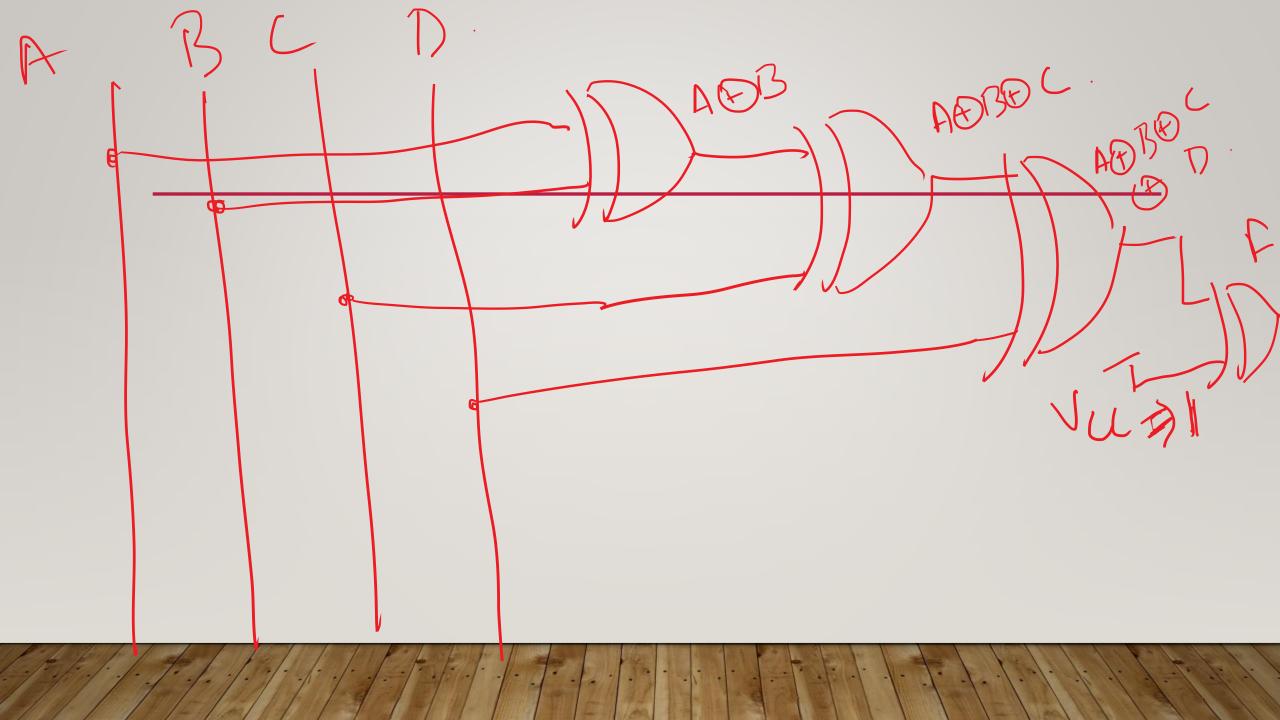
F= FBCD+FBCD+ ABCD+ABCD $F = \overline{AB} \left[\overline{CD} + \overline{CD} \right] + \overline{AB} \left[\overline{cD} + \overline{CD} \right]$ TAB [CD+CD] + AB [CD T]

-AB [CDD] + AB [CDD]

+ MS [CDD]

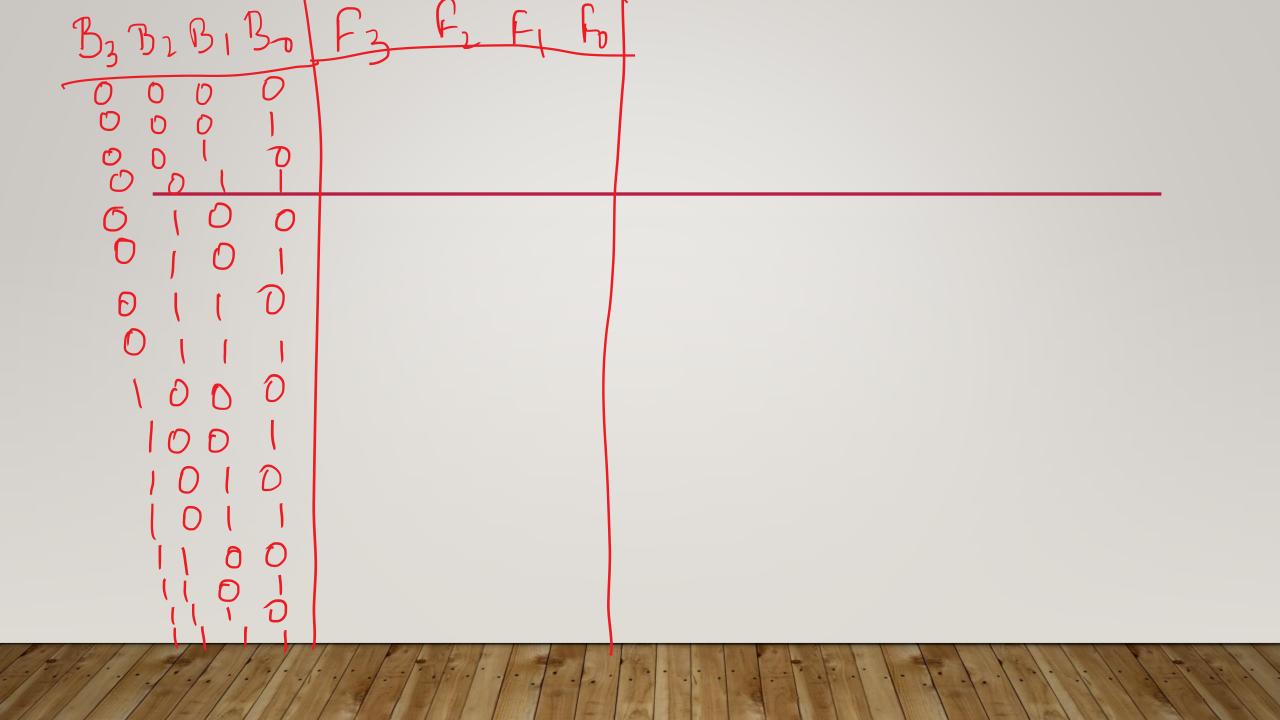
+ MS [CDD]





EXAMPLE 6:

Design a combinational circuit with 4- input lines that represents a decimal digit in BCD and 4- output lines that generates 2's complement of input digit.



EXAMPLE 7:

Design a combinational circuit that multiplies by '5' an input decimal digit represented in BCD. The output is also in BCD.