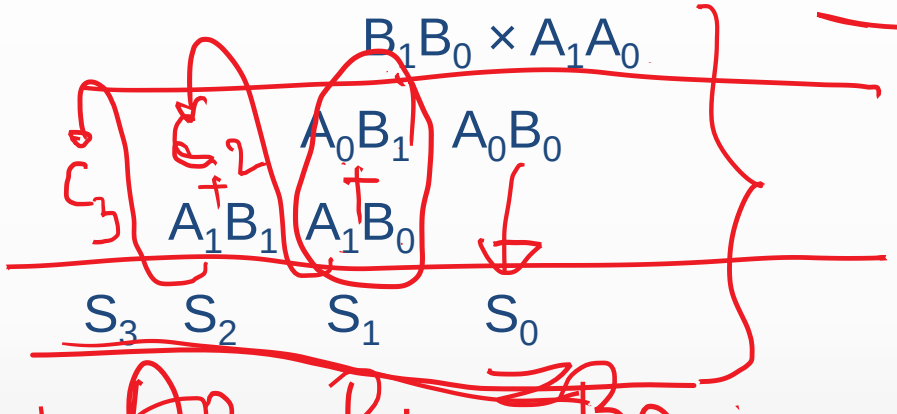
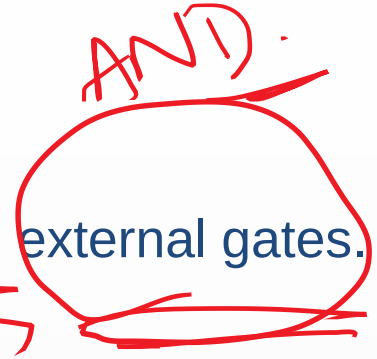
# MULTIPLIERS AND MAGNITUDE COMPARATORS

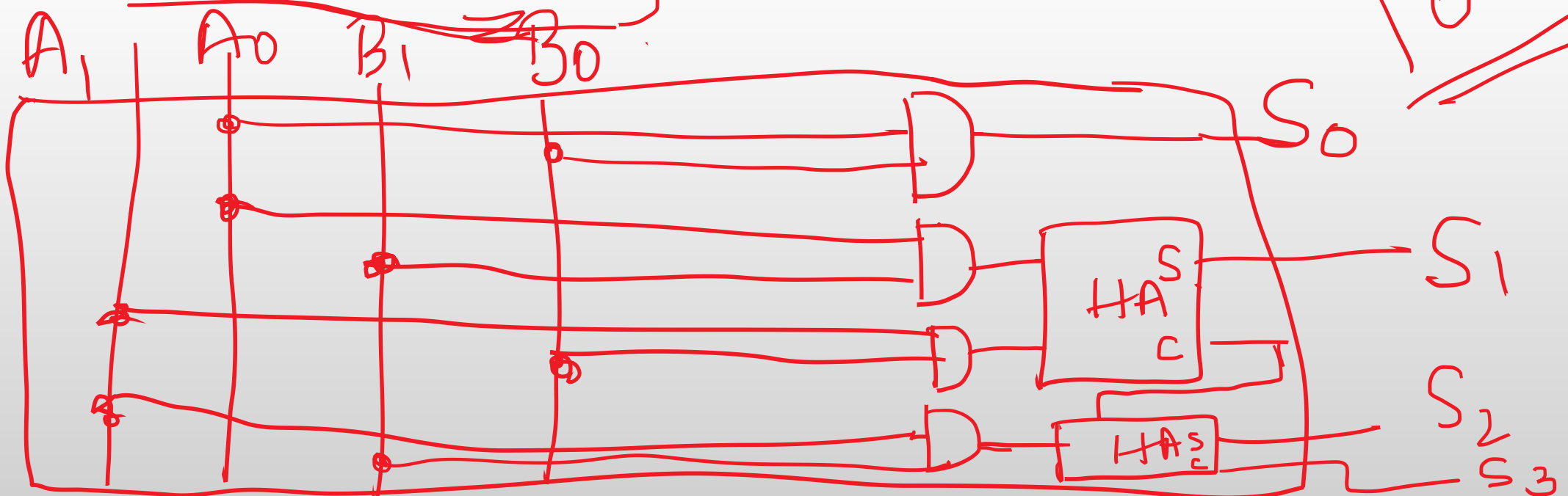
# Binary Multiplier

- 2 bit × 2 bit binary multiplier using adders and external gates.

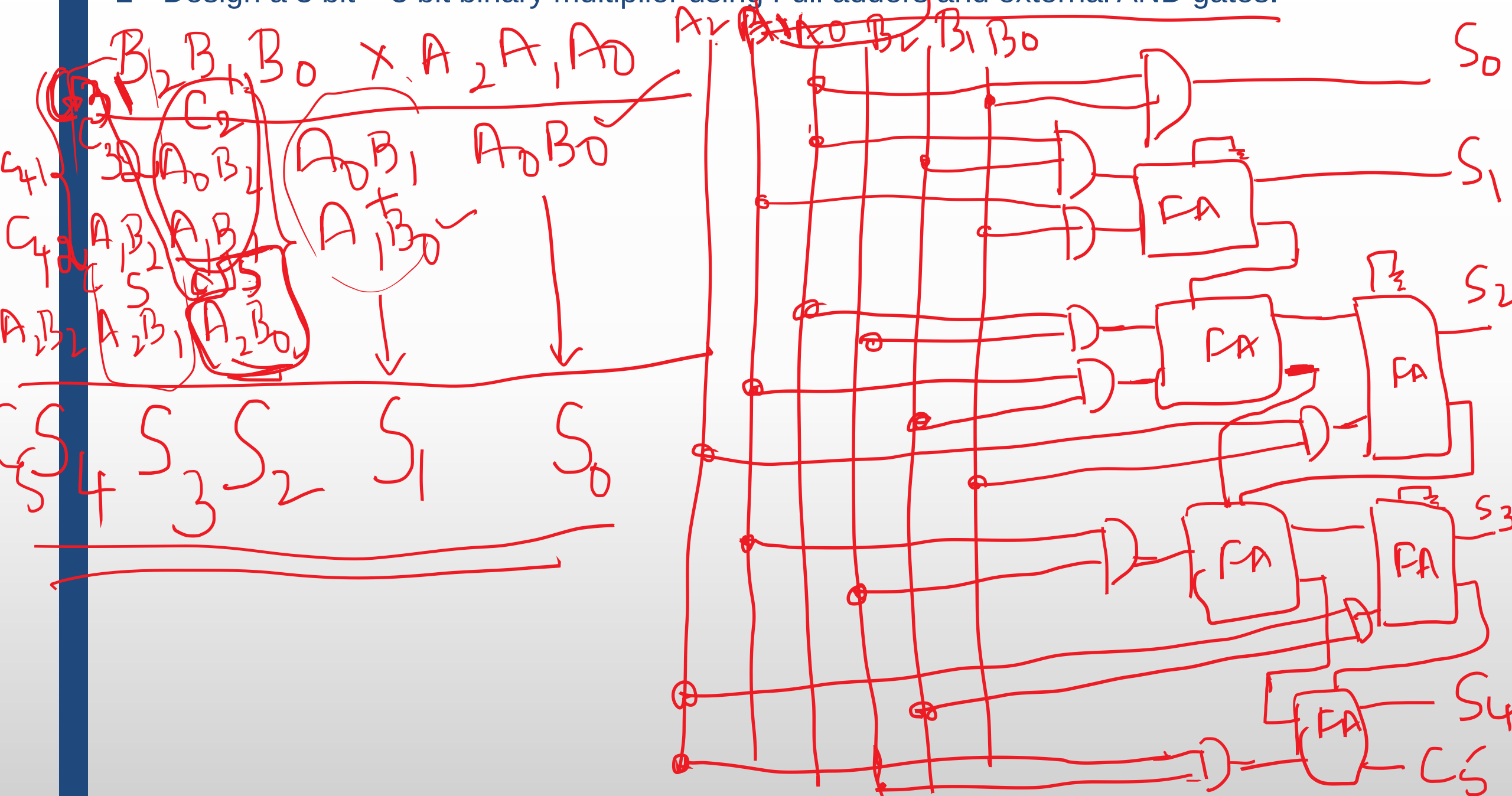


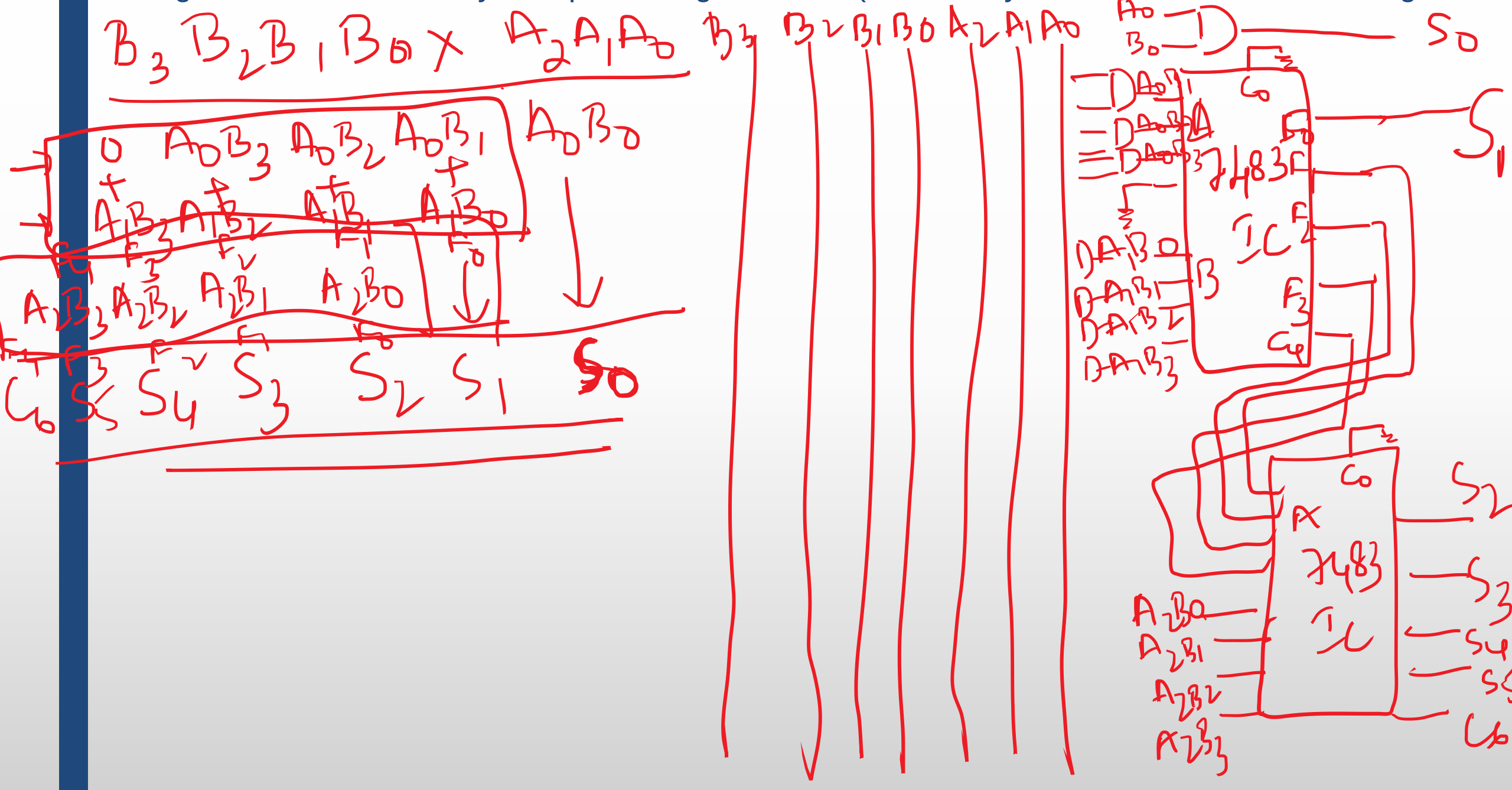




- Design a 3 bit × 3 bit binary multiplier using Full adders and external AND gates.



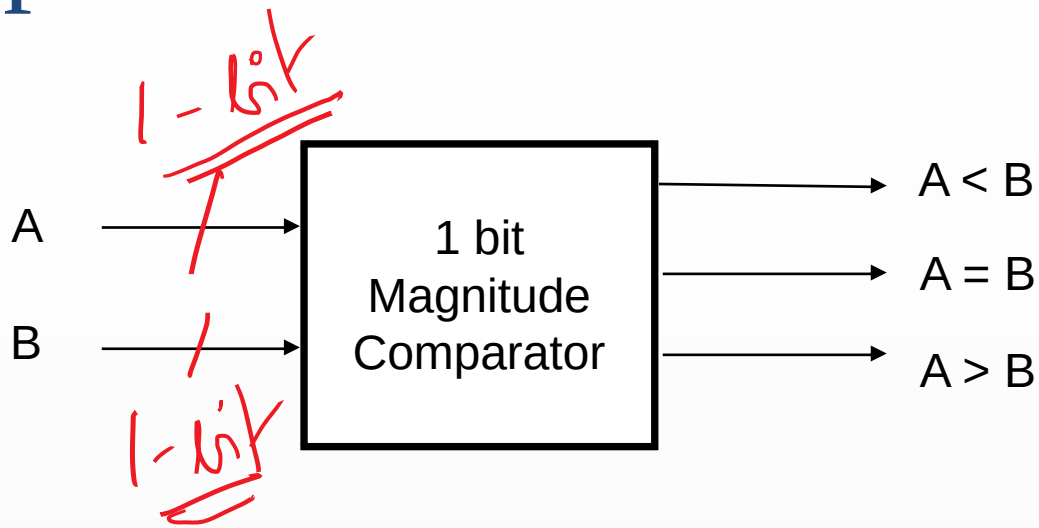
Design a 4 bit × 3 bit binary multiplier using 7483 ICs (4 bit binary adders) and external AND gates.



# Magnitude Comparator

- 1 bit Magnitude comparator

| A | B | L<br>A<B | E<br>A=B | G<br>A>B |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |



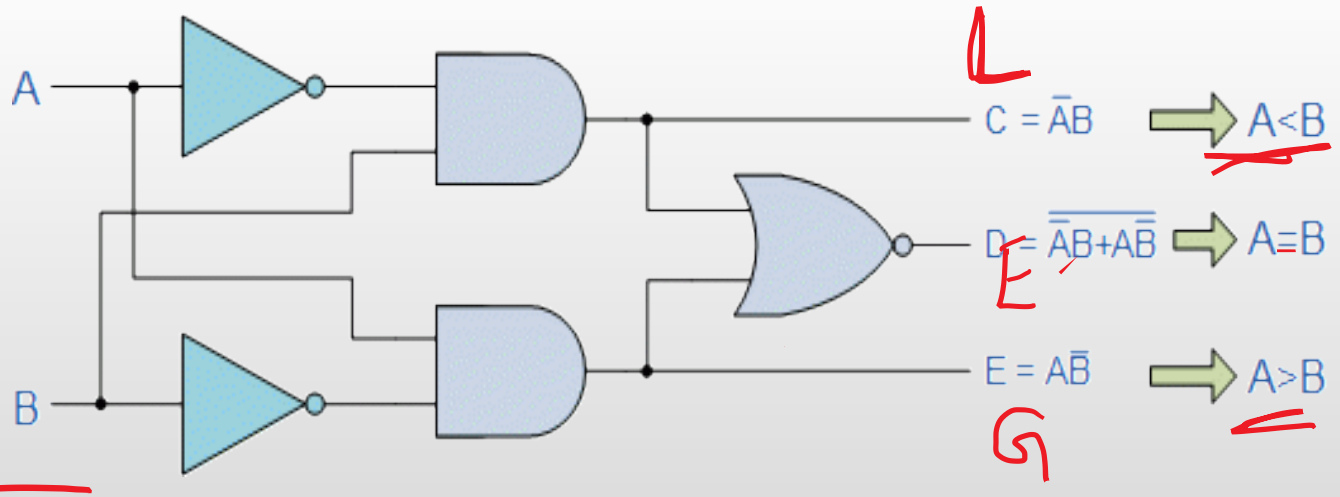

$L = \bar{A}B$

$E = \bar{A}\bar{B} + AB$

$= \overline{(A\bar{B} + \bar{A}B)}$

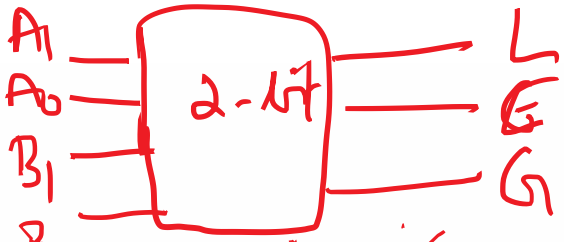
$G = A\bar{B}$

$= L + G$



- 2 bit magnitude comparator

| Inputs | | | | Outputs | | |
|---|---|---|---|---|---|---|
| $A_1$ | $A_0$ | $B_1$ | $B_0$ | A>B | A=B | A<B |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 |




Bitwise Greater than

Equal to :-

$$G_1 = A_1 \bar{B}_1$$

$$G_0 = A_0 \bar{B}_0$$

$$E_1 = \overline{G_1 + L_1}$$

$$E_0 = \overline{G_0 + L_0}$$

Less than :-

$$L_1 = \bar{A}_1 B_1$$

$$L_0 = \bar{A}_0 B_0$$

$$\overline{E} = \overline{A}_1 \overline{A}_0 \overline{B}_1 \overline{B}_0 + \overline{A}_1 A_0 \overline{B}_1 B_0 + A_1 \overline{A}_0 B_1 \overline{B}_0 + A_1 A_0 B_1 B_0$$

$$= \overline{A}_1 \overline{B}_1 \left[ \overline{A}_0 \overline{B}_0 + A_0 B_0 \right] + A_1 B_1 \left[ \overline{A}_0 \overline{B}_0 + A_0 B_0 \right]$$

$$= \left[ \overline{A}_1 \overline{B}_1 + A_1 B_1 \right] \left[ \overline{A}_0 \overline{B}_0 + A_0 B_0 \right]$$

$$= \left[ \overline{A}_1 B_1 + A_1 \overline{B}_1 \right] \left[ \overline{A}_0 B_0 + A_0 \overline{B}_0 \right]$$

$L_0$ $G_0$

$E = E_1 \cdot E_0$

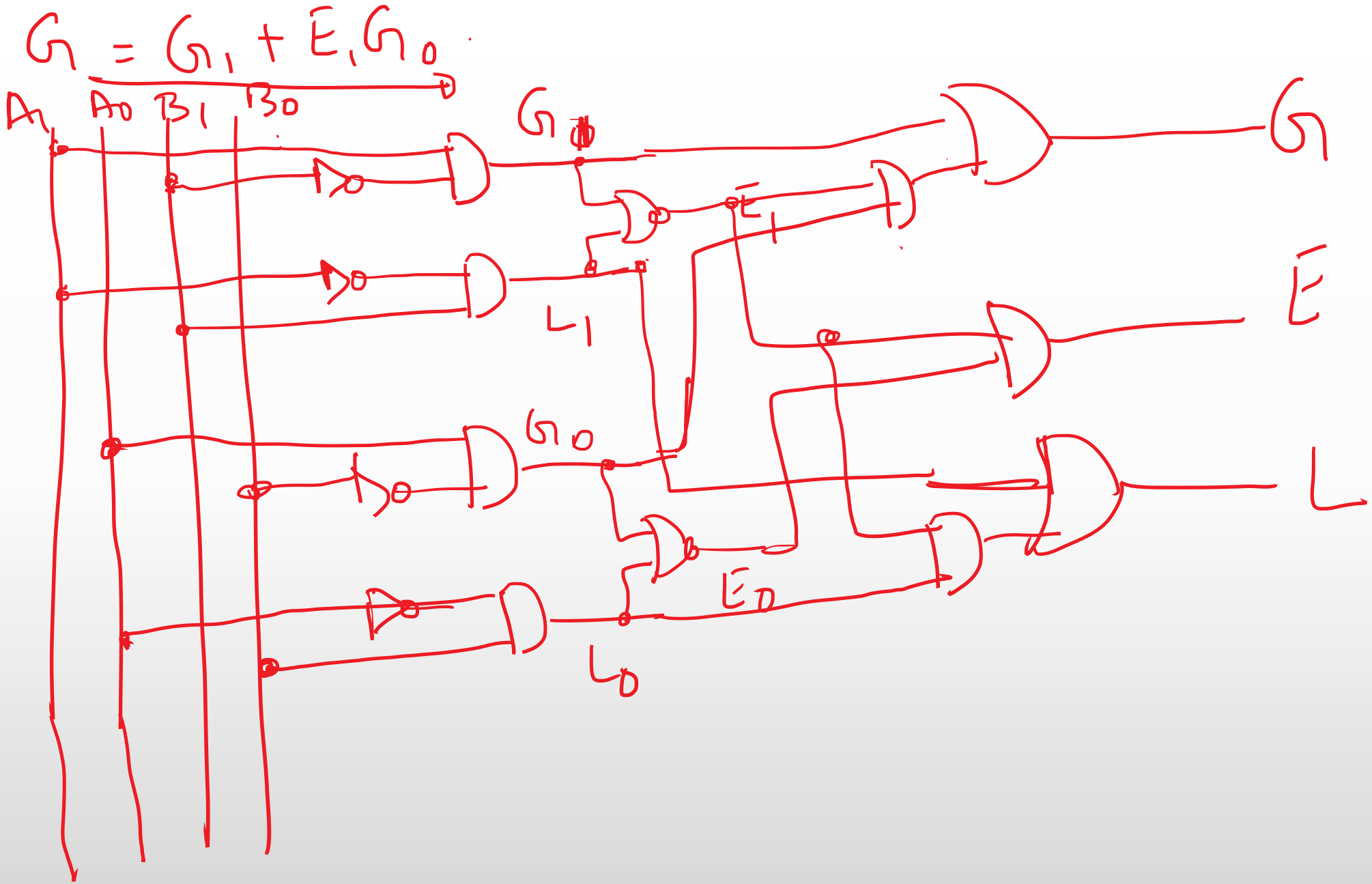
$$L = \bar{A}_1 \bar{A}_0 B_1 B_0 + A_1 \bar{A}_0 B_1 \bar{B}_0 + \bar{A}_1 A_0 B_1 B_0$$
$$+ \bar{A}_1 A_0 B_1 \bar{B}_0 + A_1 \bar{A}_0 B_1 B_0$$

$$= \bar{A}_1 \bar{B}_1 \left[ \bar{A}_0 \bar{B}_0 + \bar{A}_0 B_0 + A_0 \bar{B}_0 + A_0 B_0 \right]$$

$$= \bar{A}_1 B_1 + \bar{A}_1 \bar{A}_0 \bar{B}_1 B_0 + A_1 \bar{A}_0 B_1 B_0 + \bar{A}_1 A_0 \bar{B}_1 B_0 + A_1 A_0 B_1 B_0$$

$$= \bar{A}_1 B_1 + \bar{A}_0 B_0 \left\{ \bar{A}_1 \bar{B}_1 + A_1 B_1 \right\}$$

$$= \bar{A}_1 B_1 + \bar{A}_0 B_0 \cdot E_1 \qquad L = L_1 + L_0 E_1$$


G = G1 + E1G0
A1
A0
B1
B0
G1
G
E1
E
L1
G0
L
E0
L0

- 3 bit magnitude comparator

$$L = L_2 + E_2 L_1 + E_2 E_1 L_0$$

$$E = E_2 E_1 E_0$$

$$G = G_2 + E_2 G_1 + E_2 E_1 G_0$$

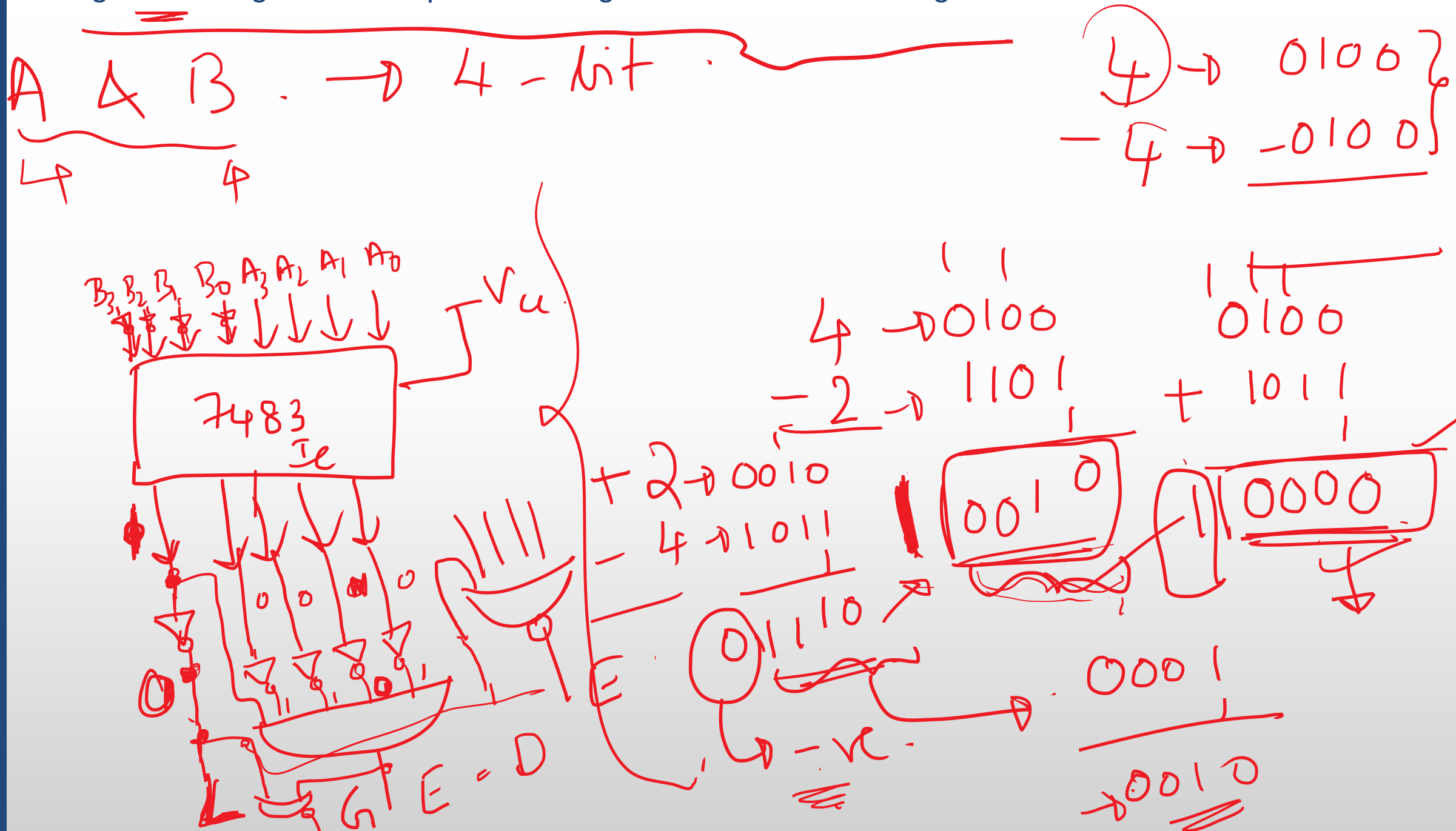
- 4 bit magnitude comparator

$$L = L_3 + E_3 L_2 + E_3 E_2 L_1 + E_3 E_2 E_1 L_0$$

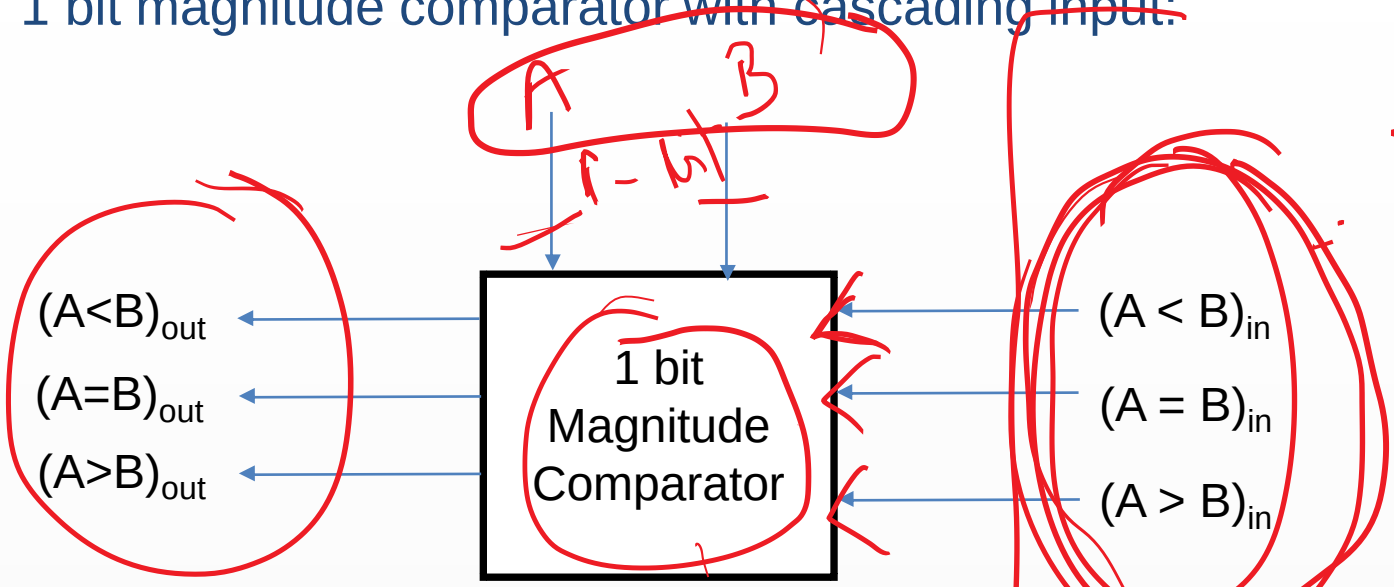
$$E = E_3 E_2 E_1 E_0$$

$$G = G_3 + E_3 G_2 + E_3 E_2 G_1 + E_3 E_2 E_1 G_0$$

# Design 4 bit magnitude comparator using 7483 IC and external gates.



- 1 bit magnitude comparator with cascading input:




$(A>B)_{out} = (A>B) + (A=B)(A>B)_{in}$

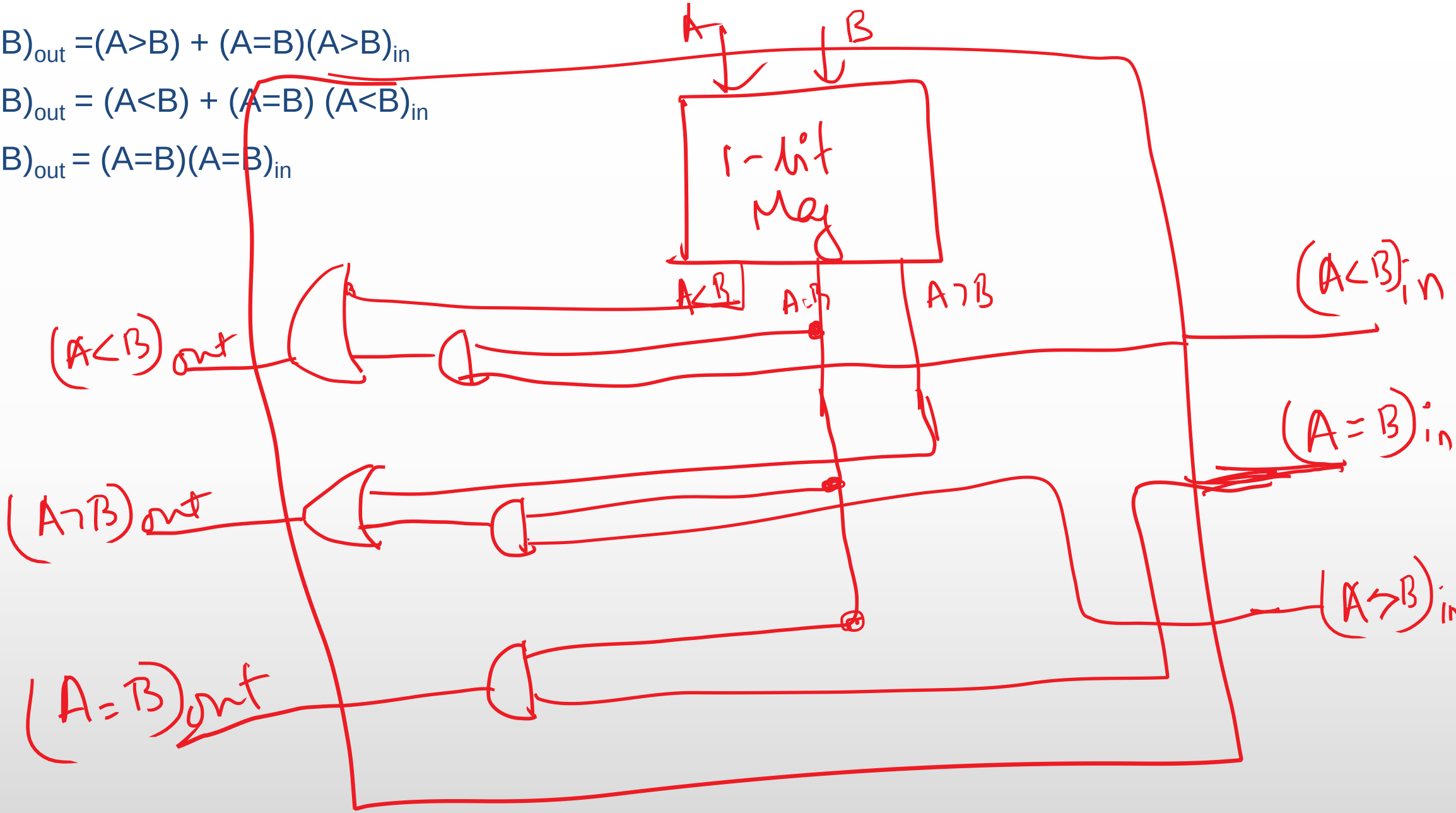
$(A<B)_{out} = (A<B) + (A=B)\,(A<B)_{in}$

$(A=B)_{out} = (A=B)(A=B)_{in}$

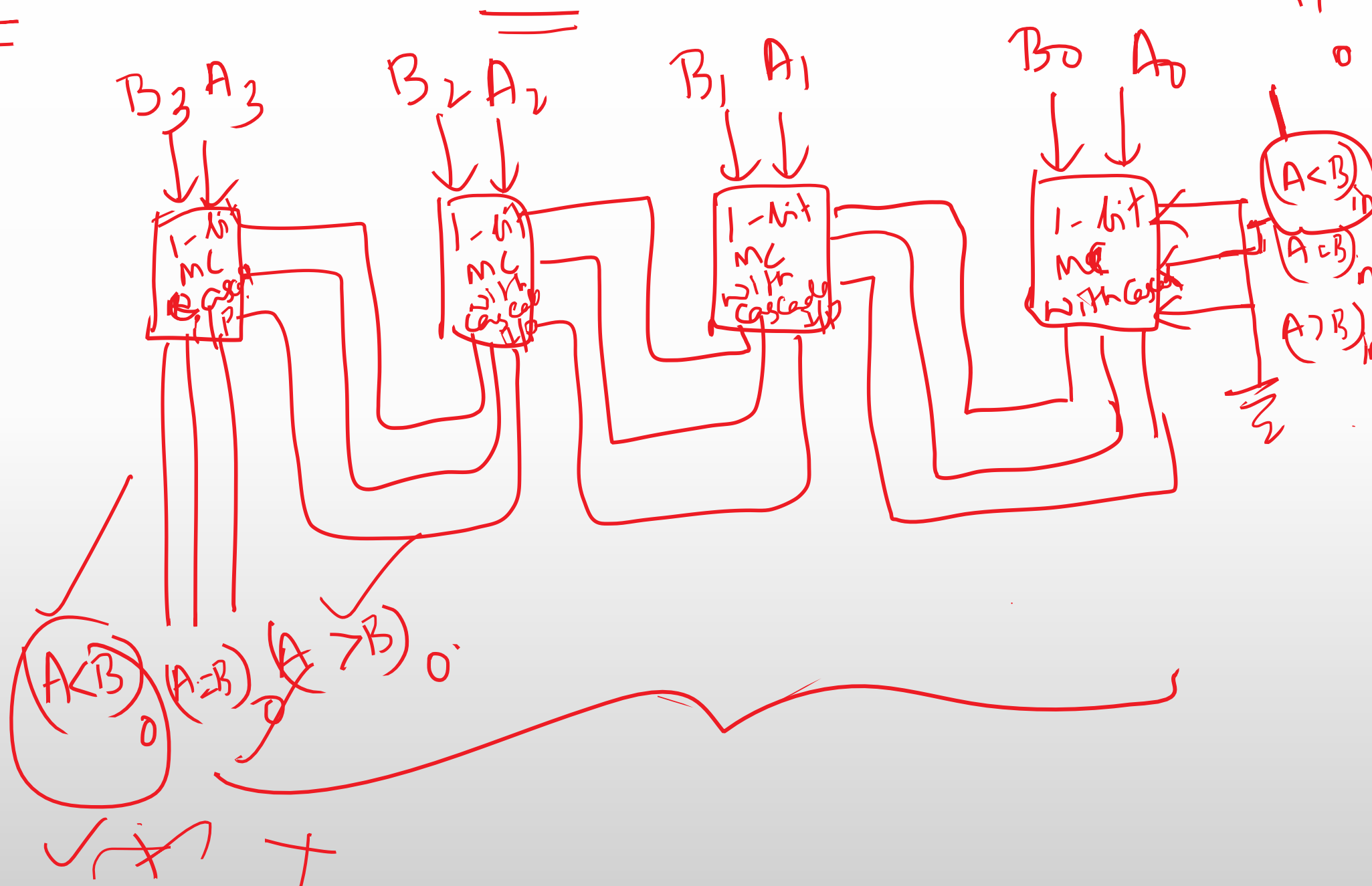
$(A>B)_{out} = (A>B) + (A=B)(A>B)_{in}$

$(A<B)_{out} = (A<B) + (A=B)\ (A<B)_{in}$

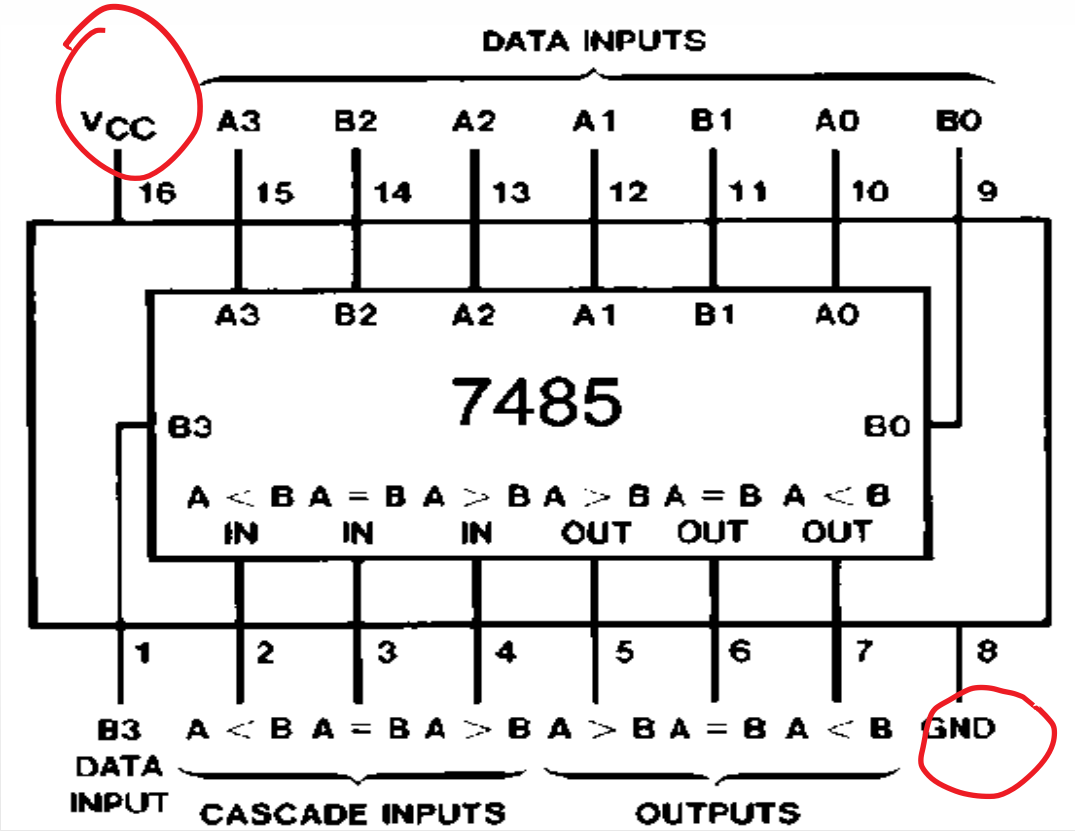
$(A=B)_{out} = (A=B)(A=B)_{in}$

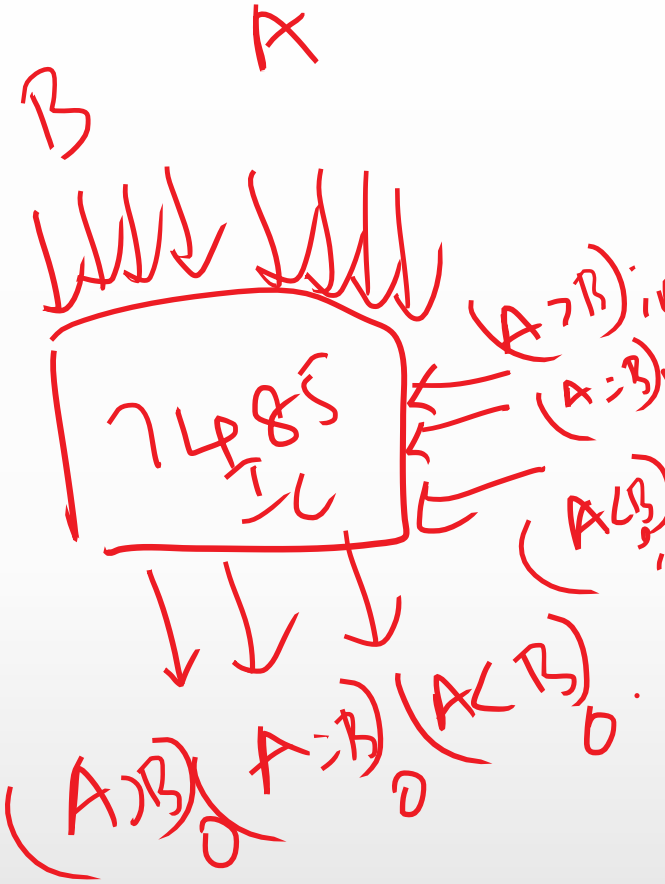


Design a 4 bit magnitude comparator using 1 bit magnitude comparator with cascading inputs.

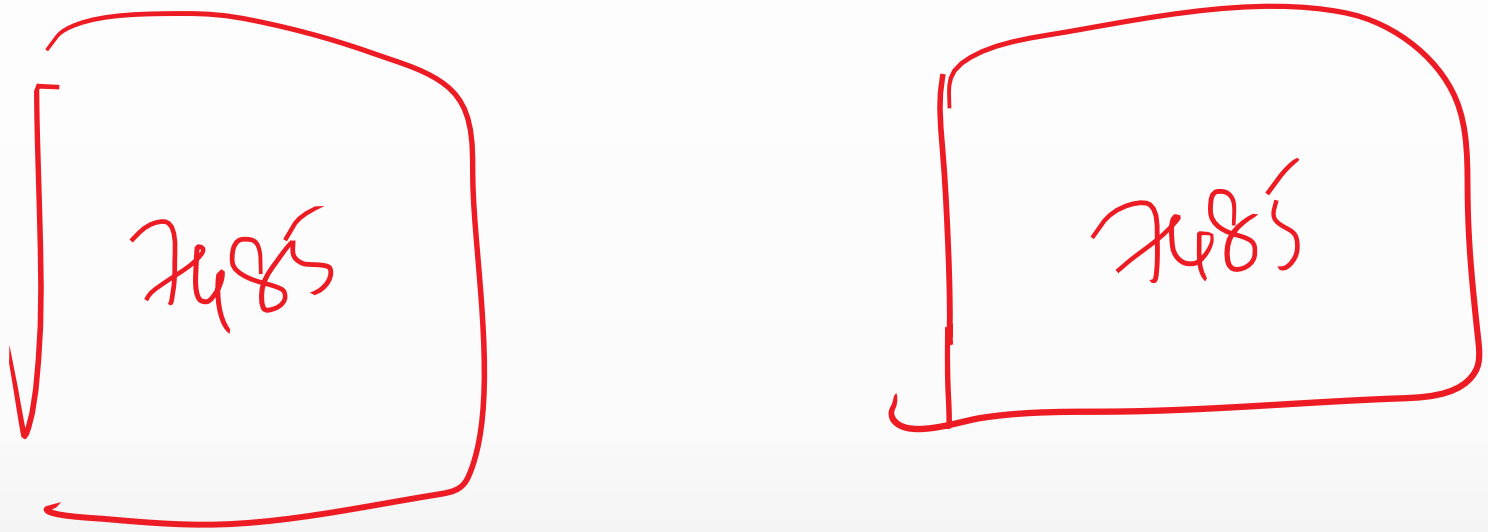


# 7485 IC ( 4 bit magnitude comparator with cascading inputs)



# Design 8 bit magnitude comparator using 7485 ICs



Design a combinational circuit using multipliers, 7483 IC and external gate to perform

F = 2X + Y when m=0,

F= X + 2Y when m=1

Where X, Y are two bit numbers and output F is a 4 bit number.