MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

III SEMESTER B. TECH (COMPUTER SCIENCE AND ENGINEERING)
MID TERM EXAMINATION, OCTOBER 2020
SUBJECT: DIGITAL SYSTEM DESIGN (CSE 2153)
REVISED CREDIT SYSTEM

Time: 90 Minutes for Writing +15 Mins for Uploading **MAX. MARKS: 20**

Note: Answer ALL the questions.

1.	Write the Verilog code for half adder. Use this as the submodule in the Hierarchical Verilog code for implementing full adder.	02
2.	Design a 16:1 Multiplexer using one 8:1, two 4:1 and two 2:1 multiplexers. Take the select signals as ABCD where A is the MSB and D is the LSB. Also take the data inputs as W0, W1,……,W15.	02
3.	Draw the logic diagram of a 2-digit BCD adder using 4-bit binary adders and other necessary gates.	02
4.	Write the expression for calculating c8 in the carry lookahead adder. Rewrite the expression for c8 by assuming the maximum fan-in constraint of all the gates as 3. What would be the gate-delay generated for the resultant expression? Justify your answer for gate delay.	03
5.	Write down the truth table for a 4-to-2 priority encoder having input W[3:0] and with priority levels in the decreasing order (i.e., W[0]-Highest, ….., W[3]-Least). Write down the Verilog code for implementing the same.	03
6.	Use functional decomposition to find the best implementation of the function $f = \prod M(1, 2, 3, 7, 8, 12, 13, 14)$ Draw the logic diagram for your implementation assuming that the input variables are available in uncomplemented form only.	04
7.	Consider the function $f(w_1, w_2, w_3, w_4) = \sum m(0, 1, 3, 6, 8, 9, 14, 15)$. With the help of Shannon's expression, derive the best implementation using 2:1 multiplexer and other necessary gates. Assume that the inputs are available in both the complemented and uncomplemented form. Draw the circuit diagram.	04