CSE 2151 Computer Organization and Architecture

Assignment 5

Instructions:

1. Write the answers in sheets of paper, scan the sheets into a single pdf document and upload. Then click Turn in or Hand in.

2. Write your name, registration number, section and put your signature

1. Construct a 1G × 32 larger memory chip using 256M × 16 smaller memory chips. Draw the structure and indicate clearly, the number of address lines and the data lines for both the small and large memory chips in the diagram. 2M

2. A block-set-associative cache consists of a total of 64 blocks, divided into 4-block sets. The main memory contains 2048 blocks, each consisting of 32 words. How many bits are there in each of the fields of the main memory address if Direct mapping is used. 1M

3. A computer has a small data cache capable of holding eight words and each word is one byte. Each cache block consists of one word. When a given program is executed, the processor reads data sequentially from the addresses given below. All addresses are given in decimal.
   7500, 7503, 7516, 7520, 7502, 7503, 7510, 7502
   Assume that the cache is initially empty. Show the contents of the cache (indicate the address of the main memory) after each memory access, for a Set associative mapped cache which uses the LRU replacement algorithm, if the set comprises of two blocks.
   2M