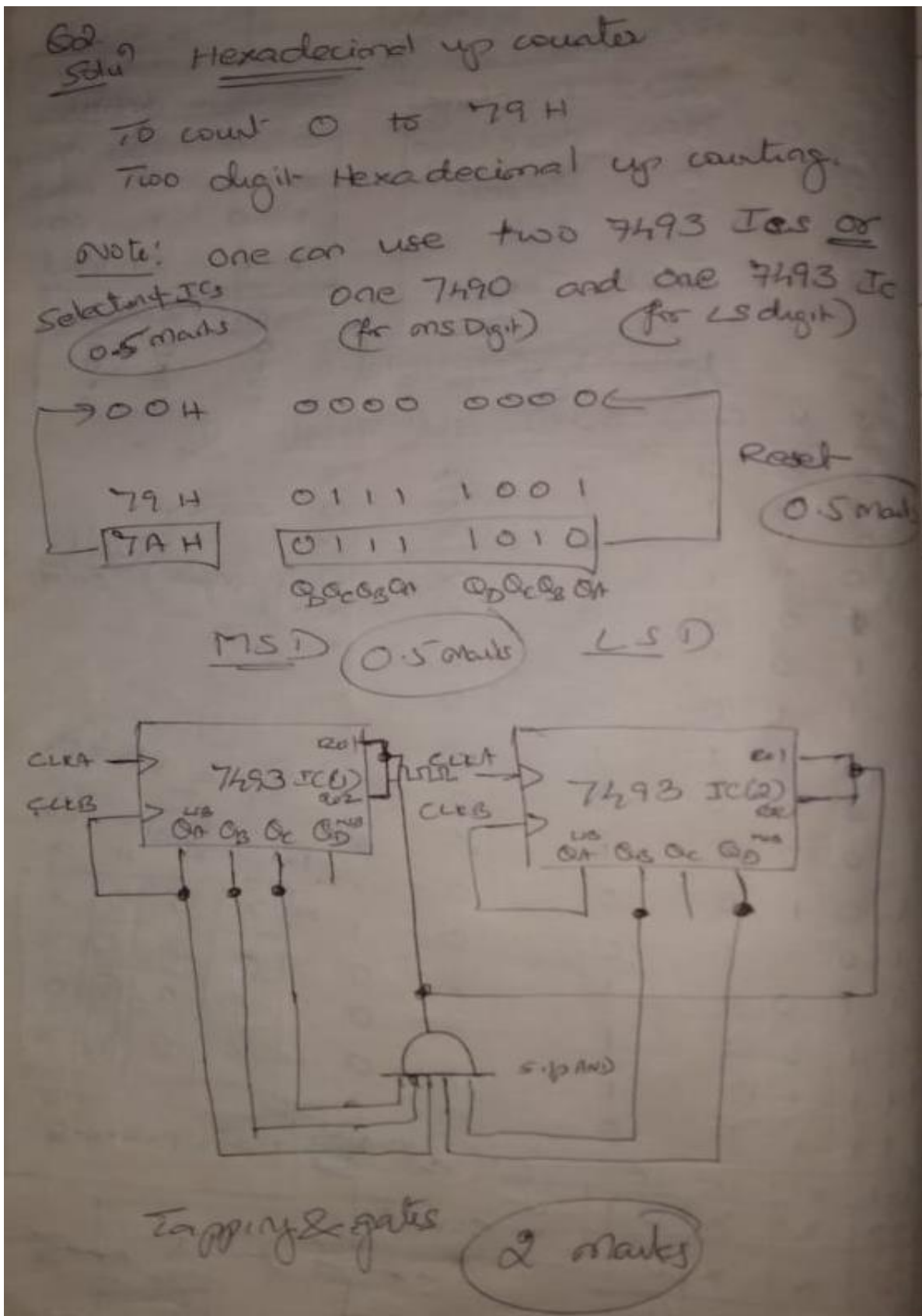
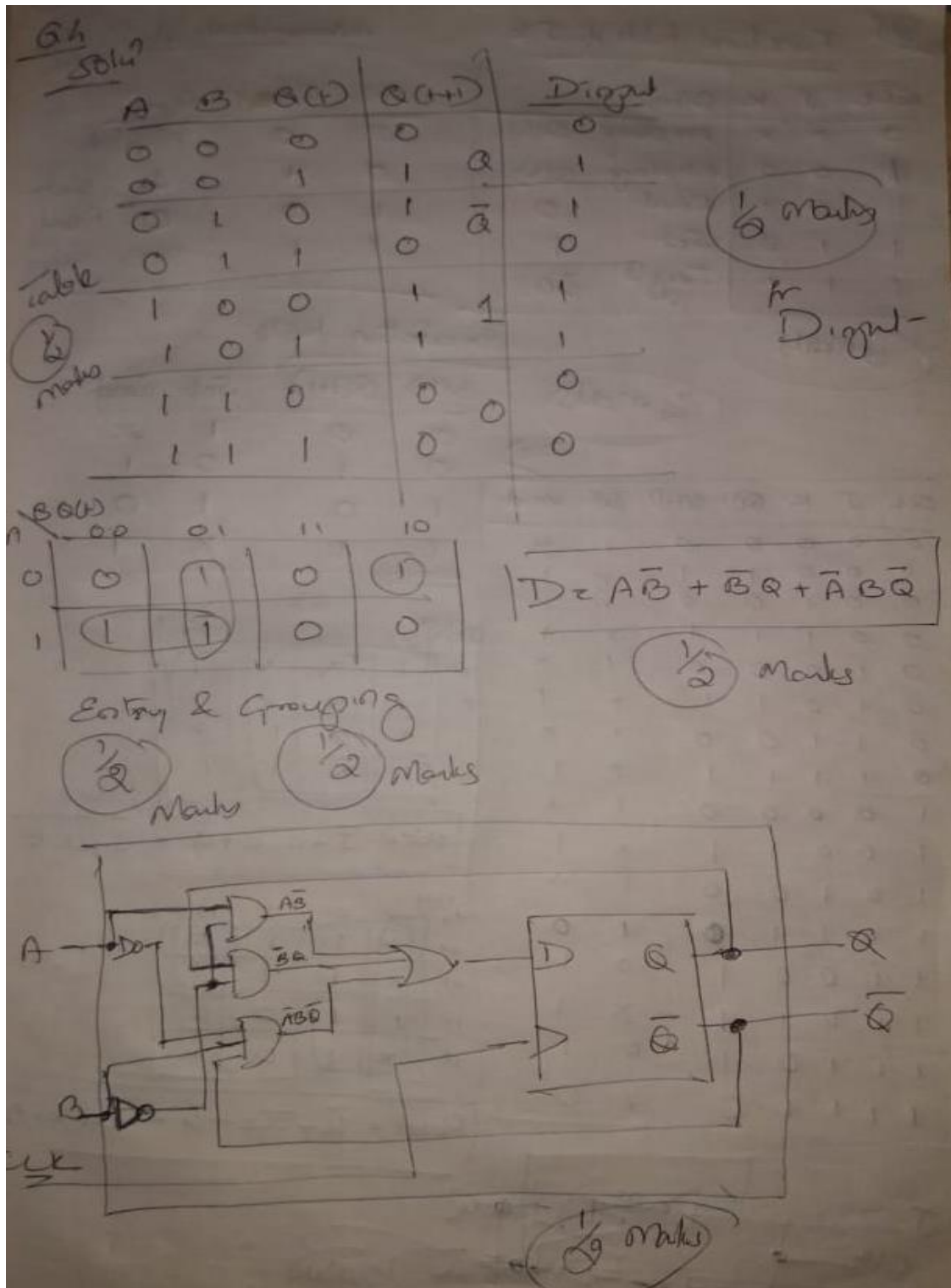


Q2. Construct a hexadecimal up counter to count from 0 to 79H using minimum asynchronous ICs and external gates. Draw the logic diagram. 3 Marks



Q4. Function table defines the working of a fictitious AB flip flop. Design the AB flip flop using D flip flop and external gates. **3 Marks**

A	B	Q(t+1)
0	0	Q
0	1	Q'
1	0	1
1	1	0



Q5. Design a JK flip flop using a basic NAND latch and gates

Q5 Functional table of JK

CLK	J	K	Q(t+1)
0	x	x	No change Q(t)
1	0	0	No change Q(t)
1	0	1	Reset 0
1	1	0	Set 1
1	1	1	Toggle $\bar{Q}(t)$

NAND-LATCH Actual table

Set	Reset	Q(t+1)
0	0	Invalid
0	1	1 Set
1	0	0 Reset
1	1	$\bar{Q}(t)$ Toggle

Execution table

Q(t)	Q(t+1)	Set	Reset
0	0	1	x
0	1	0	1
1	0	1	0
1	1	x	1

1/2 marks

Table 1/2 marks

CLK	J	K	Q(t)	Q(t+1)	Set	Reset
0	0	0	0	0	1	x
0	0	0	1	1	x	1
0	0	1	0	0	1	x
0	0	1	1	1	x	1
0	1	0	0	0	1	x
0	1	0	1	1	x	1
0	1	1	0	0	1	x
0	1	1	1	1	x	1
1	0	0	0	0	1	x
1	0	0	1	1	x	1
1	0	1	0	0	1	x
1	0	1	1	0	1	0
1	1	0	0	1	0	1
1	1	0	1	1	x	1
1	1	1	0	1	0	1
1	1	1	1	0	1	0

1/2 marks

Set 1/2 marks

Q	Q'	00	01	11	10
00	1	x	x	1	1
01	1	x	x	1	1
11	0	x	1	0	0
10	1	x	1	1	1

1/2 marks

Reset 1/2 marks

Q	Q'	00	01	11	10
00	x	1	1	x	x
01	x	1	1	x	x
11	1	1	0	1	1
10	x	1	0	1	x

Set = $\bar{J} + \bar{CLK} + Q = J \cdot CLK \cdot \bar{Q}$

Reset = $\bar{K} + \bar{CLK} + \bar{Q} = K \cdot CLK \cdot Q$

