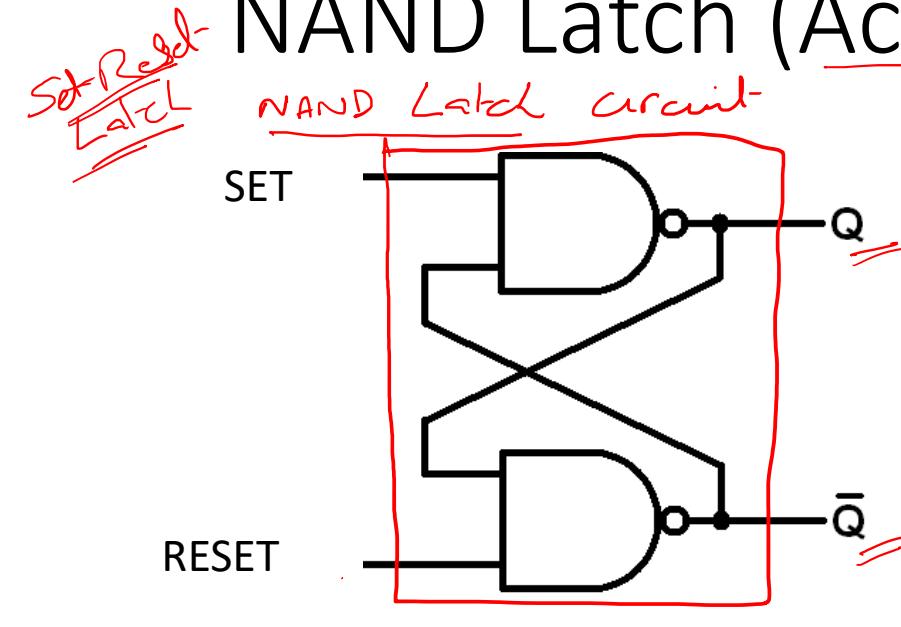


Sequential circuits

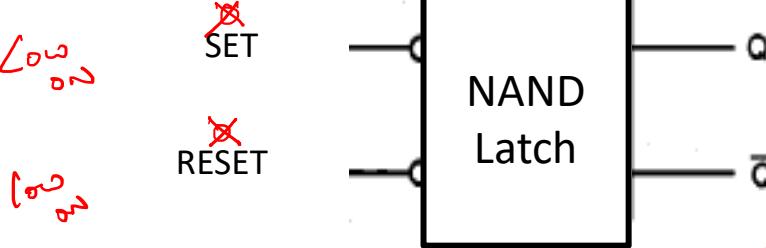
Continued

- NAND Latch
- NOR Latch
- SR, D, JK, T flip flop

NAND Latch (Active Low latch)



functionalities of NAND Latch



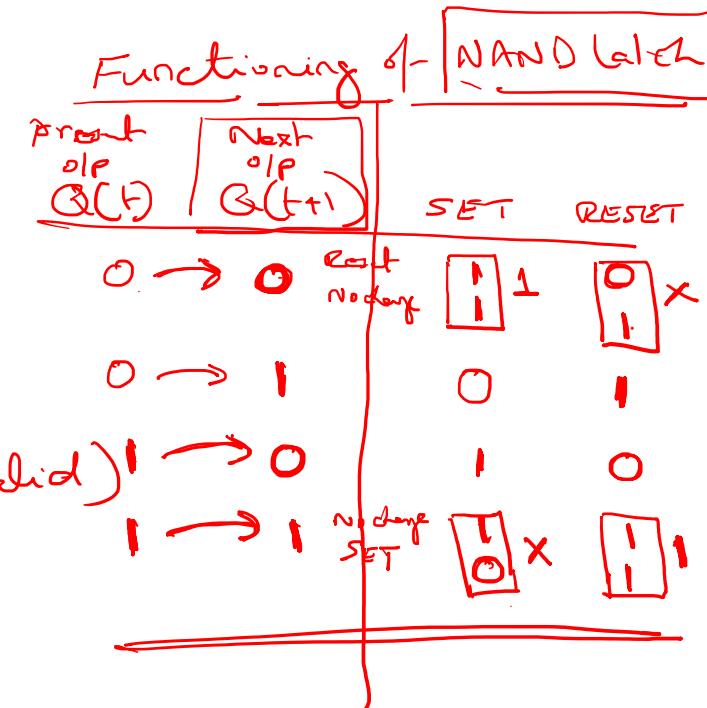
SET	RESET	Q(t)	Q(t+1)	$Q'(t+1)$
0	0	0	1	1
0	0	1	1	1
0	1	0	1	0
0	1	1	1	0
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

not desired
o/p

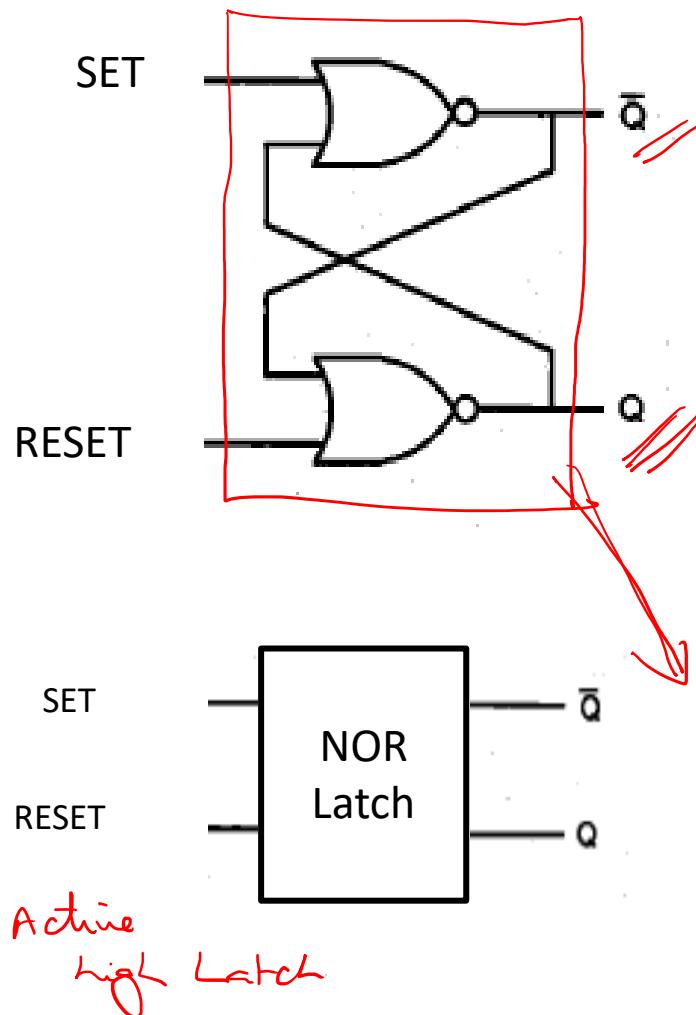
Function table

SET	RESET	Output	$Q(t+1)$
0	0	Indeterminate (Invalid)	
0	1	Set	1
1	0	Reset	0
1	1	No Change	$Q(t)$

*Not to use at o/p
& NAND latch*



NOR Latch (Active high Latch)



SET	RESET	$Q(t)$	$Q(t+1)$	$Q'(t+1)$
0	0	0	0	1
0	0	1	1	0
0	1	0	0	1
0	1	1	0	1
1	0	0	1	0
1	0	1	1	0
1	1	0	0	0
1	1	1	0	0

Function table

SET	RESET	Output	$Q(t+1)$
0	0	No Change	$Q(t)$
0	1	Reset	0
1	0	Set	1
1	1	Indeterminate	X

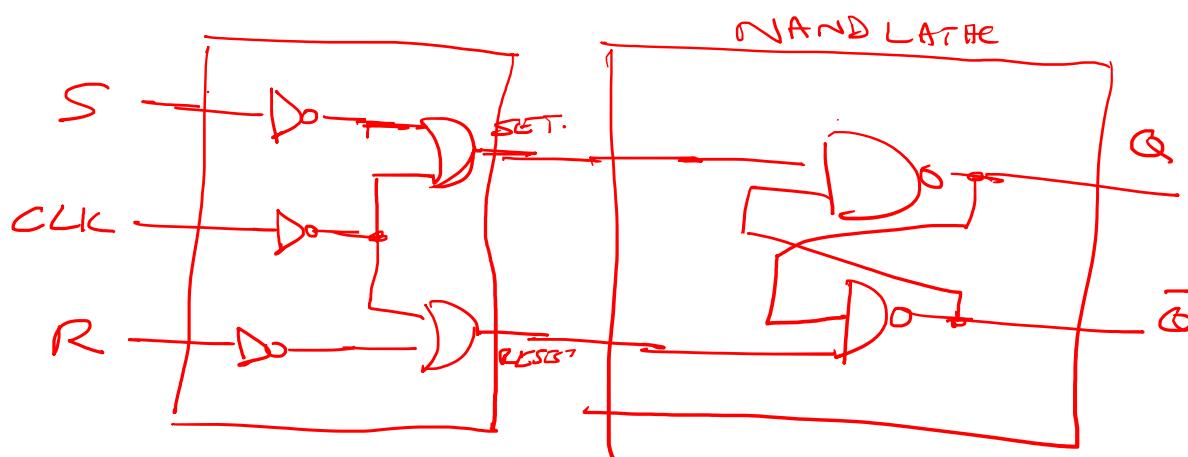
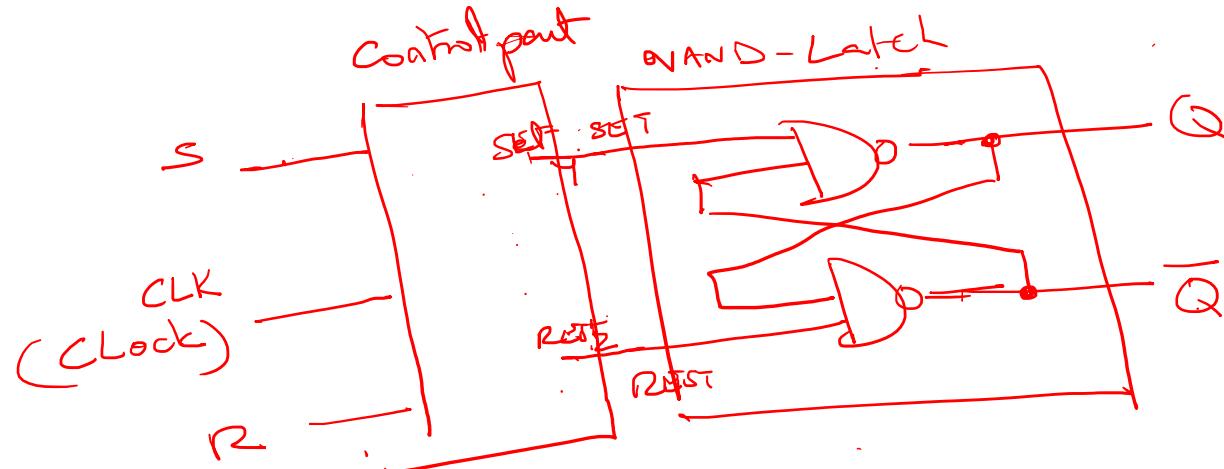
Don't use '1's on NOR Latch if '1's

functionality

$Q(t)$	$Q(t+1)$	SET	RESET
0	0	retain	0
0	1	Transition	1
1	0	Transition	0
1	1	Retain	1
		Set	X
		Reset	0

SR Flip Flop using NAND latch

Flip-Flop is a 1-bit storing circuit employs a basic latch and a control input-ckt.

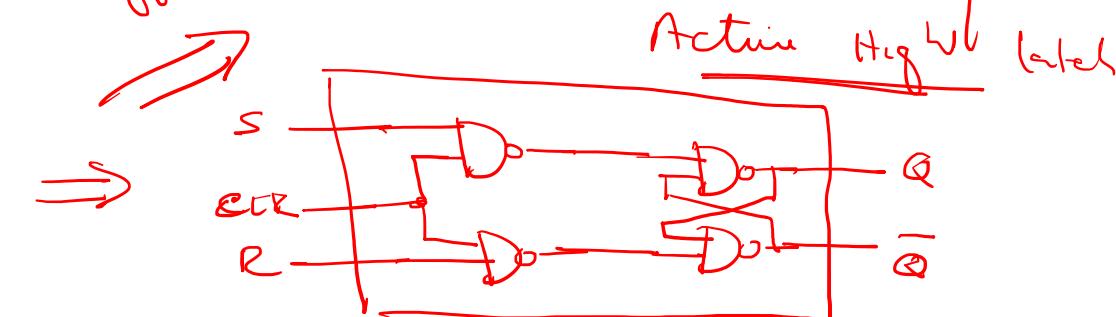


Active High Flip-flop

Requirements for SR flip flop

Clk	S	R	Output
0	x	x	No change
1	0	0	No change
1	0	1	Reset
1	1	0	Set
1	1	1	Indeterminate

level trigger



SR Flip Flop using NAND latch

Requirement of SR

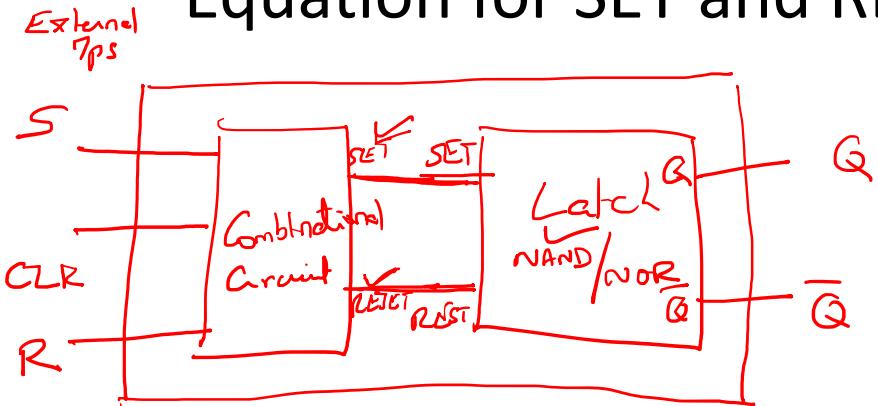
Function Table

of - SR Flip Flop

Clk	S	R	Output
0	X	X	No Change
1	0	0	No Change
1	0	1	Reset $Q(t) = 0$
1	1	0	Set $Q(t) = 1$
1	1	1	Indeterminate

level
low
high

Equation for SET and RESET



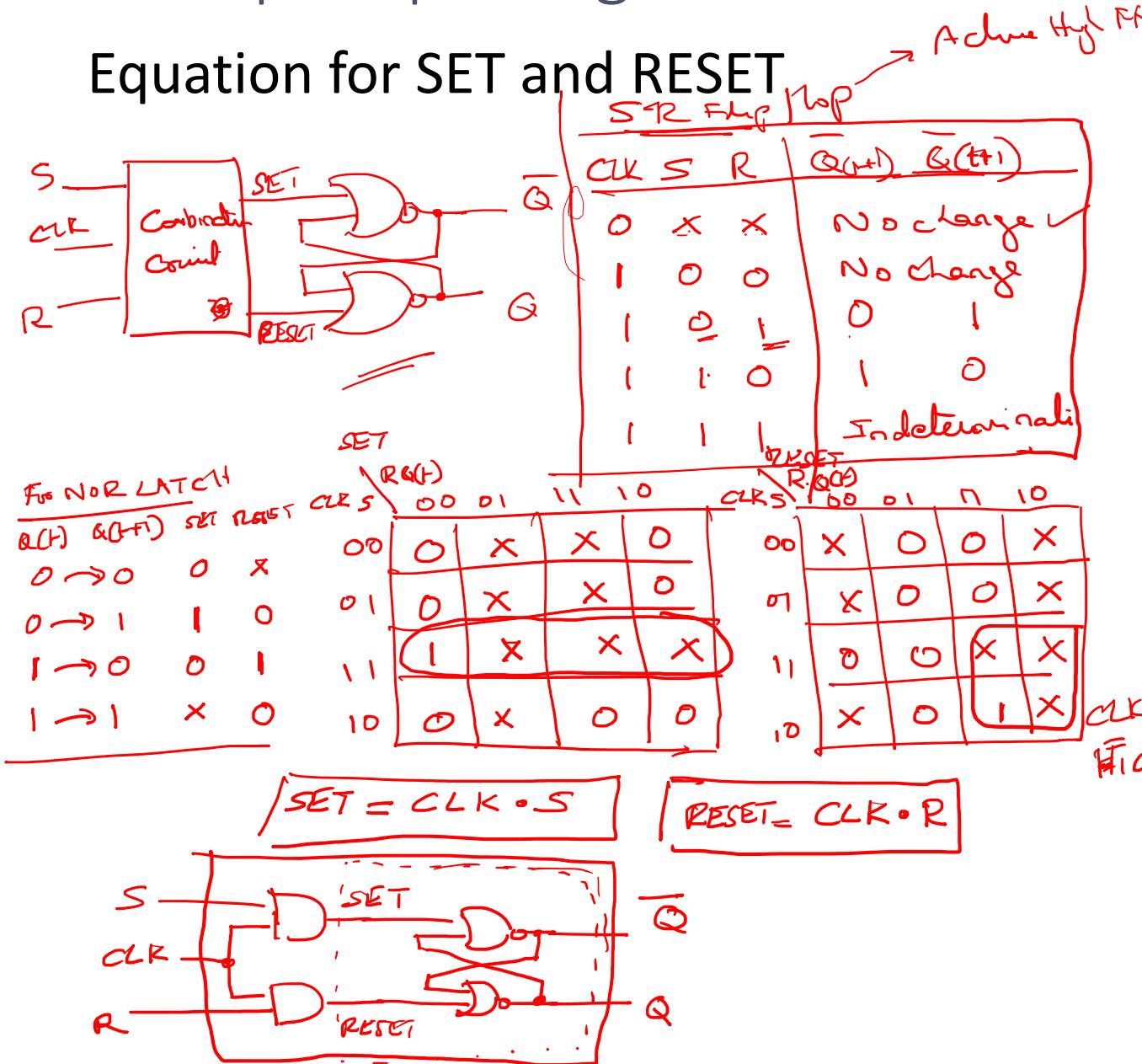
Need to clock any fb from off is required?

Excitation Table

Clk	S	R	Q(t)	Q(t+1)	SET	RESET
0	0	0	0	0	1	X
0	0	0	1	1	X	1
0	0	1	0	0	1	X
0	0	1	1	1	X	1
0	1	0	0	0	1	X
0	1	0	1	1	X	1
0	1	1	0	0	1	X
0	1	1	1	1	X	1
1	0	0	0	0	1	X
1	0	0	1	1	X	1
1	0	1	0	0	1	X
1	0	1	1	1	X	1
1	1	0	0	1	0	1
1	1	0	1	1	X	1
1	1	1	0	X	X	X
1	1	1	1	X	X	X

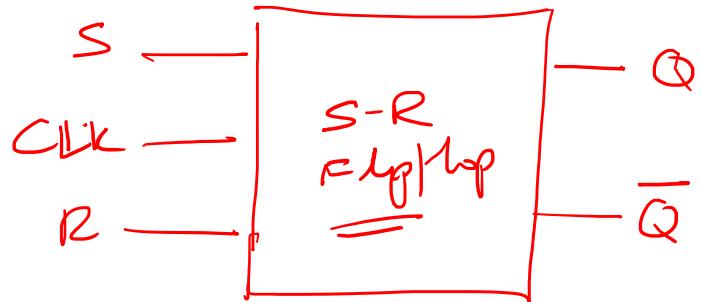
SR Flip Flop using NOR latch

Equation for SET and RESET



Excitation Table						
Clk	S	R	<u>Q(t)</u>	<u>Q(t+1)</u>	SET	RESET
0	0	0	0	0	0	X
0	0	0	1	1	X	0
0	0	1	0	0	0	X
0	0	1	1	1	X	0
0	1	0	0	0	0	X
0	1	0	1	1	X	0
0	1	1	0	0	0	X
0	1	1	1	1	X	0
1	0	0	0	0	0	X
1	0	0	1	1	X	0
1	0	1	0	0	0	X
1	0	1	1	1	1	0
1	1	0	0	1	1	0
1	1	0	1	0	0	1
1	1	1	0	X	X	X
1	1	1	1	X	X	X

Circuit and Block Diagram



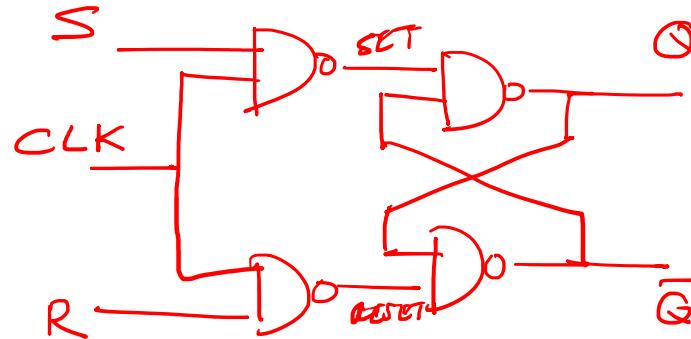
Block diagram

of SR flip flop

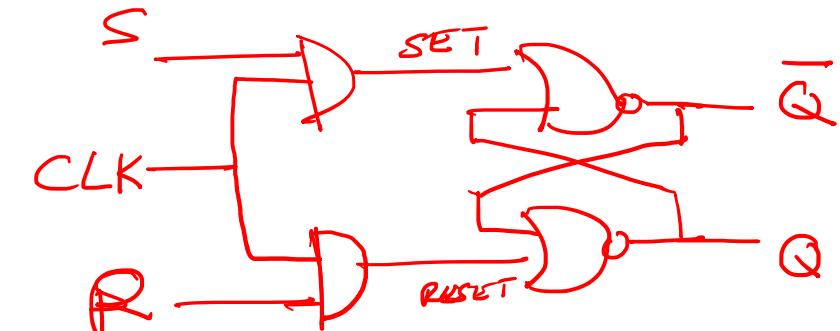
Function table

CLK	S	R	Output
0	X	X	No change
1	0	0	No change
1	0	1	Reset
1	1	0	Set
1	1	1	Indeterminate

① NAND LATCH

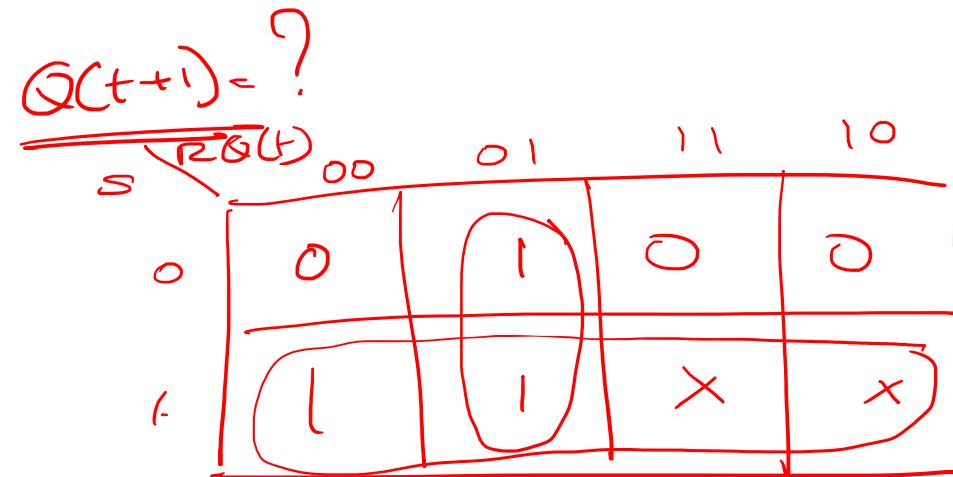


② NOR Latch



Characteristic equation: $S-R$ flip flop

Characteristic Table			
S	R	Q(t)	Q(t+1)
0	0	0	0 ✓
0	0	1	1 ✓
0	1	0	0 //
0	1	1	0 //
1	0	0	1 //
1	0	1	1 //
1	1	0	X
1	1	1	X



$$Q(t+1) = S + \bar{R} Q(t)$$

Rider or not to use

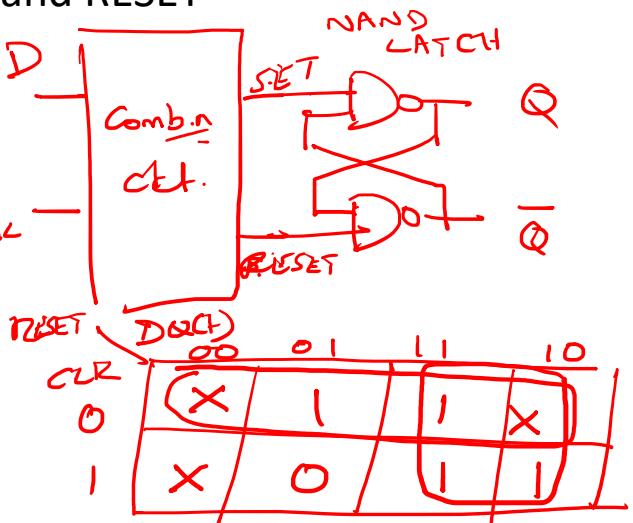
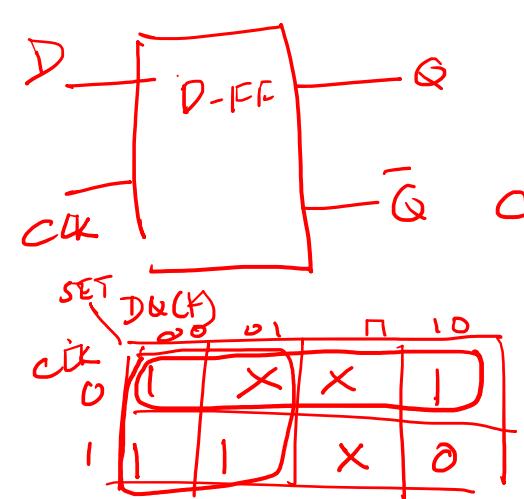
$S=1, R=1$ Not to use.

D Flip Flop using NAND latch

Function Table		
Clk	D	Output $Q(t+1)$
0	X	No change
1	0	0
1	1	1

Level

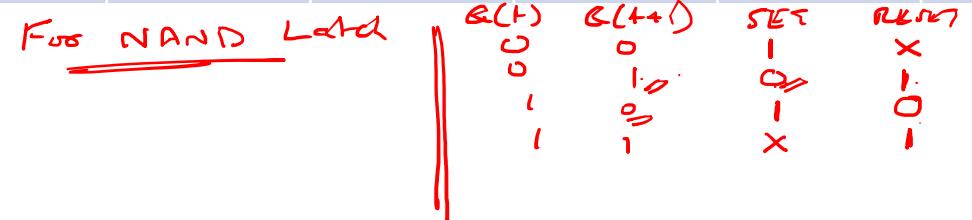
Equation for SET and RESET



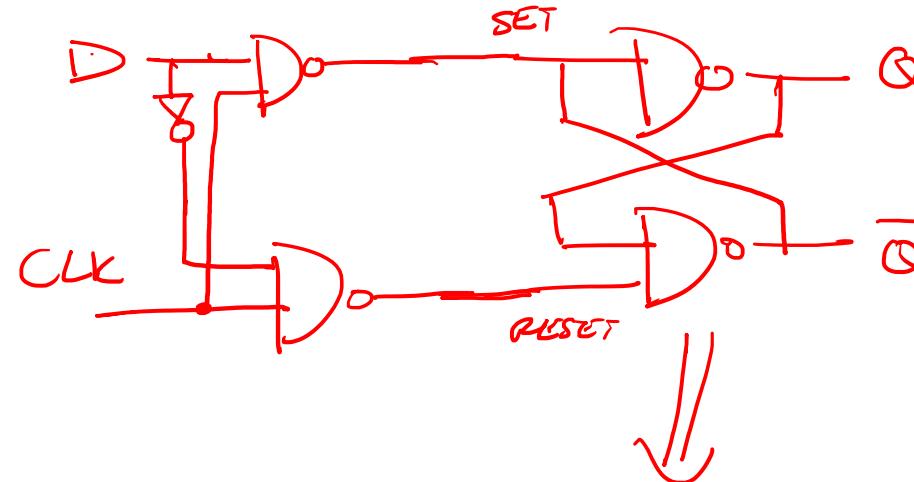
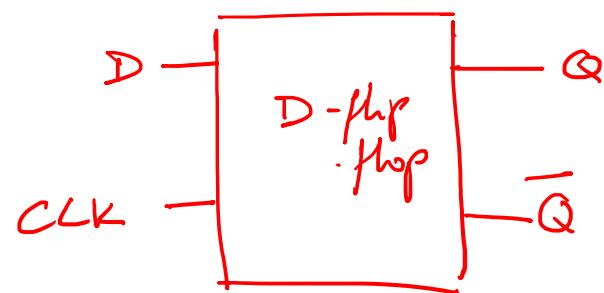
$$\boxed{\text{SET} = \overline{CLK} \cdot D}$$

$$\boxed{\text{RESET} = \overline{CLK} \cdot \overline{D}}$$

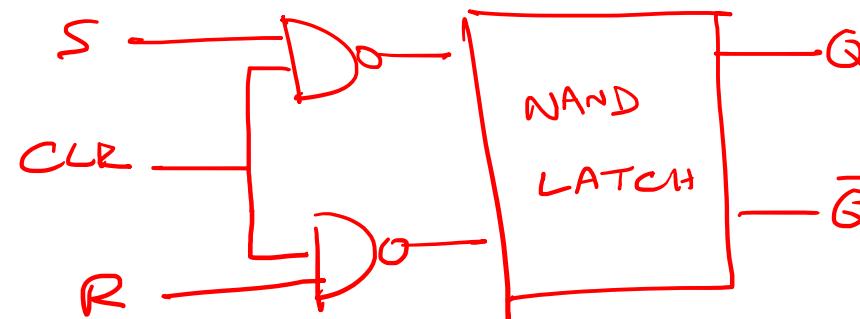
Excitation Table					
Clk	D	$Q(t)$	$Q(t+1)$	SET	RESET
0	0	0	0	1	X
0	0	1	1	X	1
0	1	0	0	1	X
0	1	1	1	X	1
1	0	0	0	1	X
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	1	0	1
1	1	1	1	X	1



Circuit and block diagram of D Flip Flop

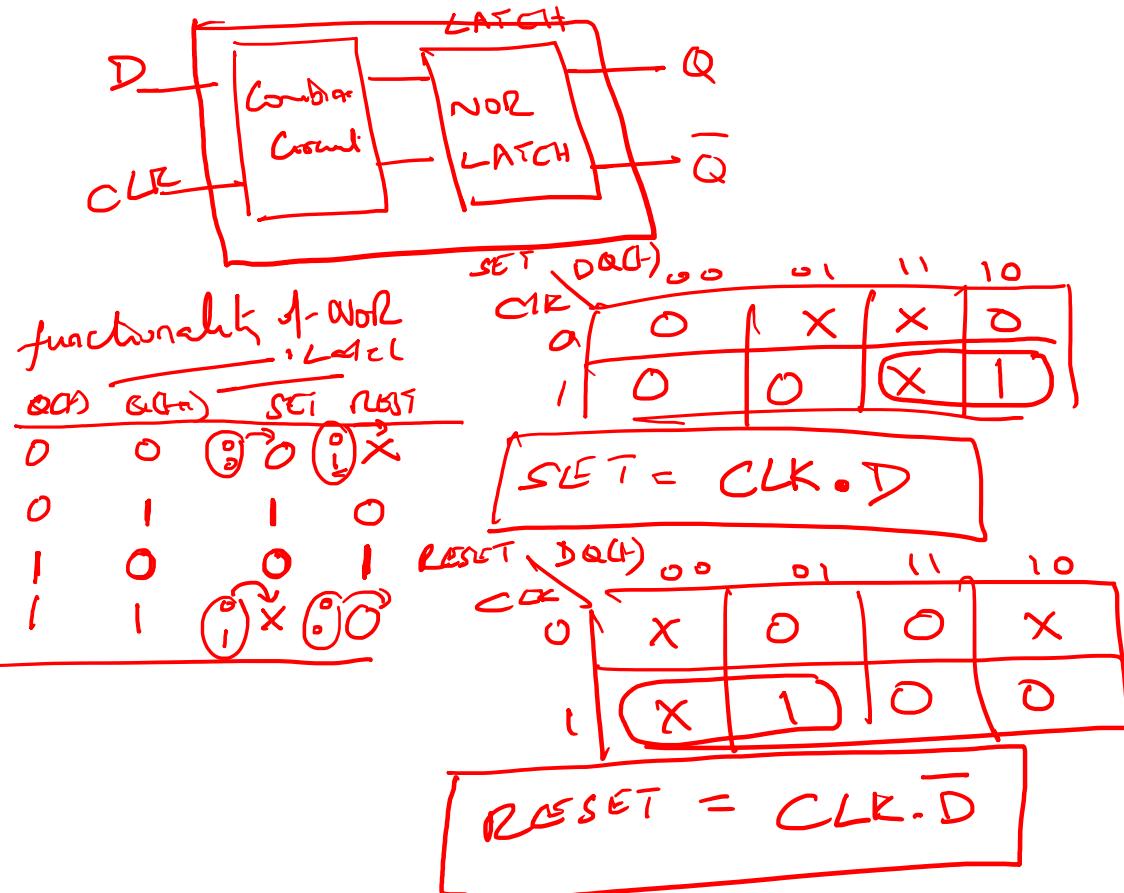


S-R flip flop w/t
NAND LATCH



D Flip Flop using NOR Latch

Equation for SET and RESET



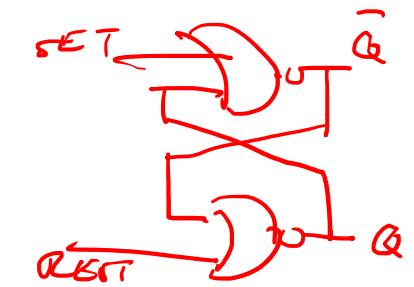
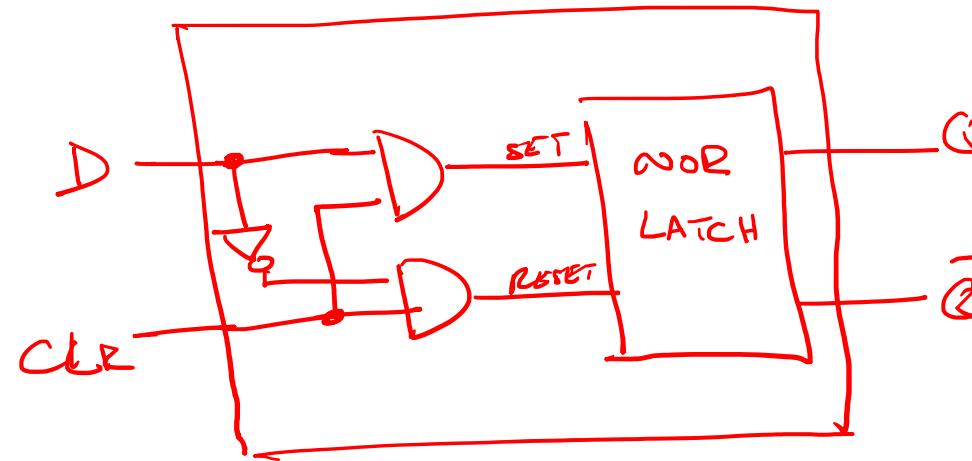
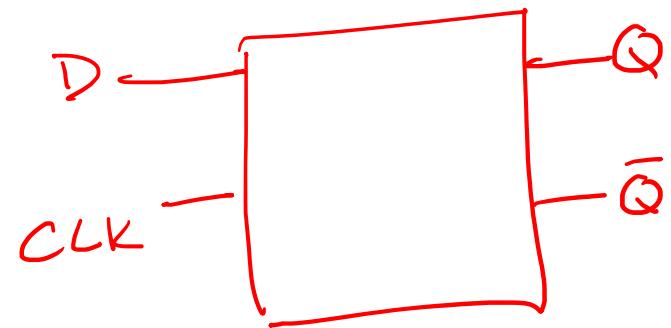
Excitation Table

Clk	D	Q(t)	Q(t+1)	SET	RESET
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	1	X	0
1	0	0	0	0	X
1	0	1	0	0	1
1	1	0	1	1	0
1	1	1	1	X	0

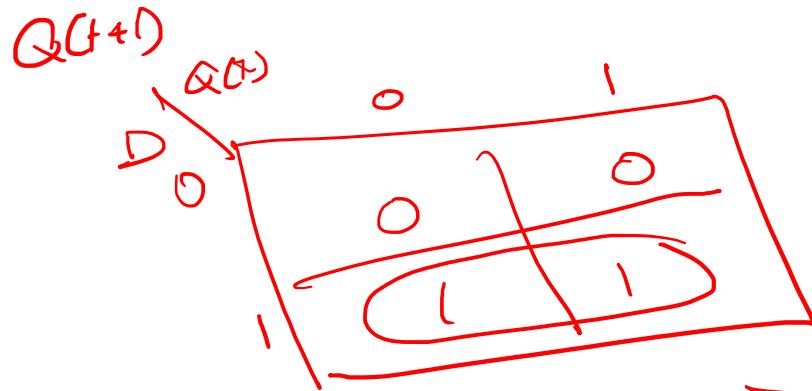
Circuit and block diagram of D Flip Flop

$$SET = CLK \cdot D$$

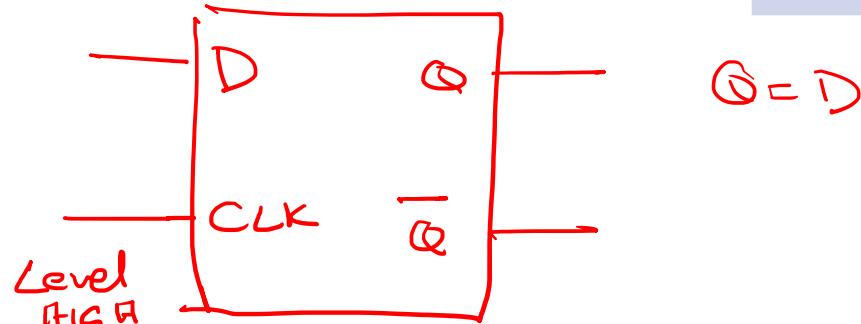
$$QRESET = CLK \cdot \bar{D}$$



Characteristic equation:



$$Q(t+1) = D$$



$$Q = D$$

	00	01	11	10
0	0	0	1	0
1	0	0	1	1

$$Q(t+1) = \bar{CLK} Q(t) + CLK D$$

Characteristic Table for D FF		
D	Q(t)	Q(t+1)
0	0	0
0	1	0
1	0	1
1	1	1

CLK	D	Q(t)	Q(t+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

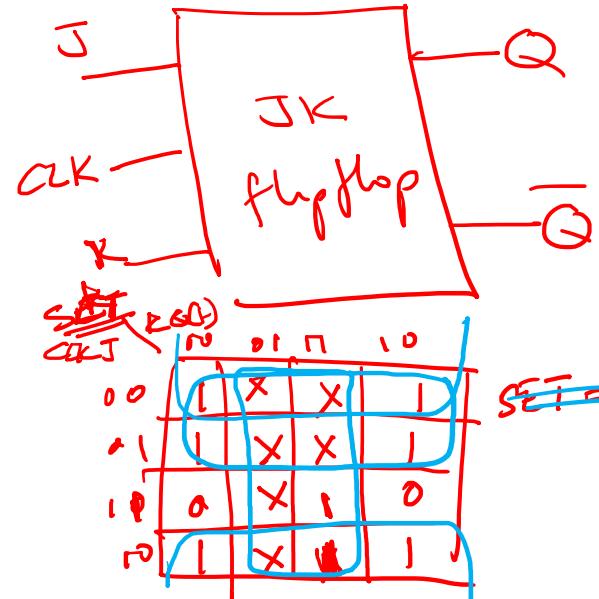
JK JK Flip Flop using NAND latch

Function Table of JK flip flop

Clk	J	K	Output	$Q(t+1)$
0	X	X	No Change	$Q(t)$ or previous state
1	0	0	No Change	$= Q(t)$
1	0	1	Reset	$Q(t) = 0$
1	1	0	Set	$Q(t) = 1$
1	1	1	Toggle	$Q(t)$

Equation for SET and RESET

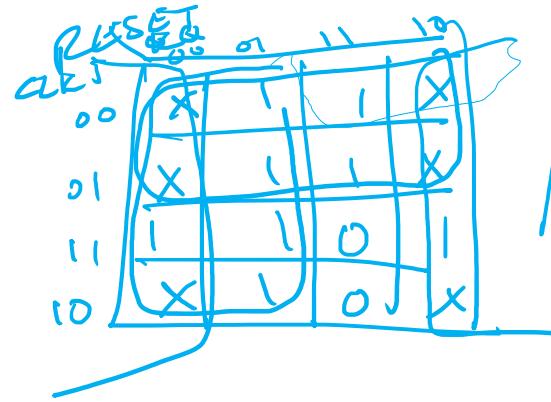
NAND LATCH Function			
$Q(t)$	$Q(t+1)$	SET	RESET
0	1	1	X
0	0	0	1
1	0	X	0
1	1	1	1



$$\begin{aligned} SET &= Q(t) \\ SET &= \overline{Q(t)} + \overline{CLK} + J \\ SET &= \overline{Q(t)} \cdot \overline{CLK} \cdot J \end{aligned}$$

Clk	J	K	Q(t)	Q(t+1)	SET	RESET
0	0	0	0	0	1	X
0	0	0	1	1	X	1
0	0	1	0	0	1	X
0	0	1	1	1	X	1
0	1	0	0	0	0	X
0	1	0	1	1	X	1
0	1	1	0	0	1	X
0	1	1	1	1	X	1
1	0	0	0	0	0	X
1	0	0	1	1	X	1
1	0	1	0	0	0	X
1	0	1	1	1	1	X
1	1	0	0	1	0	1
1	1	0	1	0	X	1
1	1	1	0	1	0	1
1	1	1	1	0	1	0

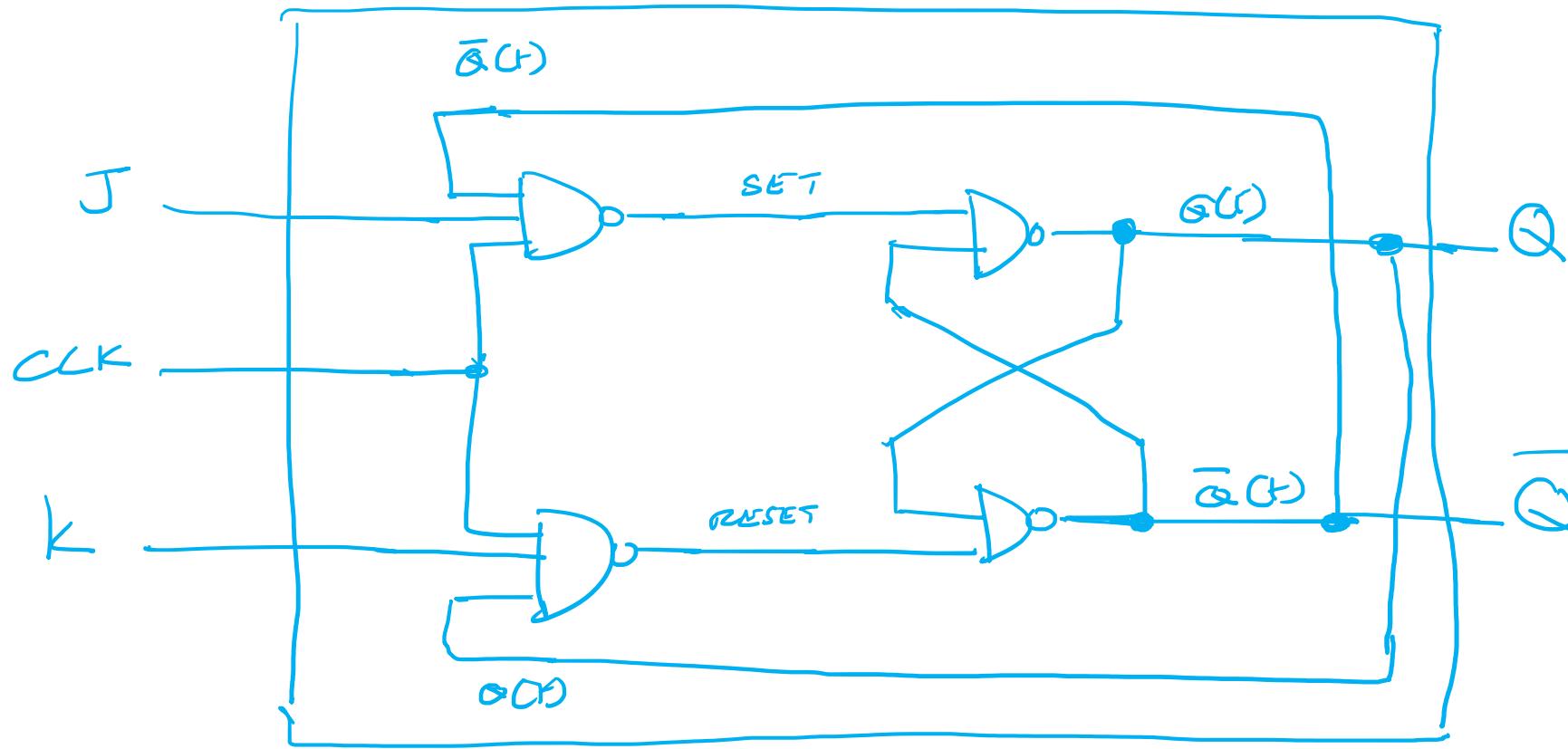
Circuit and block diagram of JK flip flop:



$$\text{RESET} = \bar{K} + \bar{C}\bar{L}K + \bar{Q}(t)$$

$$\text{RESET} = \bar{C}\bar{L}K \cdot Q(t)$$

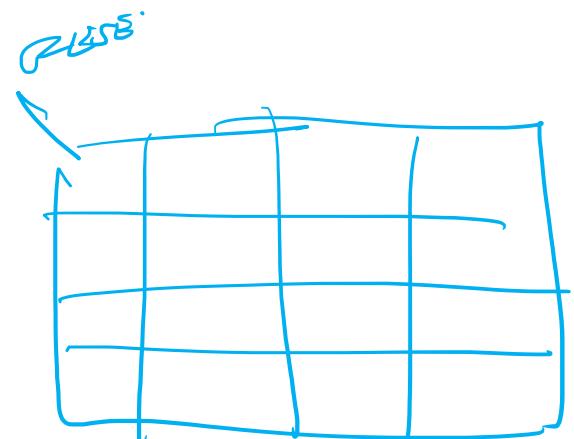
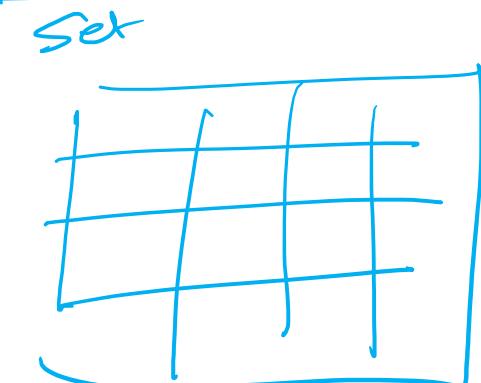
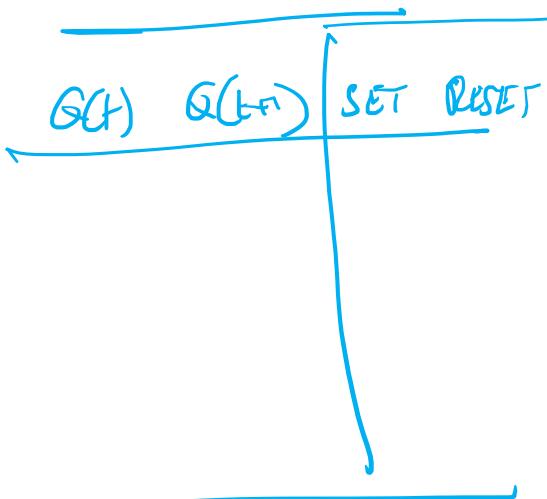
$$\text{SET} = \bar{C}\bar{L}K \cdot J \cdot \bar{Q}(t)$$



JK Flip Flop using NOR latch

Equation for SET and RESET

functionality of NOR LATCH



Functional Table of JK

CLR	J	K	output
0	x	x	No change
1	0	0	No change
1	0	1	Reset
1	1	0	SET
1	1	1	Toggle

Clk	J	K	Q(t)	Q(t+1)	SET	RESET
0	0	0	0	0		
0	0	0	1	1		
0	0	1	0	0		
0	0	1	1	1		
0	1	0	0	0		
0	1	0	1	1		
0	1	1	0	0		pls. Enter
0	1	1	1	1		
1	0	0	0	0		
1	0	0	1	1		
1	0	1	0	0		RESET
1	0	1	1	0		
1	1	0	0	0	SET	
1	1	0	1	1		
1	1	1	0	1		
1	1	1	1	0		

Circuit and Block Diagram

Circuit-

& Block diagram

Characteristic Table			
J	K	Q(t)	Q(t+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Characteristic equation:

$$\bar{J} \bar{Q}(t) + \bar{K} Q(t) = 0$$

Characteristic Equation

$$Q(t+1) = \bar{J} \bar{Q}(t) + \bar{K} Q(t)$$