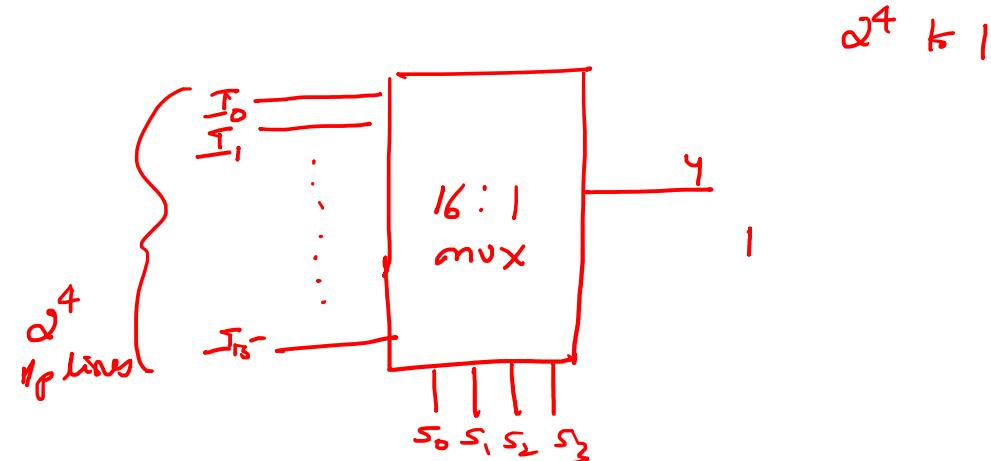
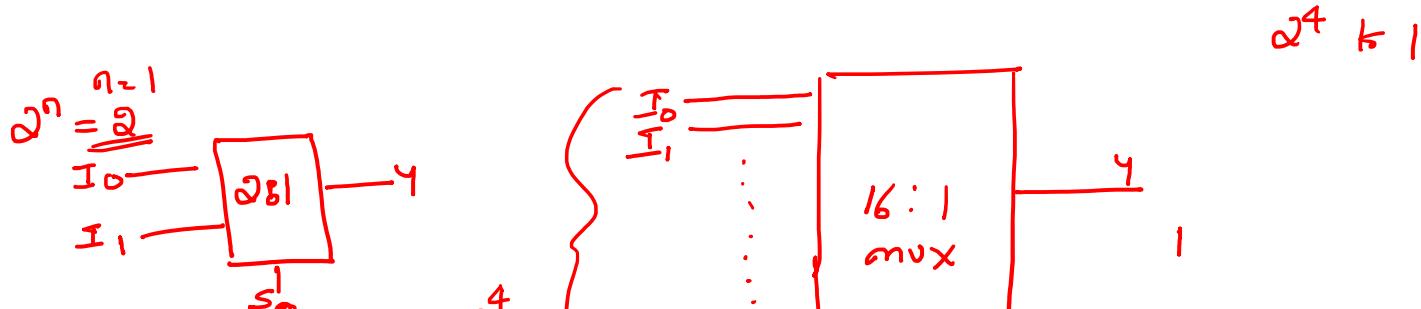
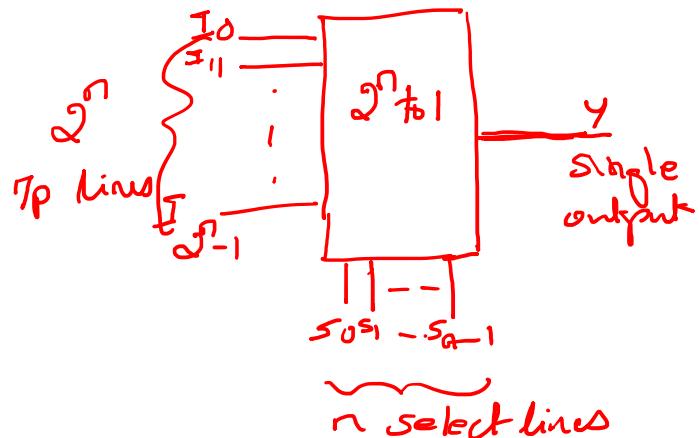


# Multiplexers

Students are advised to write down the notes for every lecture

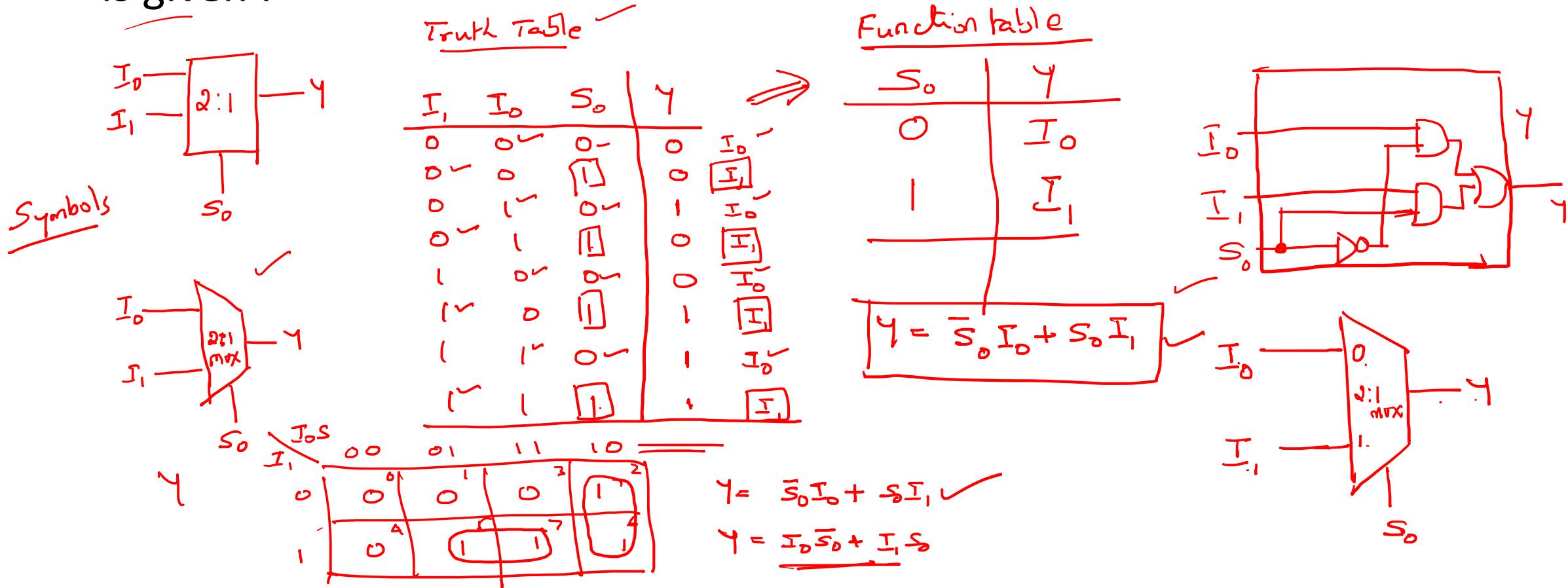
# Multiplexer

- Multiplexer is an useful MSI device and are also called as data selectors.
- Multiplexer selects one of its  $2^n$  input line and directs it to a single output line .
- n-bit select lines decide which input line is to be selected.
- Examples: 2-to-1 line MUX, 4-to-1 line MUX, 8-to-1 line MUX, 16-to-1 line MUX.

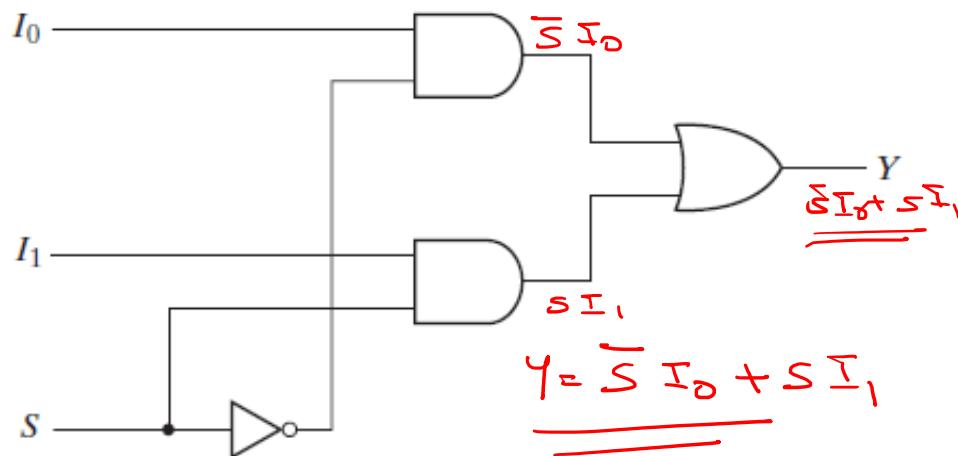


## 2-to-1 line MUX

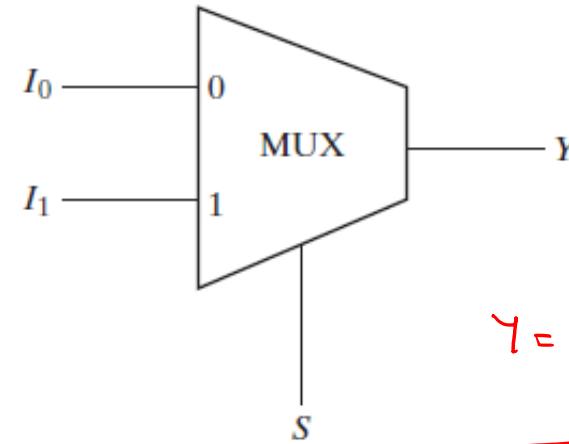
- S- selection input, y is the output, I<sub>1</sub> and I<sub>0</sub> are inputs
- Symbol/block diagram, function table, output expressions and circuit is given :



## 2-to-1 line MUX



(a) Logic diagram



(b) Block diagram

Application

Assume there are two users  
→ Transmitting data

$I_0$

$I_1$

Channel

$y = \dots I_0 I_1 I_0 I_1 I_0 I_1 I_0 I_1 \dots$

A timing diagram illustrating the transmission of data over time. The horizontal axis is labeled  $t \rightarrow$  and shows time points  $t_1, t_2, t_3, t_4, t_5, t_6, t_7, t_8, \dots$ . Vertical lines represent the data bits  $I_0$  and  $I_1$  being transmitted at different times. The sequence of bits is  $I_0, I_1, I_0, I_1, I_0, I_1, I_0, I_1, \dots$

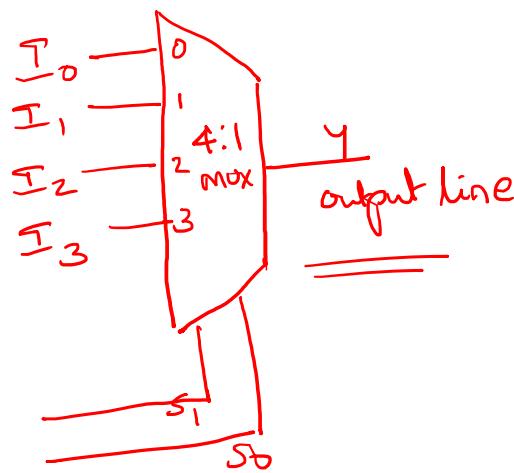
## 4-to-1 line multiplexer

2<sup>n</sup> to 1 mux

$n = \text{select lines} = \underline{\underline{2}}$

2<sup>n</sup> input lines: 4

- Write the Symbol/block diagram, Function table, output expressions and circuit .

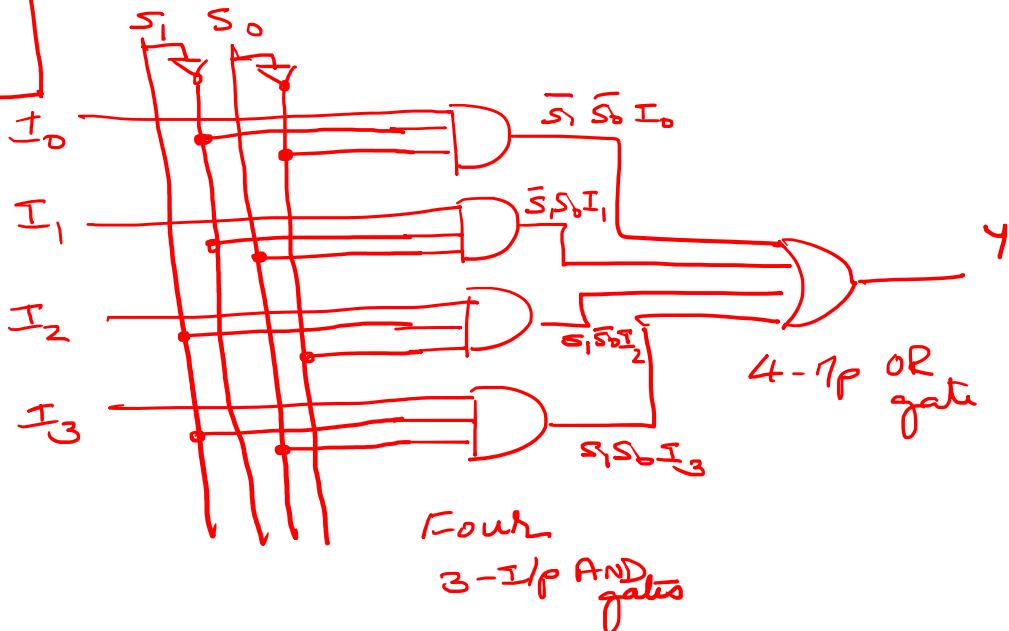


Symbol / Block diagram  
of 4:1 MUX

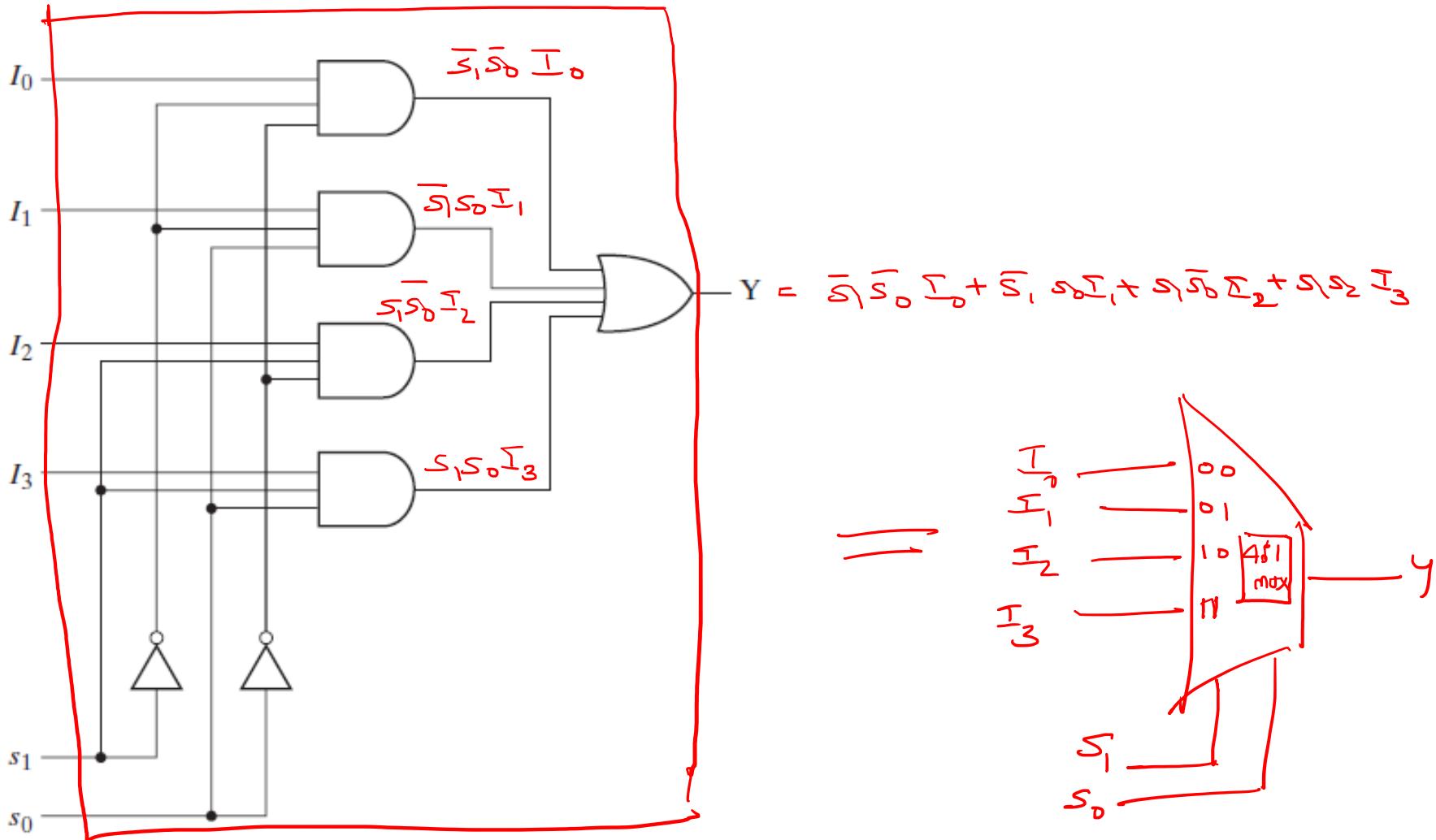
Function Table

$S_1$	$S_0$	$Y$
0	0	$I_0$
0	1	$I_1$
1	0	$I_2$
1	1	$I_3$

$$Y = \bar{s}_1 \bar{s}_0 I_0 + \bar{s}_1 s_0 I_1 + s_1 \bar{s}_0 I_2 + s_1 s_0 I_3$$



## 4-to-1 line multiplexer

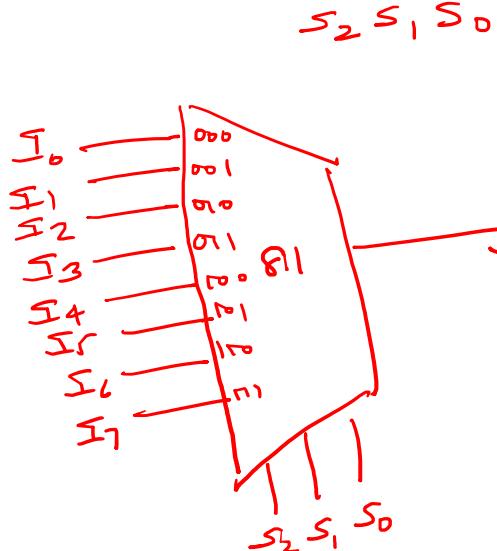


# 8-to-1 line multiplexer

- Write the Symbol/block diagram, function table, output expressions and circuit

How many  $I_P$  lines:  $2^n = 8 \Rightarrow I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7$   
Any mux has  $2^n I_P$  lines

How many select lines?  $n$  select lines = 3



=			$Y$
$S_2$	$S_1$	$S_0$	
0	0	0	$I_0$
0	0	1	$I_1$
0	1	0	$I_2$
0	1	1	$I_3$
1	0	0	$I_4$
1	0	1	$I_5$
1	1	0	$I_6$
1	1	1	$I_7$

$Y = 8$  terms

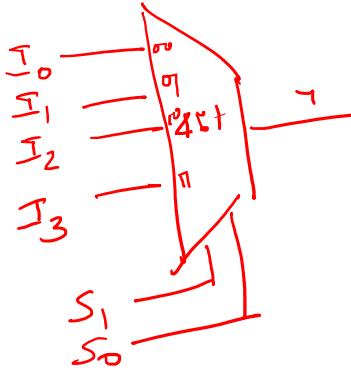
$$Y = I_0 ( ) + I_1 ( ) + \dots + \dots$$

$$= \bar{S}_2 \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_2 \bar{S}_1 S_0 I_1 + \bar{S}_2 S_1 \bar{S}_0 I_2 + \bar{S}_2 S_1 S_0 I_3$$

$$+ S_2 \bar{S}_1 \bar{S}_0 I_4 + S_2 \bar{S}_1 S_0 I_5 + S_2 S_1 \bar{S}_0 I_6 + S_2 S_1 S_0 I_7$$

$$= \bar{S}_2 ( ) + S_2 ( )$$

## Realize 4:1 using only 2:1 MUXs (Multiplexer tree)



## 4:1 mux

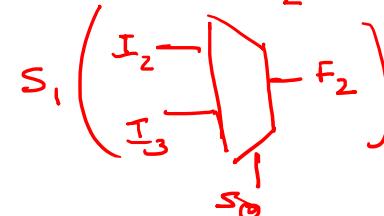
$$Y = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 \Sigma_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3$$

$$= \bar{S}_1 (\bar{S}_p \mathbb{I}_0 + S_0 \mathbb{I}_1) + S_1 (\bar{S}_0 \mathbb{I}_2 + S_0 \mathbb{I}_3)$$

281 min

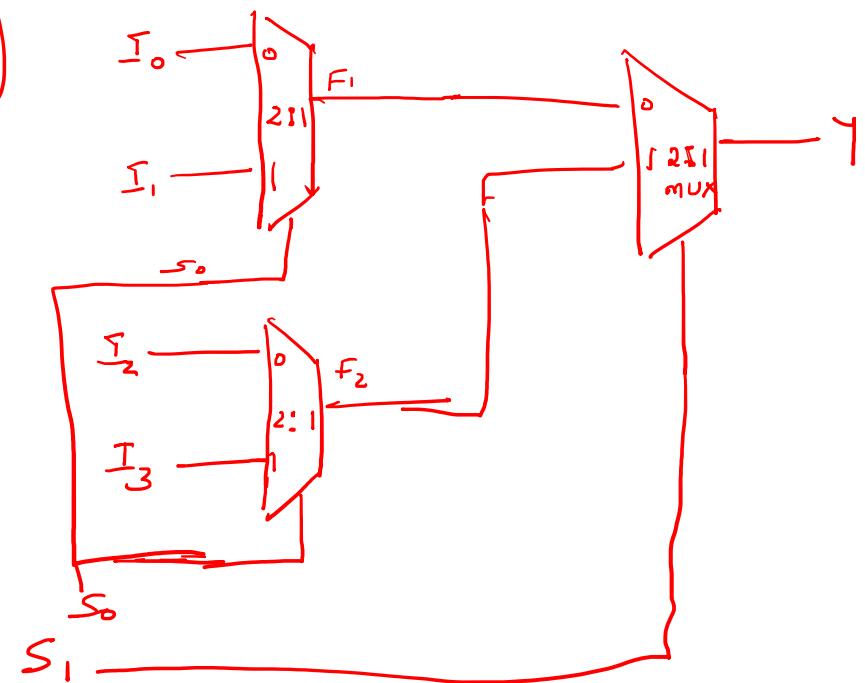
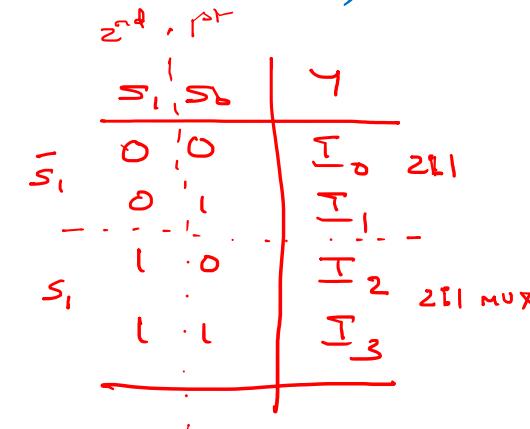


2:1 mnx



$$Y = \overline{S}_1 F_1 + S_2 F_2$$

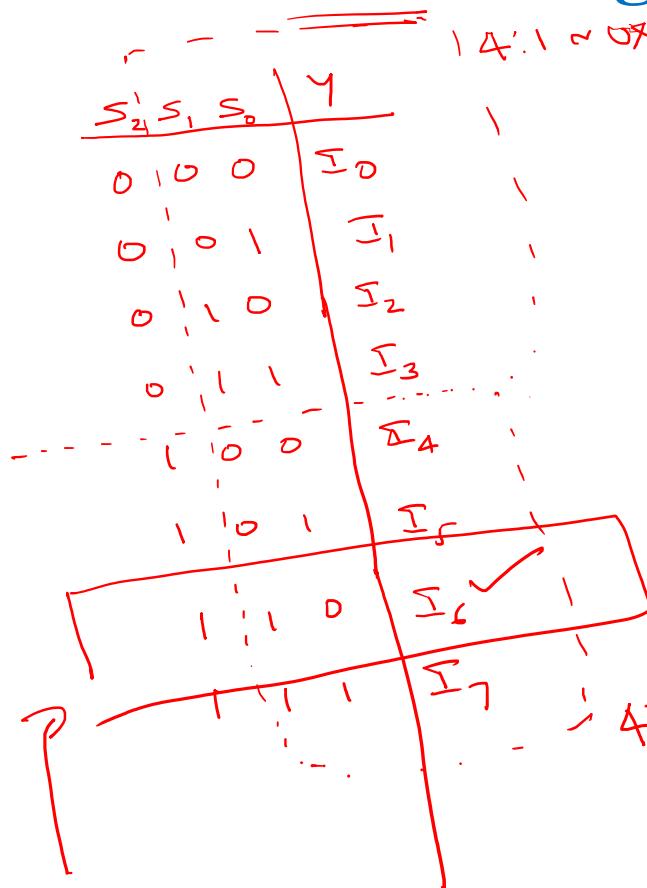
A free body diagram of a rectangular block. A vertical force  $F_1$  acts upwards at the top center. A horizontal force  $F_2$  acts to the right at the top left corner. A force  $S_1$  acts downwards and to the right at the bottom left corner. The block is labeled with a letter 'Y' at its top right corner.



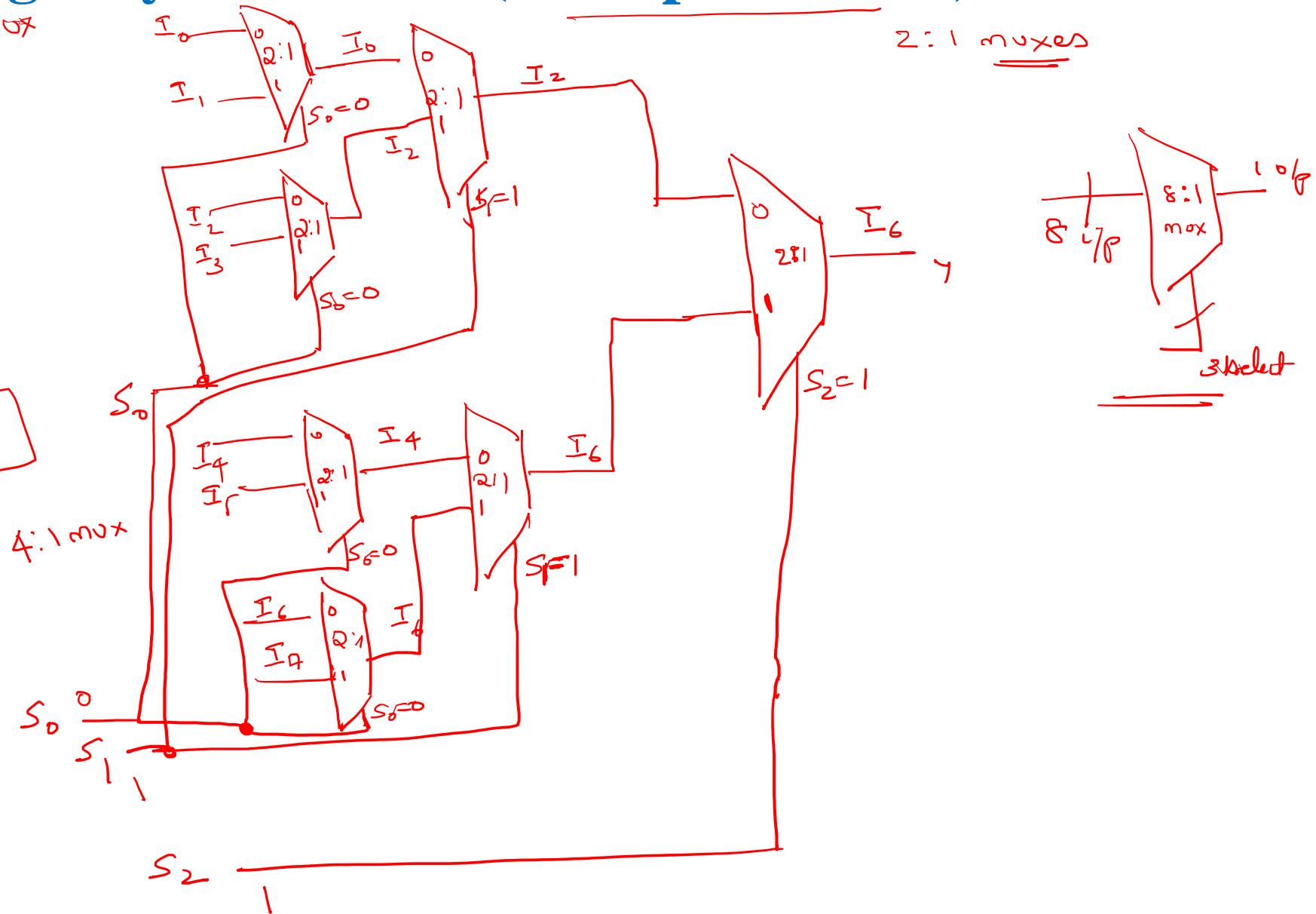
**Realize 4:1 using only 2:1 MUXs (Multiplexer tree)**

$2^3 : 1$   
3 select lines  
8 input lines

# Realize 8:1 using only 2:1 MUXes (Multiplexer tree)



Ex:  
when



# Realize 8:1 using only 4:1 MUXs and 2:1 MUX

$$\begin{aligned}
 Y &= \bar{S}_2 \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_2 \bar{S}_1 S_0 I_1 + \bar{S}_2 S_1 \bar{S}_0 I_2 + \bar{S}_2 S_1 S_0 I_3 \\
 &\quad + S_2 \bar{S}_1 \bar{S}_0 I_4 + S_2 \bar{S}_1 S_0 I_5 + S_2 S_1 \bar{S}_0 I_6 + S_2 S_1 S_0 I_7
 \end{aligned}$$

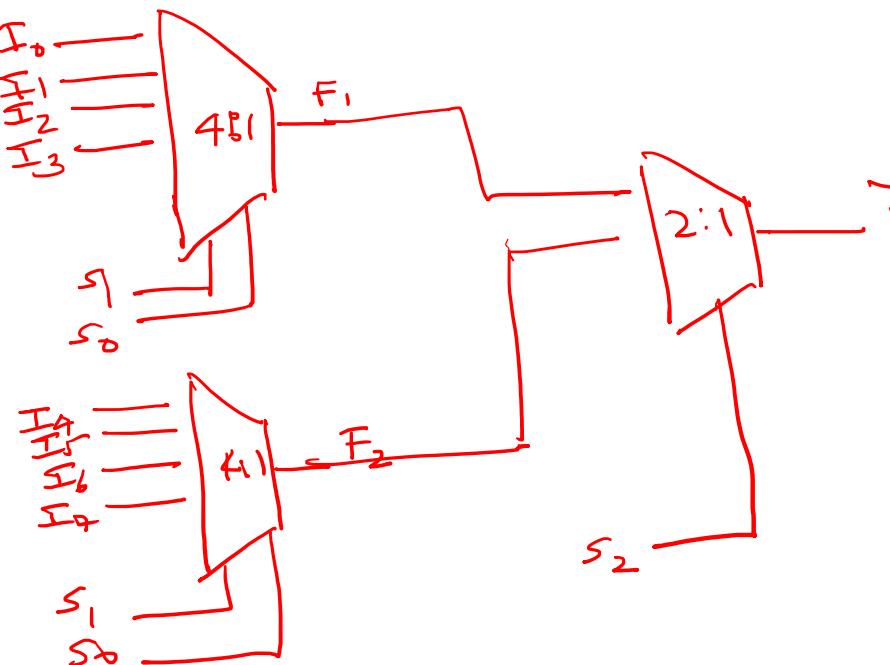
*4:1 mux*

$$= \bar{S}_2 \left( \underbrace{\bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3}_{F_1} \right) + S_2 \left( \underbrace{\bar{S}_1 \bar{S}_0 I_4 + \bar{S}_1 S_0 I_5 + S_1 \bar{S}_0 I_6 + S_1 S_0 I_7}_{F_2} \right)$$

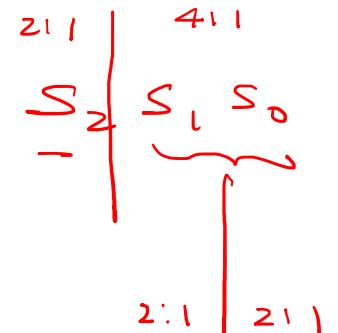
*2:1 mux*

$$= \bar{S}_2 (F_1) + S_2 (F_2)$$

output function for 8:1 mux



first select  
select lines



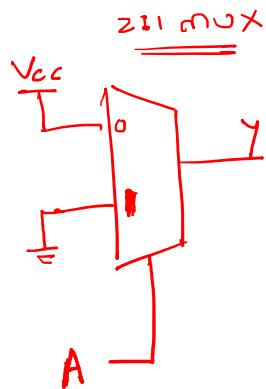
# Realize each of the basic logic gates using 2:1 MUX

NOT

OR

AND

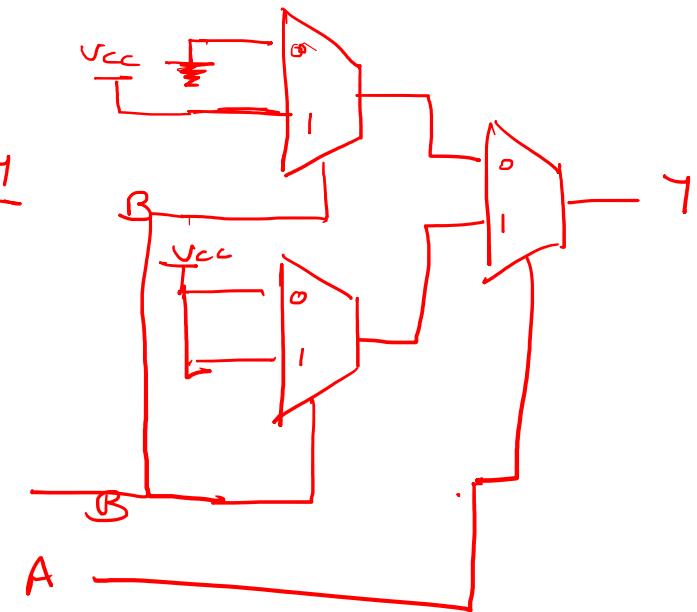
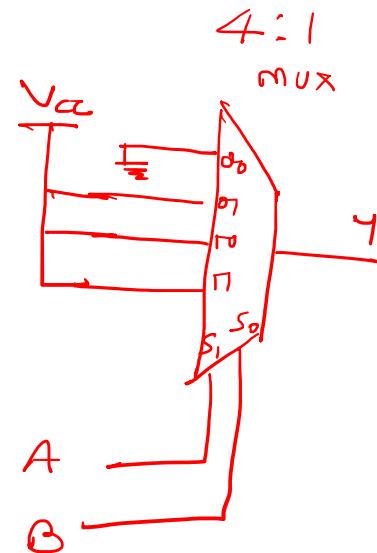
NOT

$$\begin{array}{c} Y = \bar{A} \\ \hline A & Y \\ \hline 0 & 1 \\ 1 & 0 \end{array}$$


AND Gate.

$$\begin{array}{c} S_1 \ S_0 \\ \hline A \ B & Y \\ \hline 0 \ 0 & 0 \\ 0 \ 1 & 0 \\ 1 \ 0 & 0 \\ 1 \ 1 & 1 \end{array}$$

OR Gate

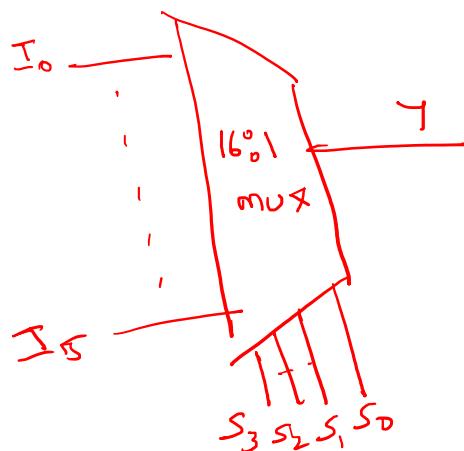
$$\begin{array}{c} S_1 \ S_0 \\ \hline A \ B & Y \\ \hline 0 \ 0 & 0 \\ 0 \ 1 & 1 \\ 1 \ 0 & 1 \\ 1 \ 1 & 1 \end{array}$$


Homework for you

# 16-to-1 line multiplexer----Exercise for you

- Write the Symbol/block diagram, function table, output expressions and circuit

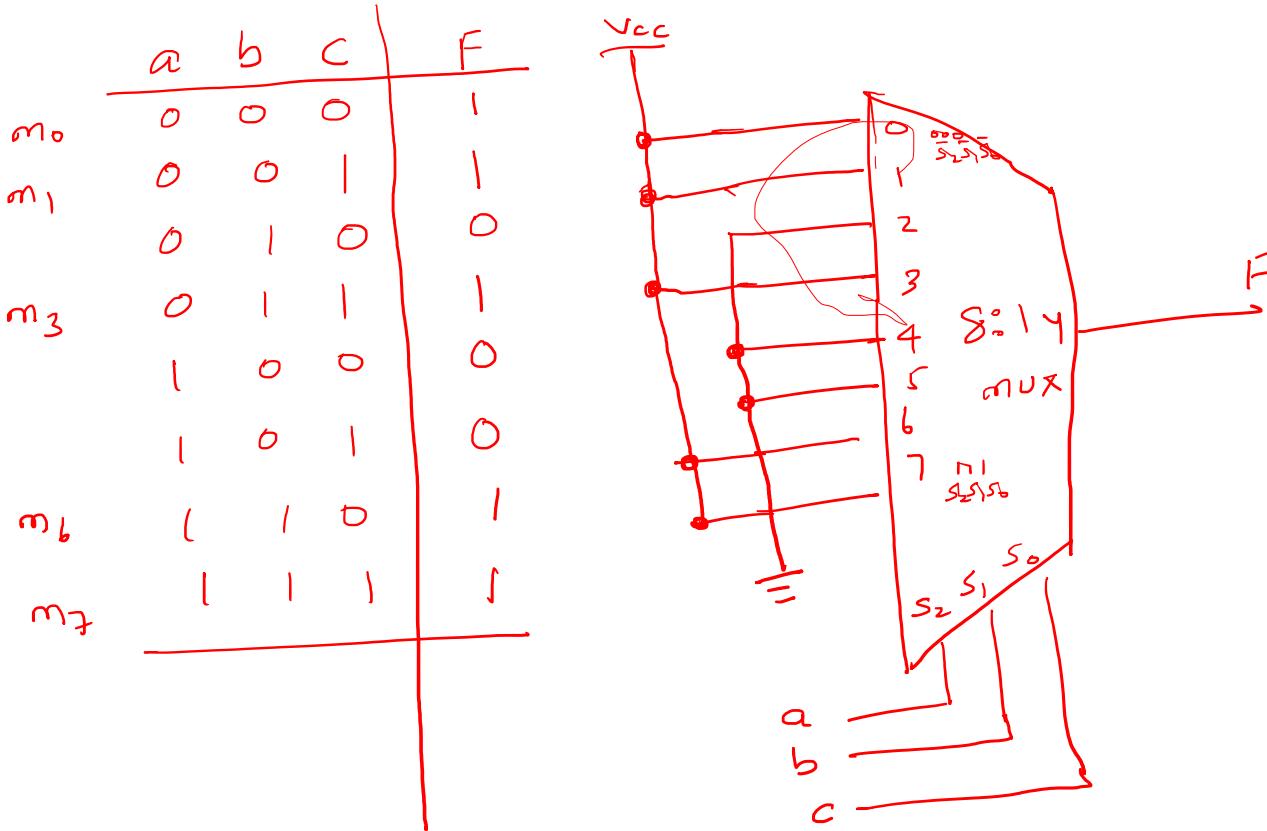
16:1 mux  
2<sup>n</sup> lines  $\therefore p = 16$   
 $n = 4 \Leftarrow \log_2^{16}$



$$Y = \bar{S}_3 \bar{S}_2 \bar{S}_1 \bar{S}_0 I_0 + \dots + S_3 S_2 S_1 S_0 I_{15}$$

# Multiplexer application in logic design

- Implement the function  $F(a,b,c) = \sum m(0,1,3,6,7)$  using
  - 8:1 MUX only
  - Minimum no. of 4:1 MUXs only

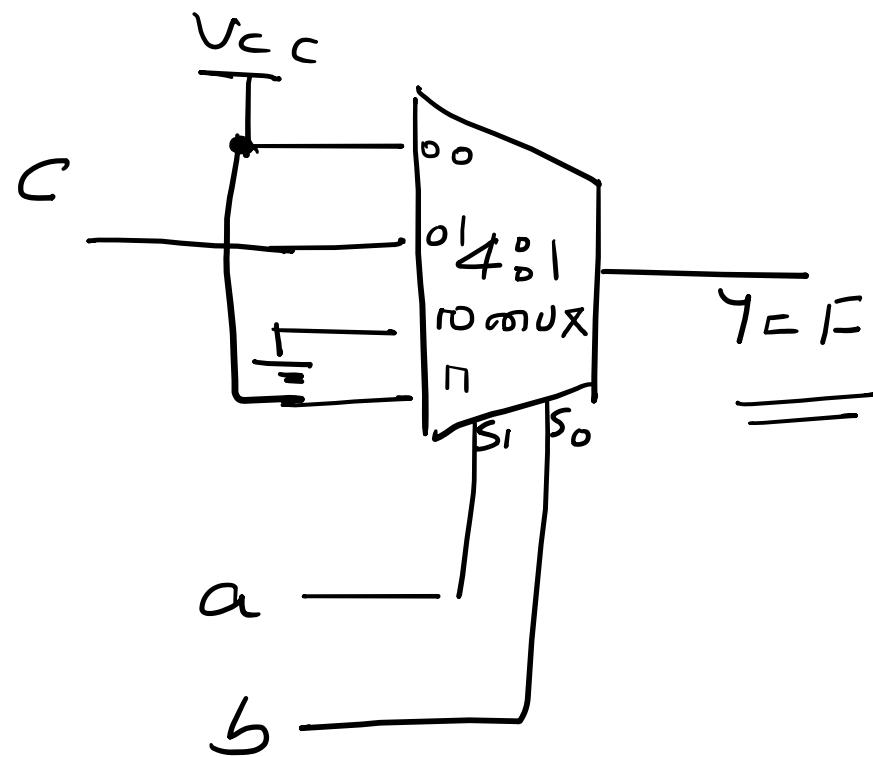


# Multiplexer application in logic design

- Implement the function  $F(a,b,c) = \sum m(0,1,3,6,7)$  using
  - 8:1 MUX only
  - Minimum no. of 4:1 MUXs only

msb      a      b      c      F       $F_{\text{NEW}}$

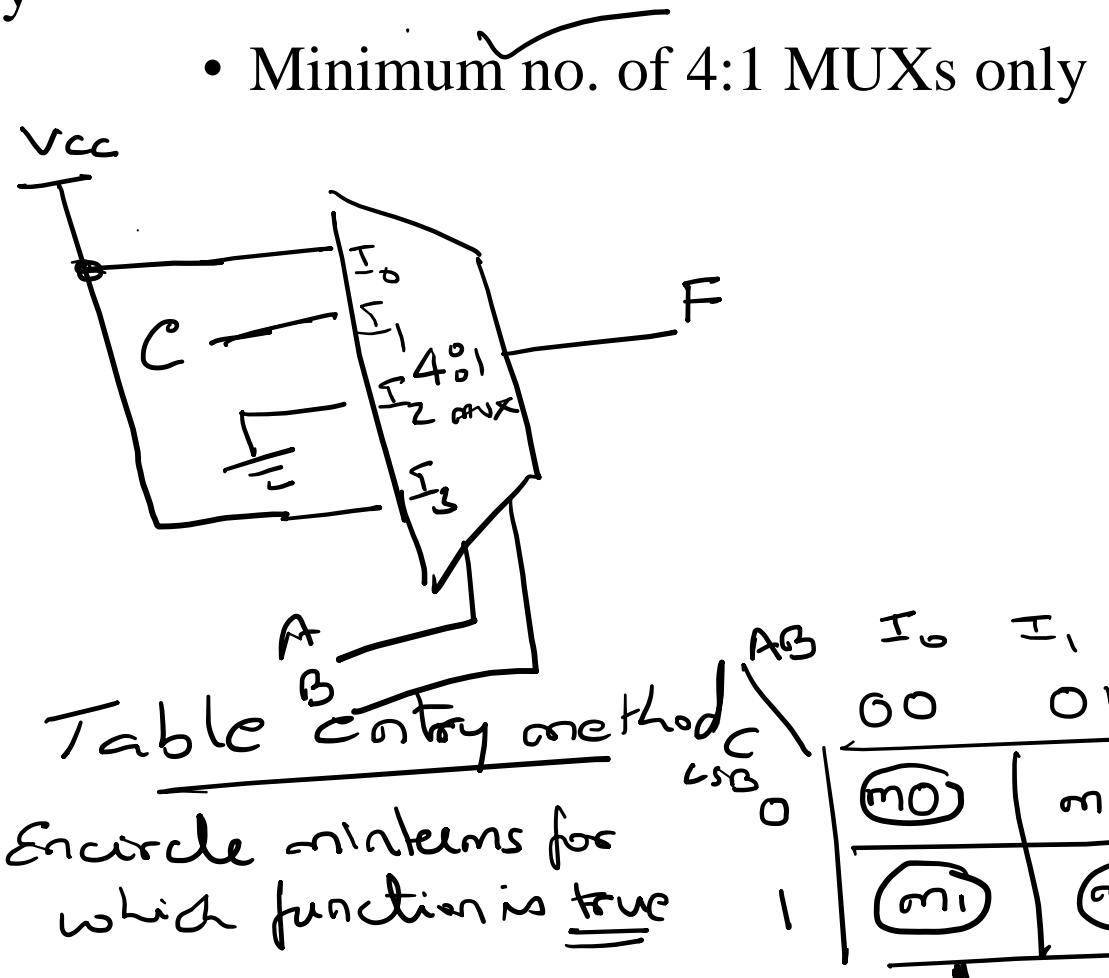
$m_0$	0	0	$\bar{c}$	1	$\bar{c} \cdot 1 + \bar{c} \cdot 1 = \bar{c} + \bar{c} = 1$
$m_1$	0	0	c	1	$\bar{c} \cdot 0 + c \cdot 1 = 0 + c = c$
$m_3$	0	1	$\bar{c}$	0	$\bar{c} \cdot 0 + c \cdot 0 = 0$
$m_6$	1	0	$\bar{c}$	0	$\bar{c} \cdot 1 + c \cdot 1 = \bar{c} + c = 1$
$m_7$	1	1	c	1	$= 1$



# Multiplexer application in logic design

- Implement the function  $F(a,b,c) = \sum m(0,1,3,6,7)$  using
  - 8:1 MUX only
  - Minimum no. of 4:1 MUXs only

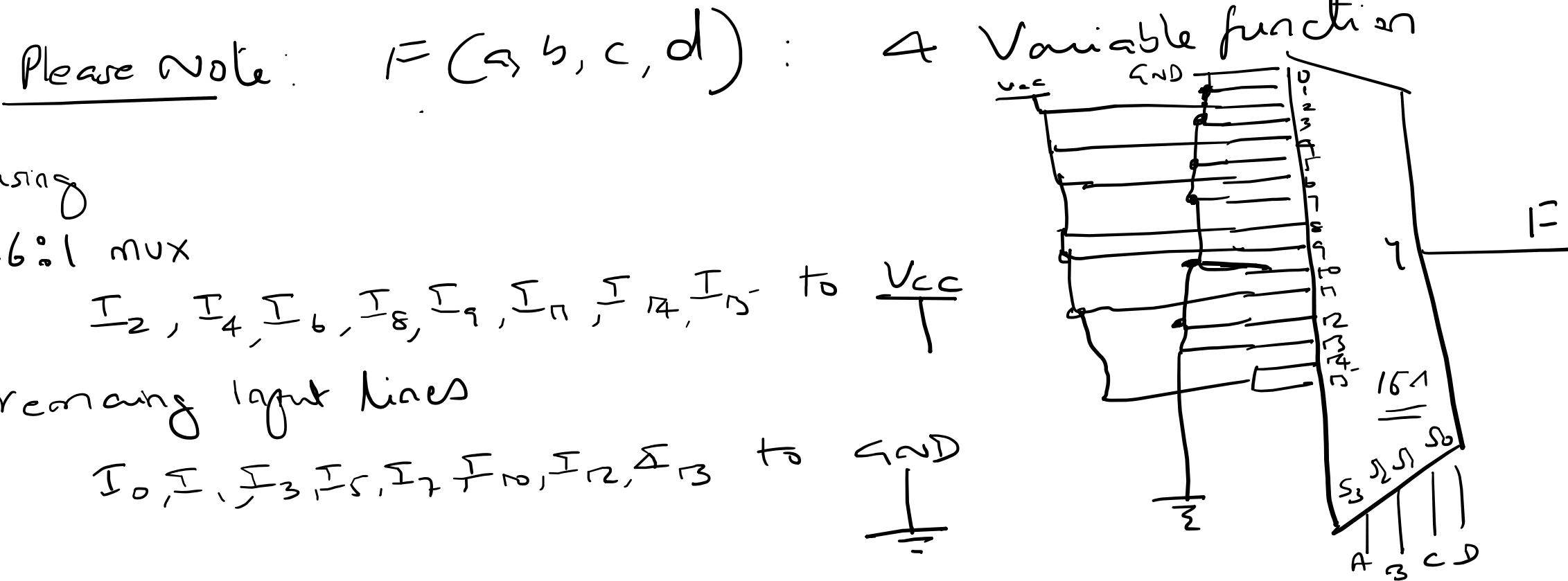
	A	B	C	F
$m_0$	0	0	0	1
$m_1$	0	0	1	1
$m_2$	0	1	0	0
$m_3$	0	1	1	1
$m_4$	1	0	0	0
$m_5$	1	0	1	0
$m_6$	1	1	0	1
$m_7$	1	1	1	1



	$I_0$	$I_1$	$I_2$	$I_3$
$C$	00	01	10	11
0	$m_0$	$m_2$	$m_4$	$m_6$
1	$m_1$	$m_3$	$m_5$	$m_7$

# Implement the function $F(a,b,c,d) = \Sigma m(2,4,6,8,9,11,14,15)$

- using
  - . 8:1 MUX and one NOT gate
  - . 4:1 MUX and external gates
  - . 4:1 MUX and 2:1MUXs only

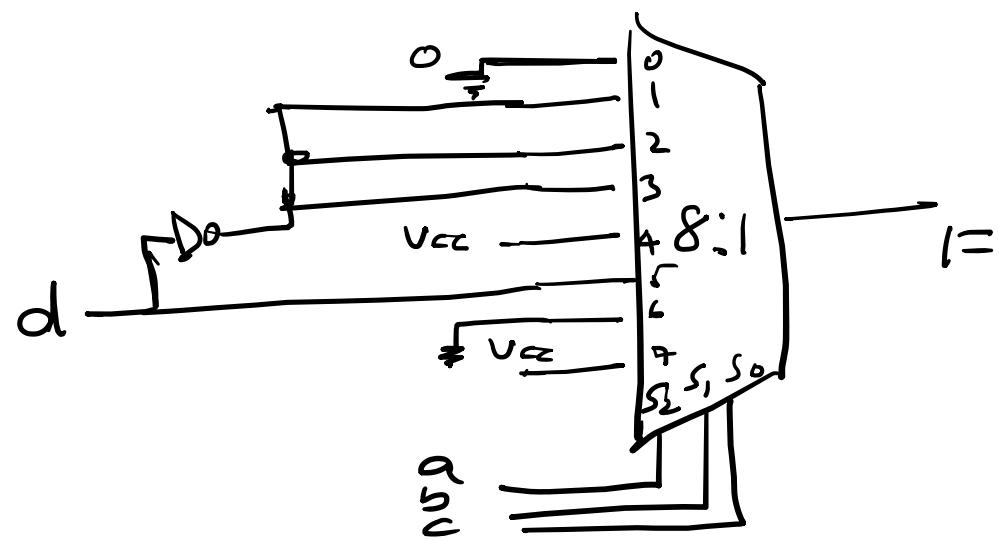


# Implement the function $F(a,b,c,d) = \sum m(2,4,6,8, 9,11,14,15)$

- using
  - . 8:1 MUX and one NOT gate ✓
  - . 4:1 MUX and external gates .
  - . 4:1 MUX and 2:1MUXs only

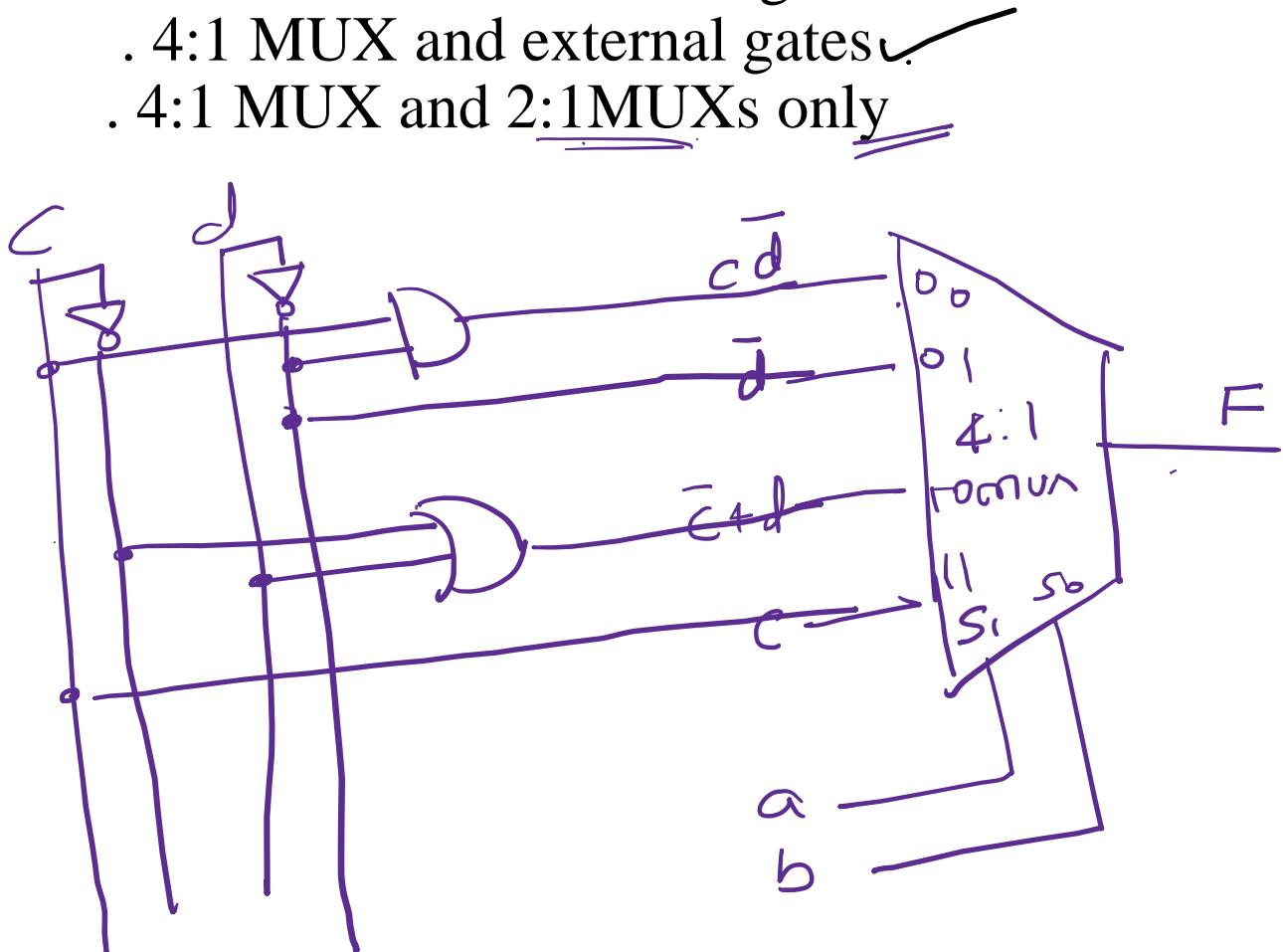
table for  $I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7$

$a$	$b$	$c$	$I_0$	$I_1$	$I_2$	$I_3$	$I_4$	$I_5$	$I_6$	$I_7$
0	0	0	000	001	010	011	100	101	110	111
0	1	0	0	2	4	6	8	10	12	14
1	0	0	1	3	5	7	9	11	13	15
1	1	0	0	d	d	d	1	d	0	1



# Implement the function $F(a,b,c,d) = \sum m(2,4,6,8,9,11,14,15)$

- using
  - . 8:1 MUX and one NOT gate
  - . 4:1 MUX and external gates ✓
  - . 4:1 MUX and 2:1MUXs only



$a$	$b$	$c$	$d$	$F$	$F_{new}$
0	0	0	0	00	
0	0	0	1	00	
0	0	1	0	1	
0	0	1	1	0	
0	1	0	0	1	$\bar{c}\bar{d}$
0	1	0	1	0	$\bar{c}d + c\bar{d}$
0	1	1	0	0	$\bar{c}\bar{d} + \bar{c}d + c\bar{d}$
0	1	1	1	0	$\bar{c}d + c\bar{d}$
1	0	0	0	1	$\bar{c} + \bar{d}$
1	0	0	1	0	$\bar{c} + d$
1	0	1	0	0	
1	0	1	1	1	
1	1	0	0	0	$c$
1	1	0	1	0	
1	1	1	0	1	
1	1	1	1	1	

# Nibble Multiplexer

a 4-bit combination in digital circuit  
NIBBLE

8-bit  $\rightarrow$  6-bit

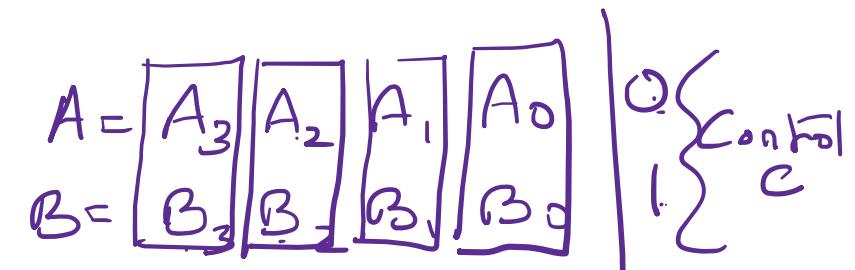
- A and B are two 4-bit numbers. Design a combinational circuit using suitable multiplexers according to following requirements.

- If  $\text{ctrl\_ip} == 0$

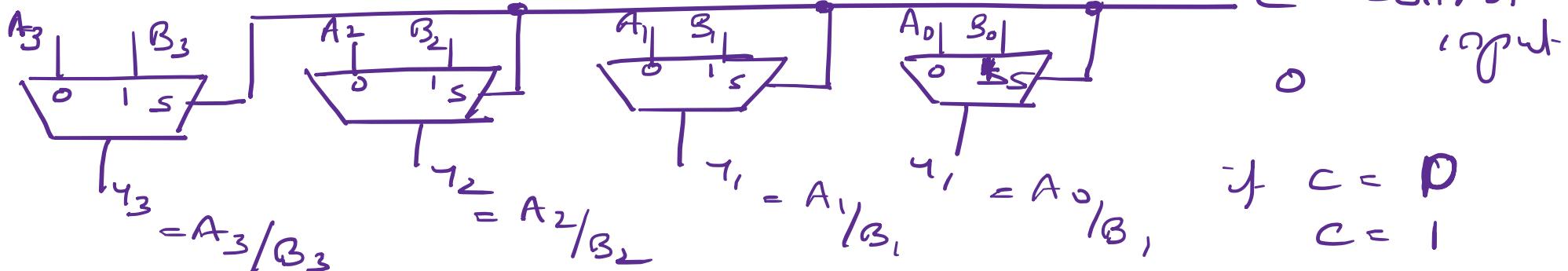
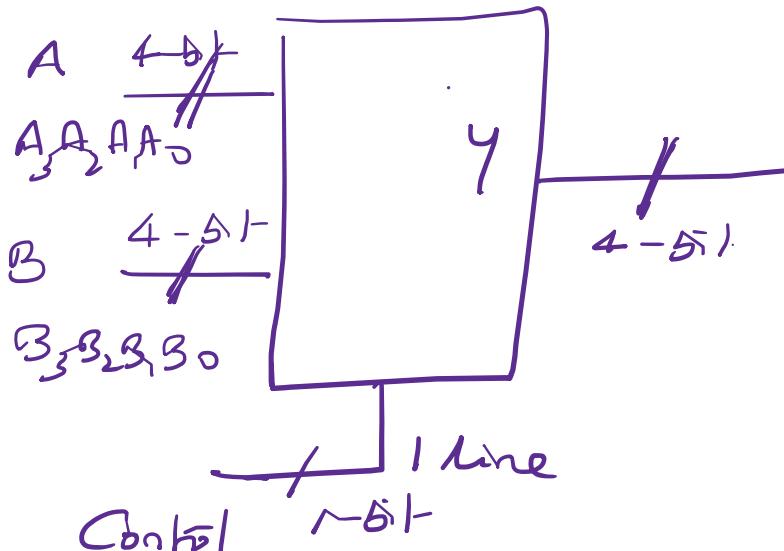
$$\text{Output} = A$$

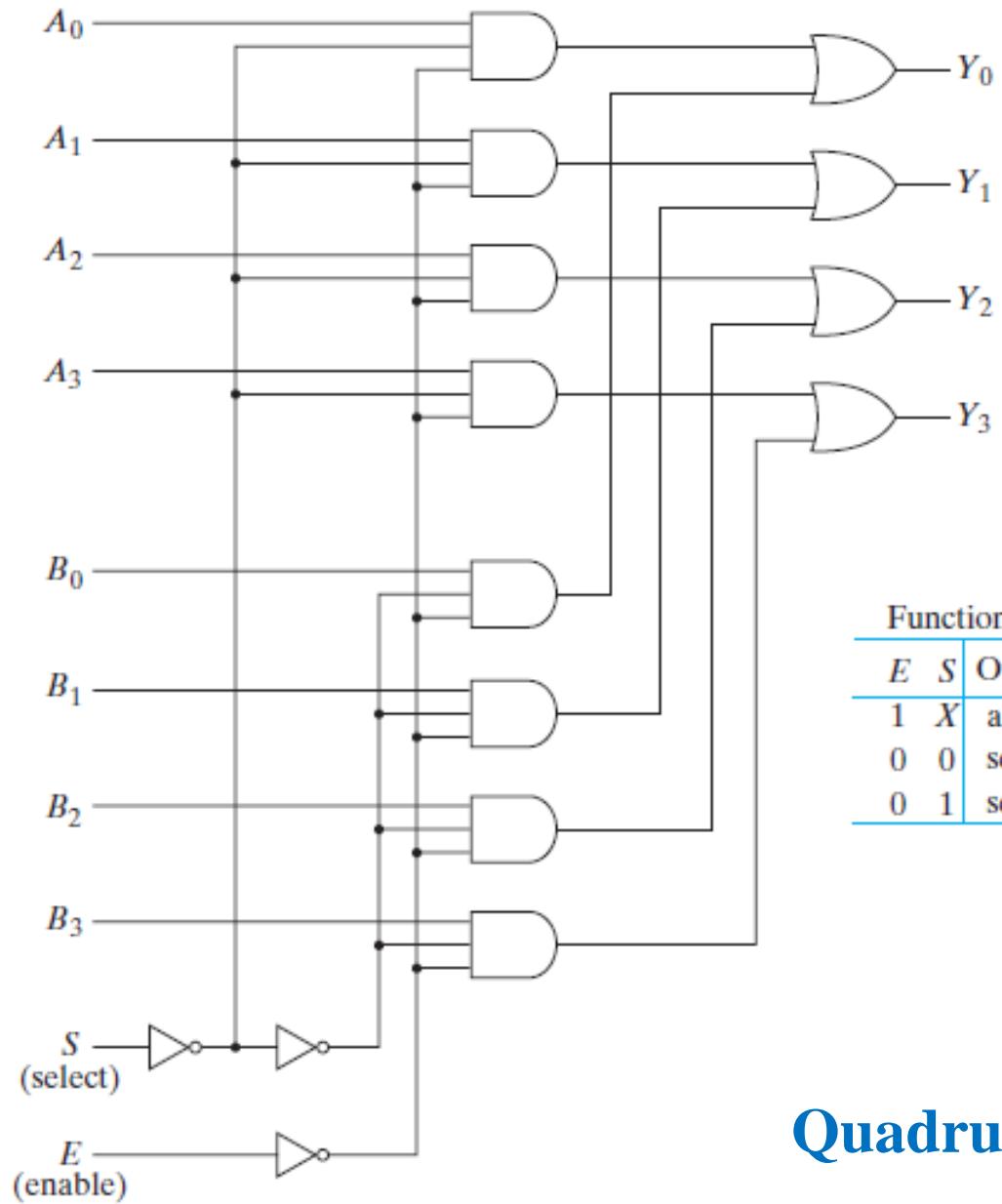
- Else

$$\text{Output} = B$$



Output





Function table

$E$	$S$	Output $Y$
1	X	all 0's
0	0	select $A$
0	1	select $B$

**Quadruple 2:1 MUX or Nibble MUX**