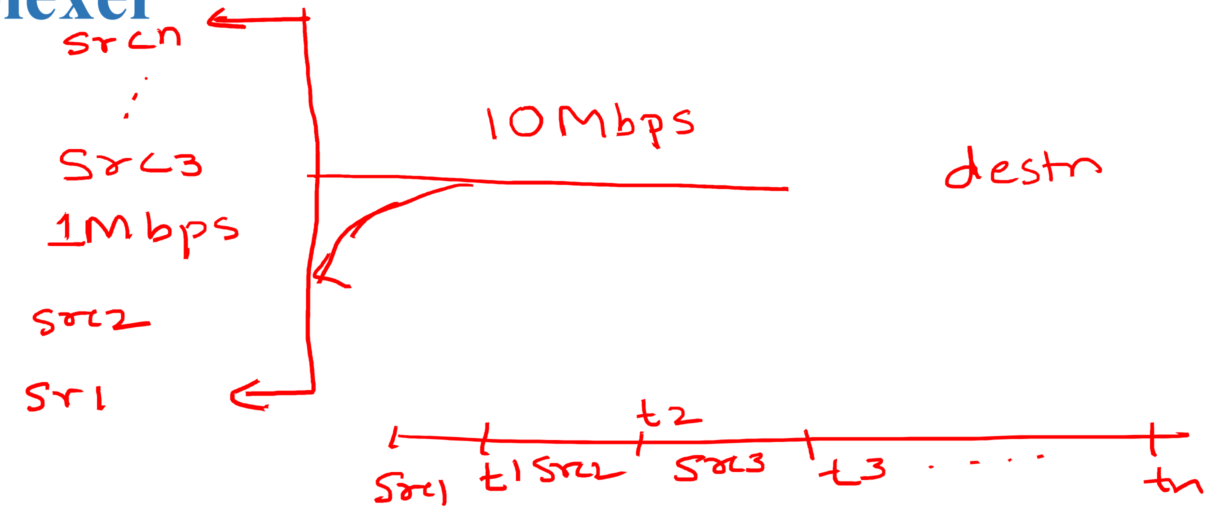
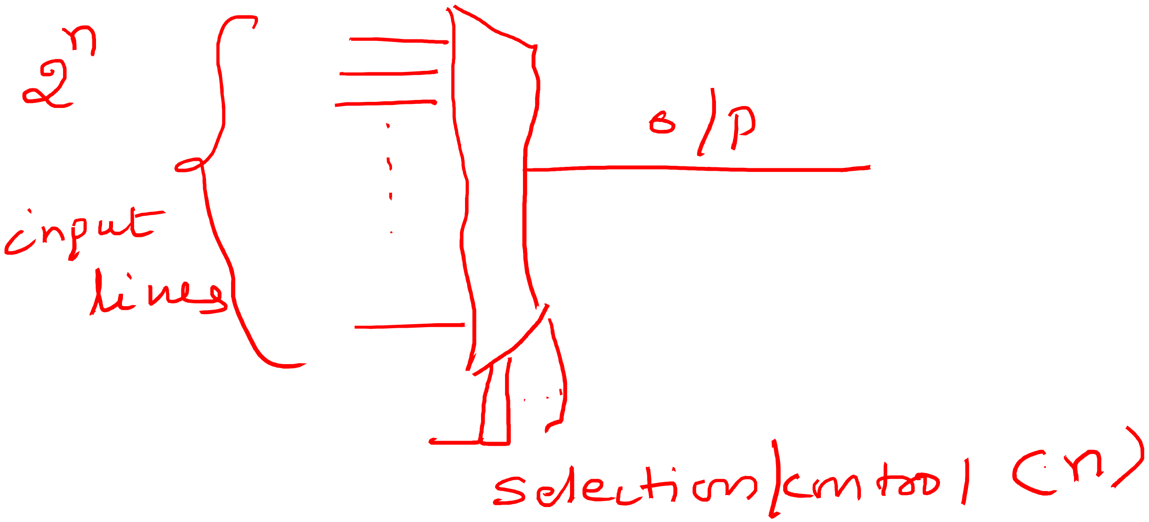
Multiplexers

Students are advised to write down the notes for every lecture

Multiplexer





Multiplexer

- Multiplexer is an useful MSI device and are also called as data selectors.
- Multiplexer selects one of its 2^n input line and directs it to a single output line .
- n-bit select lines decide which input line is to be selected.
- Examples: 2-to-1 line MUX, 4-to-1 line MUX, 8-to-1 line MUX, 16-to-line MUX.

$2^n : 1$, n => select lines

2 : 1

4 : 1

8 : 1

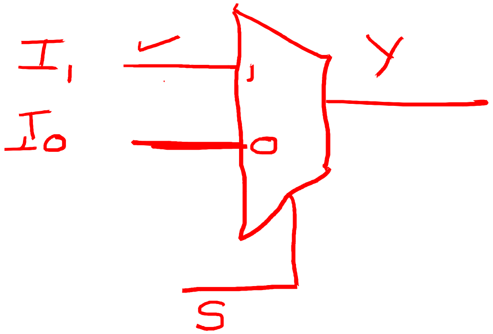
16 : 1

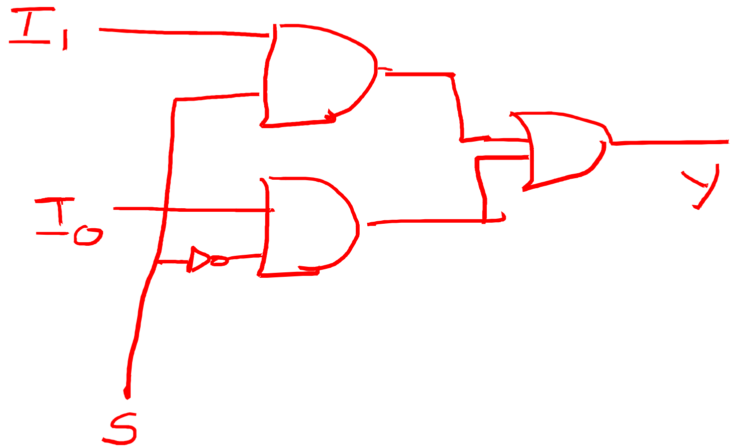
2-to-1 line MUX

- S- selection input, y is the output, I1 and I0 are inputs
- Symbol/block diagram, function table, output expressions and circuit is given :

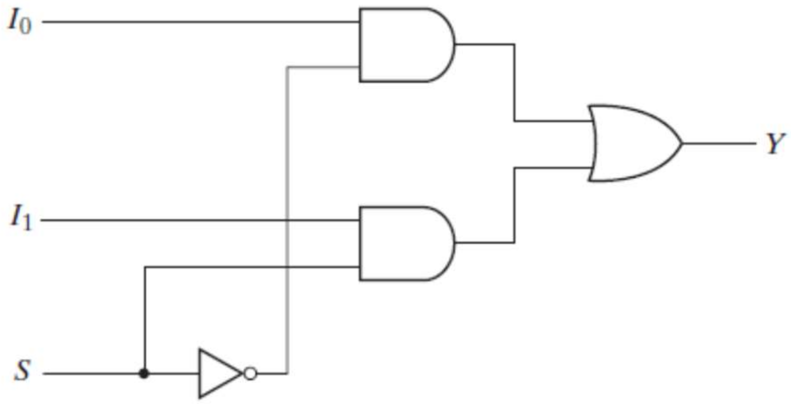
S	Y
0	I_0
1	I_1

$$\Rightarrow Y = \bar{S} I_0 + S I_1$$

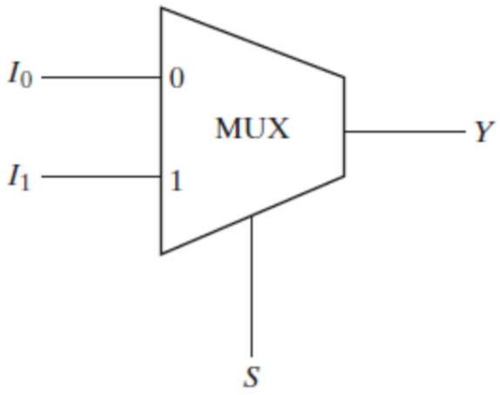




2-to-1 line MUX



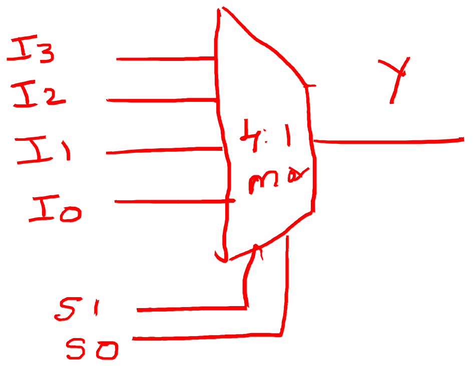
(a) Logic diagram



(b) Block diagram

4-to-1 line multiplexer

- Write the Symbol/block diagram, Function table, output expressions and circuit .



S1	S0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

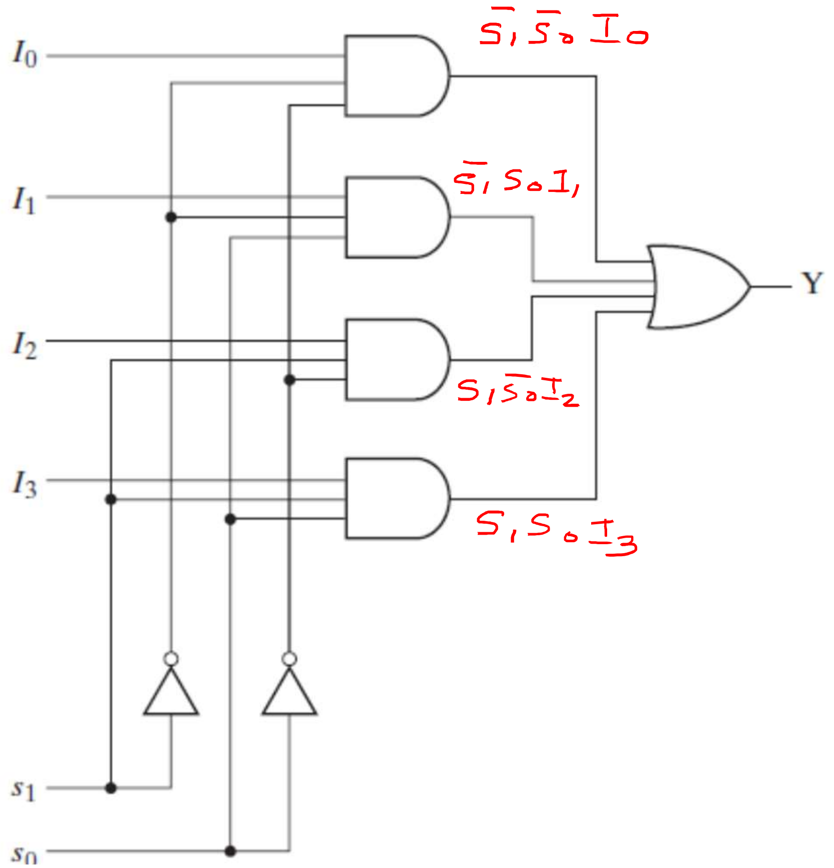
Assume

$I_3 = 1$ $\quad I_2 = 1$ $\quad I_1 = 0$ $\quad I_0 = 0$

$S_1 S_0 = 10$, $\quad Y = ?\ 1$

$$Y = \bar{S_1}\bar{S_0}.I_0 + \bar{S_1}S_0 I_1 + S_1\bar{S_0}.I_2 + S_1 S_0 I_3$$

4-to-1 line multiplexer



8-to-1 line multiplexer

- Write the Symbol/block diagram, function table, output expressions and circuit

Select lines: $S_2 S_1 S_0$

$$Y = \bar{S}_2 \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_2 \bar{S}_1 S_0 I_1 + \bar{S}_2 S_1 \bar{S}_0 I_2 + \bar{S}_2 S_1 S_0 I_3 +$$
$$S_2 \bar{S}_1 \bar{S}_0 I_4 + S_2 \bar{S}_1 S_0 I_5 + S_2 S_1 \bar{S}_0 I_6 + S_2 S_1 S_0 I_7$$

→ Draw 8 : 1 mux circuit

Realize 4:1 using only 2:1 MUXs (Multiplexer tree)

For 4:1 mux

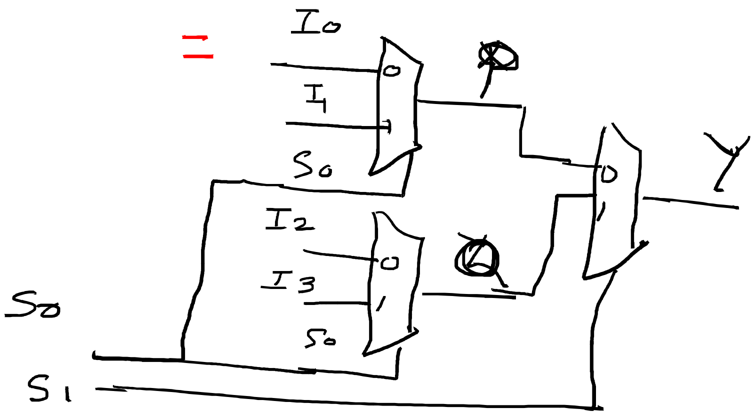
$$Y = \bar{S}_1\bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1\bar{S}_0 I_2 + S_1 S_0 I_3$$

For 2:1 mux

$$Y = \bar{S}_0 I_0 + S_0 I_1$$

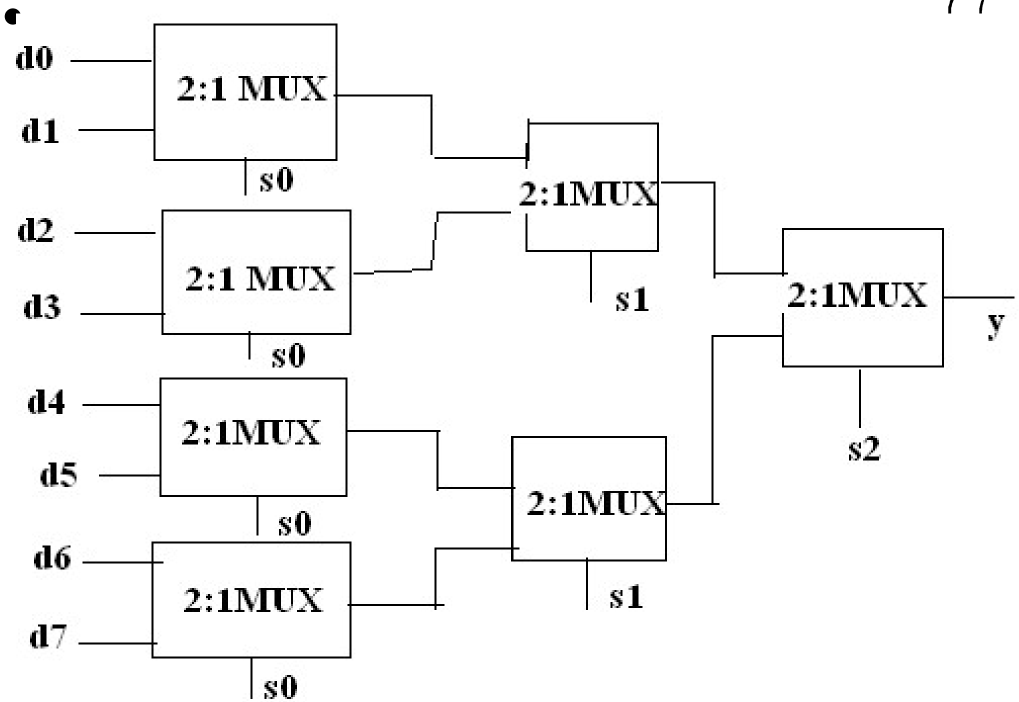
$$Y = \bar{S}_1 \underbrace{\overbrace{(\bar{S}_0 I_0 + S_0 I_1)}^{P}}_{2:1\,\text{mux}} + S_1 \underbrace{\overbrace{(\bar{S}_0 I_2 + S_0 I_3)}^{Q}}_{2:1\,\text{mux}} = \underbrace{\bar{S}_1 \cdot P + S_1 \cdot Q}_{2:1\,\text{mux}}$$

=



3, 2:1 muxs

Realize 8:1 using only 2:1 MUXs (Multiplexer tree)



((4+2+1), 2:1 MUXs)

$2^n:1$ mux using 2:1 mux

how many 2:1 mux?

$2^n - 1$ ← Ans?

Realize 8:1 using only 4:1 MUXs and 2:1 MUX

- Select lines: $S_2 S_1 S_0$

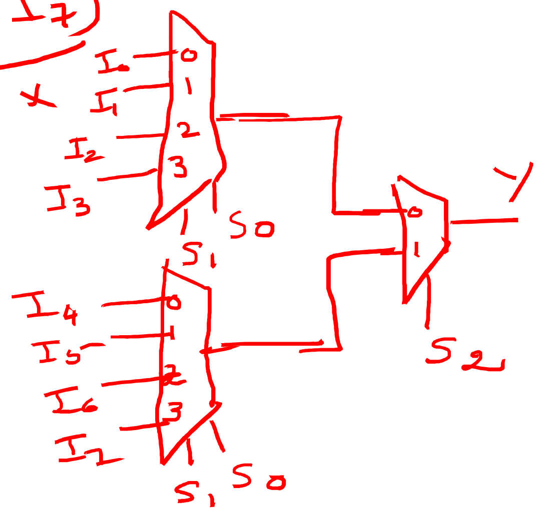
$$Y = \bar{S}_2 \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_2 \bar{S}_1 S_0 I_1 + \bar{S}_2 S_1 \bar{S}_0 I_2 + \bar{S}_2 S_1 S_0 I_3 +$$
$$S_2 \bar{S}_1 \bar{S}_0 I_4 + S_2 \bar{S}_1 S_0 I_5 + S_2 S_1 \bar{S}_0 I_6 + S_2 S_1 S_0 I_7$$

~~→ Draw 8:1 MUX circuit~~

4:1 MUX A

$$= \bar{S}_2 \left(\bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3 \right) +$$
$$S_2 \left(\bar{S}_1 \bar{S}_0 I_4 + \bar{S}_1 S_0 I_5 + S_1 \bar{S}_0 I_6 + S_1 S_0 I_7 \right)$$

B 4:1 MUX

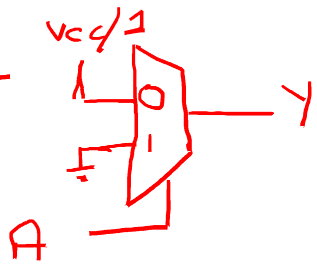


$$= \underbrace{\bar{S}_2 A + S_2 B}_{2:1\ \text{MUX}}$$

Realize each of the basic logic gates using 2:1 MUX

NOT ⇒ $Y = \overline{A}$

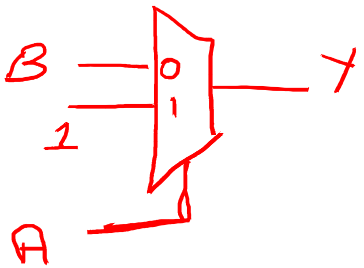
A	Y
0	1
1	0



OR gate $Y = A + B$

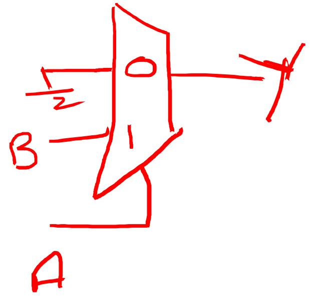
if $A = 0$ $Y = B$

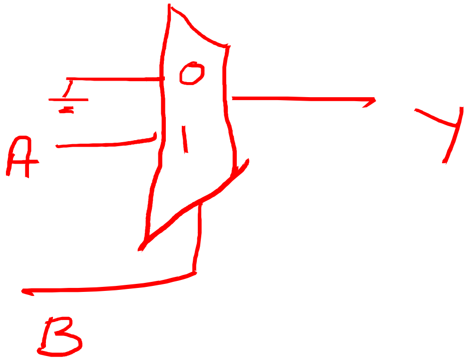
	A	B	Y	
$A=0$	0	0	0	$Y=B$
	0	1	1	
$A=1$	1	0	1	$Y=1$
	1	1	1	



AND $Y = AB$

A	B	Y	
0	0	0	$Y=0$
0	1	0	
1	0	0	$Y=B$
1	1	1	

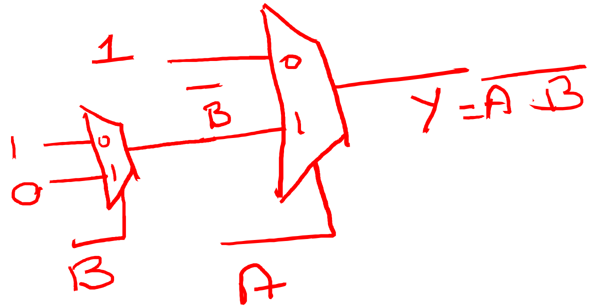




NAND gate using 2:1 MUXs

$$Y = \overline{A \cdot B}$$

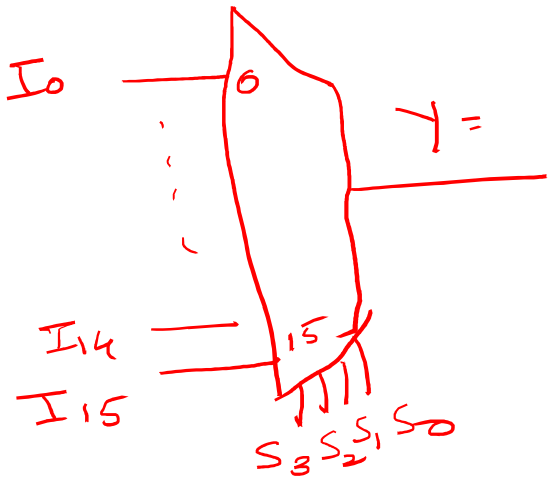
A	B	Y	
0	0	1	$\left.\right\} Y = 1$
0	1	1	
1	0	1	$\left.\right\} Y = \overline{B}$
1	1	0	



Realize NOR, XOR

16-to-1 line multiplexer----Exercise for you

- Write the Symbol/block diagram, function table, output expressions and circuit



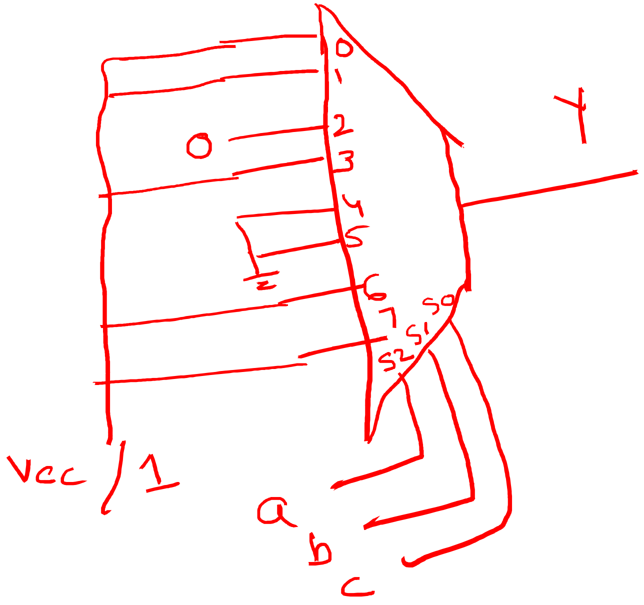
Multiplexer application in logic design

- Implement the function F(a,b,c) = Σm(0,1,3,6,7) using

equal to the no. of select lines

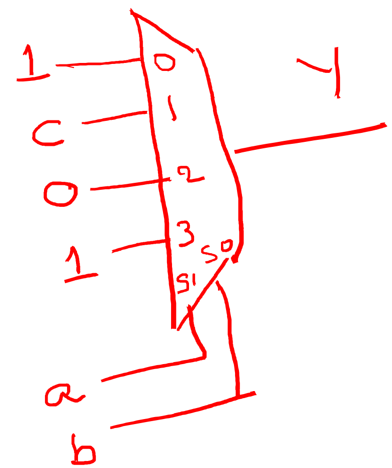
  - 8:1 MUX only
  - Minimum no. of 4:1 MUXs only

	a b c	F	
ab=00	0 0 0	1	F=1
	0 0 1	1	
ab=01	0 1 0	0	F=c
	0 1 1	1	
ab=10	1 0 0	0	F=0
	1 0 1	0	
ab=11	1 1 0	1	F=1
	1 1 1	1	



8:1 mux

4:1 MUX



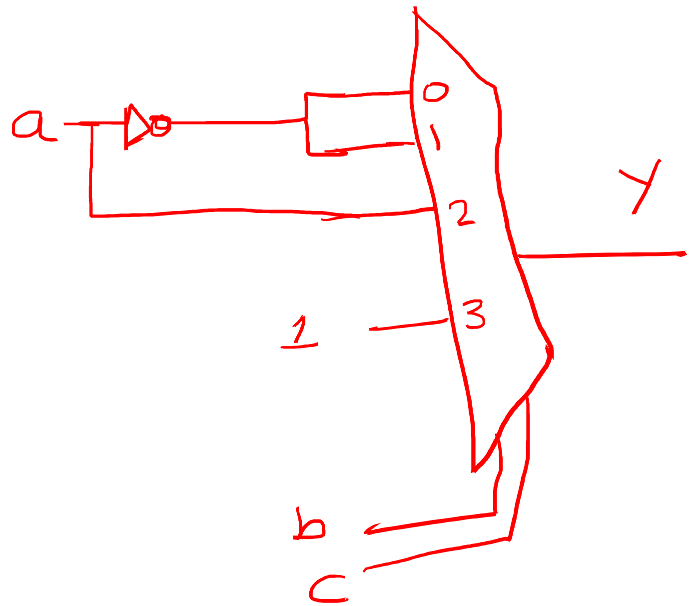
Implement the function $F(a,b,c) = \Sigma m(0,1,3,6,7)$ using bc as selection lines for 4:1 mux

	$\bar{b}\bar{c}$	$\bar{b}c$	$b\bar{c}$	bc
$\bar{a}$ 0	0: 1	1: 1	2: 0	3: 1
a=1	4: 0	5: 0	6: 1	7: 1

bc = 00 01 10 11

$Y = \bar{a} \quad \bar{a} \quad a \quad 1$

TT is rewritten



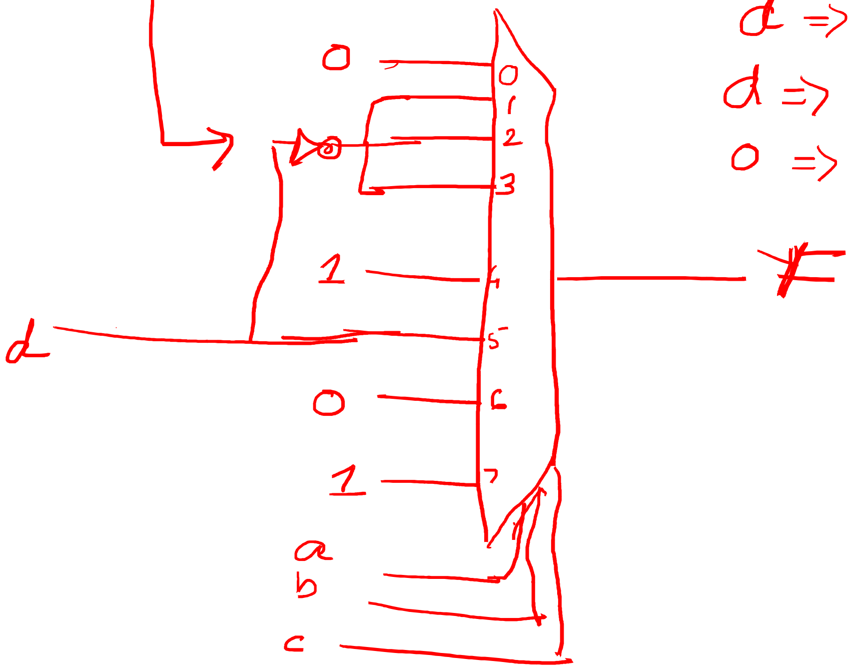
Implement the function F(a,b,c,d) = Σm(2,4,6,8, 9,11,14,15)

- using
  - . 8:1 MUX and one NOT gate ✓ a,b,c as the selection inputs
  - . 4:1 MUX and external gates
  - . 4:1 MUX and 2:1MUXs only

$\bar{d} \Rightarrow 1, 2, 3$ $\quad\quad$ $1 \Rightarrow 7, 4$

$d \Rightarrow 5$

$0 \Rightarrow 0, 6$



F(a,b,c,d) = Σm(2,4,6,8, 9,11,14,15)

a b c d	F
0 0 0 0	0
0 0 0 1	0
0 0 1 0	1
0 0 1 1	0
0 1 0 0	1
0 1 0 1	0
0 1 1 0	1
0 1 1 1	0
1 0 0 0	1
1 0 0 1	1
1 0 1 0	0

abc = 000

ab = 00: F = 0, F = $c\bar{d}$, F = $\bar{d}$

ab = 01: F = $\bar{d}$, F = $\bar{d}$

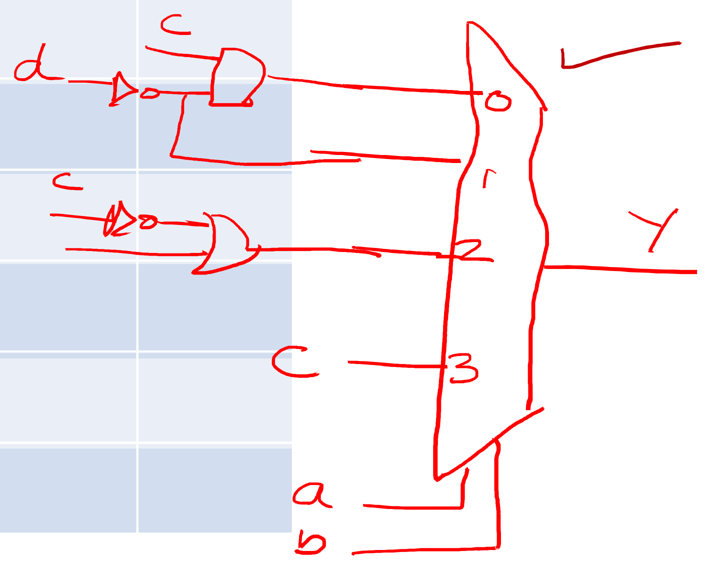
ab = 10: F = 1, $\bar{c} + d$

a b c d	F
1 0 1 1	1
1 1 0 0	0
1 1 0 1	0
1 1 1 0	1
1 1 1 1	1

F = d

ab = 11: F = 0, c, F = 1

8:1 mux



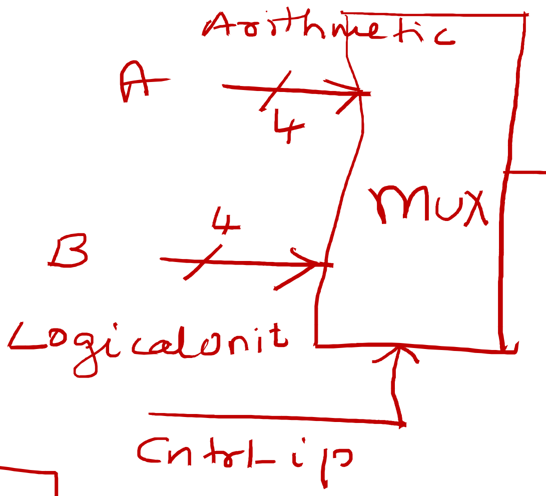
F(a,b,c,d) = $\Sigma m(2,4,6,8, 9,11,14,15)$ realization contd…

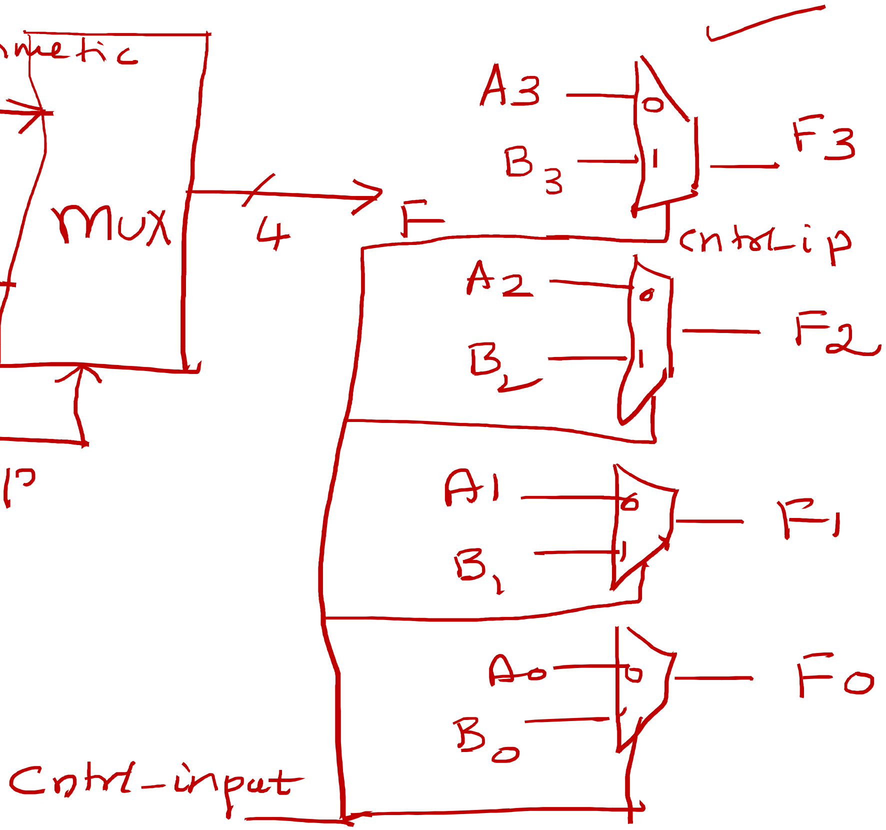
Nibble Multiplexer

- A and B are two 4-bit numbers. Design a combinational circuit using suitable multiplexers according to following requirements.
  - If cntrl_ip ===0

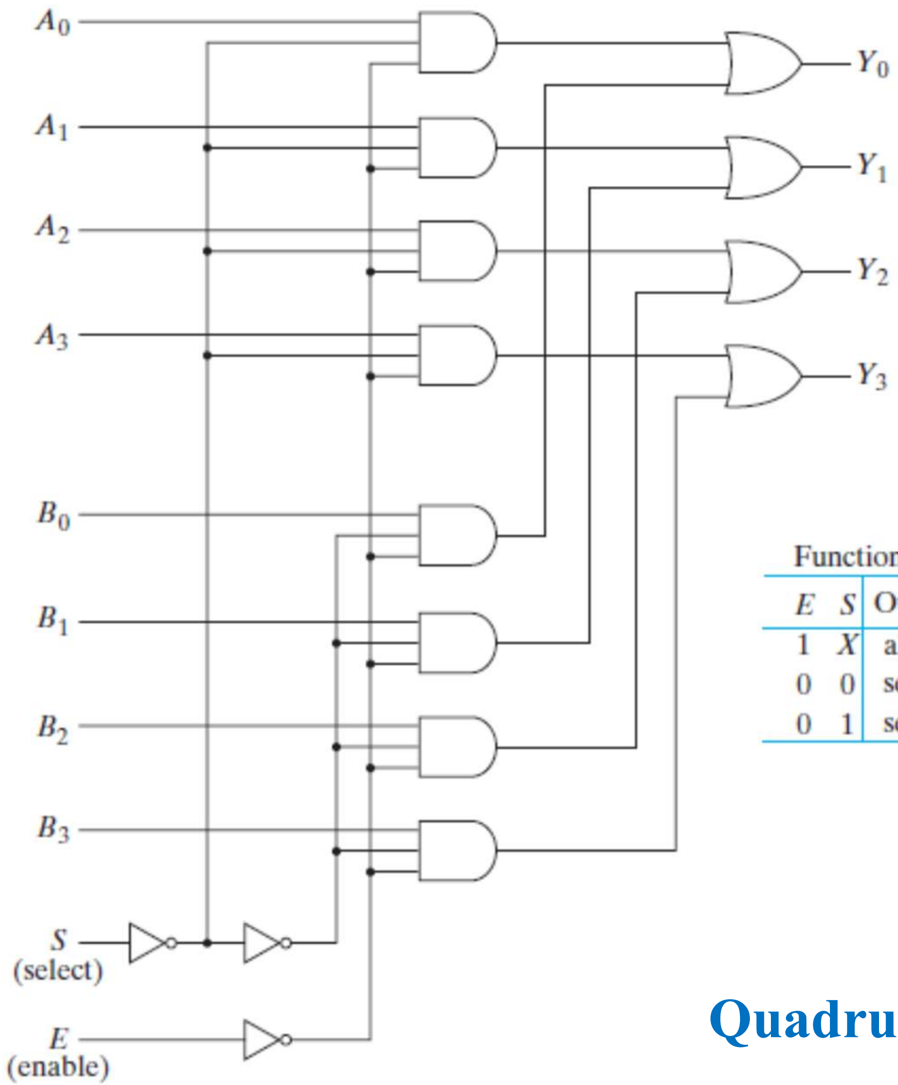
    Output=A
  - Else

    Output =B





A_3	A_2	A_1	A_0
B_3	B_2	B_1	B_0
F_3	F_2	F_1	F_0

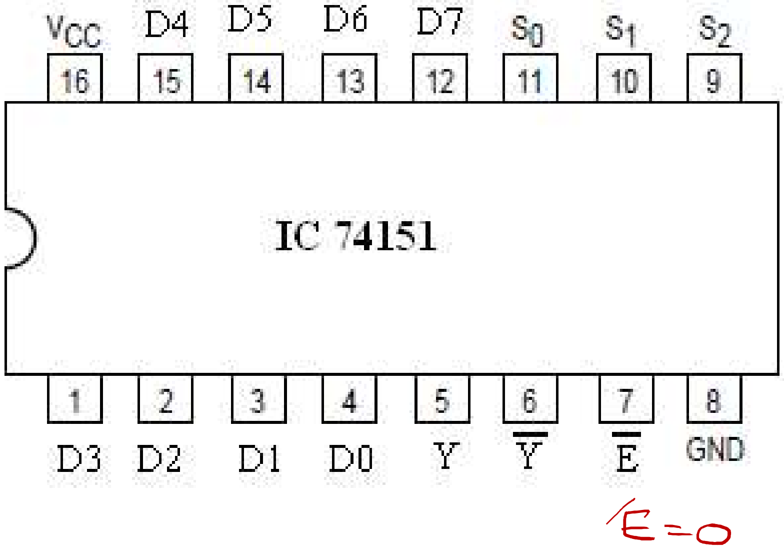


Function table		
E	S	Output Y
1	X	all 0's
0	0	select A
0	1	select B

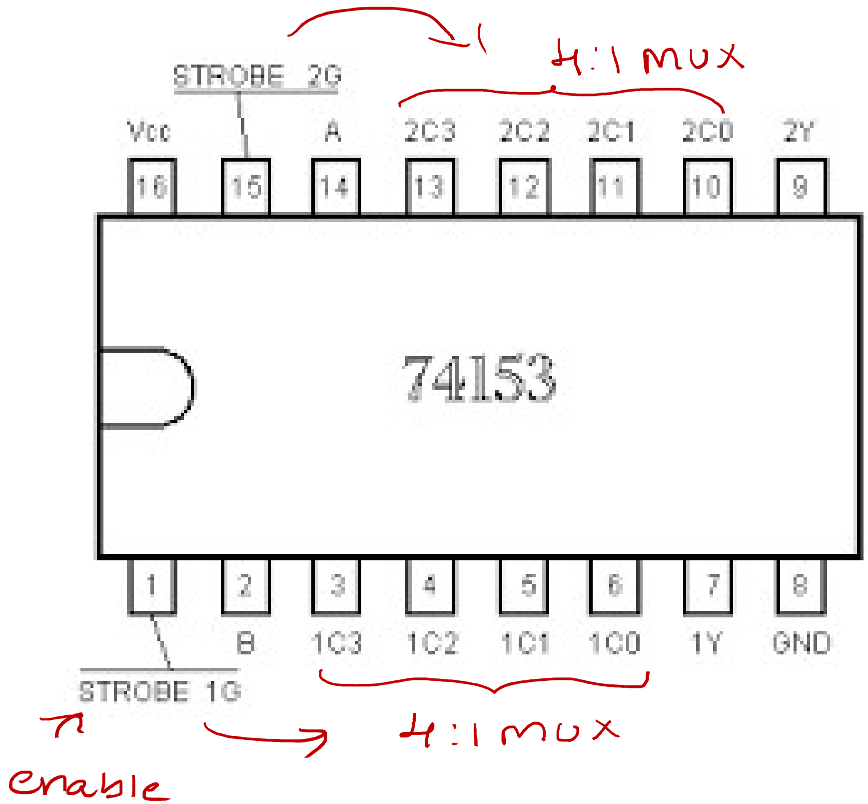
Quadruple 2:1 MUX or Nibble MUX

Multiplexer ICs :

74151- 8:1 MUX

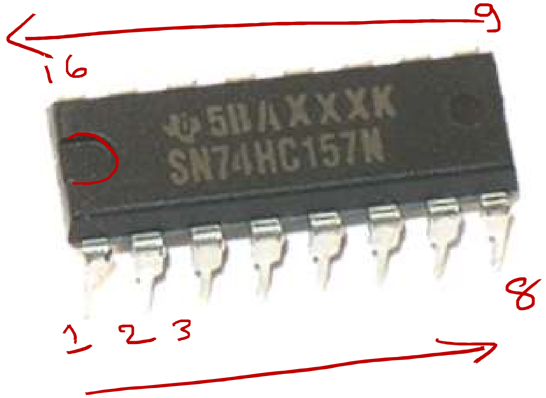


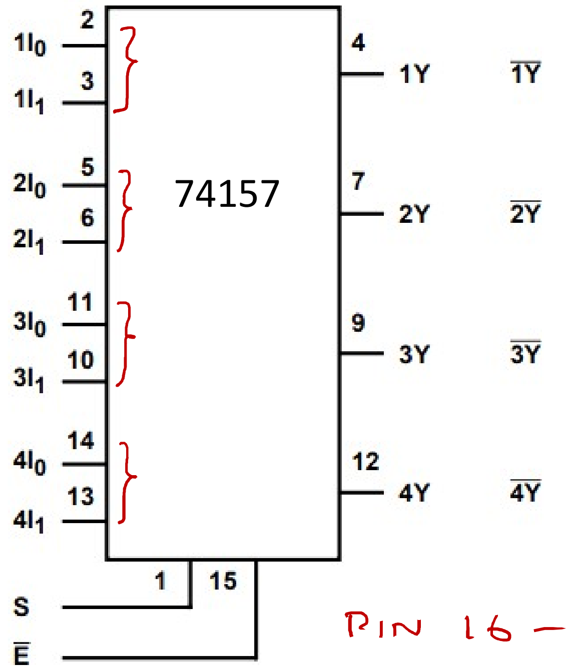
74153- 4:1 MUXs



74157 Quad 2:1 MUX IC

4,





PIN 16 – Vcc
8 – Gnd

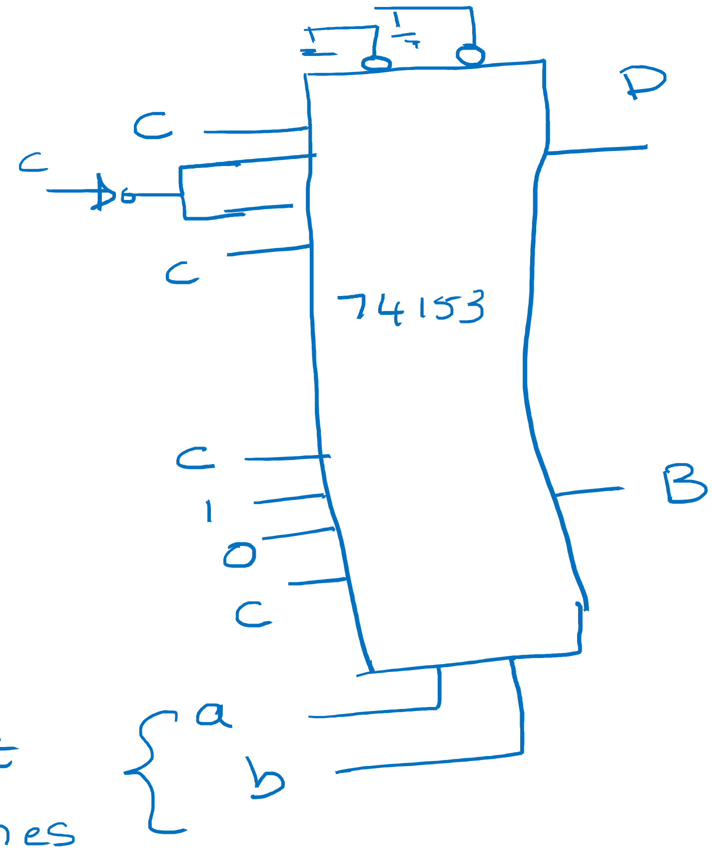
Design a full subtractor using 74153 IC and one external gate.

(a, b, c)

$D = \Sigma m(1, 2, 4, 7)$ $B = \Sigma m(1, 2, 3, 7)$

ab	00	01	10	11
c = 0	0	1	1	0
c = 1	1	0	0	1
D =	C	$\bar{C}$	$\bar{C}$	C

ab	00	01	10	11
c = 0	0	1	0	0
c = 1	1	1	0	1
B =	C	1	0	C



Full subtractor using 74153 IC and one external gate contd…

Design a full adder/ subtractor using 74153 IC and two external gates

if $m = 0$ adder $F = a + b + C_{in} = 0$

else substractor $F = a - b$

$= \cancel{0}$

$FA \Rightarrow S = \Sigma m(1, 2, 4, 7)$ $C = \Sigma m(3, 5, 6, 7)$

$FS \Rightarrow D = \Sigma m(1, 2, 4, 7)$ $B = \Sigma m(1, 2, 3, 7)$

Full adder/subtractor using 74153 IC and two external gates contd…

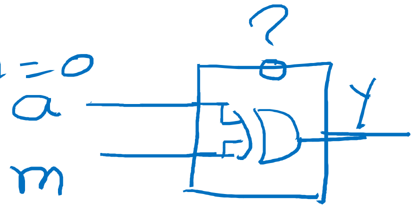
Choose bc as selection i/p

bc	00	01	10	11
a=0	0	1	1	0
a=1	1	0	0	1
Sum/Diff =	a	$\bar{a}$	$\bar{a}$	a

bc	00	01	10	11
a=0	0	0	0	1
a=1	0	1	1	1
Carry =	0	a	a	1

bc	00	01	10	11
a=0	0	1	1	1
a=1	0	0	0	1
borrow =	0	$\bar{a}$	$\bar{a}$	1

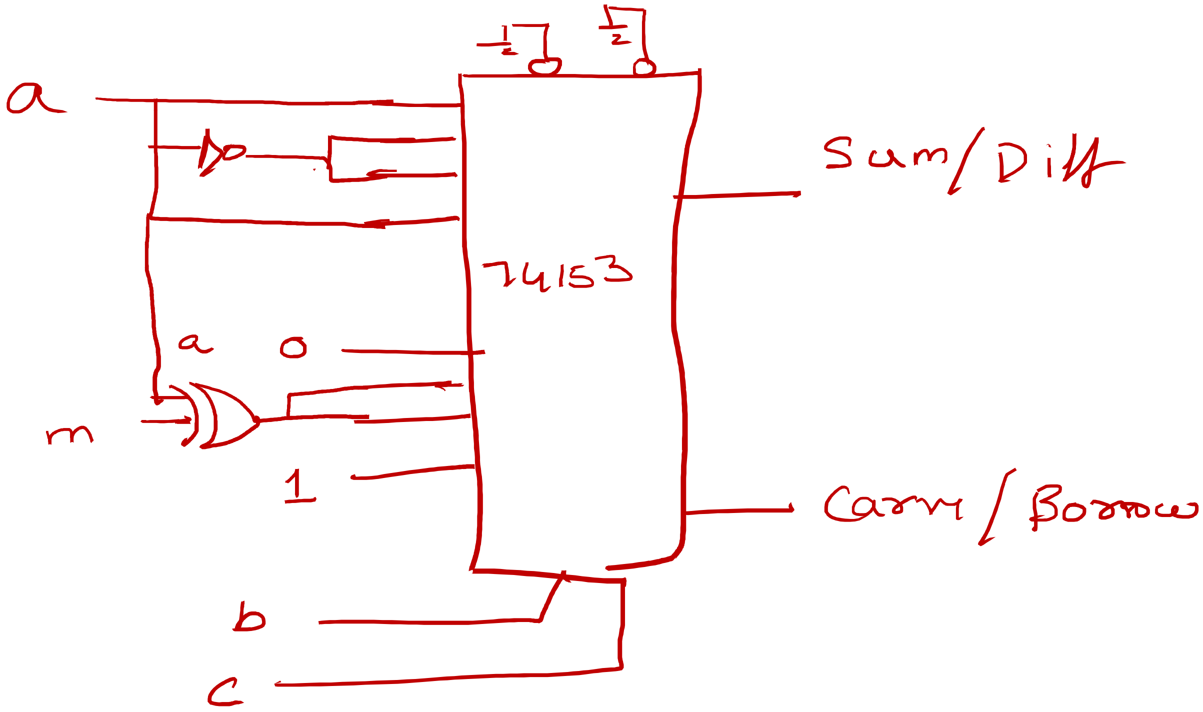
if $m=0$



m	a	Y
0	0	0
0	1	1

m	a	Y
1	0	1
1	1	0

Full adder/subtractor using 74153 IC and two external gates contd..



Exercise:

- Realize the Boolean expression $f(w,x,y,z) = \Sigma m(4,5,7,8,10,12,15)$ using
  - 74151 multiplexer and external gate
  - 74153 IC and external gates

  - Refer the prescribed book for additional problems

Question?