# LECTURE 5

KARNAUGH MAP (K – MAP)

EXAMPLE 5:

DESIGN A COMBINATIONAL CIRCUIT WITH 4- INPUT LINES THAT REPRESENTS A DECIMAL DIGIT IN BCD AND 4- OUTPUT LINES THAT GENERATES 2'S COMPLEMENT OF INPUT DIGIT.

| Decimal digit | 8 4 2 1<br>A B C D | 2's Complement<br>$Y_3 Y_2 Y_1 Y_0$ |
|---|---|---|
| 0 | 0000 | 0000 |
| 1 | 0001 | 1111 |
| 2 | 0010 | 1110 |
| 3 | 0011 | 1101 |
| 4 | 0100 | 1100 |
| 5 | 0101 | 1011 |
| 6 | 0110 | 1010 |
| 7 | 0111 | 1001 |
| 8 | 1000 | ~~0001~~ 1000 |
| 9 | 1001 | 0111 |

0100 ⇒ 1's comp = 1011 +

(4)                                   1

1100 ← 2's compl. of (0100)

(−4)

Sign bit = 0 = +ve

1 = −ve

0100

LSB

2's compl. 1100

4-bit i/p = $2^4$ = 16 input combinations

0000 — 1001

= 10 combinations

1000 → 4-bits = signed no.

5-bits

0 →

$(-8)_{10}$ ← 0 → $(0111)_2$

$(+7)_{10}$

$2^5 - 1$

5-bits

Unsigned ⇒ 00000 – 11111 ⇒ (0) to (31)

Signed ⇒ ~~000~~ 10000 ⟵ 00000 ⟶ 01111

(−16) $(+15)_{10}$

unsigned short int A; 1 byte = 8bits ⇒ $2^8 = 256$

0 ⟶ 255

1

2

A = −3;

A = 257; ⟶

?

To find 2's complement contd:

$$Y_3 = \begin{cases} \Pi M(0,\ 9) \cdot d(\ '' \ ) \\ \Sigma m(\cancel{8}\,1,2,3,4,5,6,7,\cancel{8}) + d(10,11,12,13,14,15) \end{cases}$$

---

$$Y_2 = \begin{cases} \Pi M(0,5,6,4,7,8) \cdot d(\cancel{D, X, \Phi})\ '' \ ) \\ \Sigma m(1,2,3,\cancel{8},\cancel{6},9) + d(10,11,12,13,14,15) \end{cases}$$

$$Y_1 = \{ \Sigma m(1,2,5,6,9) + d(10,11,12,13,14,15)$$

$$Y_0 = \{ \Sigma m(1,3,5,7,9) + d(\ '' \ )$$

$Y_3$

| AB \ CD | 00 | 01 ($\bar{A}D$) | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 1 | 1 | 1 |
| 01 | 1 | 1 | 1 | 1 |
| 11 | d | d | d | d |
| 10 ($A\bar{D}$) | 1 | 0 | d | d |

$$Y_3 = B + C + \bar{A}D + A\bar{D}$$

$$Y_2 = \cancel{2} + \bar{B}D + \bar{B}C = B\bar{C}\bar{D} + \bar{B}D + \bar{B}C$$

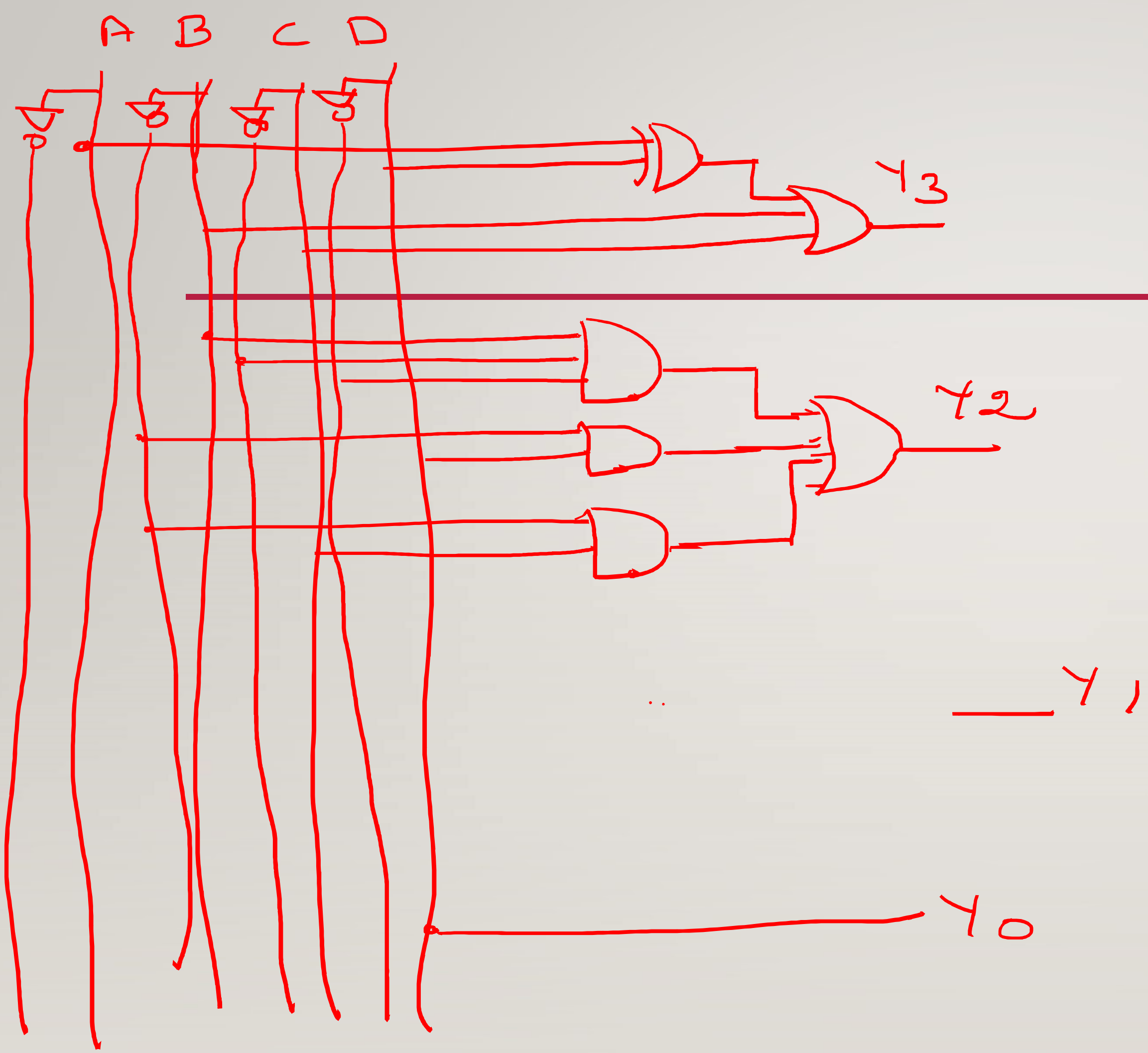
$\cancel{B\bar{C}\bar{D}}$

$$Y_1 = ? \quad \bar{C}D + C\bar{D} = C \oplus D$$

$Y_0 = D^{\circ}$, from truth table

$$Y_3 = B + C + \underbrace{\bar{A}D + A\bar{D}}_{A \oplus D}$$

$$Y_2 = B\bar{C}\bar{D} + \bar{B}D + \bar{B}C$$



# EXAMPLE 6:

Design a combinational circuit to check for even parity of 4 bits. A logic '1' output is required when the 4 bits constitute an even parity.

# EXAMPLE 7:

Design a combinational circuit that multiplies by '5' an input decimal digit represented in BCD. The output is also in BCD.

Input : $(0)_{10}$ to $(9)_{10}$ (0000) to (1001) in BCD
output : $(0)_{10}$ to $(45)_{10}$ (000000) to (0100 0101) in BCD