Title: CMOS Inverter Design and Simulation Using Cadence Virtuoso

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CMOS INVERTER USING CADENCE VIRTUOSO

Introduction

This project demonstrates the design and simulation of a **CMOS inverter** using **Cadence Virtuoso** and the **GPDK 90nm technology library**. The CMOS inverter is the most basic logic gate and serves as a foundational building block in digital circuit design. The project involves schematic creation, symbol generation, testbench setup, and both DC and transient simulations.

CMOS Inverter:

A Complementary Metal-Oxide-Semiconductor (CMOS) inverter is a fundamental building block in digital electronics, particularly in CMOS technology, used to invert an input signal.

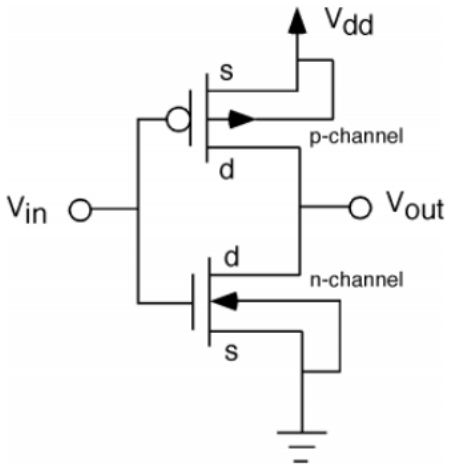


Fig. 1: schematic of a cmos inverter

A CMOS inverter consists of two main transistors: an n-channel MOSFET (NMOS) and a p-channel MOSFET (PMOS). These transistors are connected in a specific manner:

▪ NMOS Transistor:

✓ Source (S) is connected to the ground (0V).
✓ Drain (D) is connected to the output.
✓ Gate (G) is connected to the input.

▪ PMOS Transistor:

✓ Source (S) is connected to the supply voltage (VDD).
✓ Drain (D) is connected to the output (same node as the NMOS drain).
✓ Gate (G) is connected to the input (same node as the NMOS gate).

Working of a CMOS Inverter

A CMOS inverter consists of a **PMOS** transistor connected to the positive supply voltage (**VDD**) and an **NMOS** transistor connected to ground (**GND**). Both transistors share a common gate (input) and their drains are connected together to form the output. When the input is **low (0V)**, the PMOS is **ON** and the NMOS is **OFF**, pulling the output **high (VDD)**. Conversely, when the input is **high (VDD)**, the PMOS turns **OFF** and the NMOS turns **ON**, pulling the output **low (0V)**. This complementary switching action ensures low power consumption and full voltage swing, making CMOS inverters ideal for digital logic circuits.

Objectives

- To design a CMOS inverter schematic using gpdk090
- To generate a reusable symbol for the inverter
- To create a testbench for simulation
- To perform and analyze DC and transient simulations.

Tools and Technology Used

Tool	**Purpose**
Cadence Virtuoso	Schematic entry and simulation
Spectre Simulator	DC & Transient analysis
GPDK090	90nm technology PDK used for transistor models

CMOS Inverter Design

The CMOS inverter is designed with:

- **PMOS** transistor connected to **VDD**
- **NMOS** transistor connected to **VSS**
- A common input gate and common output drain

Steps to Design a CMOS Inverter in Cadence Virtuoso

1. Launch Cadence Virtuoso

Start the Cadence environment using virtuoso & in the terminal. Create ‘new Library’ name it ‘inverter123’ and select ‘Attach to existing technology library’.

2. Create Inverter Schematic

Go to File → New → CellView. Set:

- **Cell Name**: inv_1x
- **View Name**: schematic

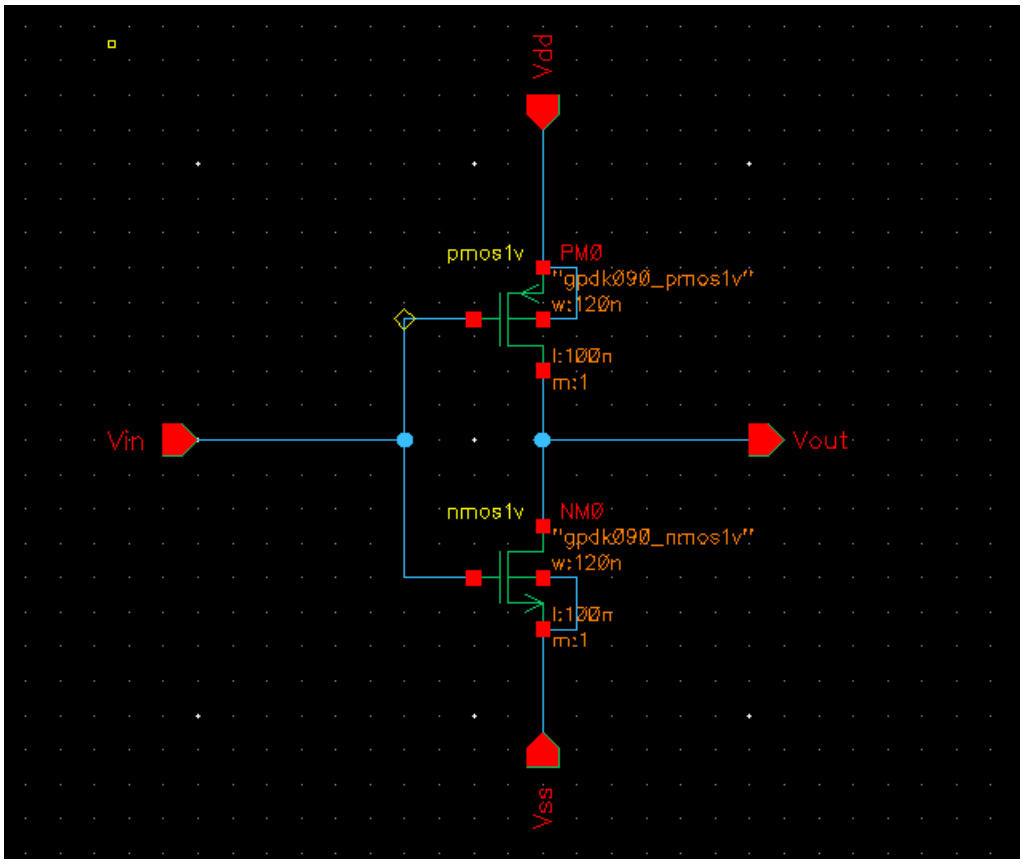
- Use pmos1v and nmos1v from gpdk090
  Connect gates as input, drains as output, PMOS source to VDD, NMOS source to VSS.

3. Add Pins and Save

Use Create → Pin to add:

- Vin,Vdd,Vss as inputs
- Vout as output
- Connect all elements using narrow wires

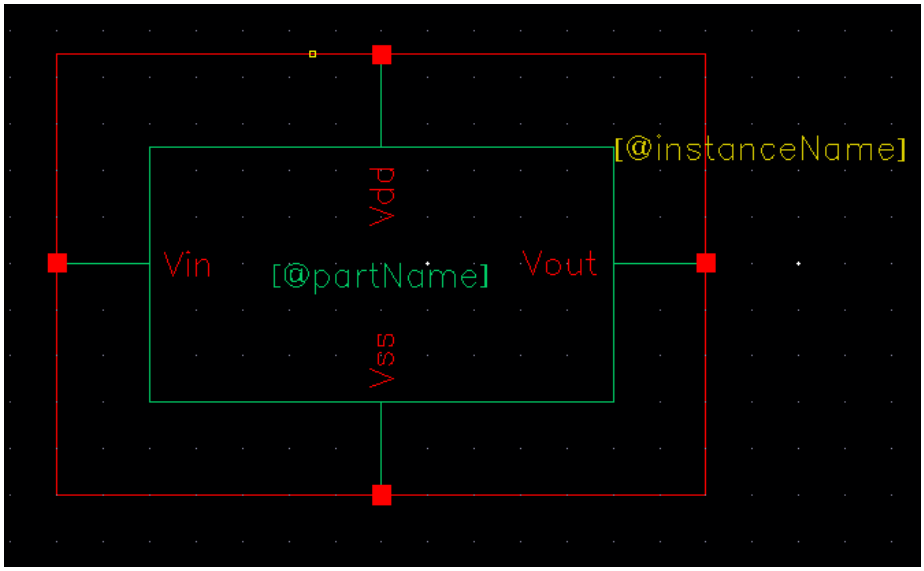
Then run Check and Save.



4. Generate Inverter Symbol

From schematic: Create → CellView → From CellView

This creates a symbol view. Adjust the pin placements and bounding box, then save it.



5. Create Testbench Schematic

Create a new cell (e.g., inv_tb).

Instantiate the inverter symbol. Add:

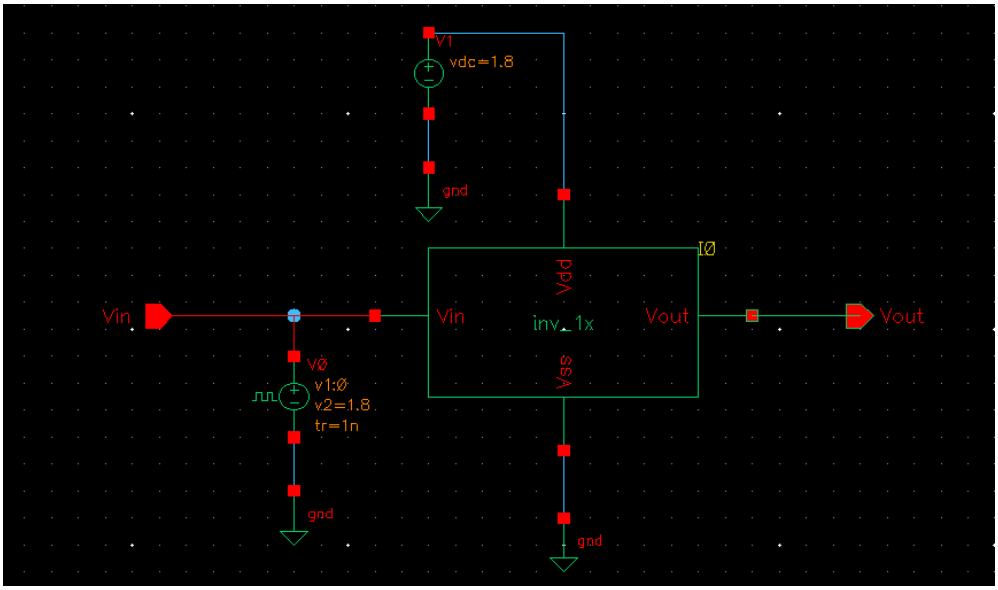
- vdc for VDD,
- vpulse for input,
- Output wire to probe vout.

6. Set Source Parameters

Set **VDD = 1.8V**.

Configure **vpulse**:

- V1 = 0V, V2 = 1.8V,
- Rise/Fall = 1ns, Pulse Width = 10ns, Period = 20ns.

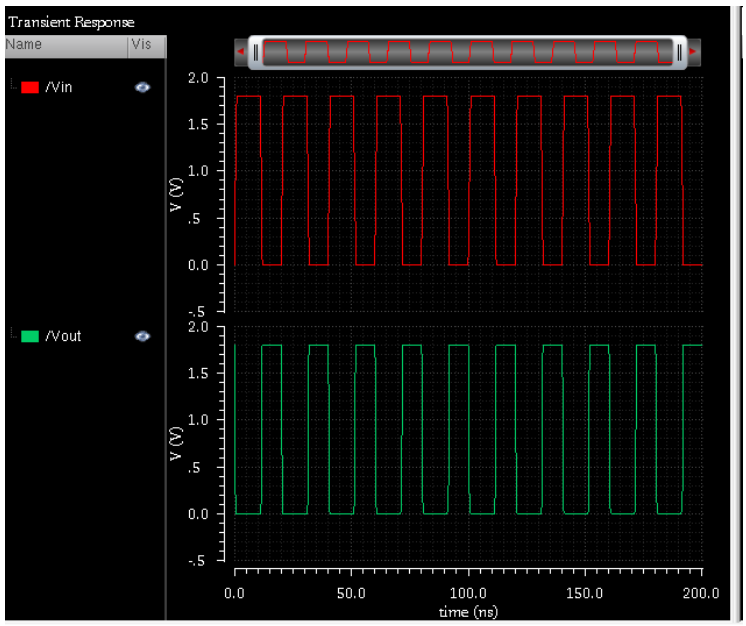


7. Launch ADE for Simulation
Go to Launch → ADE → L (Analog Design Environment).
Select **Spectre** as the simulator. Setup environment if required.

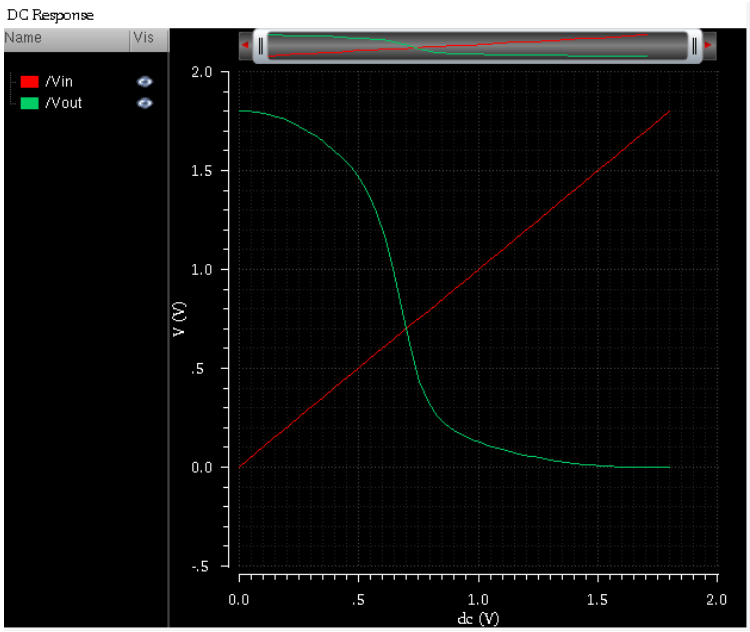
8. Configure Analyses
In ADE:

- For **DC Analysis**: Sweep vin from 0 to 1.8V.
- For **Transient Analysis**: Set Period 200ns to observe switching.

9. Select Output and Run Simulation
Go to Outputs → To Be Plotted → Select on Schematic. Click on vin and vout.
Then run the simulation using Simulation → Netlist & Run.



Transient analysis



DC Analysis

10. View and Export Results
Check the waveforms for logic behavior, switching, and noise margins.
Use File → Export Image in the waveform viewer to save graphs for reports or presentations.

Observations

Parameter	**Value / Note**
Technology Node	90nm (GPDK090)
Supply Voltage	1.8V
Output Swing	Rail-to-rail
Simulation Type	DC Sweep, Transient
Tool Flow	Schematic → Symbol → Testbench → Simulation

Conclusion

The CMOS inverter was successfully designed and simulated using the GPDK090 library in Cadence Virtuoso. Symbol generation and testbench creation enabled reuse and modular testing. DC and transient simulations confirmed correct inverter behavior, forming a solid foundation for future CMOS circuit design.

Future Work

- Design and simulate NAND/NOR gates using this inverter as a building block
- Extend to full-custom layout and perform DRC/LVS
- Analyze power consumption and propagation delay in detail

References

- Cadence Virtuoso Documentation
- GPDK090 PDK Guidelines
- CMOS VLSI Design – Weste & Harris