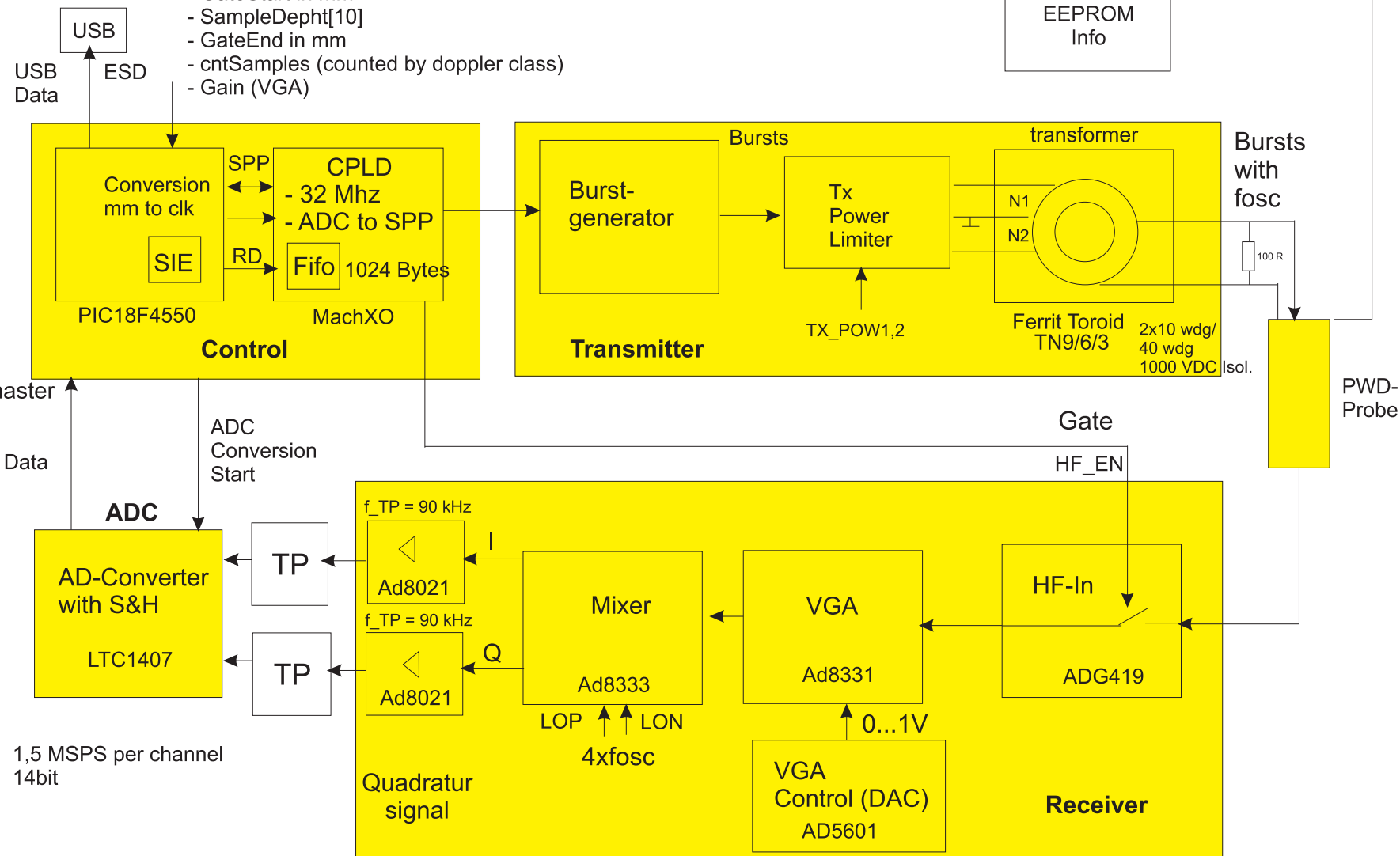


### Parameter:

- PRF
- BurstStart in mm
- BurstEnd (length in mm)
- GateStart in mm
- SampleDepth[10]
- GateEnd in mm
- cntSamples (counted by doppler class)
- Gain (VGA)

USB-SIE  
liest Daten  
direkt aus  
CPLD FIFO

Pic ist Lesemaster,  
CPLD ist Schreibmaster

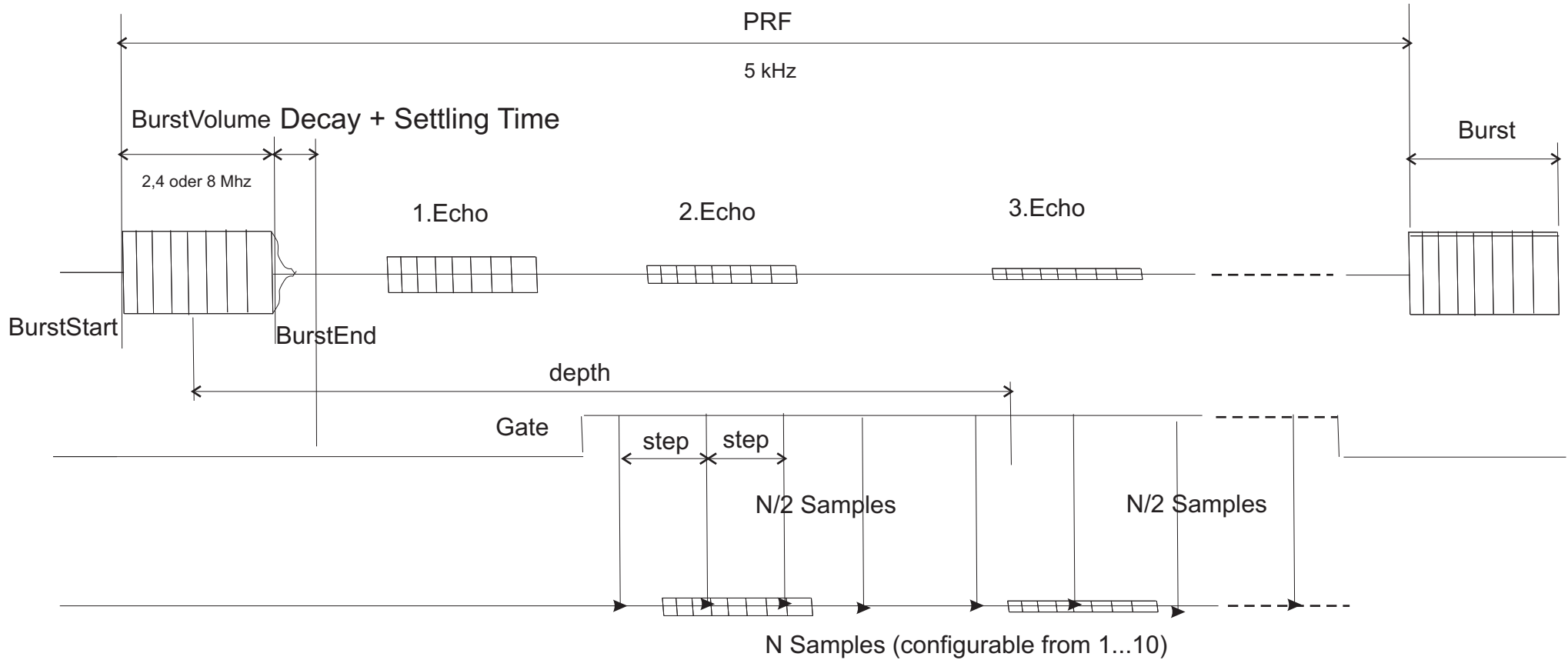


### Power Regulation

- + 5 V Analog
- + 3,3 V
- 5 V Generation
- + 5 V Burst-Voltage

Rev.	Änderung	Datum	Name	Bearb.	Datum	Name	Benennung
				Gepr.			PW-Doppler functional diagram
				Norm			(Hw Architecture)
				Project:		PWD_B	Blatt von
				File:		FL_06_PWD_Functiendiagram	

# PW-Doppler timing diagram



Burst Start = 0 mm (nur Null sinnvoll!)

Burst End = burstStart + Burst volume

Gate start = 8

Sample1 = 10 mm

Sample 2 = 12 mm...


Sample 9 =

Sample 10 = 50

Gate end

step: min. 1 mm ("Äquisamples")

Ultraschall: 1 mm:= 660 ns

					Datum	Name	Benennung			
				Bearb.	2.11.09	Huber	PW-Doppler timing diagram			
				Gepr.						
				Norm						
							Project:			
							PWD_B		Blatt von	
							File: FL_06_PWD_Functiondiagramm			
Rev.	Änderung	Datum	Name							