

Project **Ultrasonic Doppler 2015**

Title **Bandpass**

Size: **A4**

Number:*

Revision:*

Date: **15.10.2015**

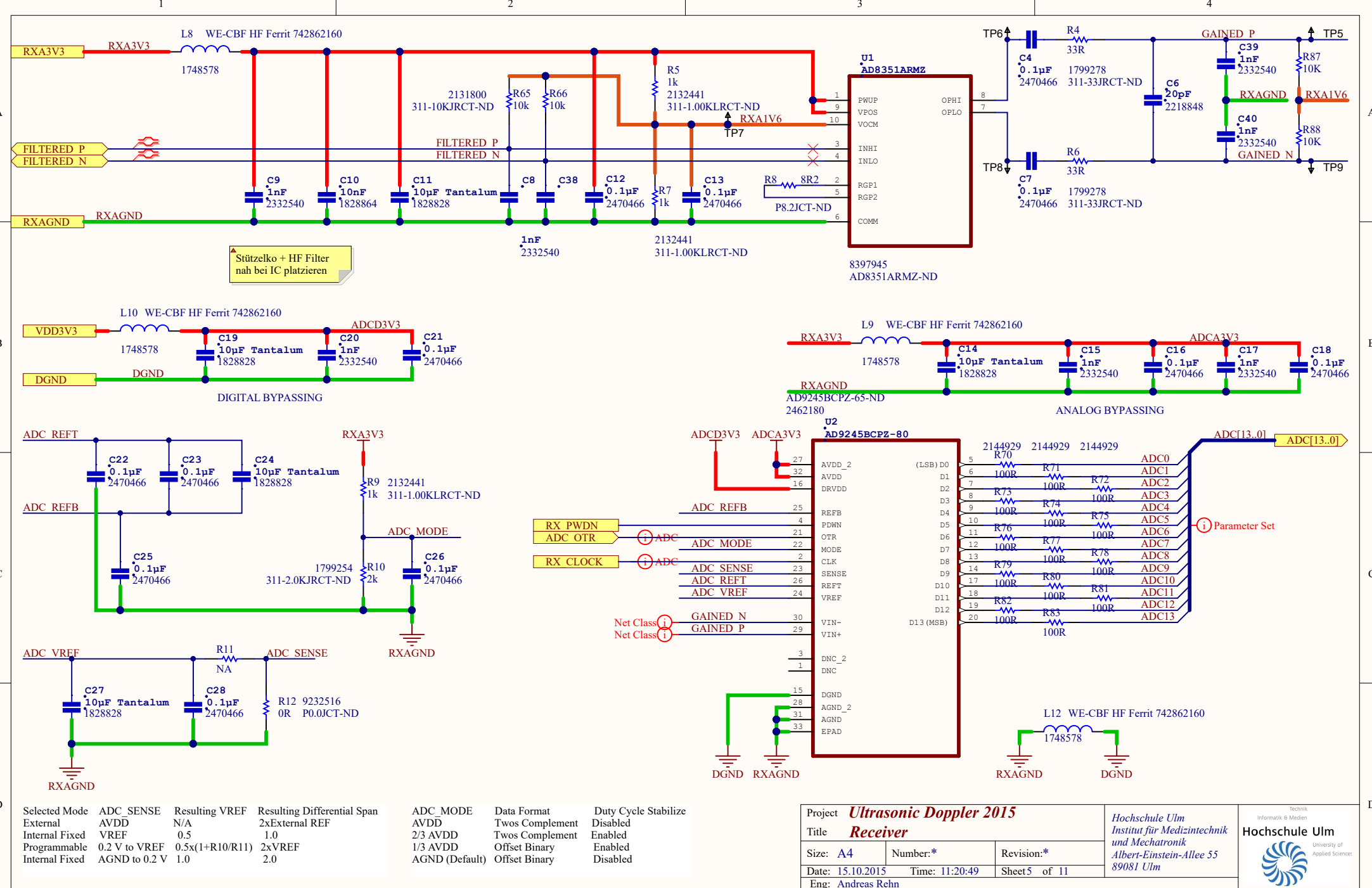
Time: 11:20:49

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Eng: **Andreas Rehn**

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und Mechatronik
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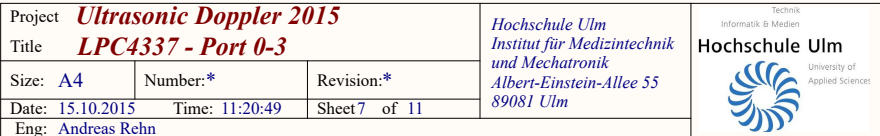


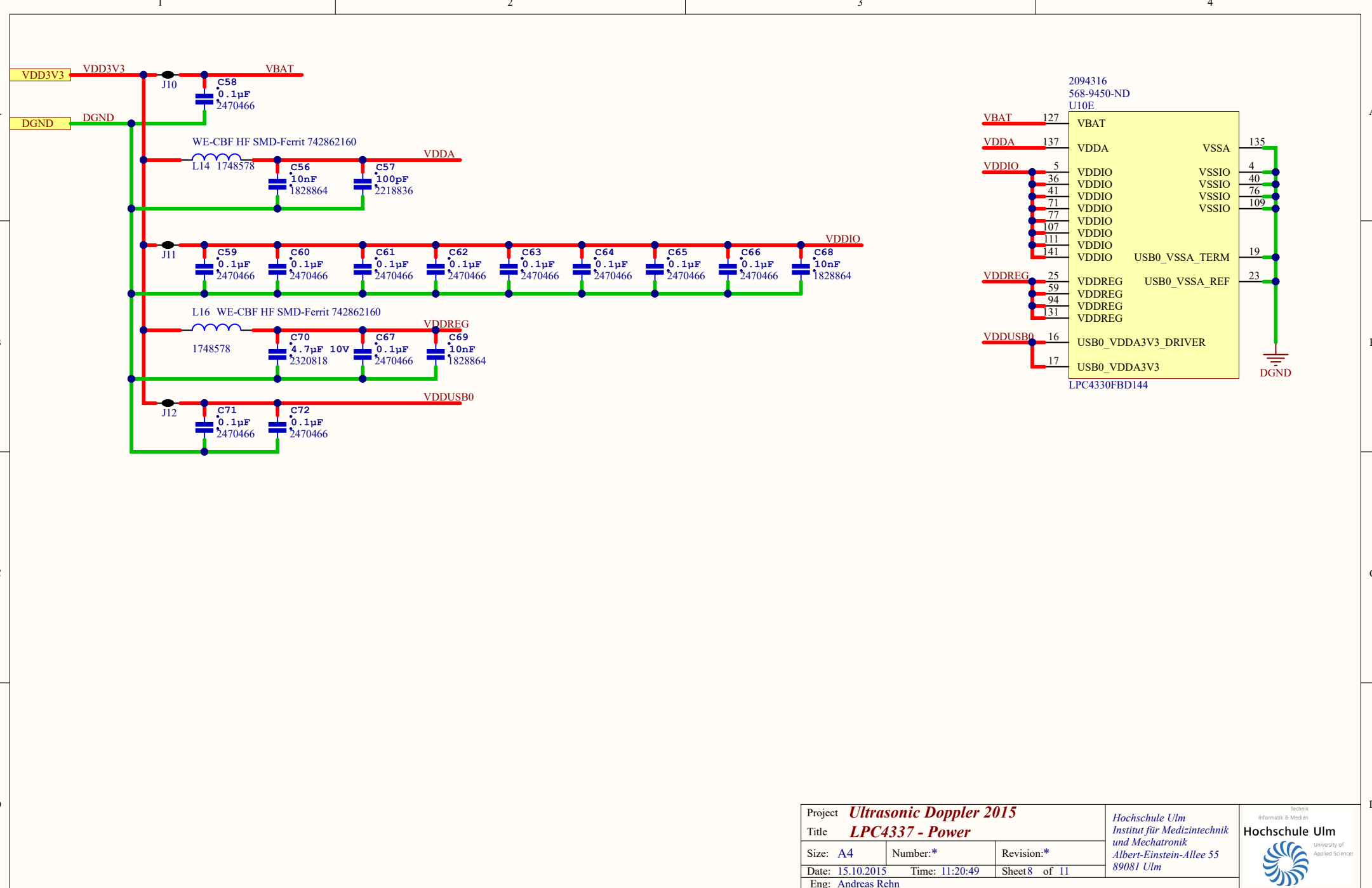


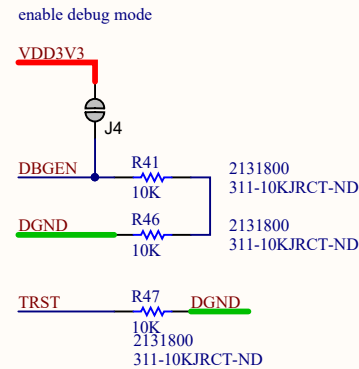
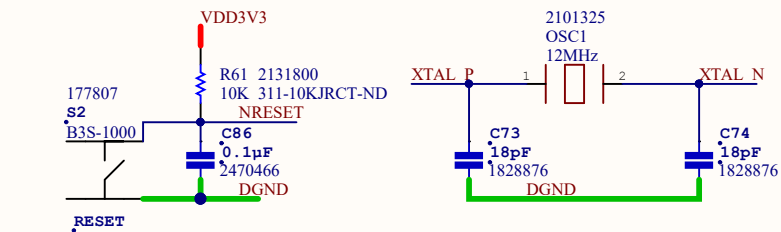
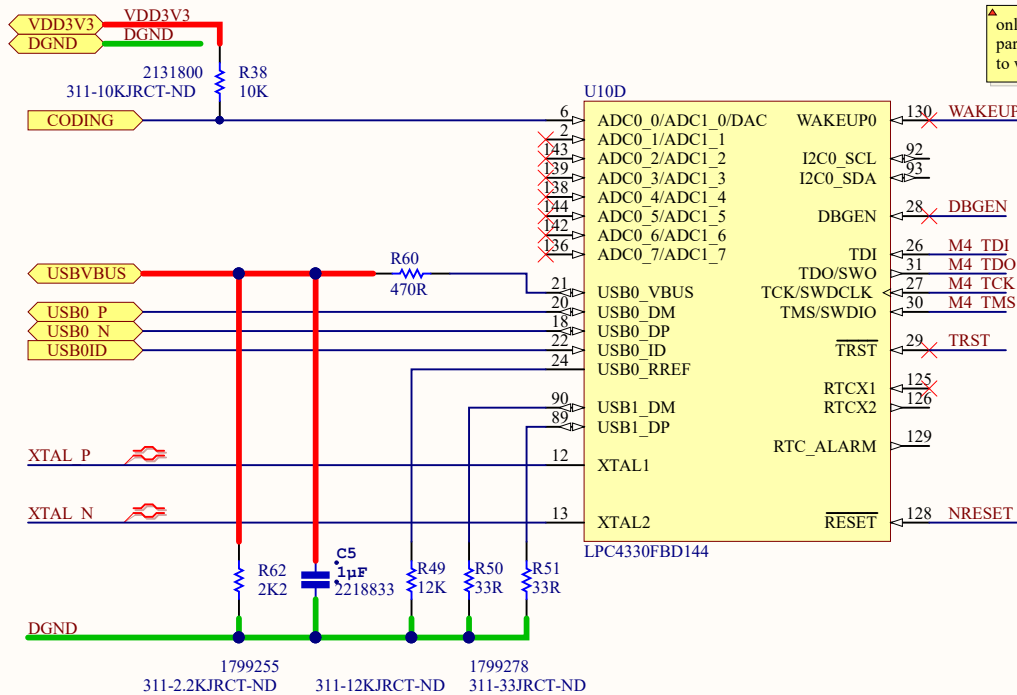
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External	AVDD	N/A	2xExternal REF	AVDD	Twos Complement	Disabled
Internal Fixed	VREF	0.5	1.0	2/3 AVDD	Twos Complement	Enabled
Programmable	0.2 V to VREF	0.5x(1+R10/R11)	2xVREF	1/3 AVDD	Offset Binary	Enabled
Internal Fixed	AGND to 0.2 V	1.0	2.0	AGND (Default)	Offset Binary	Disabled

Project	<i>Ultrasonic Doppler 2015</i>			<div>Hochschule Ulm Institut für Medizintechnik und Mechatronik Albert-Einstein-Allee 55 89081 Ulm</div> <div><div><div>Technik Informatik & Medien</div><div><div>Hochschule Ulm</div><div>University of Applied Sciences</div></div></div></div>
Title	<i>Receiver</i>			
Size:	A4	Number:*	Revision:*	
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Eng:	Andreas Rehn			









A

B

C

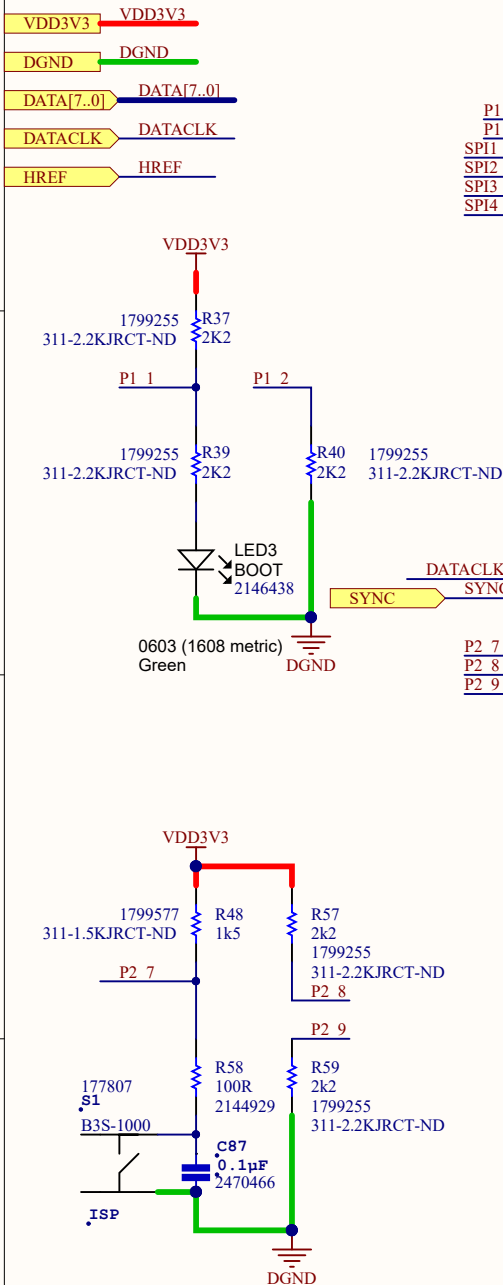
D

A

B

C

D



U10A

32	P0_0/GPIO0[0]/SSP1_MISO/ENET_RXD1/SGPIO0/I2S0_TX_WS/I2S1_TX_WS
34	P0_1/GPIO0[1]/SSP1_MOSI/ENET_COL/SGPIO1/ENET_TX_EN/I2S1_TX_SDA
38	P1_0/GPIO0[4]/CTIN_3/EMC_A5/SSP0_SSEL/SGPIO7
42	P1_1/GPIO0[8]/CTOUT_7/EMC_A6/SGPIO8/SSP0_MISO
43	P1_2/GPIO0[9]/CTOUT_6/EMC_A7/SGPIO9/SSP0_MOSI
44	P1_3/GPIO0[10]/CTOUT_8/SGPIO10/EMC_OE/USB0_IND1/SSP1_MISO/SD_RST
47	P1_4/GPIO0[11]/CTOUT_9/SGPIO11/EMC_BLS0/USB0_IND0/SSP1_MOSI/SD_VOLT1
48	P1_5/GPIO1[8]/CTOUT_10/EMC_CS0/USB0_PWR_FAULT/SSP1_SSEL/SGPIO15/SD_POW
49	P1_6/GPIO1[9]/CTIN_5/EMC_WE/SGPIO14/SD_CMD
50	P1_7/GPIO1[0]/U1_DSR/CTOUT_13/EMC_D0/USB0_PPWR
51	P1_8/GPIO1[1]/U1_DTR/CTOUT_12/EMC_D1/SD_VOLT0
52	P1_9/GPIO1[2]/U1_RTS/CTOUT_11/EMC_D2/SD_DAT0
53	P1_10/GPIO1[3]/U1_RI/CTOUT_14/EMC_D3/SD_DAT1
55	P1_11/GPIO1[4]/U1_CTS/CTOUT_15/EMC_D4/SD_DAT2
56	P1_12/GPIO1[5]/U1_DCD/EMC_D5/T0_CAP1/SGPIO8/SD_DAT3
60	P1_13/GPIO1[6]/U1_TXD/EMC_D6/T0_CAP0/SGPIO9/SD_CD
61	P1_14/GPIO1[7]/U1_RXD/EMC_D7/T0_MAT2/SGPIO10
62	P1_15/GPIO2[2]/U2_TXD/SGPIO2/ENET_RXD0/T0_MAT1
64	P1_16/GPIO0[3]/U2_RXD/SGPIO3/ENET_CRIS/T0_MAT0/ENET_RX_DV
67	P1_17/GPIO0[12]/U2_UCLK/ENET_MDIO/T0_CAP3/CAN1_TD/SGPIO11
68	P1_18/GPIO0[13]/U2_DIR/ENET_TXD0/T0_MAT3/CAN1_RD/SGPIO12
68	P1_19/ENET_TX_CLK(ENET_REF_CLK)/SSP1_SCK/CLKOUT/I2S0_RX_MCLK/I2S1_TX_SCK
70	P1_20/GPIO0[15]/SSP1_SSEL/ENET_TXD1/T0_CAP2/SGPIO13
75	P2_0/SGPIO4/U0_TXD/EMC_A13/USB0_PPWR/GPIO5[0]/T3_CAP0/ENET_MDC
81	P2_1/SGPIO5/U0_RXD/EMC_A12/USB0_PWR_FAULT/GPIO5[1]/T3_CAP1
84	P2_2/SGPIO6/U0_UCLK/EMC_A11/USB0_IND1/GPIO5[2]/CTIN_6/T3_CAP2
87	P2_3/SGPIO12/I2C1_SDA/U3_TXD/CTIN_1/GPIO5[3]/T3_MAT0/USB0_PPWR
88	P2_4/SGPIO13/I2C1_SCL/U3_RXD/CTIN_0/GPIO5[4]/T3_MAT1/USB0_PWR_FAULT
91	P2_5/SGPIO14/CTIN_2/USB1_VBUS/ADCTRIG1/GPIO5[5]/T3_MAT2/USB0_IND0
92	P2_6/SGPIO7/U0_DIR/EMC_A10/USB0_IND0/GPIO5[6]/CTIN_7/T3_CAP3
95	P2_7/GPIO0[7]/CTOUT_1/U3_UCLK/EMC_A9/T3_MAT3
96	P2_8/SGPIO15/CTOUT_0/U3_DIR/EMC_A8/GPIO5[7]
98	P2_9/GPIO1[10]/CTOUT_3/U3_BAUD/EMC_A0
102	P2_10/GPIO0[14]/CTOUT_2/U2_TXD/EMC_A1
104	P2_11/GPIO1[11]/CTOUT_5/U2_RXD/EMC_A2
105	P2_12/GPIO1[12]/CTOUT_4/EMC_A3/U2_UCLK
106	P2_13/GPIO1[13]/CTIN_4/EMC_A4/U2_DIR
112	P3_0/I2S0_RX_SCK/I2S0_RX_MCLK/I2S0_TX_SCK/I2S0_TX_MCLK/SSP0_SCK
114	P3_1/I2S0_TX_WS/I2S0_RX_WS/CAN0_RD/USB1_IND1/GPIO5[8]
116	P3_2/I2S0_TX_SDA/I2S0_RX_SDA/CAN0_TD/USB1_IND0/GPIO5[9]
118	P3_3/SPI_SCK/SSP0_SCK/SPIFI_SCK/CGU_OUT1/I2S0_TX_MCLK/I2S1_TX_SCK
119	P3_4/GPIO1[14]/SPIFI_SIO3/U1_TXD/I2S0_TX_WS/I2S1_RX_SDA
121	P3_5/GPIO1[15]/SPIFI_SIO2/U1_RXD/I2S0_TX_SDA/I2S1_RX_WS
122	P3_6/GPIO0[6]/SPI_MISO/SSP0_SSEL/SPIFI_MISO/SSP0_MISO
123	P3_7/SPI_MOSI/SSP0_MISO/SPIFI_MOSI/GPIO5[10]/SSP0_MOSI
124	P3_8/SPI_SSEL/SSP0_MOSI/SPIFI_CS/GPIO5[11]/SSP0_SSEL

LPC4330FBD144

U10C

45	CLK0/EMC_CLK0/CLKOUT/SD_CLK/EMC_CLK01/SSP1_SCK/ENET_TX_CLK(ENET_REF_CLK)
99	CLK2/EMC_CLK3/CLKOUT/SD_CLK/EMC_CLK23/I2S0_TX_MCLK/I2S1_RX_SCK

LPC4330FBD144

U10B

1	P4_0/GPIO2[0]/MCOA0/NMI/U3_UCLK
8	P4_1/GPIO2[1]/CTOUT_1/U3_TXD/ENET_COL/ADC0_1
9	P4_2/GPIO2[2]/CTOUT_0/U3_RXD/SGPIO8
10	P4_3/GPIO2[3]/CTOUT_3/U3_BAUD/SGPIO9/ADC0_0
11	P4_4/GPIO2[4]/CTOUT_2/U3_DIR/SGPIO10/DAC
12	P4_5/GPIO2[5]/CTOUT_5/SGPIO11
14	P4_6/GPIO2[6]/CTOUT_4/SGPIO12
15	P4_7/GP_CLKIN/I2S1_TX_SCK/I2S0_TX_SCK
33	P4_8/CTIN_5/GPIO5[12]/CAN1_TD/SGPIO13
35	P4_9/CTIN_6/GPIO5[13]/CAN1_RD/SGPIO14
37	P4_10/CTIN_2/GPIO5[14]/SGPIO15
39	P5_0/GPIO2[9]/MCOB2/EMC_D12/U1_DSR/T1_CAP0
46	P5_1/GPIO2[10]/MCI2/EMC_D13/U1_DTR/T1_CAP1
54	P5_2/GPIO2[11]/MCI1/EMC_D14/U1_RTS/T1_CAP2
57	P5_3/GPIO2[12]/MCI0/EMC_D15/U1_RI/T1_CAP3
58	P5_4/GPIO2[13]/MCOB0/EMC_D8/U1_CTS/T1_MAT0
63	P5_5/GPIO2[14]/MCOA1/EMC_D9/U1_DCD/T1_MAT1
65	P5_6/GPIO2[15]/MCOB1/EMC_D10/U1_TXD/T1_MAT2
73	P5_7/GPIO2[7]/MCOA2/EMC_D11/U1_RXD/T1_MAT3
74	P6_0/I2S0_RX_MCLK/I2S0_RX_SCK
78	P6_1/GPIO3[0]/EMC_DYCS1/U0_UCLK/I2S0_RX_WS/T2_CAP0
79	P6_2/GPIO3[1]/EMC_CKEOUT1/U0_DIR/I2S0_RX_SDA/T2_CAP1
80	P6_3/GPIO3[2]/USB0_PPWR/SGPIO4/EMC_CS1/T2_CAP2
82	P6_4/GPIO3[3]/CTIN_6/U0_TXD/EMC_CAS
83	P6_5/GPIO3[4]/CTOUT_6/U0_RXD/EMC_RAS
85	P6_6/GPIO0[5]/EMC_BLS1/SGPIO5/USB0_PWR_FAULT/T2_CAP3
86	P6_7/EMC_A15/SGPIO6/USB0_IND1/GPIO5[15]/T2_MAT0
87	P6_8/EMC_A14/SGPIO7/USB0_IND0/GPIO5[16]/T2_MAT1
97	P6_9/GPIO3[5]/EMC_DYCS0/T2_MAT2
100	P6_10/GPIO3[6]/MCABORT/EMC_DQMOUT1
101	P6_11/GPIO3[7]/EMC_CKEOUT0/T2_MAT3
103	P6_12/GPIO2[8]/CTOUT_7/EMC_DQMOUT0
110	P7_0/GPIO3[8]/CTOUT_14/SGPIO4
113	P7_1/GPIO3[9]/CTOUT_15/I2S0_TX_WS/U2_TXD/SGPIO5
115	P7_2/GPIO3[10]/CTIN_4/I2S0_TX_SDA/U2_RXD/SGPIO6
117	P7_3/GPIO3[11]/CTIN_3
132	P7_4/GPIO3[12]/CTOUT_13/TRACEDATA[0]/ADC0_4
133	P7_5/GPIO3[13]/CTOUT_12/TRACEDATA[1]/ADC0_3
134	P7_6/GPIO3[14]/CTOUT_11/TRACEDATA[2]
140	P7_7/GPIO3[15]/CTOUT_8/TRACEDATA[3]/ENET_MDC/SGPIO7/ADC1_6
69	P9_5/MCOA1/USB1_PPWR/GPIO5[18]/ENET_TXD3/SGPIO3/U0_TXD
72	P9_6/GPIO4[11]/MCOB1/USB1_PWR_FAULT/ENET_COL/SGPIO8/U0_RXD
120	PF_4/SSP1_SCK/GP_CLKIN/TRACECLK/I2S0_TX_MCLK/I2S0_RX_SCK

LPC4330FBD144

PWR ON

RESET

SPI[4..0]

Project **Ultrasonic Doppler 2015**Title **LPC4337 Ports**Size: **A4**

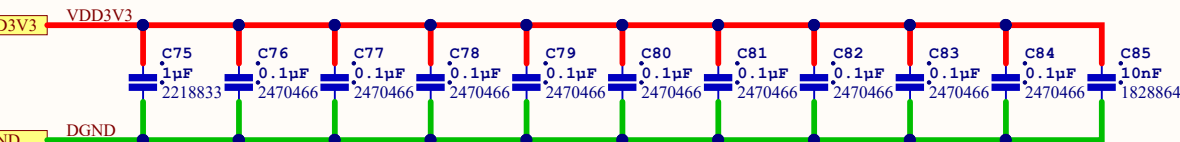
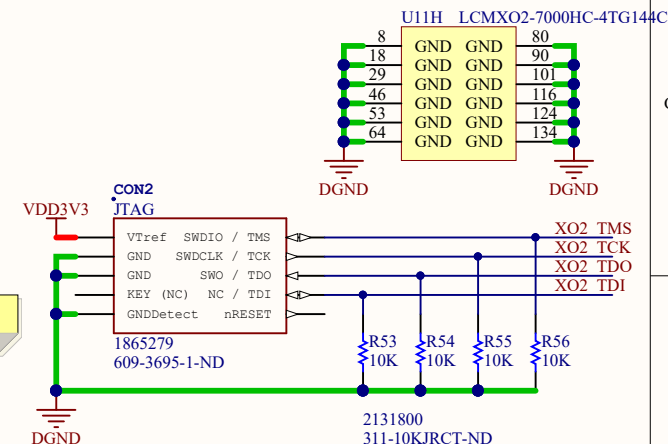
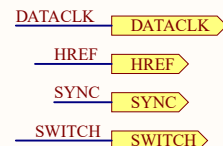
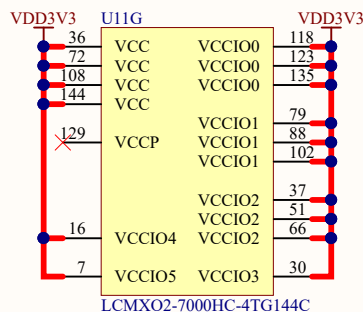
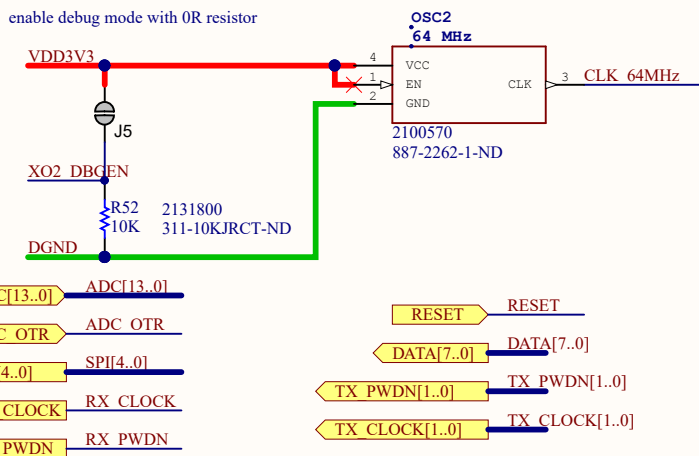
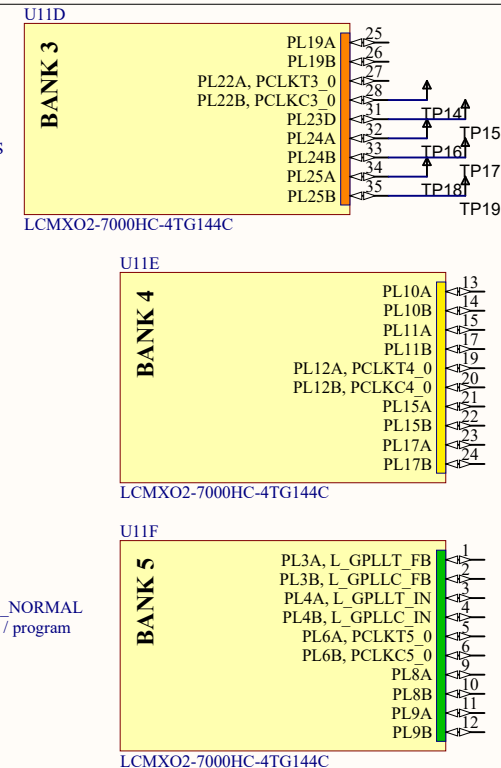
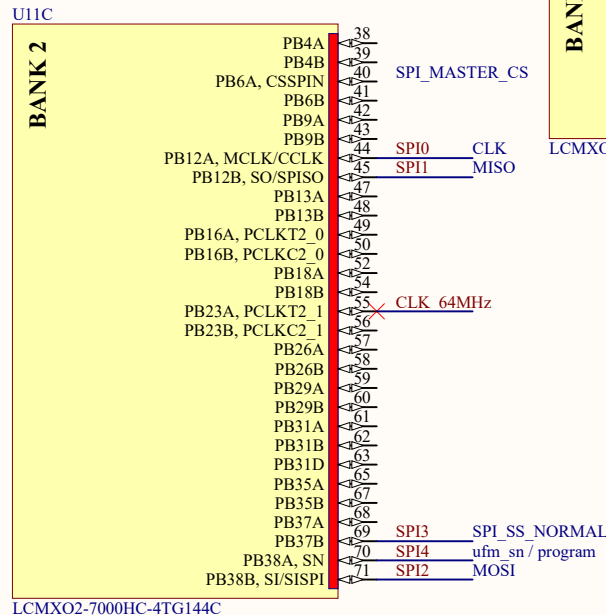
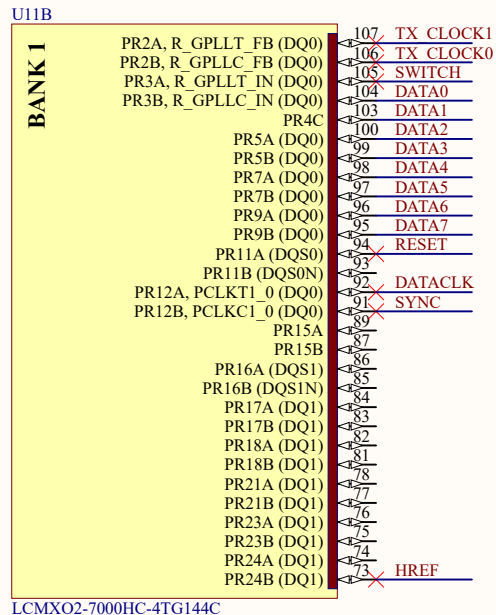
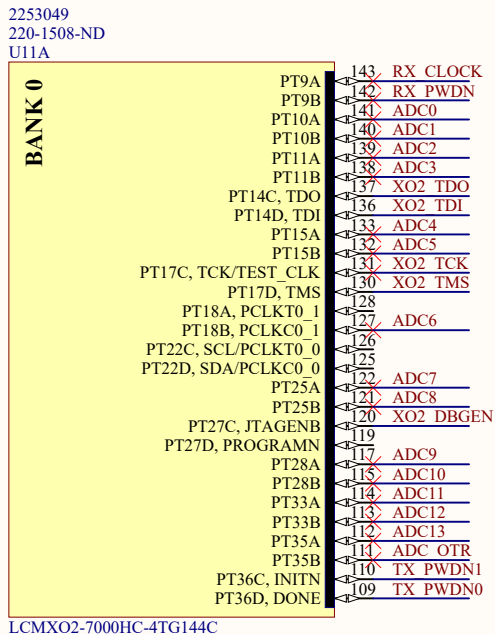
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Date: **15.10.2015**Time: **11:20:49**Sheet **10** of **11**Eng: **Andreas Rehn**

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Project **Ultrasonic Doppler 2015**

Title **CPLD**

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Eng: Andreas Rehn

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