

# OENG1168: Engineering Capstone Project

## Part B

### Completion Report

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# 1 Project Review: A Parametric Digital Transducer Array Loudspeaker

The design in which the Capstone B project is based is called a Parametric Digital Transducer Array Loudspeaker (PDTAL). A PDTAL combines the design attributes of both the Parametric Loudspeaker Array (PLA), and the one-bit per transducer Digital Transducer Array Loudspeaker (DTAL).

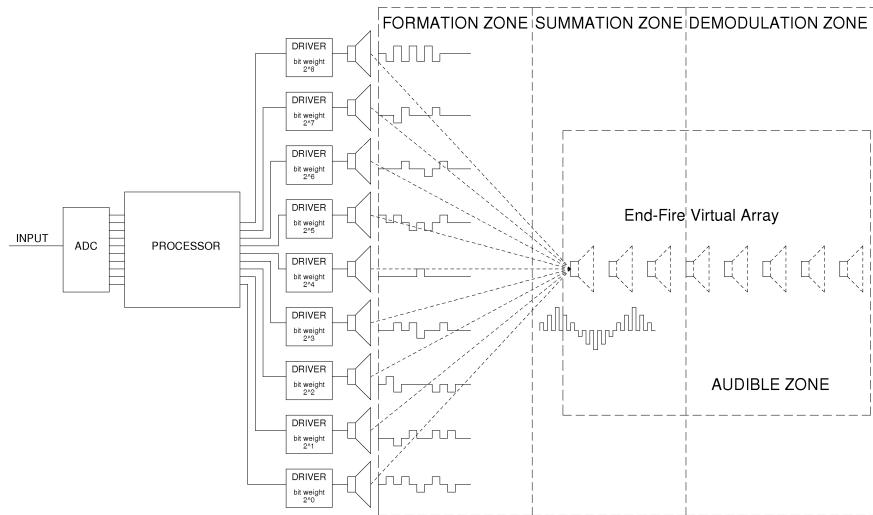


Figure 1: A beamforming capable PDTAL in air. [1]

The PLA is a highly directive loudspeaker array that consists of an array of ultrasonic transducers that exploit the nonlinear properties of air to self-demodulate modulated ultrasonic signals with the aim of creating audible sound waves [1].

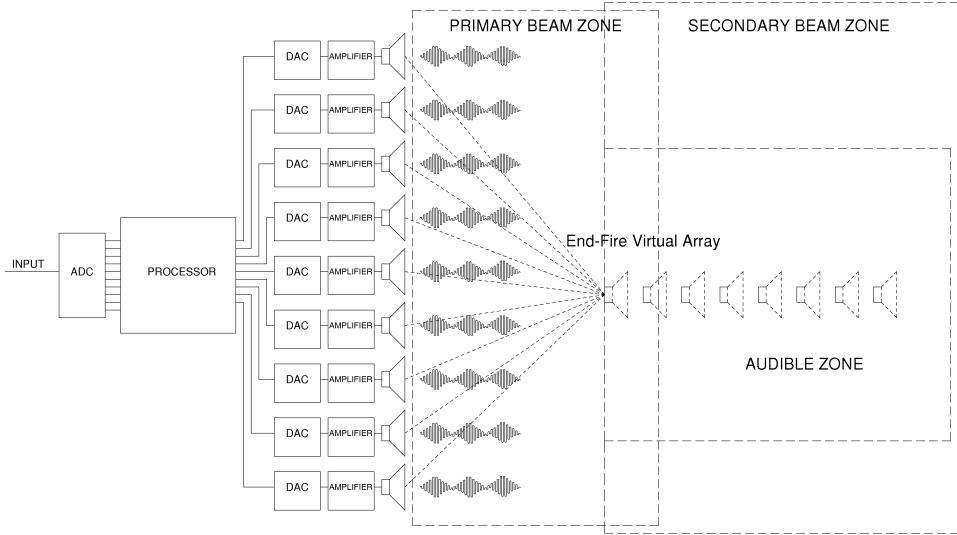


Figure 2: A beamforming capable PLA in air. [1]

The one-bit per transducer DTAL works on the principle that each weighted bit in a pulse code modulated input signal is represented by one transducer. Each transducer element has a surface area proportional to its bit weight, or is driven by a signal proportional to its bit weight [1]. The DTAL is capable of performing Direct Acoustic Digital-to-Analog Conversion (DADAC), which is the process of creating acoustically decoded sound pressure signals by driving and emitting digital streams through a loudspeaker with conversion taking place via acoustic summation [1].

It is hoped the design will enable the production of PLA devices that can perform beamforming without the need for many Digital-to-Analog Converter (DAC) integrated circuits, thus reducing overall the cost for beamforming capable PLAs.

## 2 Design Requirements

### 2.1 Software

To build a PDTAL, various design requirements must be fulfilled. Double side-band (DSB) modulation must be applied to an audio signal, and the resulting digital signal must be split up in to individual bit streams based on each weighted bit within the DSB modulated signal.

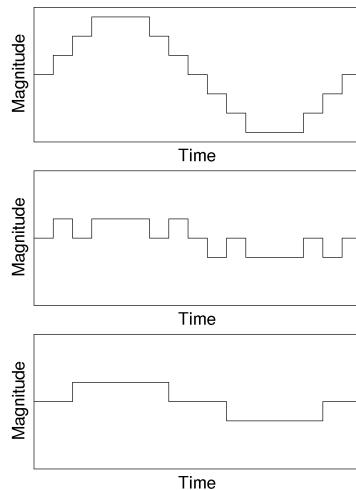


Figure 3: "Bit spilling" producing multiple weighted bit streams. [1]

Each bit steam must then be converted in to the double-sided pulse width modulation (PWM) signal. These resulting PWM signals will have a duty cycle which reflects the weighted bit that each bit-stream represents.

Finally, the double-sided PWM signal is encoded in a fashion that allows it to drive h-bridge drivers, which in turn drives individual ultrasonic piezo transducers directly, thus negating the need for costly DACs.

### 2.2 Hardware

The hardware design requirements for the project include an FPGA development board, where the software requirements will be implemented. In

addition, a PCB will need to be designed and built that will need to interface with the FPGA as well as providing a way for the H-bridge drivers to be powered and connected to the FPGA. Finally, the loudspeaker array will need to be constructed. The array will consist of 28 piezo ultrasonic transducers arranged in a circular fashion on a separate PCB. This PCB will also need to be designed and manufactured in a way that will allow the array to be connected to the mother PCB where the h-bridge drivers are located.

### **2.3 Simulation**

In an attempt to characterise the overall system prior to building the device, extensive simulation using MATLAB will be used to validate the system design. This will include time and frequency domain analysis of the different modulation techniques being used, as well as the resulting non-linear demodulation equation that defines how modulated ultrasonic signals are able to demodulate in air.

### **2.4 Implementation**

In order to reduce design complexity and hardware costs, a programmable oscillator will be implemented on the FPGA as an input to the system. This negates the need for any kind of external signal generation and Analog-to-Digital (ADC) conversion. The DSB modulation, PWM conversion, and h-bridge encoding will all be implemented using VHDL for the FPGA development board. The PCB design will be completed using EAGLE, and manufactured by an online manufacturer. Simulations of the entire system will be completed in MATLAB to try and characterise the device before it is built.

### **2.5 Test and Verification**

In order to test and verify the device, a microphone with bandwidth characteristics of 100Hz to 80Khz is required in order to measure the response of the speaker. A quiet room is required, although it does not necessarily need to be anechoic. Gated measuring techniques will be utilised to ensure the measurements are valid. This room will most likely be located at RMIT, pending of the sourcing of a microphone that is suitable for the purposes of the experiment.

### 3 Completion Plan

#### 3.1 Previous timeline

Previously a timeline for the entirety of the project was defined. This timeline was broadly followed but significant changes have occurred with the project since its creation. With this in mind, a new timeline has been created taking in to account tasks that have been changed, and task that have already been completed.

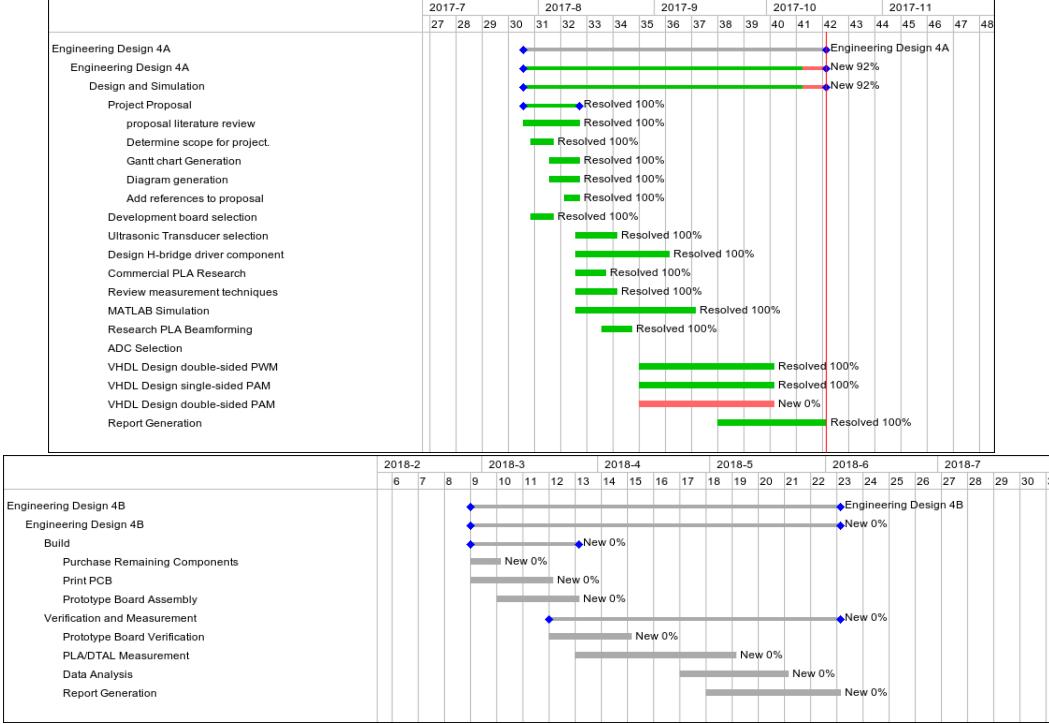


Figure 4: Previously defined timeline for project. [1]

#### 3.2 All Tasks and their Completion Status

The following table shows a list of all tasks that are require to be completed for the project to be completed. The completion status of each task is clearly identified.

Task	Completed?
Project proposal	Yes
Development board selection	Yes
Ultrasonic transducer selection	Yes
H-bridge driver selection	Yes
Commercial PLA research	Yes
Measurement techniques review	Yes
MATLAB simulation	Yes
PLA beamforming research	Yes
Engineering 4A report	Yes
VHDL input programmable oscillator	No
VHDL DSB modulation	Yes
VHDL PWM	No
VHDL H-bridge encoding	No
FPGA synthesis	No
Mother board PCB design	No
Loudspeaker array PCB design	Yes
PCB ordering	No
PCB populating	No
PCB verification	No
FPGA test and verification	No
PDTAL test and verification	No
Final Report	No

Table 1: Completion status of all tasks.

### 3.3 Gantt Chart

The following Gantt chart outlines a new timeline for the completion of tasks that are yet to be completed in the project.

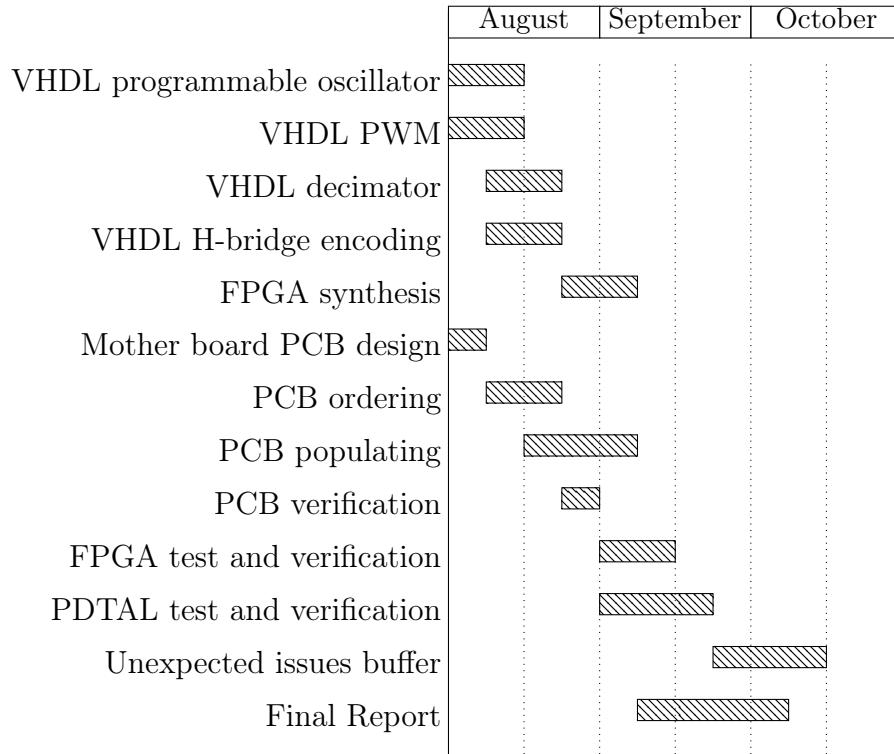


Figure 5: A Gantt chart of the proposed project schedule.

## 4 Detailed Explanation of Remaining Tasks

While many of these tasks are simple, I have provided wide time buffers for each task to ensure that each task will get done properly. I have also provided an additional "Unexpected issues buffer" at the end of the project to account for any significant issues.

## 4.1 VHDL Programmable Oscillator

The programmable oscillator exists primarily as software in the form of VHDL code. It is required as the source of various input signals that will be used to drive the PDTAL. These signals will be useful in the test and verification phase of the loudspeaker array, so we can characterise the device and see if the design is valid.

The design of such oscillators can be complicated depending on the requirements. However I have already designed simple oscillators in VHDL using the Xilinx ISE IP tools. Using these tools is simple and I anticipate that this task will only take a couple of hours to complete. This includes the using of the tools to generate the code, and the simulation of the resulting VHDL module in Isim to ensure the oscillator works as intended. No apparent obstacles exist for this task.

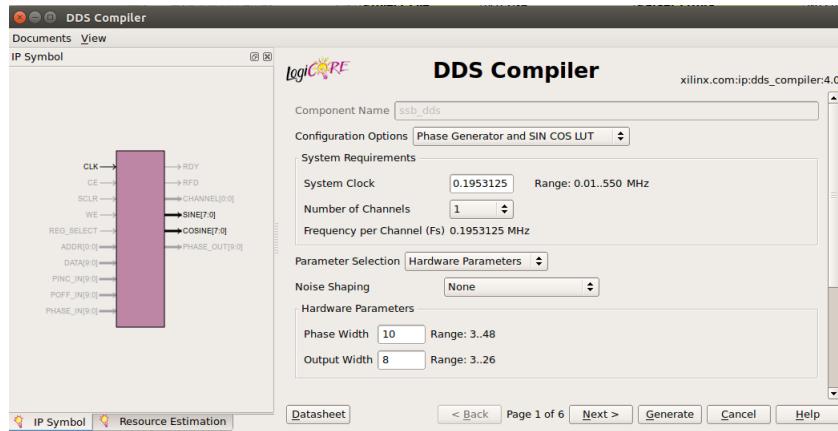


Figure 6: The ISE DDS Compiler what produces VHDL code for programmable oscillators.

## 4.2 VHDL PWM

The PWM VHDL module provides a way to drive the individual transducers in the PDTAL with different weighted signals, thus it is a very important part of the project. This VHDL module is one of the core modules that allows DADAC to occur properly.

The design and implementation of PWM modules in VHDL are straight forward and simple. I anticipate it will only take one day to design, implement, and simulate the module in Isim. No apparent obstacles exist for this task.

### 4.3 VHDL Decimator

In MATLAB simulations it proved vital to decimate the PWM outputs in order for the modulated acoustics waves to demodulate in air correctly, thus the VHDL decimator is also vital to the project.

The design and implementation of decimation modules in VHDL are straight forward and simple. I anticipate it will only 2 hours to design, implement, and simulate the module in Isim. No apparent obstacles exist for this task.

### 4.4 VHDL H-bridge encoder

The h-bridge encoding of the decimated PWM signals is necessary to be able to correctly drive the H-bridge driver ICs which in turn drive the piezo transducers directly

The design and implementation of this kind of encoding in VHDL uses simple logic and is simple to implement. I anticipate it will only 2 hours to design, implement, and simulate the module in Isim. No apparent obstacles exist for this task.

### 4.5 FPGA Synthesis

FPGA Synthesis involves taking the FPGA code that was simulated and performing the compilation required to flash the FPGA in real life. Once the code is compiled, it will become possible to flash the FPGA, and begin the test and verification process.

My main concerns with the FPGA synthesis is that I have never completed it before. While I am confident that there will be no significant issues, I have factored in generous time buffers with this step due to my lack of experience with the process as a way to mitigate the risks that the task has

unforeseen complications.

Some of these complications might be:

- Driver issues between the FPGA development board, Xilinx ISE, and my linux computer.
- Development board does not function, or has unforeseen issues due to it being in storage for a significant period
- Logic limitations exceeded for my particular development board.

The largest issue is potential driver issues when trying to flash the XEM6010-LX45 FPGA board. To mitigate this, I have created generous time buffers. I have also arranged access to a Windows PC with Xilinx ISE software installed in case the driver issues persist. To mitigate the risk that the FPGA board is broken, I have sourced a second FPGA board that I can replace the potentially broken one with.



Figure 7: The XEM6010-LX45 Opal Kelly FPGA board being used.

## 4.6 Mother Board PCB Design, Ordering, Population, and Verification

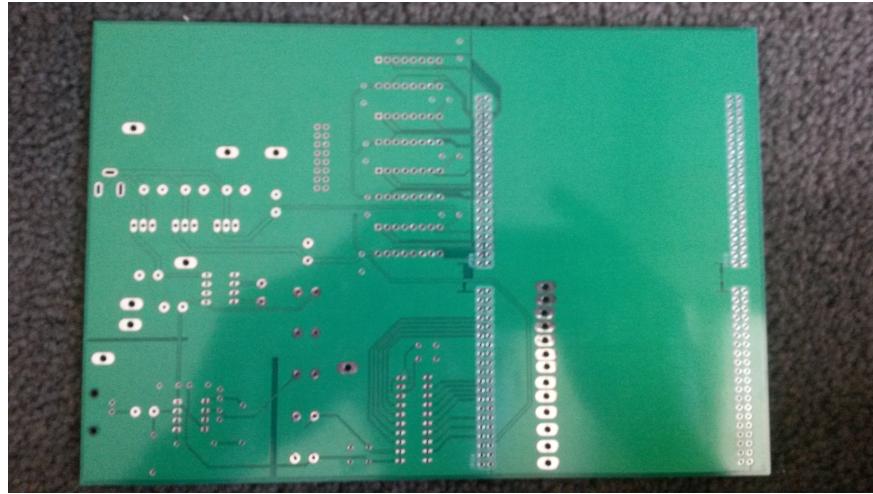


Figure 8: The first iteration of the mother board PCB design.

The mother board PCB will be the PCB that interfaces with the XEM6010-LX4, H-bridge drivers, and PDTAL together. The design is straight forward and simple. One iteration of the PCB has already been designed and printed, however design changes and errors on the PCB have occurred, thus necessitating the design of a new PCB.

Due to the fact that most of the first design is reusable, it should not take more than 5 hours to complete and order the new PCB to be manufactured. Once the PCB arrives, it should take one additional day to populated and verify the PCB.

There is a slight risk that another PCB design error can occur, which is why I assigned generous time buffers to allow the potential order of modified boards. I will get a fellow student to review my PCB design, lowering the risk an error will go unnoticed.

## 4.7 FPGA Test and Verification

The FPGA test and verification will occur after the FPGA has been flashed. It will involve ensuring that the VHDL code is functioning as intended on the FPGA using an oscilloscope.

Due to the way that VHDL functions, the simulations conducted while writing the code should ensure I catch any mistakes in the simulation phase of coding. Thus this step should be completed in only one week provided I have access to an oscilloscope.

There is a slight risk that my simulations were not comprehensive enough, and that I could miss potential bugs in my code, which is why I have assigned a large time buffer to this task. However, changes to the code will be relatively easy to rectify, simulate, and flash.

## 4.8 PDTAL Test and Verification

The PDTAL test and verification will occur after all PCBs are populated and the XEM6010-LX45 is flashed. It will involve measuring different voltages and signals on all aspects of the project, and ensuring system functionality. This includes power supply lines, oscillator output frequency, DSB modulation output, PWM output, and H-bridge encoder output. Once this has been verified, the physical measurement of the PDTAL will take place using a quiet room and a microphone that is capable of measure frequency from 100Hz to 80Khz. Gating techniques will be utilised to ensure the integrity of the results. These microphone gating techniques involve eliminating the room reflections from the measured results by putting a time gate on the input of the microphone.

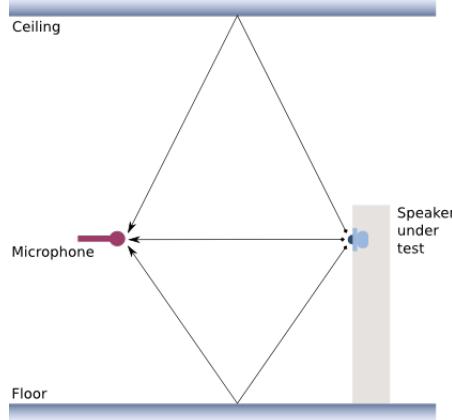


Figure 9: Example of room reflections effecting measured result. [2]

This will possibly be the most time consuming aspect of the project due to the wide range of components that require testing. I will use a variety of tools such as multimeters, oscilloscopes, and a microphone to validate the design.

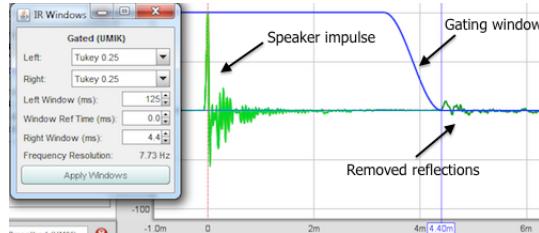


Figure 10: Example of time gating implementation. [2]

Some risks include errors in any of the project modules, as well as gaining access to a microphone suitable for conducting the measurements. To mitigate these risks I have assigned a large time buffer to the task, as well as sourced a potential backup microphone and preamp to perform measurements with. This backup is however only capable of measuring audio frequencies, thus the usefulness of the results will be limited.

A quiet room has been found within RMIT that is isolated which will be used. The source of the microphone if available will come from a facility at

Monash University, and is being organised through my supervisor Richardt Wilkinson.

## **4.9 Final Report Generation**

The final report will be generated predominately after the mid semester break will I am completing the project. Due to my extensive logging and record keeping, this should provide enough time to develop a well thought out professional report.

## 5 Communication with Supervisor

The communication with my supervisor, Richardt Wilkinson, primarily occurs at our weekly meetings which have been organised for the remainder of the semester. Correspondence via email is also common, and occasionally replaces our weekly meeting due to different circumstances. When this happens, a small progress report document is created and shared with Richardt in order to keep each other up to date with progress on the project.

During SWOT week I will be away from Melbourne in which we will continue to communicate through email. Work will continue on the project, and a project report will be created during this period to report any progress.

Feedback from Richardt on individually completed tasks is delivered at our weekly meetings, and thus broadly follows the same timeline as the defined Gantt chart.

## **6 Conclusion**

In conclusion, I am confident that the timelines I have defined in this document are well conceived, realistic, and responsible. I have a high degree of confidence that I will be able to complete the project within this time frame, and that enough redundancy has been planned for so that if any problems persist there will be plenty of time to rectify them.

Much work has been completed on this project before the beginning of the semester, and this has put me in a strong position in regards to completing the project in a timely fashion.

## References

- [1] D. Giancono, *Parametric Direct Acoustic Digital-to-Analog Conversion Capable Loudspeaker Arrays for Beamforming Applications*.
- [2] “Microphone gating techniques.” [Online]. Available: <https://www.minidsp.com/applications/acoustic-measurements/loudspeaker-measurements>