

Parametric Direct Acoustic Digital-to-Analog Conversion Capable Loudspeaker Array for Beamforming Applications

Assessment Task 2: Final Report

*This report is submitted in partial fulfillment of the requirements
for the course*

OENG1168: Engineering Capstone Project Part B

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Abstract

Parametric Loudspeaker Arrays provide a means to output highly directional audio in a small footprint due to the nonlinear self-demodulating properties of air. The characteristics of such arrays other than sharp directivity patterns are high total harmonic distortion, poor low frequency output, and low audible output due to poor conversion efficiency. Parametric Loudspeaker Arrays also provide opportunities to create beamforming arrays that can electronically steer audible acoustic waves. However commercial applications of this steerable technology have been limited due to the additional system cost involved in providing this capability. To reduce the total system cost of Parametric Loudspeaker Arrays with beamforming capability, this project aims to describe a new variant Parametric Loudspeaker Array type design by utilising digital amplifiers and Digital Transducer Loudspeaker Array techniques to drive transducer elements directly without the use of digital-to-analog converters. Simulations and measurements of a prototype system show that Parametric Digital Transducer Array Loudspeaker designs produce similar total harmonic distortion to that of conventional Parametric Transducer Arrays and lower off axis total harmonic distortion to that of Digital Transducer Array Loudspeakers while also having extended low frequency performance and beamforming capability without the use of digital-to-analog converters.

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1 Introduction

The Parametric Loudspeaker Array (PLA) and the Digital Transducer Array Loudspeaker (DTAL) have been used in both research and commercial applications to provide highly focused audio with narrow directivity patterns as a method to have better control over the distribution of audible sound from loudspeakers.

Many different modulation schemes, transducer array configurations, and design topologies have been researched to find a way to reduce the on-axis and off-axis Total Harmonic Distortion (THD), low conversion efficiency, and complicated circuitry required to design and perform intelligent beamforming with these devices.

To provide the ability to beamform with PLAs and DTALs, multiple Digital-to-Analog Converters (DACs) are often employed to provide unique signal processing to discrete transducer elements or transducer groups. This increases system cost and has resulted in a lack of beamforming capable PLAs in the marketplace.

To reduce these problems a new design has been developed that combines the design properties of PLAs and DTALs with the aim of exploiting the positive attributes of both systems to eliminate off-axis THD and reduce the circuitry required to perform beamforming. The Parametric Digital Transducer Array Loudspeaker (PDTAL) design aims to reduce the overall system cost of PLAs capable of beamforming by removing the need for any DACs in the system design. The design also hopes to improve the off-axis THD of DTAL type designs.

2 Literature Review

Direct Acoustic Digital-to-Analog Conversion (DADAC) is the process of creating acoustically decoded sound pressure signals by driving and emitting digital streams through a loudspeaker with conversion taking place via acoustic summation [1]. Devices that can perform DADAC provide exciting opportunities for high performing miniature loudspeakers, flat loudspeakers, and loudspeakers with beamforming capabilities as demonstrated in [2][3].

One such device that can perform DADAC is the one-bit per transducer DTAL. The one-bit per transducer DTAL configuration works on the principle that each weighted bit in a Pulse Code Modulated (PCM) input signal is represented by one transducer. Each transducer element has a surface area proportional to its bit weight, or is driven by a signal proportional to its bit weight [4][1][5]. This minimises the number of transducers required, reducing path distances between transducers. However, mismatches can occur between different transducer elements due to the differing surface areas and individual transducer nonlinearities [6].

It has been concluded that path differences between transducer elements are the main cause for high overall THD in DTALs [6][7][8]. Simulations and real-world results have shown that grouped geometries combined with random bit-to-transducer assignments dramatically improve on and off-axis THD [1][9][10]. DTALs utilising stepped digital input streams appear to result in a higher Sound Pressure Level (SPL) output, however pulsed digital input streams may generate cleaner waveforms [11].

A PLA is a highly directive loudspeaker that consists of an array of ultrasonic transducers that exploit the nonlinear properties of air to self-demodulate modulated ultrasonic signals with the aim of creating audible sound waves [13]. By using these properties, it is possible to produce devices that use beamforming to directly control the direction and dispersion of audio, as well as produce devices capable of precise directivity patterns, potentially reducing environmental noise and providing an isolated audio experience in many applications such as public-address systems, home theatre, and exhibition spaces [12].

The PLA is often characterised by its high directivity, high THD, beam-

forming ability to produce steerable arrays, poor low frequency output, and low audible output due to the poor conversion efficiency of the same mechanism that allows self-demodulation in the first place [13]. Many different array configurations and pre-processing modulation schemes have been experimented with to decrease THD, decrease side lobes, increase audible output, and produce steerable arrays [14][15][16][17].

Multiple studies have determined that single-sideband (SSB) pre-processing modulation schemes result in the lowest THD when driving PLAs [17][18]. Circular geometries when used with standard piezo emitters can increase the low frequency response and narrow the directivity pattern of the PLA, however increasing transducer packing density by using a hexagonal configuration results in optimum conversion efficiency [13]. Novel methods and calculations for developing beamforming capabilities in PLAs have been explored [16], simplifying the creation of a steerable PLA.

3 Design

To create steerable PLA devices, multiple DACs that feed various amplifier topologies are often used as a simple and flexible solution to adding beam-forming capability to PLA devices [17][19][20]. However, the use of multiple DACs increases the cost of steerable PLA devices and the signal processing resources required. The proposed design does not require any DAC in the system design, significantly reducing the overall system cost. The use of H-bridge drivers facilitates a simpler amplifier topology that can be driven directly from signal processors. Overall, this innovation in PLA design reduces the signal processing requirements and total system cost, paving the way for PLA designs with beamforming capability that are more affordable than related products that are currently on the market.

3.1 Parametric Loudspeaker Array Fundamentals

3.1.1 Concept

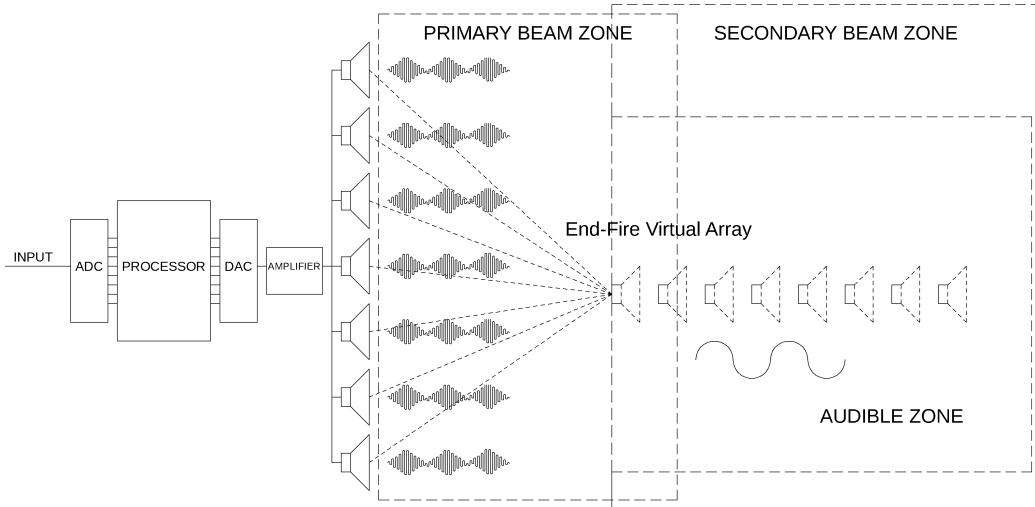


Figure 1: Parametric Loudspeaker Array without beamforming capability utilising digital processing.

PLAs exploit the nonlinearity of acoustic waves in air to create highly directive audio sources. An ultrasonic amplitude modulated signal is emitted

from a transducer consisting of a carrier frequency and sideband frequencies. This initial signal is referred to as the primary beam of the PLA. A new spectral component, the secondary beam, is created at a frequency that is the difference between the carrier frequency and sideband frequency due to the non-linear interaction between these two spectral components in air along the same beam as the primary beam [21]. This newly created spectral component is said to be the demodulated version of the signal that was emitted from the transducer. PLAs are an array of discrete transducers that form a loudspeaker that exploit this property. Berklay's solution describes the non-linear demodulation of the emitted signal [22].

$$p(\tau) \approx \frac{\beta p_o^2 a^2}{16 p_o c_o^4 z a_o} \frac{d^2}{d\tau^2} E^2(\tau) \quad (1)$$

Where:

- $p(\tau)$ = modulated signal pressure
- p_o = pressure source amplitude
- a = source radius
- a_o = absorption coefficient of the ultrasound carrier
- $E(\tau)$ = modulation envelope function of the carrier
- β = non-linear fluid parameter
- c_o = small signal sound velocity

Berklay's farfield solution

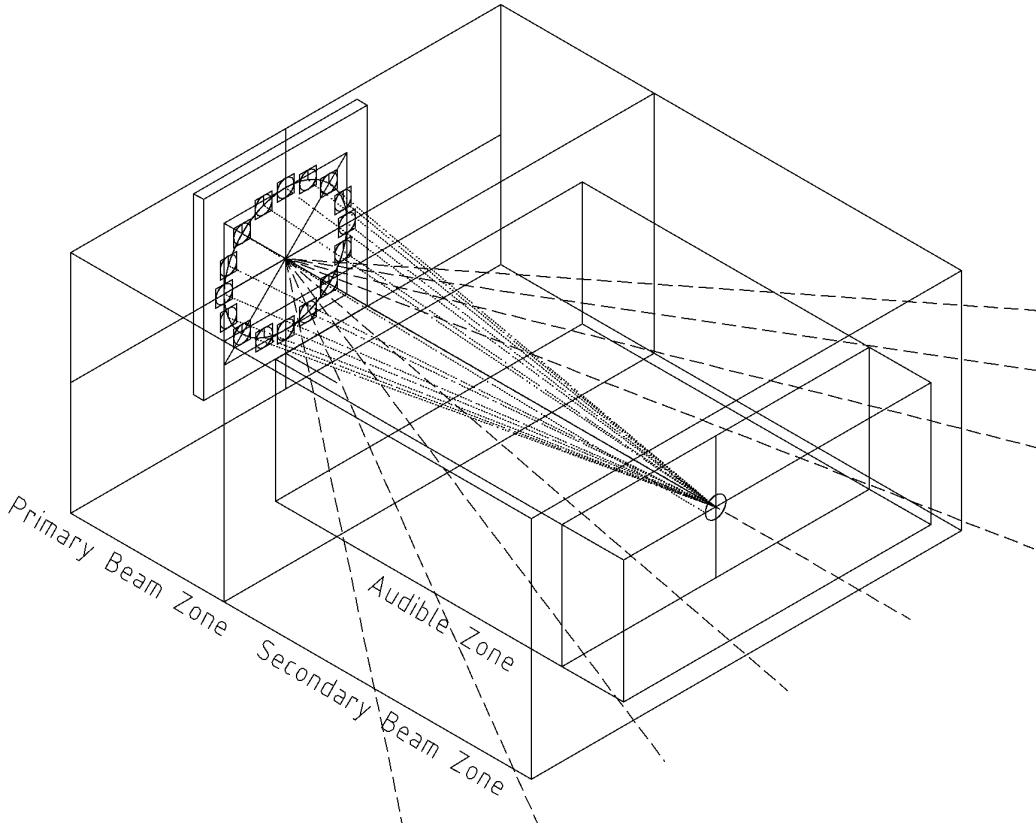


Figure 2: Parametric Loudspeaker Array with beamforming capability utilising circular geometry.

3.1.2 Modulation Techniques

Due to the non-linear mechanism that allows modulated signals to demodulate in air, signals that are modulated for the purpose of audible sound wave generation using PLAs must contain the carrier signal. Merklinger's solution shows the demodulated signals amplitude is directly proportional to the amplitude of the modulated signals pressure level [23].

$$p(\tau) \propto p_o^2 \frac{\partial^2}{\partial \tau^2} E^2(\tau) \quad (2)$$

Where:

$p(\tau)$ = modulated signal pressure

p_o = pressure source amplitude

$E(\tau)$ = modulation envelope function of the carrier

Merklinger's solution

Double-sideband Modulation The following block diagram and equation represents how a double-sideband (DSB) signal can be generated for use in a PLA design.

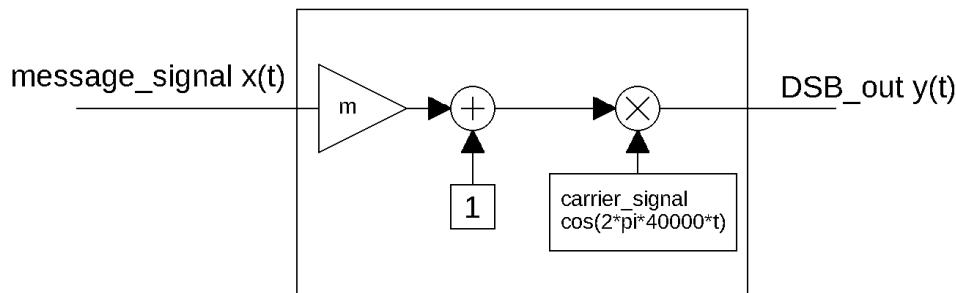


Figure 3: DSB with carrier generation block diagram

$$am(n) = [1 + mx(n)] * Acos(2\pi f_c n T_s) \quad (3)$$

Where:

m = modulation index

x = message signal

f_c = carrier frequency (Hz)

DSB Modulation with carrier

When modulating a message signal for use with a PLA consisting of ultrasonic piezo transducers, the carrier frequency must equal that of the resonant frequency of the piezo transducer if significant audible sound pressure level (SPL) is to be produced. Although DSB modulation is simple to produce, research has shown that due to the squaring of the signal during the non-linear demodulation process as per Berkay's solution, it is inevitable that DSB modulation schemes when used in parametric speaker applications will produce substantial amounts of THD [17][18].

3.1.3 Array Geometries

The array geometry used in a PLA design has an effect on both the frequency response and directivity pattern of the system. The most common geometries used are the circular geometry, the hexagonal geometry, and the square geometry. Examples of these three array geometries are shown in Figure 4. Research has shown that circular geometries can increase the low frequency response and narrow the directivity pattern of a PLA design at the cost of conversion efficiency, resulting in lower overall SPL output. By using geometries that have increased packing density, conversion efficiency and therefore SPL output can be increased. Array geometries with increased packing density include the hexagonal and square geometries [13].

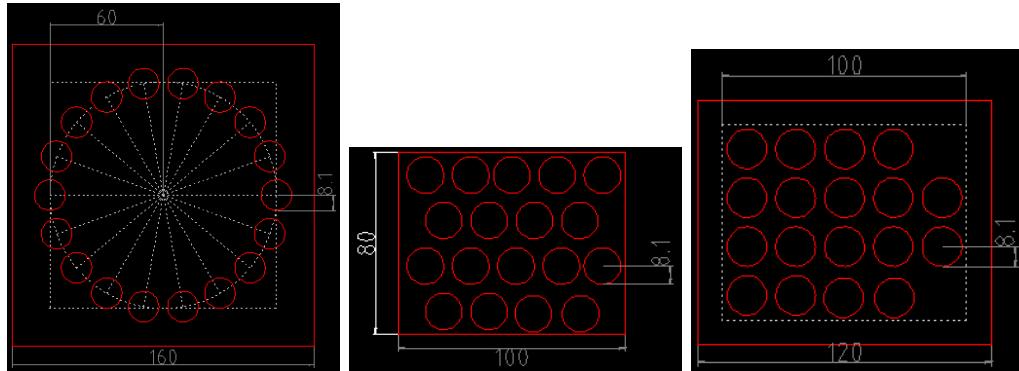


Figure 4: Various Parametric Loudspeaker Array geometries utilising 18 transducer elements.

3.1.4 Acoustic Beamforming Capability

Acoustic beamforming is a form of spatial filtering in which through signal processing techniques it is possible to control the transmission of directional sound waves. It is achieved by utilising an array of transducers and adding small amounts of differing delay values to individual transducers. This in effect creates a phased array. Destructive phase differences between transducers at many listening positions except for a specific position that has been mathematically calculated are created as a result of these added delay lines.

Due to the multiple transducers involved, acoustic beamforming is intrinsically possible when utilising a PLA. Figure 5 shows a PLA design with beamforming capability. This is achieved by adding DACs and drivers to each individual transducer element, thus making it possible to add differing delay values between transducer elements.

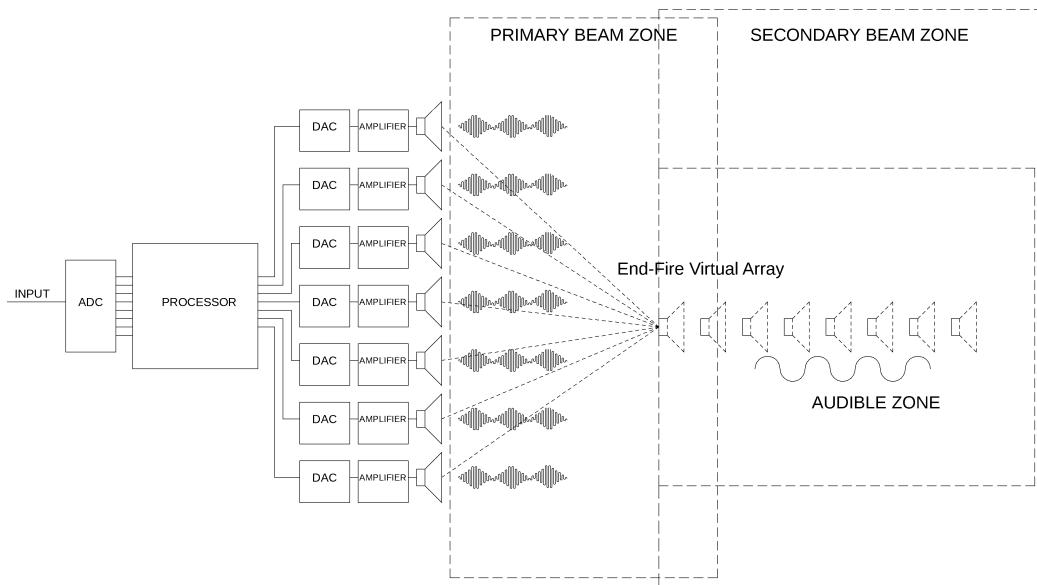


Figure 5: Parametric Loudspeaker Array with beamforming capability utilising digital processing.

3.2 Pulse Width Modulated Parametric Loudspeaker Array Fundamentals

3.2.1 Concept

The Pulse Width Modulated Parametric Loudspeaker Array (PWMPLA) functions in an almost identical way to that of a conventional PLA. A PLA can be driven directly with PWM signals, forgoing the use of a DAC in PLA designs utilising digital processing. The PWMPLA works on the principle that piezo transducers can be driven directly with PWM signals. Many of the harmonics contained within a PWM signal are attenuated or eliminated by the transducers narrow bandwidth. By driving the transducers with a digital signal such as a PWM signal, it is possible to use digital amplifiers such as H-bridge amplifiers to drive the transducer elements directly without the use of a DAC. This potentially reduces the overall system cost by a significant margin.

3.2.2 Double-sided Pulse Width Modulated Parametric Loudspeaker Array Design

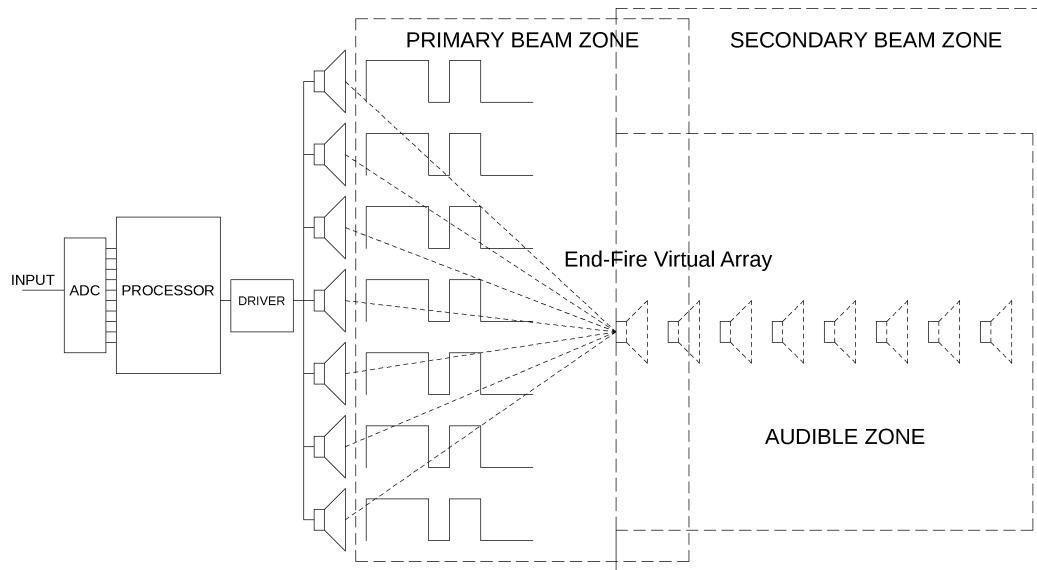


Figure 6: Pulse Width Modulated Parametric Loudspeaker Array without beamforming capability.

Double-sided PWMPLA designs are achieved by modulating a digital message signal with an Amplitude Modulation (AM) scheme. This modulated signal is then converted to a double-sided PWM signal. The PWM signal is encoded to a signal that is capable of driving a H-bridge amplifier directly. The H-bridge amplifier drives the array of piezo transducers. Due to the limited bandwidth of the transducer, the harmonics generated during the PWM conversion process are attenuated. This method can also result in higher THD, lower signal-to-noise ratio (SNR), and lower audible output than that of non-PWM signals, however due to the usage of double-sided PWM it is possible to achieve superior results to that of the a single-sided PWM method.

Designing a beamforming capable PWMPLA utilising H-bridge amplifiers is desirable due to minimised circuit complexity and cost compared to comparable designs. The circuit complexity and cost reduction is possible due to the simplicity of H-bridge amplifiers and the ability to produce double-sided PWM signals with a single rail power supply.

3.2.3 Limitations of Pulse Width Modulated Parametric Loudspeaker Designs

PWM Clock Frequency Requirements PWM circuits generated in the digital domain have finite resolution. When generating double-sided PWM signals for PLA designs, the minimum clock frequency is dependent on the following equation:

$$PWM_{cf} = PWM_{mf}2^{PWM_{bitdepth}-1} \quad (4)$$

Where:

$$\begin{aligned} PW_{cf} &= \text{PWM clock frequency (Hz)} \\ PWM_{mf} &= \text{PWM modulation frequency (Hz)} \\ PWM_{bitdepth} &= \text{PWM digital bit resolution} \end{aligned}$$

PWM clock frequency equation for PLA designs utilising PWM

Bit resolutions required for high fidelity audio are impractical to implement. A PWMPLA design utilising a bit resolution of 16 and a sampling

frequency of 120kHz would require a PWM clock frequency of the following to accurately produce the entire range of PWM values:

$$\begin{aligned} PWM_{cf} &= 120000Hz * 2^{16-1} \\ &= 3.93216GHz \end{aligned}$$

Clock frequency for 16 bit PWM generation.

Transducer SPL Output with Varying PWM Duty Cycle Piezo ultrasonic transducer SPL output does not correspond in a linear manner with PWM duty cycle. A short experiment was conducted involving two transducers. A Murata MA40S4R [24] receiving transducer was placed directly in front of a Murata MA40S4S [25] transmitting transducer. The transmitting transducer was driven with a square wave, and the duty cycle of said square wave was altered. Voltage output from the receiving transducer was recorded for each driving duty cycle.

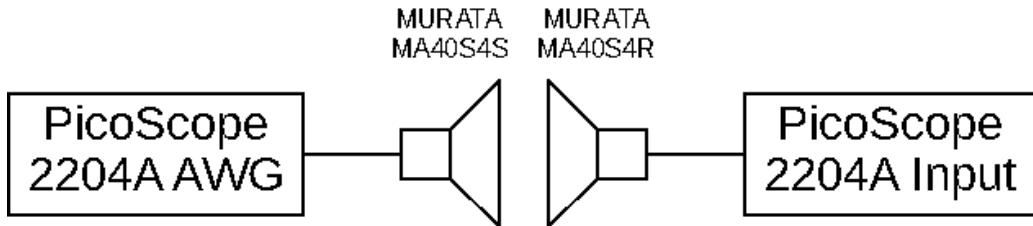


Figure 7: Experiment setup for the testing of Murata MA40S4S SPL output when driven by 40KHz square wave signal.

Figure 8 shows the results from this experiment. Maximum SPL output is achieved with a duty cycle of 50%, while each subsequent halving of the duty cycle does not result in an exact halving of SPL output. This phenomenon would result in additional THD when used in a PWMPLA design.

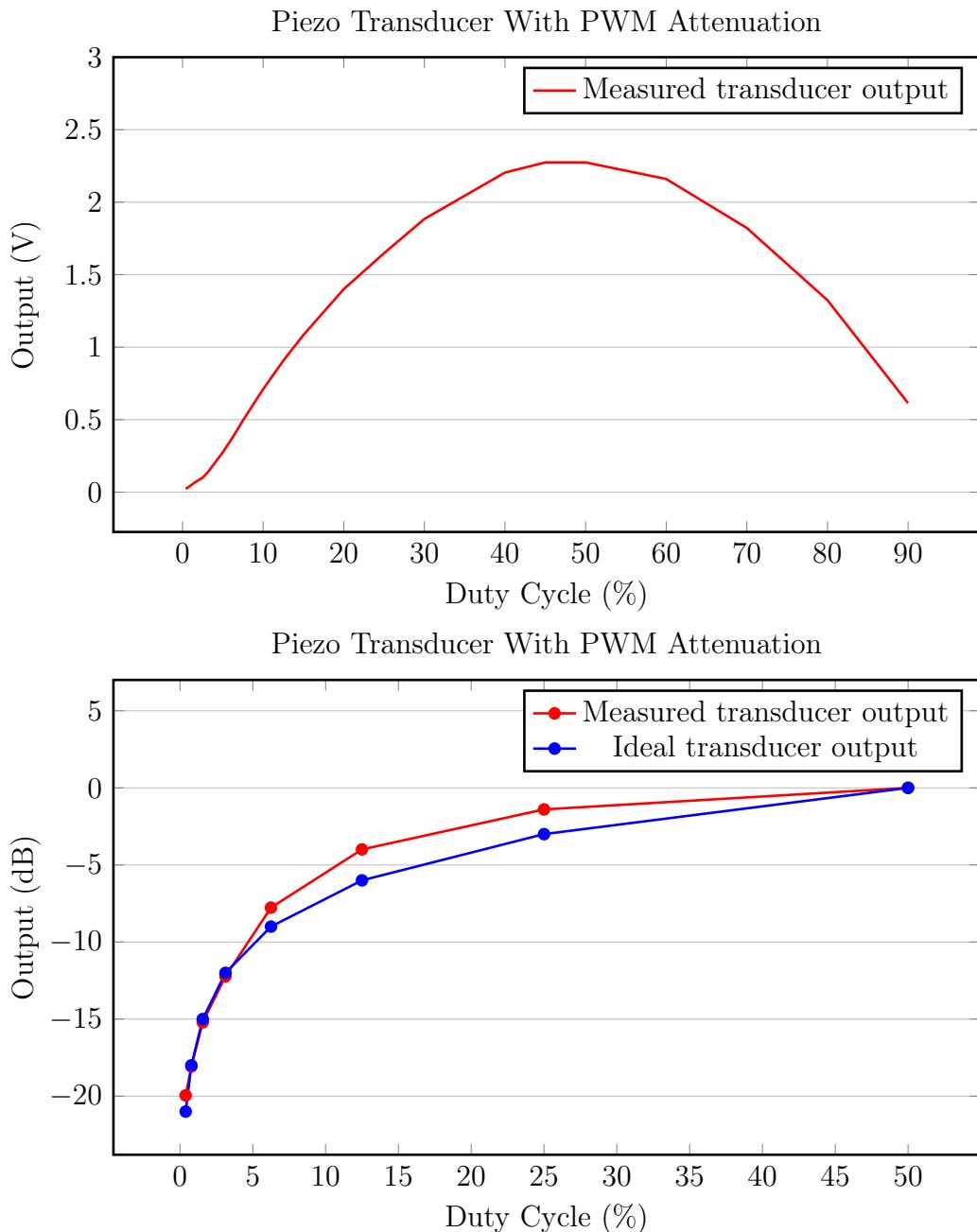


Figure 8: Results from driving Murata MA40S4S transducer with 40Khz PWM signal.

THD Increase due to PWM Harmonics When driven with a PWM signal a piezo transducers limited bandwidth attenuates many unwanted harmonics. However it does not attenuate them all, particularly when driven with DSB modulated signals with message signals containing spectral content under 1KHz. This results in a significantly lower Signal to Noise Ratio (SNR) compared to other PLA designs, as well as higher THD.

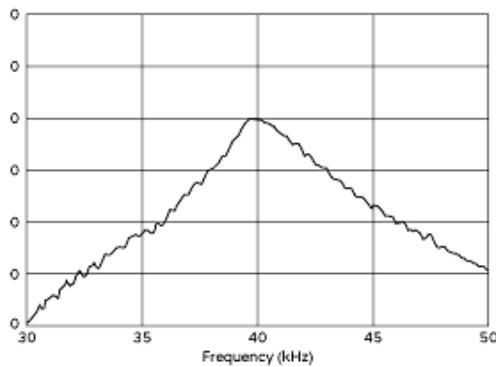


Figure 9: The frequency response of a MA40S4S ultrasonic piezo transdcuer [25].

3.3 Digital Transducer Loudspeaker Array Fundamentals

3.3.1 Concept

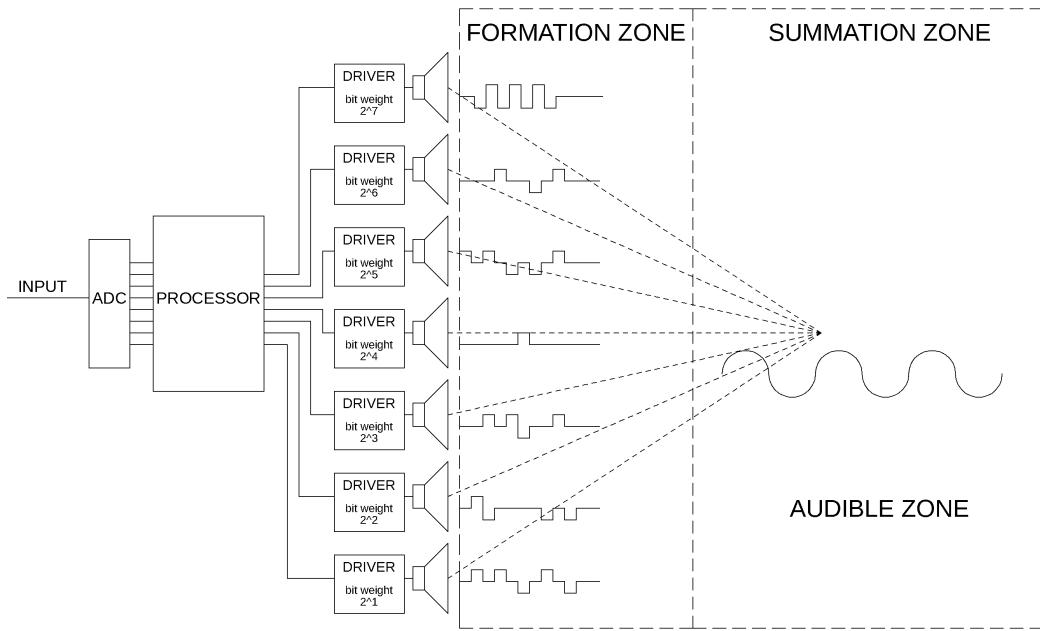


Figure 10: Digital Transducer Array Loudspeaker with beamforming capability.

DTALs are loudspeaker arrays that perform DADAC through a mechanism that digitally encodes a signal and performs a bit-spill operation. A bit-spill operation works by taking an encoded signal and creating multiple signals based on the individual streams of each bit in that signal. These individual bit streams are then weighted to reflect their weighted value in the digital encoded signal they were generated from. Figure 11 shows a double-sided 2-bit signal and the two resulting signals generated from a bit-spill operation.

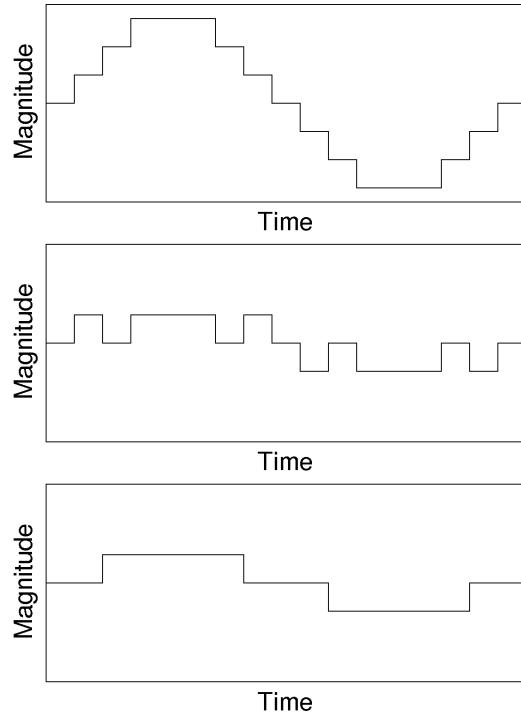


Figure 11: Bit spilled signal example. Top: Double-sided 2 bit signal.
Middle: LSB spilled signal. Bottom: MSB spilled signal

3.3.2 One-Bit-Per-Transducer Configuration

By routing bit-spilled signals to individual weighted amplifiers, it is possible to design a One-Bit-Per-Transducer (OBPT) DTAL. When driving identical transducers with different amplifier magnitudes or pulse widths, an amplifier calibration is required to ensure each transducer group is outputting an accurate SPL that reflects its assigned bit weight.

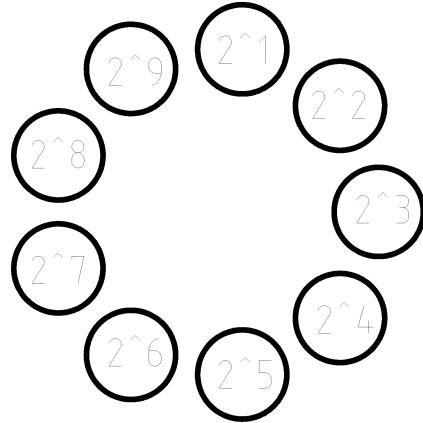


Figure 12: An example of a 10 bit circular OBPT DTAL array that utilises 9 individual transducer elements.

The minimum number of transducers required for the OBPT design is defined by the following equation:

$$n = \text{bitdepth} - 1 \quad (5)$$

Where:

n = minimum number of transducer elements
 bitdepth = input signal bit resolution

Figure 13: Minimum number of transducers required in a One-Bit-Par-Transducer DTAL design

The OBPT design can be scaled in to a One-Bit-Per-Transducer-Group (OBPTG) design by simply increasing the number of transducers available to each bit-weighted amplifier. When trying to add more transducers to the design, the amount of total transducer elements used must be an integer multiple of this number. This is to ensure that the SPL output for each group of transducers maintains the correct weighting.

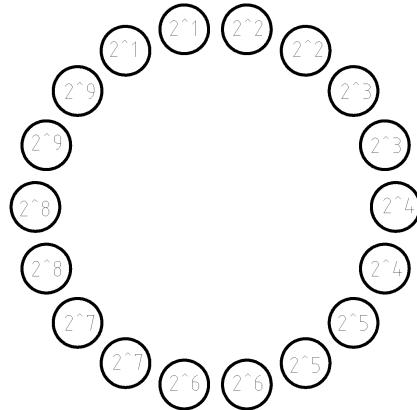


Figure 14: An example of a 10 bit circular OBPTG DTAL array that utilises 18 individual transducer elements. 2 transducer elements share one bit-weighted amplifier.

3.3.3 Acoustic Beamforming

Acoustic beamforming with DTAL devices is possible through the same mechanism described earlier in reference to PLA designs. By adding differing signal delays to individual transducer elements, a phased array can be constructed. This in effect creates a beamforming capable device.

3.4 Proposed Parametric Digital Transducer Loudspeaker Array Design

3.4.1 Concept

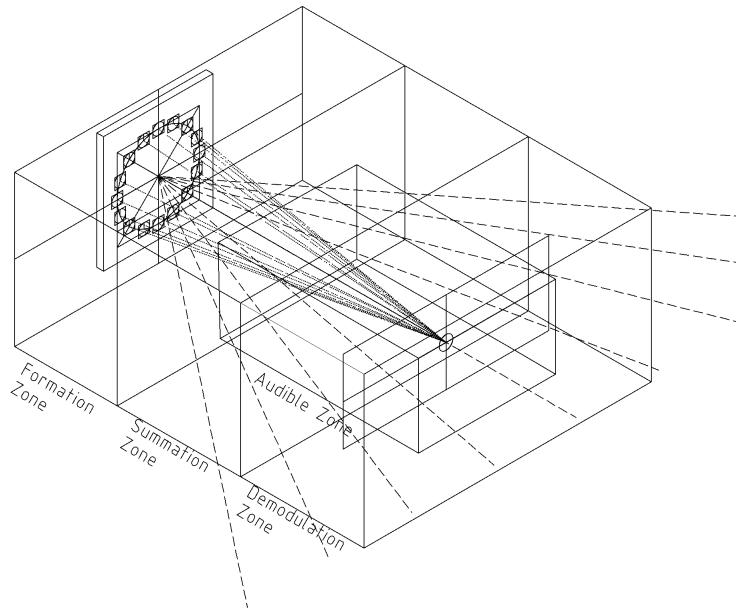


Figure 15: Parametric Digital Transducer Array Loudspeaker with beamforming capability diagram.

The proposed Parametric Digital Transducer Array Loudspeaker (PDTAL) design uses the attributes of both PWMPLA's and scalable OBPTG DTAL's. A PDTAL design performs DADAC with bit-spilled PWM Double-sideband Amplitude Modulated (DSB-AM) ultrasonic input signals that drive an array of ultrasonic piezo transducers arranged in a OBPTG DTAL configuration.

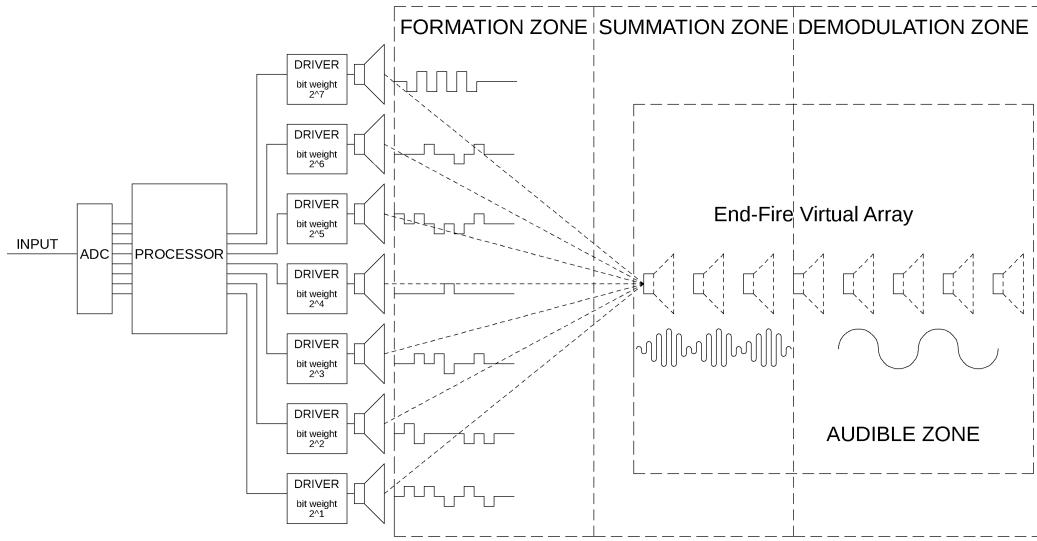


Figure 16: Parametric Digital Transducer Array Loudspeaker with beamforming capability diagram.

Within the design, a digital signal is first modulated with a DSB-AM modulation scheme. A bit-spilling operation is then performed on the modulated signal, resulting in multiple signals that contain individual weighted bit streams. These bit-spilled bit streams are then converted to double-sided PWM signals, before being encoded to a format that is suitable for directly driving H-bridge amplifiers. The H-bridge amplifiers then drive their assigned transducer groups.

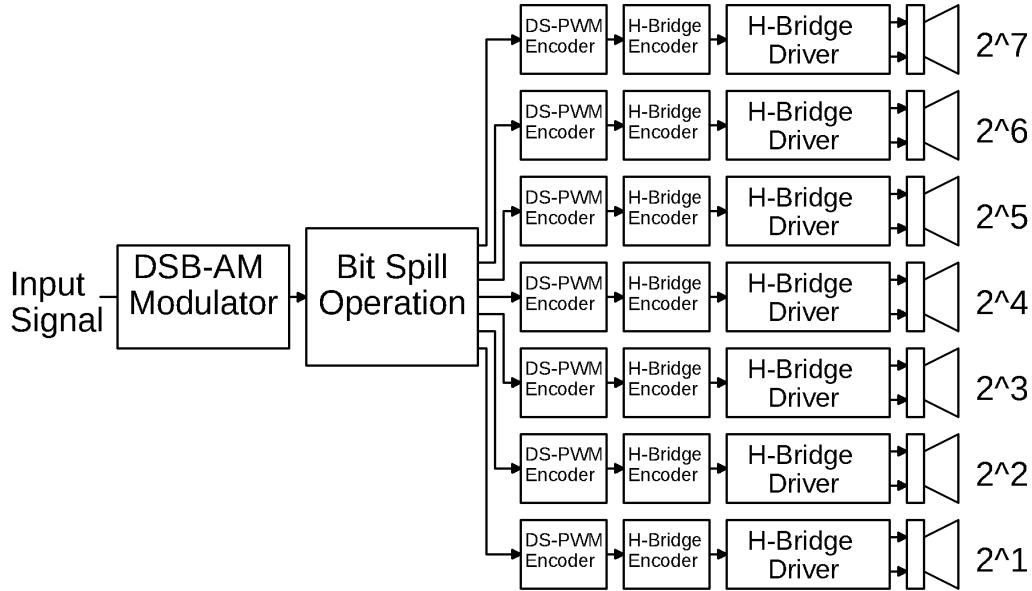


Figure 17: Parametric Digital Transducer Array Loudspeaker block diagram.

The advantages of the proposed PDTAL design are related to additional capabilities, reduced system cost, and reduced circuit complexity compared to that of conventional PLA designs. By utilising H-bridge amplifiers on groups of transducer elements beamforming becomes possible without the use of DACs, reducing overall system cost. Only a single rail power supply for the system is required due to the usage of H-bridge amplifiers, decreasing circuit complexity.

The disadvantages of the proposed PDTAL design include lower audible SPL output than that of conventional PLA designs with the same number of transducer elements. This is due to the weighted amplifier configuration used within the DTAL type design. An 8 bit PDTAL design as per Equation 5 requires at least 7 transducers. The transducer group assigned the most significant amplifier weight will be the only transducer emitting its maximum possible SPL. While other transducer groups will output less SPL than is possible based on their individual bit-weight assignment. The following equation describes the multiple of transducers required for a PDTAL design to produce the same amount of audible SPL as a conventional PLA design:

$$k = \frac{n - 1}{2} \quad (6)$$

Where:

k = Multiple of transducers required.

n = Number of transducers in similar PLA design.

Multiple of transducers required for PDTAL and PLA designs to produce the same SPL output

In the case of a 8 bit design, a PDTAL requires 3.5 times the transducers as that of a conventional PLA or design. In a 16-bit design, this increases to a multiple of 7.5. Finally, Due to the utilisation of PWM signals to directly drive the transducer groups higher THD and lower SNR is to be expected compared to conventional PLAs.

3.4.2 Design Considerations

PWM Phase Coherency For the proposed PDTAL design to function correctly, the output from each H-bridge driver in the system must have the same phase response. Phase differences have the potential to cause imperfect summation of output signals in air. This could result in lower SPL output, higher THD, and lower SNR. In order to achieve different SPL output levels for the different transducer groups in the PDTAL design, various PWM duty cycles are utilised. Without phase compensation, these different duty cycles cause phase delays that may hinder the performance of a PDTAL.

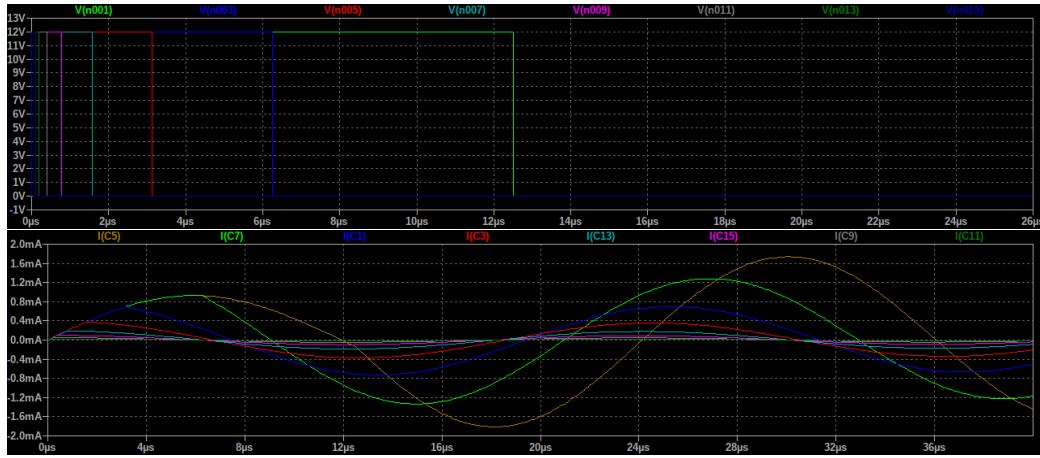


Figure 18: Simulated PWM signals driving MA40S4S equivalent circuit [26] without phase correction. Top: Input. Bottom: Output

By applying the following equation to each PWM signal, phase coherency can be achieved by correcting the phase delays introduced by differing duty cycles.

$$\tau = \frac{0.5 - \text{duty}}{2mF} \quad (7)$$

Where:

- τ = delay in seconds
- duty = PWM duty cycle (0 to 1)
- mF = PWM modulation frequency

Phase coherence delay equation

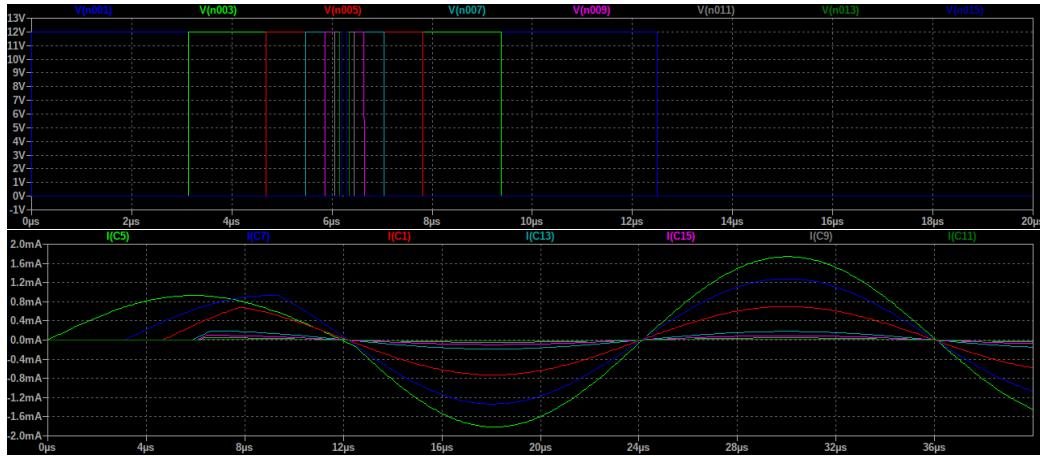


Figure 19: Simulated PWM signals driving MA40S4S equivalent circuit [26] with phase correction. Top: Input. Bottom: Output

PWM Width Calibration As mentioned in Section 3.2.3, transducer SPL output does not correspond in a linear manner with PWM duty cycle. Without PWM width compensation this could result in high THD and lower SNR.

4 Methodology

4.1 PDTAL Prototype System Specification

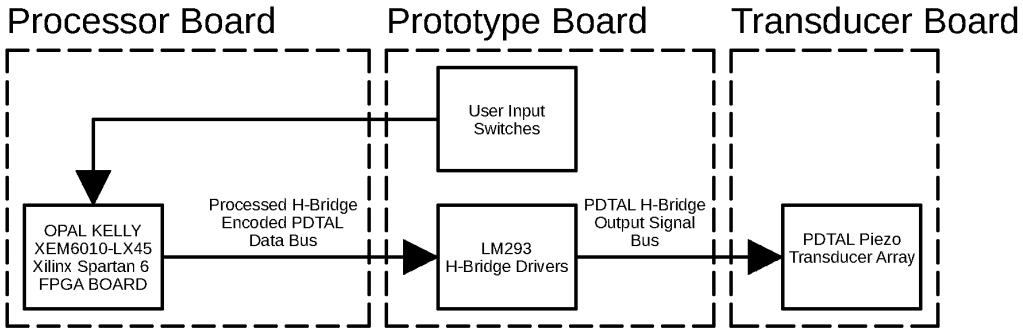


Figure 20: Hardware block diagram of prototype.

To validate the PDTAL design a series of simulations was carried out along with the design, build, and verification of a prototype. A set of design specifications was decided upon in order for any simulations to match to real world measurements as closely as possible. In order to correlate the simulation as closely as possible to the prototype, the system was implemented using VHDL, with all processing being handled by an Opal Kelly XEM6010-LX45 board that utilises a Xilinx Spartan 6 Field Programmable Gate Array (FPGA). Using this VHDL code, accurate simulations were computed using Xilinx's ISE Simulator (ISim) that directly correspond to the prototype implementation. The results of this simulation were then outputted to a Comma-separated Value (CSV) file format where the data could be loaded in to MATLAB for further analysis.



Figure 21: The Opal Kelly XEM6010-LX45 board attached to Opal Kelly BRK6110 breakout board.

The system has an output signed bit resolution of 8. It features a sampling frequency of 97.65625KHz for signal generation, DSB carrier signal generation, and PWM modulation frequency. This allows frequencies up to 48.828125KHz to be accurately reproduced as per Nyquist's theorem. The carrier frequency used in the DSB modulation is 40Khz. The PWM clock frequency is set at 12.5MHz, allowing a 7 bit PWM counter to be used for the generation of the 8 bit double sided PWM.

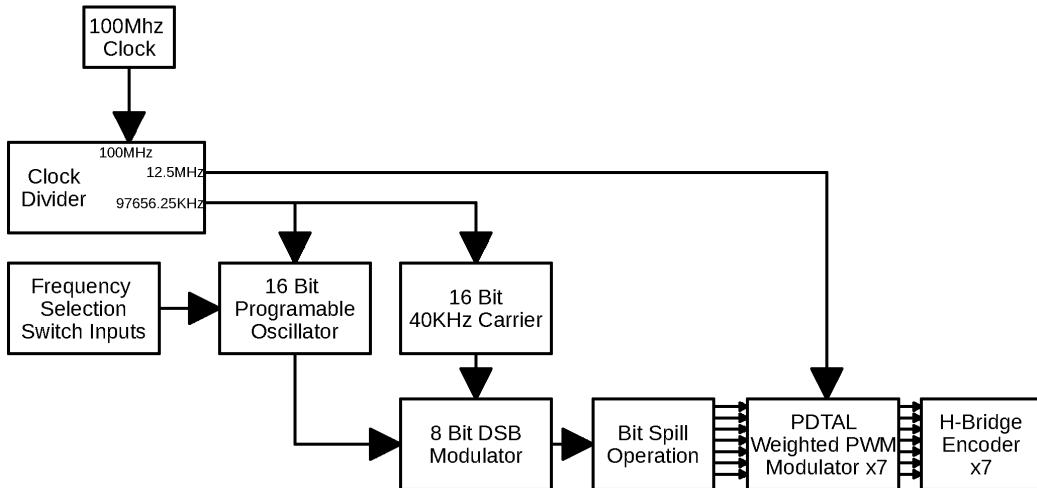


Figure 22: VHDL module block diagram.

The prototype board has an on-board 16 bit programmable digital oscilla-

tor capable producing 50Hz, 100Hz, 200Hz, 400Hz, 800Hz, 1600Hz, 3200Hz, and 6400Hz sinusoidal signals implemented on the Spartan 6 FPGA. The oscillator output frequency is controlled by a 4 way DIP switch. DSB modulation is performed on the FPGA, as well as the necessary bit-spill operation, weighted PWM encoding, and H-bridge encoding.

In line with Equation 5, A 28 transducer element array is used with 4 Murata MA40S4Ss in each transducer group. A circular array geometry is used in the array design, with transducer element groups placed next to each other. Transducer elements within each transducer group are connected in parallel, before being driven by the transducer group assigned H-bridge driver.

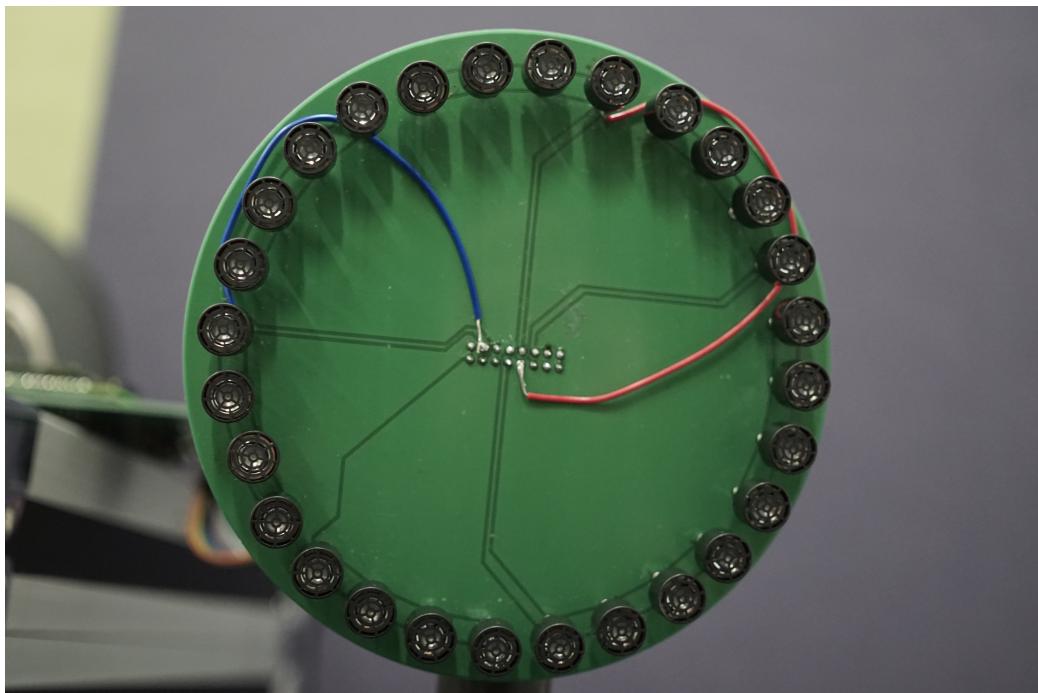


Figure 23: PDTAL speaker prototype utilising 28 MA40S4S piezo transducers in 7 transducer groups.

An array of H-bridge amplifiers will be used to drive both transducer arrays, enabling double-sided modulation schemes for the PDTAL design with-

out the requirement of a dual-rail power supply. The use of H-bridge drivers will also eliminate the need for any form of digital-to-analog conversion. By using this configuration, the elimination of DACs will reduce the cost of the project, while still providing powerful and affordable beamforming capability.

The H-bridge driver that will be used to drive the individual transducer groups in the prototype is a Texas Instruments LM293.

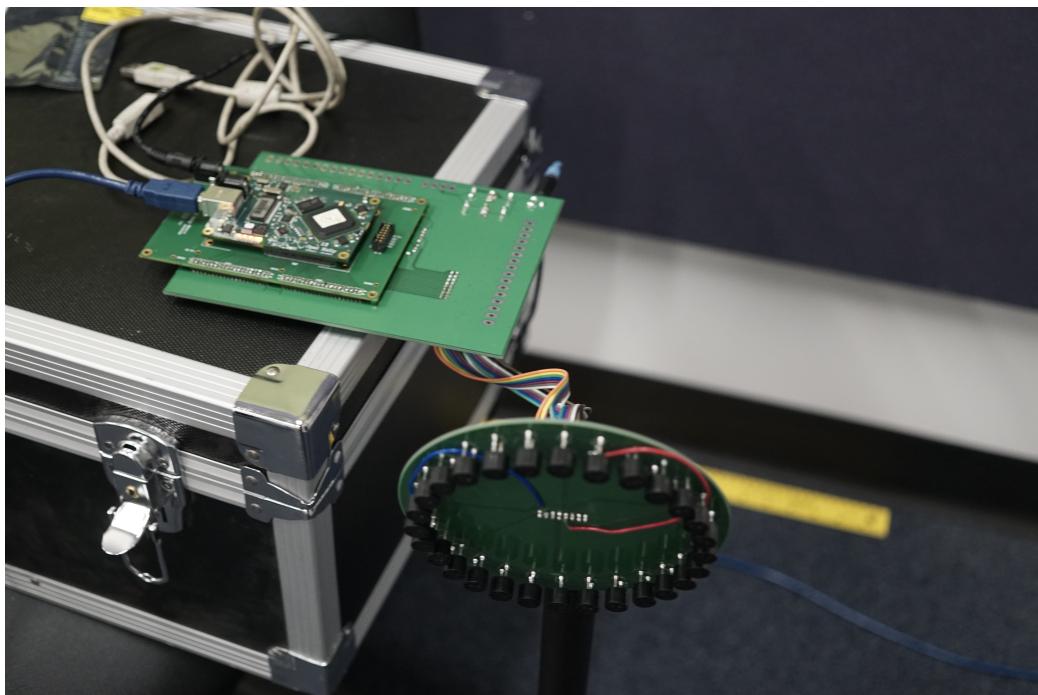


Figure 24: PDTAL prototype including Opal Kelly XEM6010-LX45 board, mother board PCB with H-bridge drivers, and loudspeaker array components.

4.2 Simulation

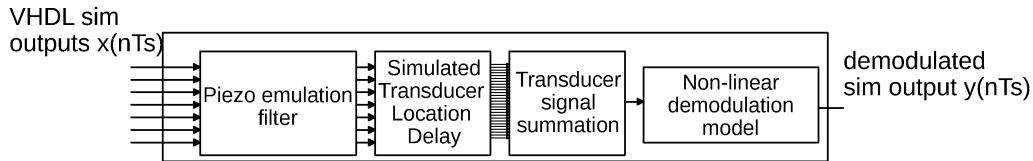


Figure 25: Simulation block diagram

To simulate the design, 7 individual double-sided PWM outputs destined for driving transducer groups are outputted to a CSV format when conducting VHDL module simulations using ISim. These signals are then loaded into MATLAB where further processing takes place to complete the simulation. This further processing includes a piezo transducer emulation filter, transducer location delay calculation, transducer signal summation, and the application of a non-linear demodulation model that simulates the demodulation of the ultrasonic signals in air.

4.2.1 Piezo Transducer Emulation Filter

A piezo transducer emulation filter was developed to try and replicate the real world response of a MA40S4S ultrasonic transducer. An IIR filter was designed using MATLAB's `designfilt` function that closely follows the frequency response of that published on the MA40S4S datasheet. This filter is then applied to each bit-spilled double-sided PWM signal generated from the simulation of the system VHDL modules.

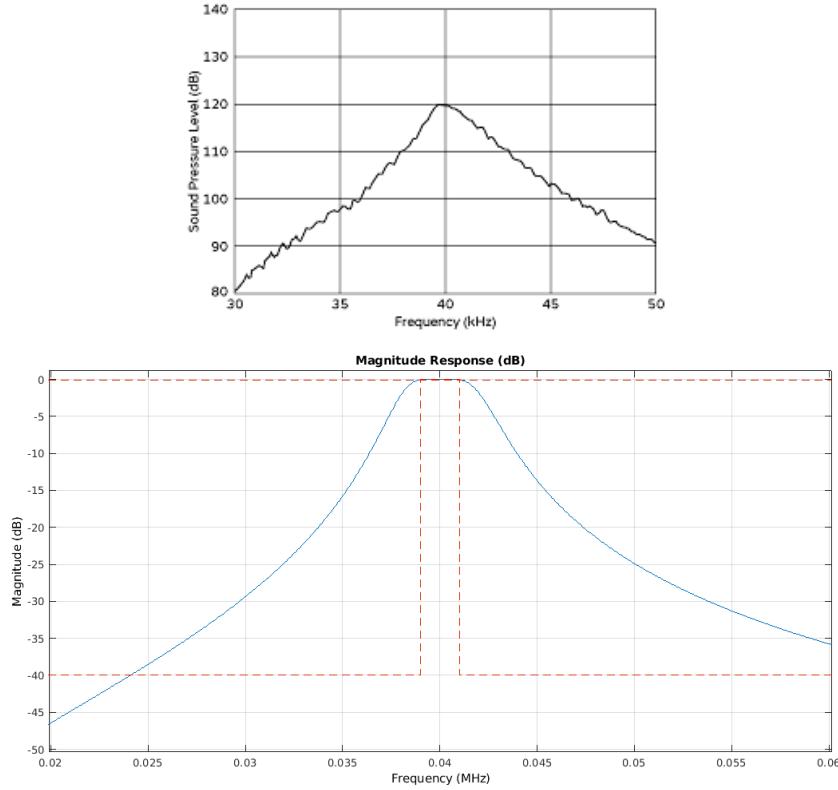


Figure 26: Top: Transducer response from MA40S4S datasheet [25].
 Bottom: Piezo transducer emulation filter response used in MATLAB simulation.

4.2.2 Transducer Location Delay Compensation

A transducer location delay compensation scheme is used to calculate the time it takes for an acoustic signal to travel from a transducers location to a point in space. Path differences between transducer elements are the main cause for high overall THD in DTAL type designs such as the PDTAL [6][7][8], thus it is important to simulate these path differences between transducers. Each transducer group PWM signal is routed through individual transducer location delay modules.

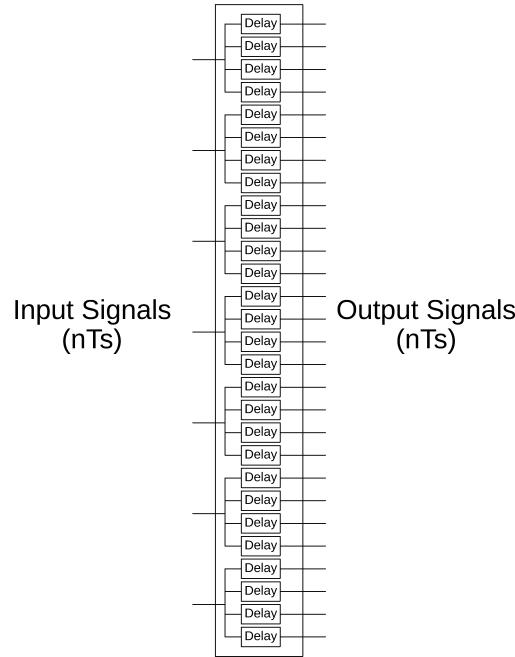


Figure 27: Transducer origin-to-listening-point delay calculation block diagram.

Equation 8 shows the calculation for defining the distance between a transducer and a specific location in space.

$$p_d = \sqrt{(p_x - o_x)^2 + (p_y - o_y)^2 + (p_z - o_z)^2} \quad (8)$$

Where:

p_d = Distance from transducer to measuring position

p_x = x coordinate of measuring position in space

p_y = y coordinate of measuring position in space

p_z = z coordinate of measuring position in space

o_x = x coordinate of transducer in space

o_y = y coordinate of transducer in space

o_z = z coordinate of transducer in space

Distance from transducer to measuring position equation

This distance must be converted to a time delay that can be applied to the transducer group PWM signals. Equation 9 can be used to calculate the time delay.

$$d = \frac{p_d}{343m/s} \quad (9)$$

Where:

d = Signal travel time delay in seconds

p_d = distance from transducer to measuring position

Time from transducer to measuring position equation

The transducer element positions as defined by the prototype PCB were used to generate the plots shown in Figure 29 utilising MATLAB. By using these coordinates and the equations 8 and 9, a matrix of individual transducer path delays were generated for on-axis and off-axis listening path positions located 300 millimetres away from the centre of the transducer array. This matrix of delays was used to add delays to the transducer group PWM signals generated from VHDL module simulation after piezo transducer emulation filters were applied.

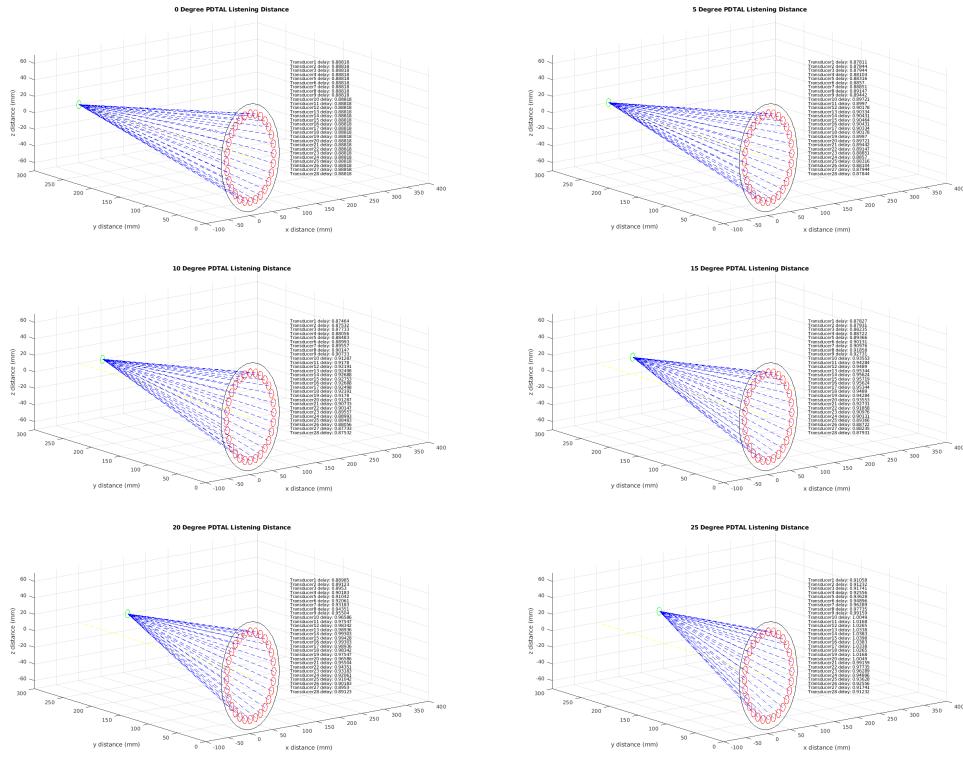


Figure 28: MATLAB generated images showing the transducer delay calculation position used for simulation purposes.

4.2.3 Transducer Signal Summation

The summation of each transducer signal is necessary to replicate the summation of the individual transducer outputs in air. Figure 29 shows a block diagram that describes this process.

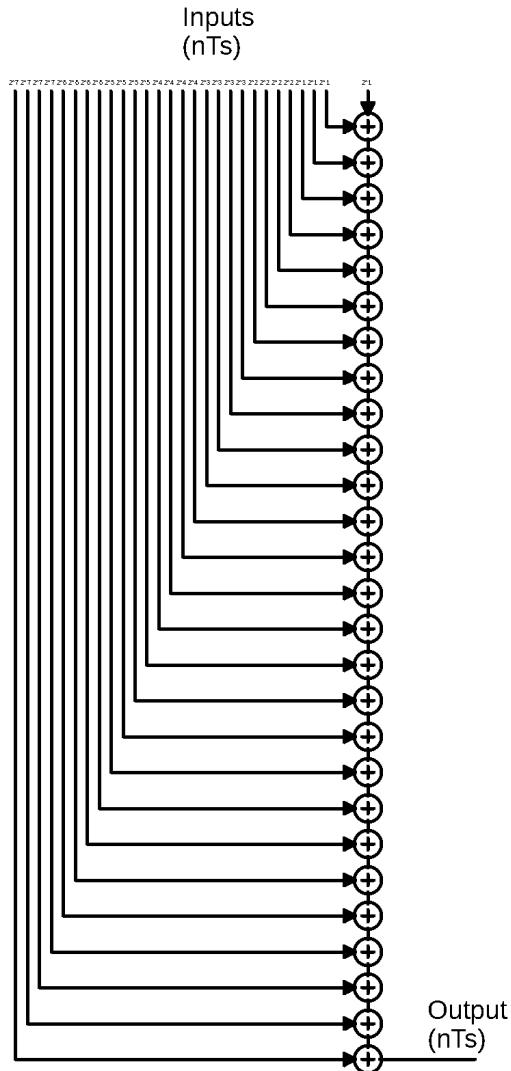


Figure 29: Transducer signal summation block diagram.

4.2.4 Non-linear Demodulation Model

The non-linear demodulation simulates the demodulation of ultrasonic signals in air as per Merklinger's solution [23]. This model includes the second order differentiation and squaring of the signal. Finally, DC components from the result signal are removed.

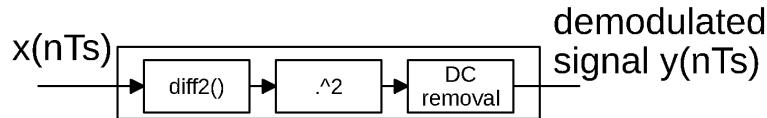


Figure 30: Simulation demodulation software block diagram

4.2.5 Parametric Loudspeaker Array Comparison Simulation

In order to gain comparison data of PDTAL and PLA designs, a PLA simulation was also conducted using message and carrier signal data generated from the VHDL module simulations. DSB modulation was performed in MATLAB using this data, as well as the application a piezo emulation filter and non-linear demodulation model.

4.3 Design and Performance Criteria

The design and performance criteria of the prototype will focus on SPL output, frequency response, THD, SNR, directivity of output, and beamforming capability. The design should have an audible output 300 millimetres away from the device. The frequency response should be reasonably linear across frequencies in the range of 1kHz to 5kHz. The THD should remain under 50%, and not significantly increase at off-axis positions compare to DTAL type designs. A sharp directivity pattern should be recognisable at the output of the device.

4.4 Design Validation, Measurement, and Verification

In order to measure and verify the design prototype, a series of acoustic measurements were conducted. A GRAS 40BF microphone capsule was used with a GRAS 26AC capsule preamplifier and GRAS 12AA power module. The system was calibrated using a GRAS 42AA pistonphone. To allow the analysis of the measurement data, a Brüel & Kjær ZE0948 audio interface was used as an analog-to-digital converter (ADC) and interface between the microphone and a computer. The Room EQ Wizard software was used as a real time analyser to view the measurements. CSV data was produced using this software, that could then be imported in to MATLAB.



Figure 31: Pistonphone 42AA used for calibration, and ZE0948 audio interface used for measurements.

Measurements were performed in a quiet, but not anechoic room. They were conducted 300 millimetres away from the device. To measure the specified performance criteria, the prototype board was measured when producing sinusoidal signals with frequencies of 50H, 100Hz, 200Hz, 400Hz, 800Hz, 1600Hz, 3200Hz, and 6400Hz. Frequency response, THD, and SNR data was calculated from this data when possible. Due to the excessive ambient noise conditions encountered in the room where measurements took place, as well as the low SPL emitted from the PDTAL prototype, accurate off-axis measurements were not possible. Finally, the measurements were compared against the generated simulation data.

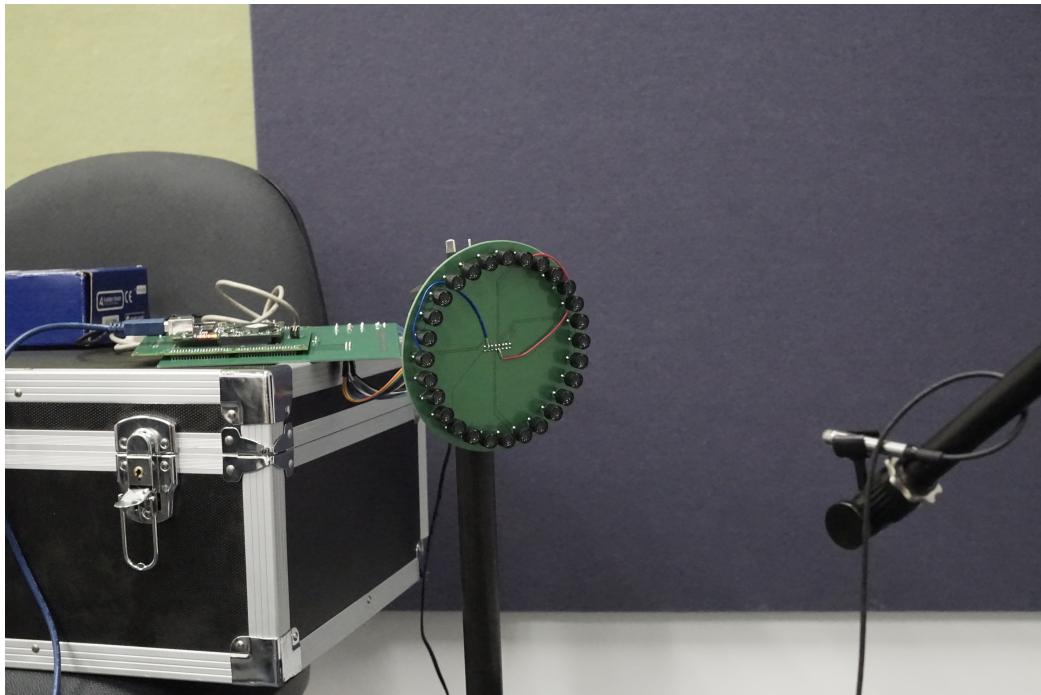


Figure 32: PDTAL prototype characterisation setup.

5 Findings

5.1 Simulation Results

Figure 33 shows time and frequency domain results from the summation of 800Hz VHDL simulated double-sided PWM signals that have been filtered with piezo transducer emulation filters at on-axis and off-axis positions.

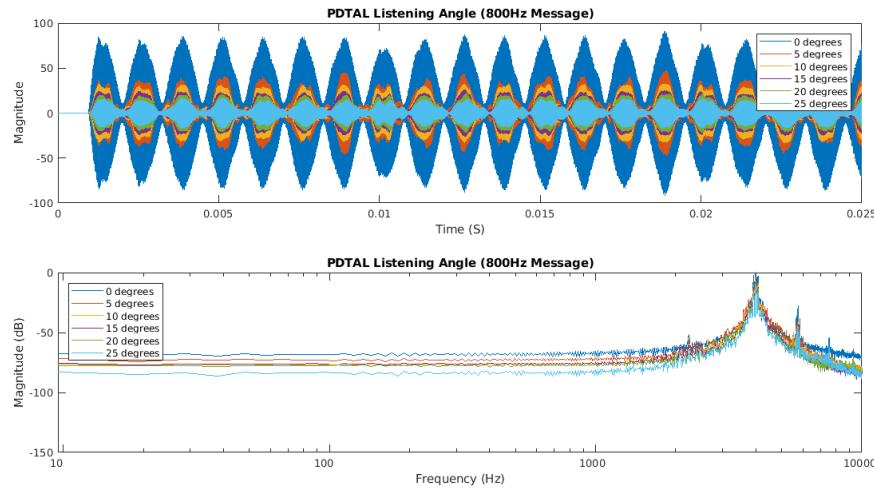


Figure 33: Relative listening position frequency response analysis of VHDL produced 800Hz PDTAL DSB signal.

Figure 34 shows time and frequency domain results from the summation of 800Hz VHDL simulated double-sided PWM signals that have been filtered with piezo transducer emulation filters with subsequent demodulation with a non-linear demodulation model at on-axis and off-axis positions.

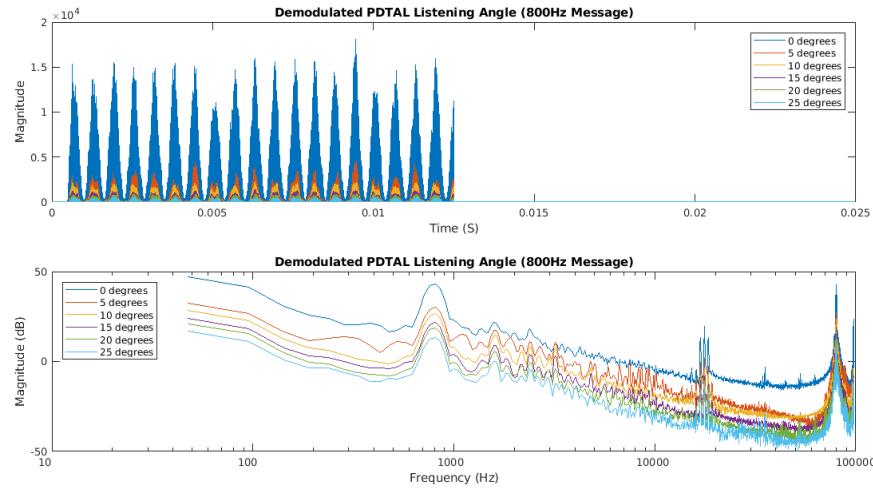


Figure 34: Relative listening position frequency response analysis of simulation demodulated VHDL produced 800Hz PDTAL DSB signal.

Using the data from the previous two simulations, relative SPL output for each simulated listening position can be calculated. Figure 35 shows both PDTAL and PLA simulated SNR and relative SPL output across a variety of listening angles. From these plots it can be noted that the simulated PDTAL has a slightly larger directivity pattern than that of the simulated PLA. PLA SNR does not change as the listening position moves to off-axis areas, while PDTAL SNR decreases rapidly.

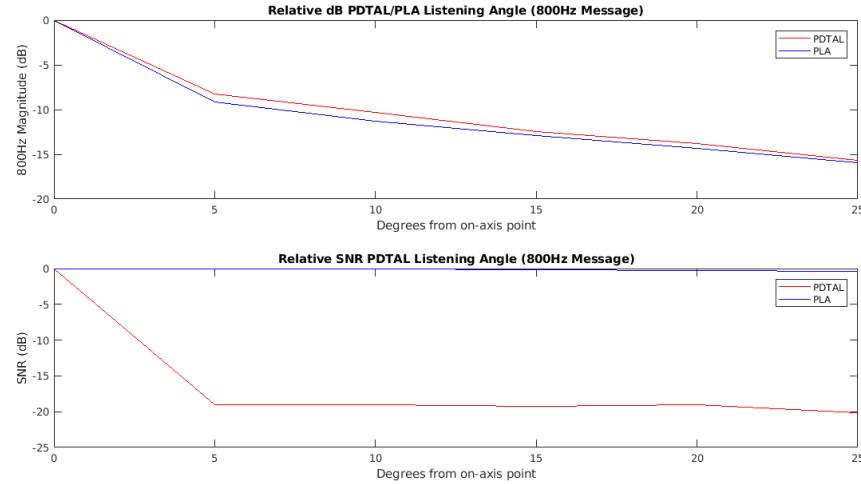


Figure 35: Relative listening position magnitude and SNR analysis of simulation demodulated VHDL produced 800Hz PDTAL DSB signal.

Relative THD and overall THD levels were also calculated from the previous simulations. Figure 36 shows both PDTAL and PLA simulated THD and relative THD values across a variety of listening angles. From these plots it can be noted that the simulated PDTAL has a relative THD increase between 15% and 20% at off-axis positions, while PLA THD does not increase at off-axis positions. Despite this, the simulated PDTAL produces significantly lower THD at on-axis listening positions compared to that of the simulated PLA.

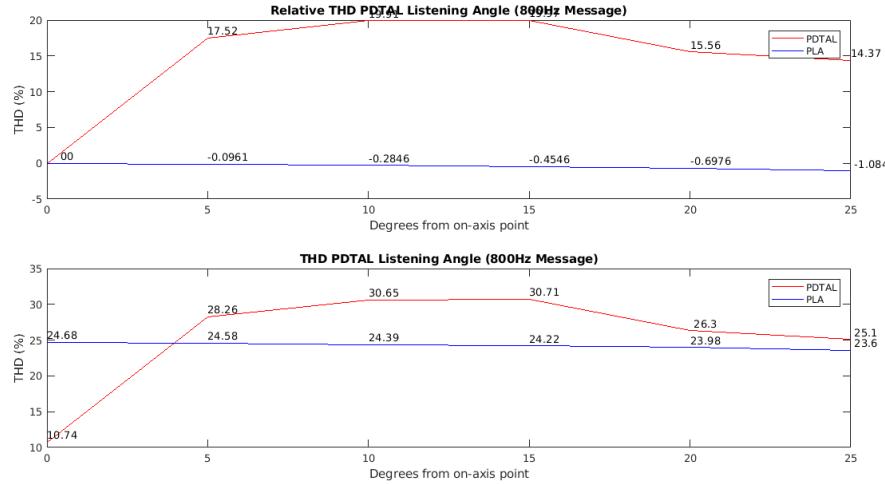


Figure 36: Relative listening position THD and relative THD simulation demodulated VHDL produced 800Hz PDTAL DSB signal.

Further results from simulations with message signal frequencies of 50Hz, 100Hz, 200Hz, 400Hz, 1600Hz, 3200Hz, and 6400Hz can be found in the Appendix in Section 9.

5.2 Laboratory Measurements

Figure 37 shows the frequency domain measurement of the PDTAL prototype with an input message signal of 800Hz. The ambient room noise is also displayed. It can be observed that strong second order harmonics exist.

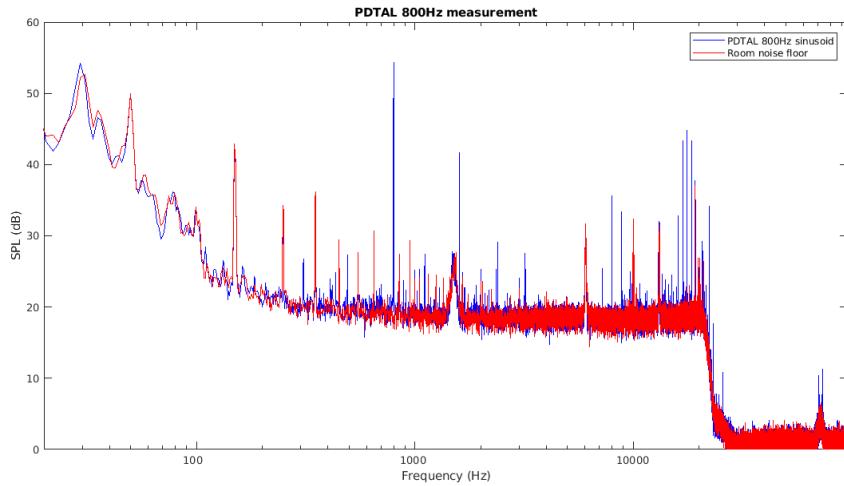


Figure 37: Frequency response analysis of system measurement with 800Hz input signal.

Figure 38 shows the frequency domain measurement of individual transducer groups as well as the summation of all transducer groups within the PDTAL prototype when using an input message signal of 800Hz. It can be noted that due to the ambient noise within the room and the low SPL output, only 3 individual transducer groups could be accurately measured. Each transducer group is ideally able to produce a demodulated message signal that is 3dB less than that of its next weighted transducer group. From these 3 transducer groups, it can be observed that due to a lack of PWM width calibration, this is not occurring. This is likely resulting in higher THD than if a calibration was performed.

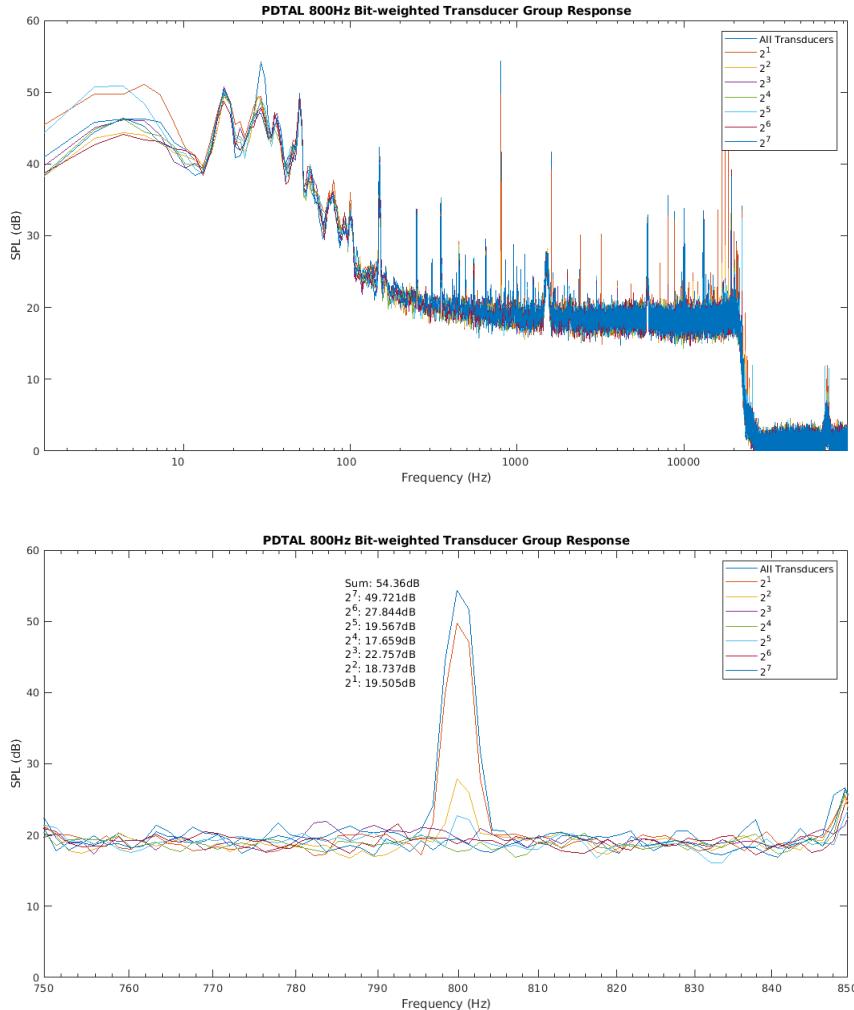


Figure 38: Frequency response analysis of individual transducer groups with 800Hz input signal.

Figure 39 shows the THD breakdown of both the summation of all transducer groups, and individual transducer groups within the PDTAL prototype when using an input message signal of 800Hz. It can be noted that due to the ambient noise within the room and the low SPL output, only THD for the 2 most significant transducer groups could be accurately calculated. It can be observed that despite the lack of PWM calibration, THD for the summation of the transducer groups decreases as new transducer groups are added.

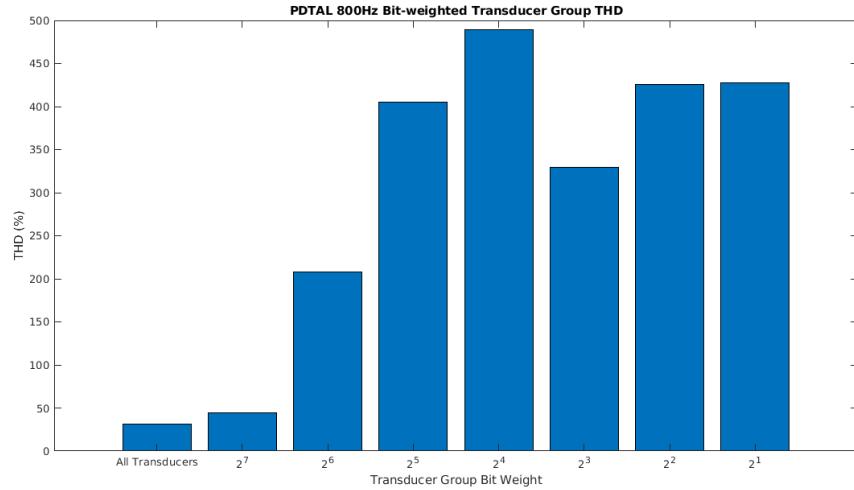


Figure 39: THD analysis of individual transducer groups with 800Hz input signal.

Figure 40 shows the frequency response of the system as taken over a number of measurements. A $6dB_{SPL}$ per octave low pass filter with a 900Hz roll off frequency can be observed.

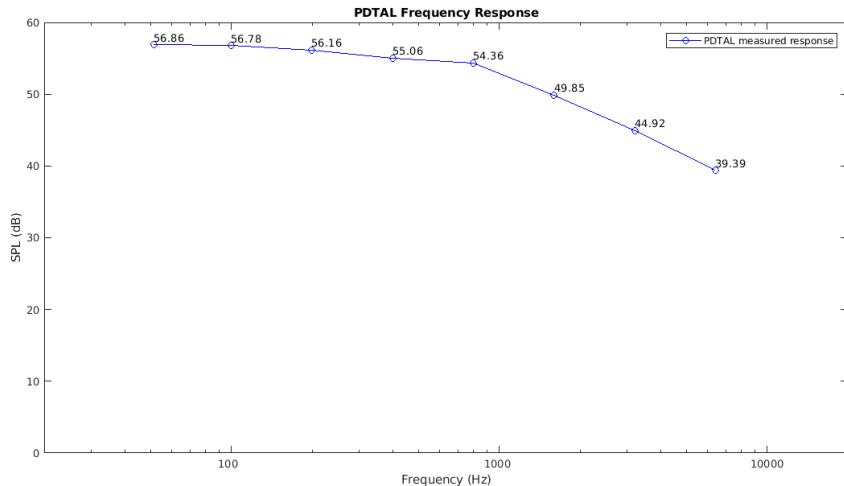


Figure 40: Frequency response of system.

Figure 41 shows THD against output frequency of the PDTAL prototype. THD generally decreases as output frequency increases, except for frequencies above 6KHz. The cause of this is most likely due to PWM harmonics causing aliasing within the system.

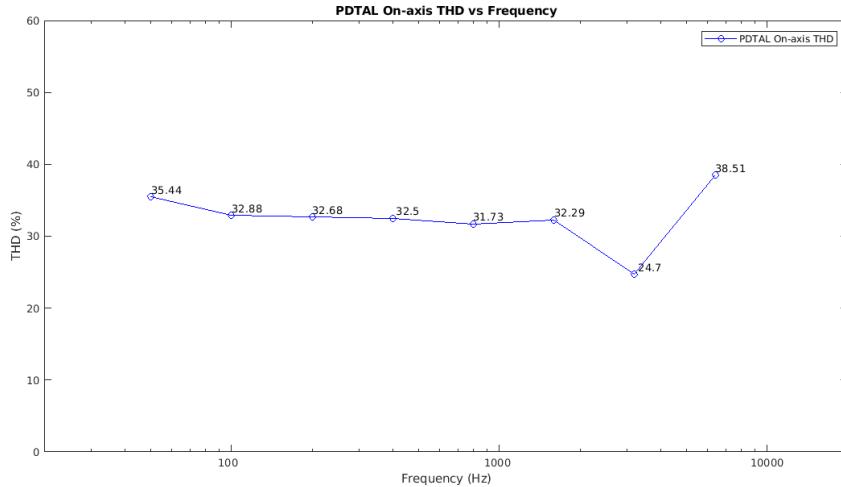


Figure 41: THD against frequency of system.

Further results from laboratory measurements with message signal frequencies of 50Hz, 100Hz, 200Hz, 400Hz, 1600Hz, 3200Hz, and 6400Hz can be found in the Appendix, Section 9.

6 Discussion

By analysing the simulation and measurement data, the following conclusions can be made. THD calculated in the simulation appeared significantly higher than that of the THD calculated from the real world measurements at lower frequencies, and significantly lower at higher frequencies. Despite this, the simulated and real world measurements still correlate reasonably well. Some possible explanations for this discrepancy include lack of PWM width calibration, and the failure of the simulation to take in circuit considerations such as H-bridge driver performance and piezo transducer tolerances. Due to this, flaws in the simulation design are likely to exist. Despite the lower simulated THD, the real world calculated PDTAL THD performs similarly to that of PLA design that utilise DSB modulation with high modulation indexes [14]. It is highly likely that switching to SSB modulation would reduce the THD of the PDTAL design significantly. In addition, performing PWM width calibration would also likely reduce THD.

Due to the high ambient noise that existed within the room where measurements took place, it was not possible to measure the SNR and off-axis THD performance of the PDTAL design. However, data gained through simulation suggests that the THD of PDTAL devices increases between 15 and 20 percent in off-axis positions. This is significantly less off axis THD increase than comparable DTAL designs [27] [28]. This higher THD in off-axis positions can be considered inferior to conventional PLA designs, as off-axis THD does not increase in off-axis positions with conventional PLA designs. Data gained through simulation also suggests that the SNR of PDTAL devices lowers significantly in off axis positions. This is in contrast to PLA design where SNR remains constant in off-axis positions.

The simulated frequency response closely matches the frequency response of the prototype. The device has a flat frequency response until 900Hz where a 6dB per octave slope can be observed. This slope is due to the narrow frequency response of the MA40S4S piezo transducer. To extend the high frequency performance of the PDTAL design, a transducer with an extended frequency response should be used. The design appears to be able to produce low frequency signals with frequencies as low as 50Hz. Due to the second order differentiation present in Merklinger's solution [23], a high pass like filter is present during demodulation, usually preventing the reproduction of

signals below 500Hz in PLA type designs [14][11][13]. One possible explanation for the ability of the PDTAL design to reproduce these low frequencies is that higher frequency distortion harmonics produce a beat frequency that is equal to fundamental frequency of the message signal. Regardless, the ability of the PDTAL design to reproduce these low frequencies can be considered a positive design attribute over conventional PLA designs.

Based on these observations, it can be concluded that the THD performance of the PDTAL design using DSB modulation is comparable to PLA and DTAL designs in on-axis positions. Low frequency performance appears to exceed that of PLA designs. Off axis THD and SNR performance from simulations indicate that PDTALs exceed the performance of DTAL type designs, while PLA type designs may exceed the performance of PDTAL designs. This performance compromise may be deemed acceptable for the lower system cost and beamforming capability included in PDTAL type designs.

7 Conclusion

This report has presented a unique variant type design that combines the design attributes of both PLA and DTAL designs. The PDTAL aims to incorporate beamforming ability in a cost-effective manner to PLA type designs by eliminating the use of DACs and complex amplifier circuitry. This becomes possible by driving transducer elements with digital signals directly from H-bridge amplifiers. The PDTAL design uses design attributes from DTALs by driving transducers with digitally modulated signals that have been separated into weighted bit streams.

The validity of the design was confirmed by simulation, and by the construction, testing, and verification of a prototype. It was found that PDTAL designs produce similar THD to conventional PLA and DTAL designs in on axis positions when using DSB modulation with high modulation indexes. Low frequency performance of PDTAL designs is significantly better than that of PLA type designs. Through simulation it was found that off-axis SNR and THD performance was better than DTAL type designs, but worse than PLA type designs. This performance compromise may be deemed acceptable for the lower system cost and beamforming capability included in PDTAL type designs.

8 Future Work

8.1 Off-Axis Verification and Characterisation

Due to the high ambient noise present where the measurements were conducted on the prototype, it was impossible to measure the off-axis performance of the PDTAL design. Off-axis performance is potentially significantly superior to that of DTAL type designs, and it is important that it is characterised. By conducting measurements in an anechoic chamber, it would be possible to complete this off-axis verification and characterisation.

8.2 SSB Modulation

The utilisation of SSB modulation in PLA type designs has been shown to dramatically reduce THD in comparison to designs that use DSB modulation [17][18]. By using SSB modulation in a PDTAL type design, it is expected that THD will be far less than what was measured with the current prototype.

8.3 PWM Width Calibration

As shown in Section 3.2.3, ultrasonic piezo transducer output does not respond in a linear manner to varying PWM duty cycle. A PWM width calibration should be performed to ensure that individual transducer groups in PDTAL designs are outputting the correct SPL. Failure to do so will result in higher THD and lower SNR. In the future, a method for performing PWM width calibration should be developed in an attempt to reduce THD and raise SNR.

8.4 Increasing PDTAL SPL Output and Reducing PWM Clock Frequency Requirements

One of the largest disadvantages to the PDTAL design is the extra transducer elements required to produce the same SPL output as a comparable PLA design, and the extremely high PWM clock frequency required when using bit resolutions over 8. Both of these design deficiencies can be overcome by using an alternative numeral system that allows more than one duty cycle to be used per transducer group.

As an example, by having 7 transducer groups that are capable of being driven by 4 duty cycles of 25%, 50%, 75%, and 100%, a bit resolution of 15 can be achieved with a PWM modulation frequency of 97.65625KHz and a PWM clock frequency of 390.625KHz.

$$br = \log_2(N_d^{N_{tg}}) + 1 \quad (10)$$

Where:

br = PDTAL bit resolution

N_d = Number of different duty cycles per transducer group

N_{tg} = Number of transducer groups

Bit resolution of alternate PDTAL design

$$PWM_{cf} = PWM_{mf} N_{tg} \quad (11)$$

Where:

PWM_{cf} = PWM clock frequency

PWM_{mf} = PWM modulation frequency

N_{tg} = Number of transducer groups

PWM clock frequency of alternate PDTAL design

For the PDTAL design used in the construction of the prototype to accomplish similar specifications, a PWM clock frequency of PWM 1.6GHz would be required. The design would also produce much less SPL. When using the alternate design, due to all transducer groups when driven with duty cycles of up to 100%, the output of the PDTAL design will be comparable to a PLA design.

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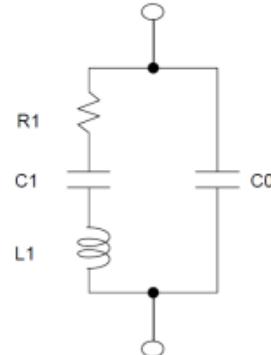
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9 Appendix

9.1 MA40S4S data

3.2 Equivalent circuit



R1:Resonant Resistance.(Serial Resistance)

C1:Serial Capacitance.

L1:Serial Inductance.

C0:pararel Capacitance.

Type	R1(ohm)	C1(pF)	L1(mH)	C0(pF)
MA40S4R	320	300	58	2200
MA40S4S	340	300	48	2150

Fig.3 Equivalent Circuit parameter

Figure 42: MA40S4S equivalent circuit as defined in datasheet. [26].

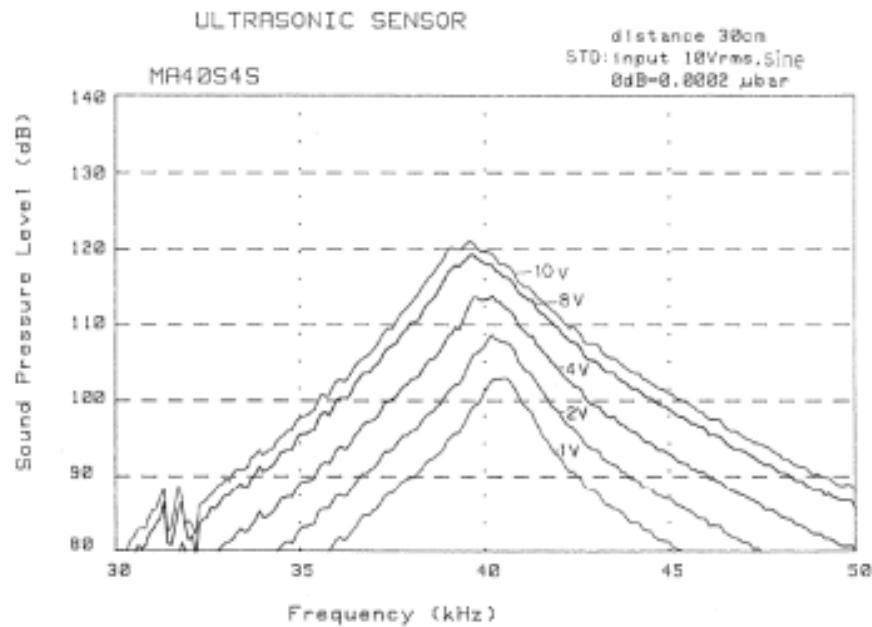


Figure 43: MA40S4S output SPL for different driving voltages as defined in datasheet. [26].

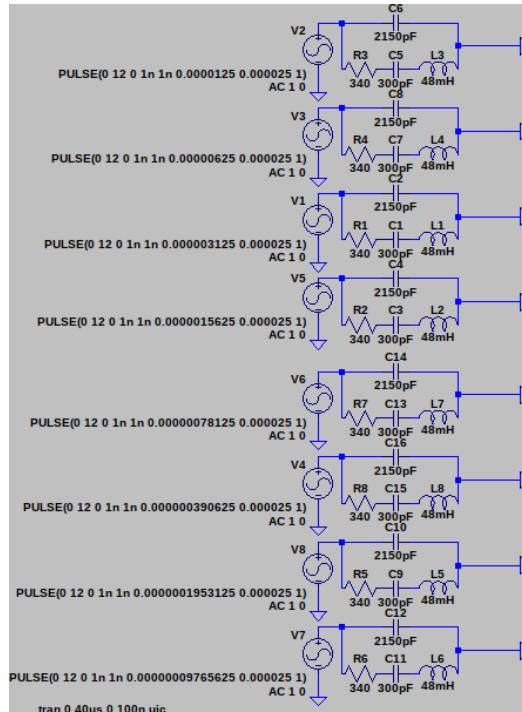


Figure 44: LTSpice circuit used for phase coherency test as described in Section 3.4.2.

9.2 Simulations

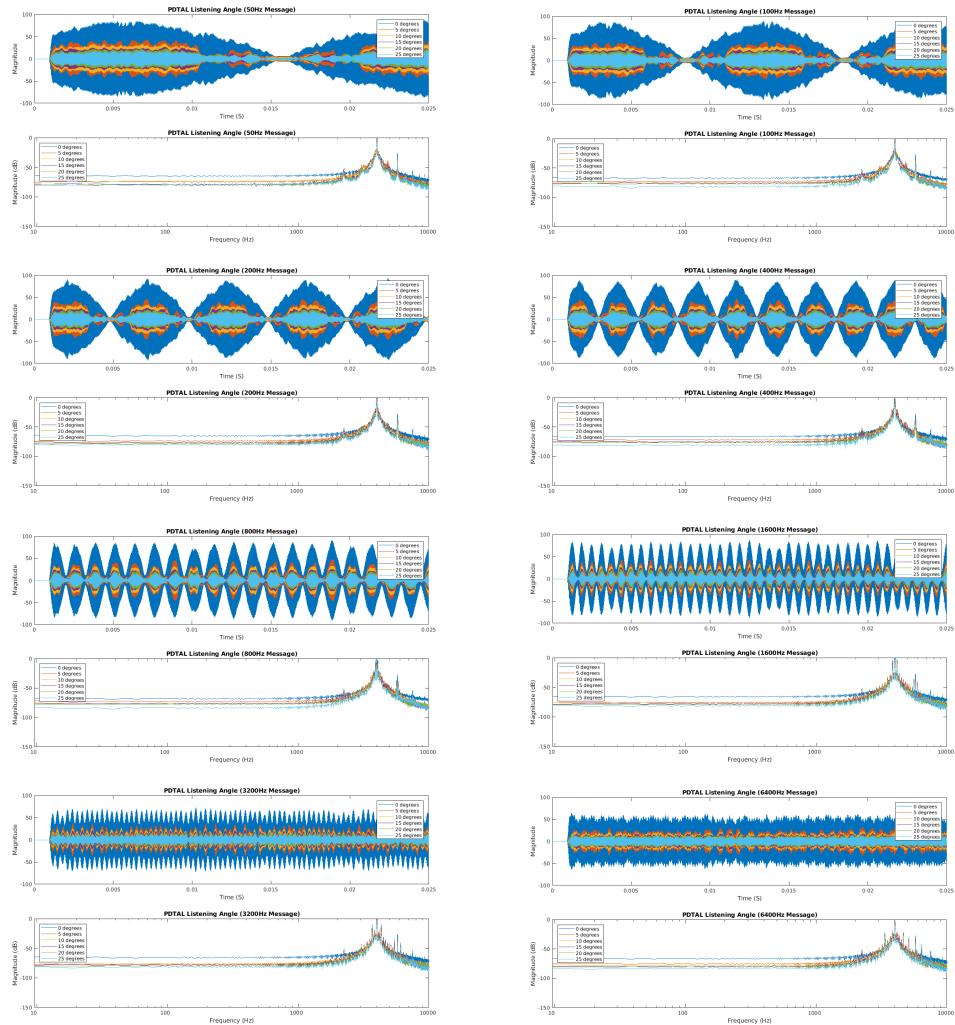


Figure 45: Simulation results for summed PDTAL output signals with different message signal frequencies over a variety of listening positions.

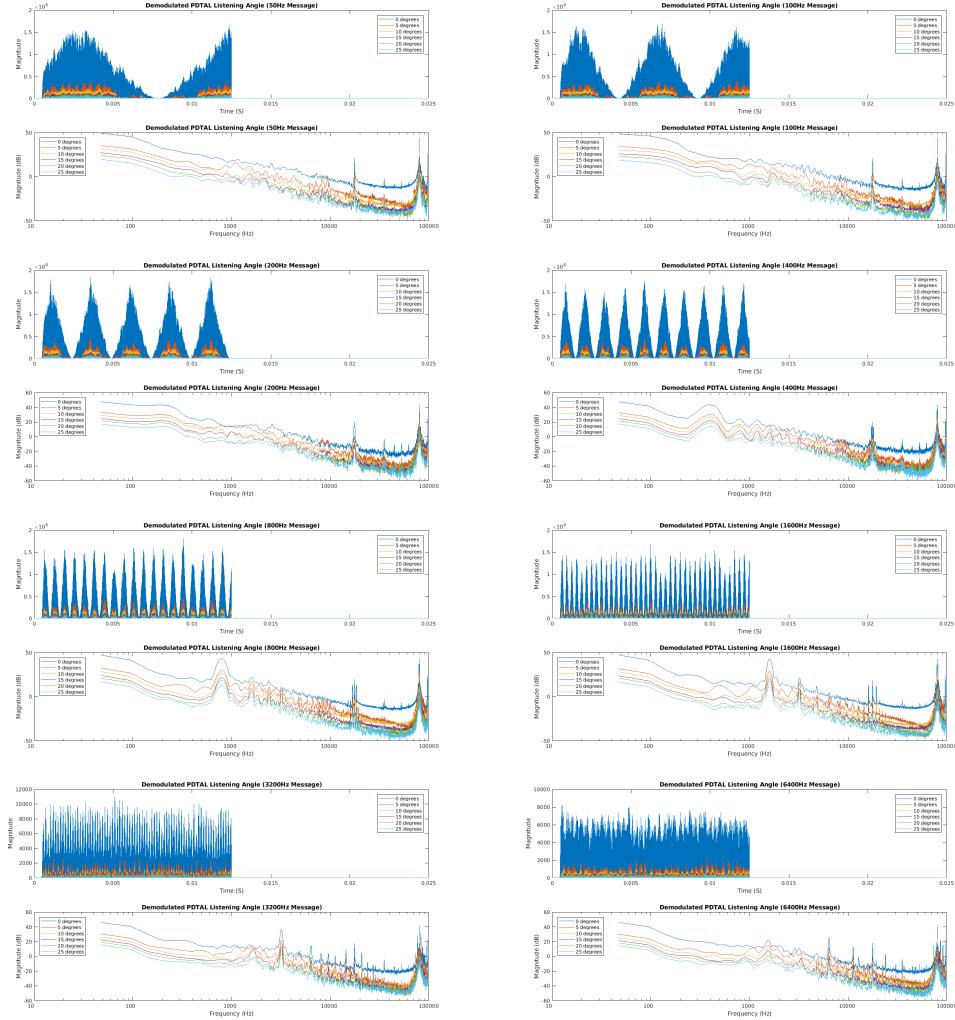


Figure 46: Simulation results for summed demodulated PDTAL output signals with different message signal frequencies over a variety of listening positions.

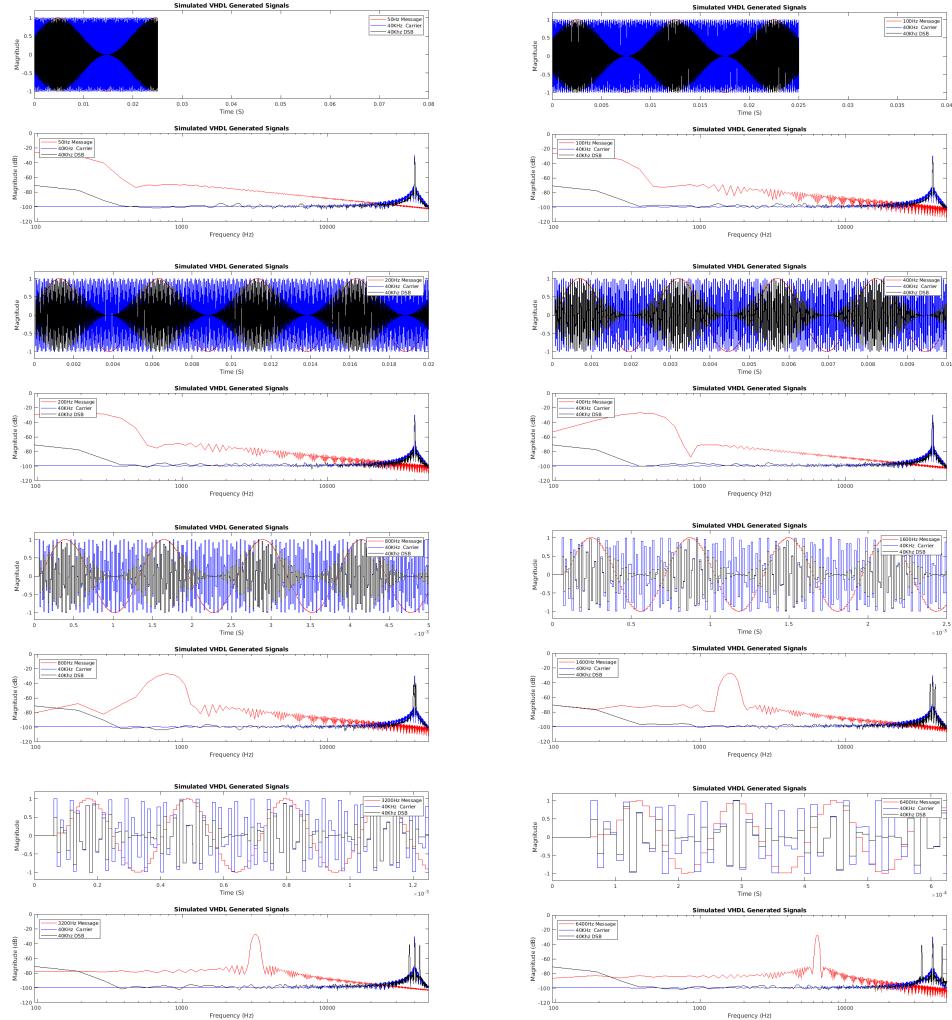


Figure 47: Simulation results for VHDL module generated input and DSB modulated signals with different message signal frequencies.

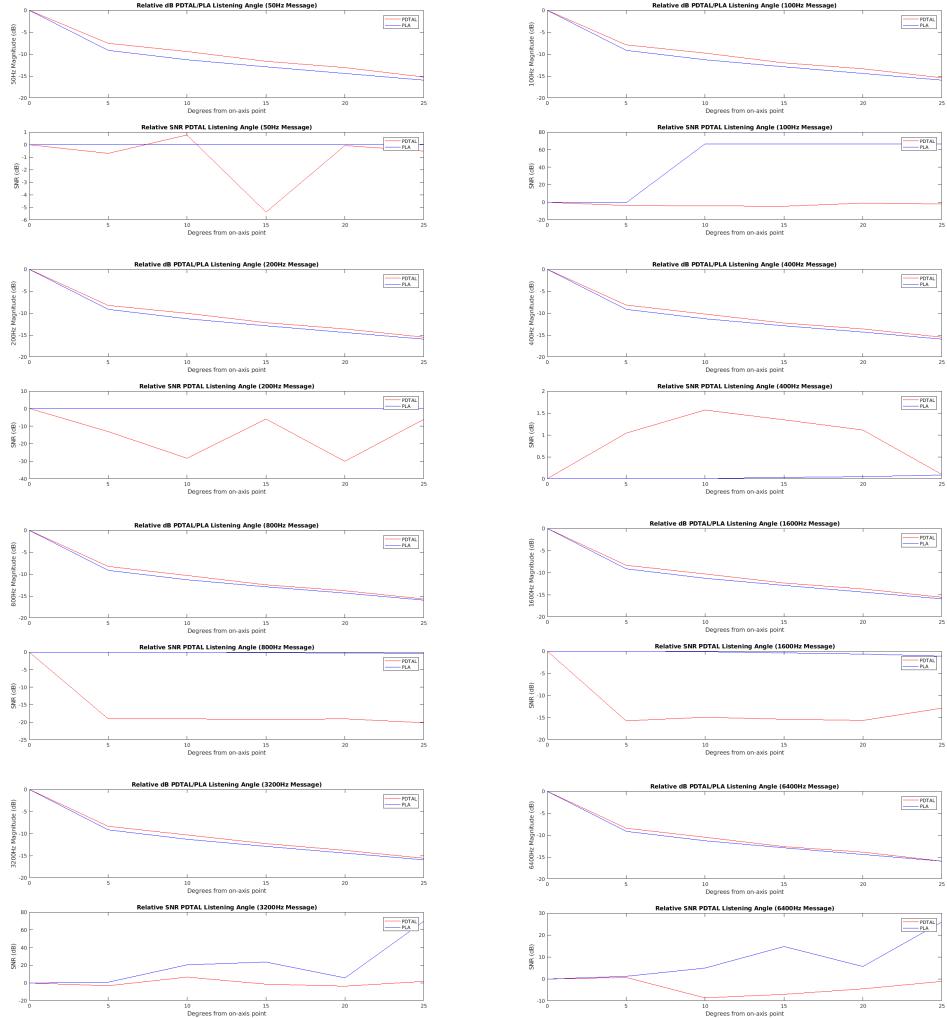


Figure 48: Simulation results for relative magnitude and SNR with different message signal frequencies over a variety of listening positions.

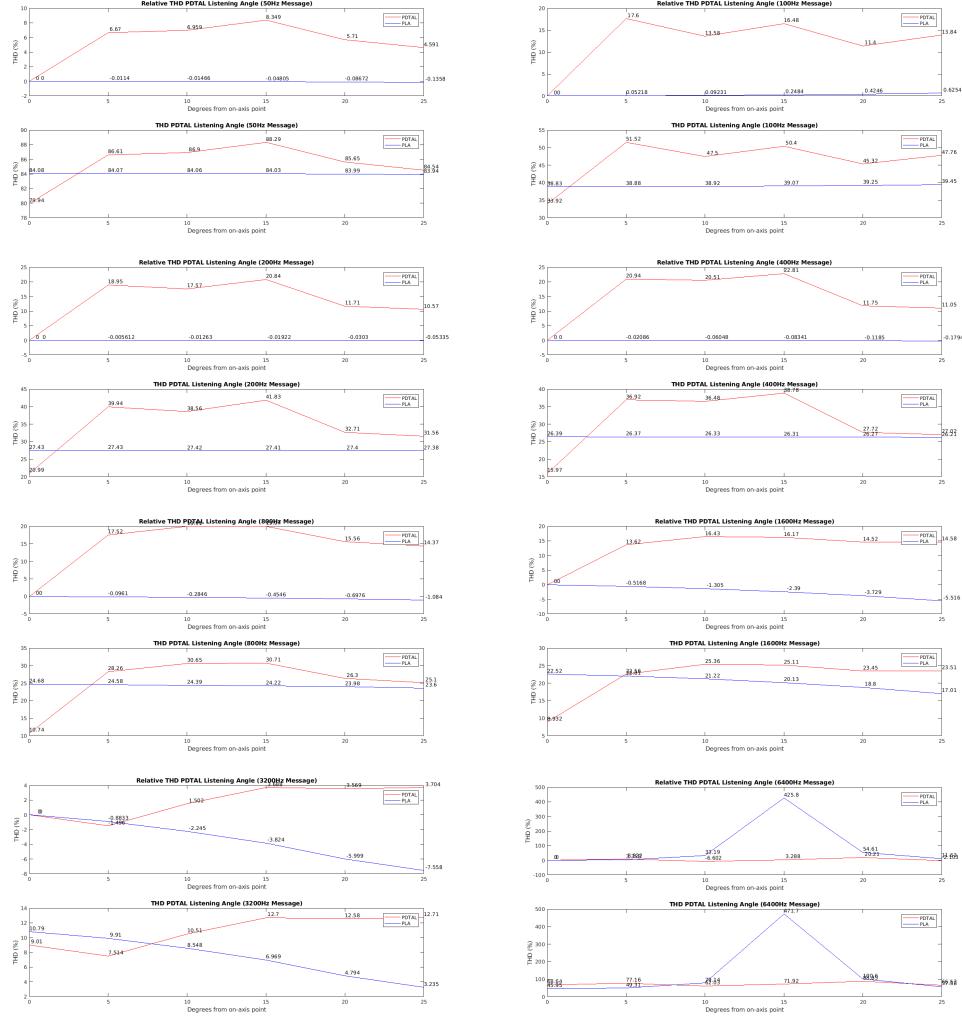


Figure 49: Simulation results for relative THD and absolute THD with different message signal frequencies over a variety of listening positions.

9.3 Measurements

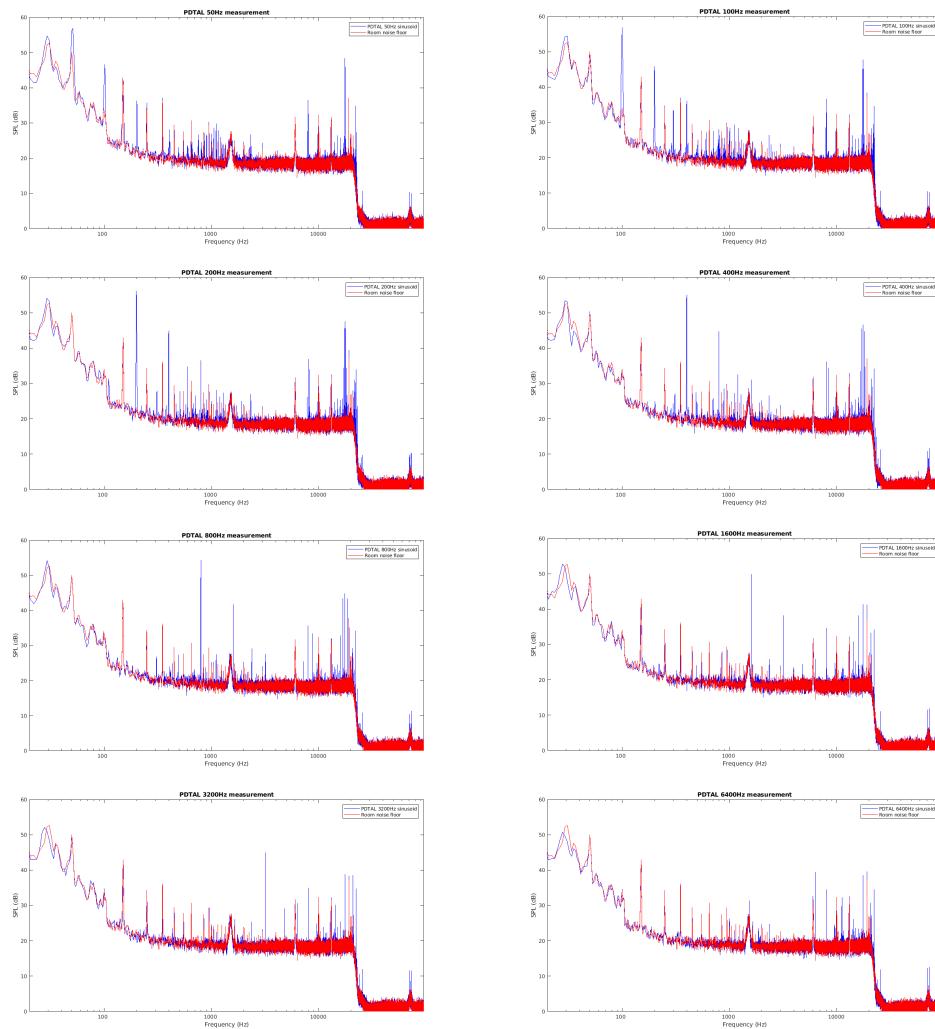


Figure 50: Measured frequency spectrum response with a variety of message signal frequency of PDTAL prototype.

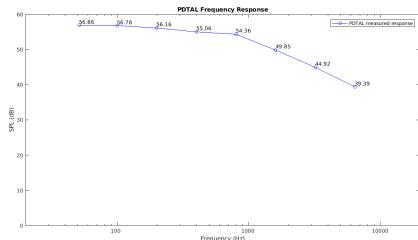


Figure 51: Measured frequency response of PDTAL prototype.

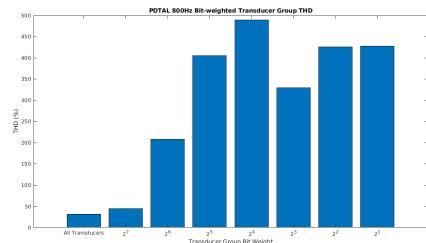


Figure 52: Measured PDTAL THD with 800Hz message signal frequency.

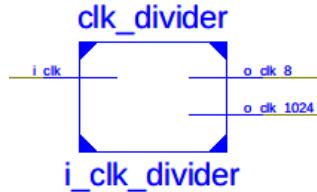


Figure 53: VHDL clock divider module schematic.

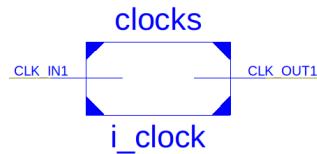


Figure 54: VHDL clock module schematic.

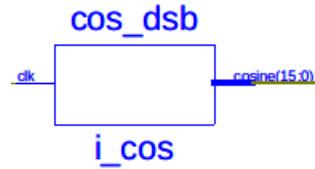


Figure 55: VHDL DSB carrier generation module schematic.

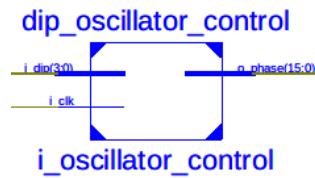


Figure 56: VHDL message signal oscillator control module schematic.

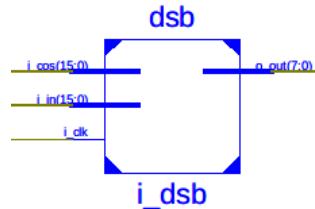


Figure 57: VHDL DSB modulator module schematic.

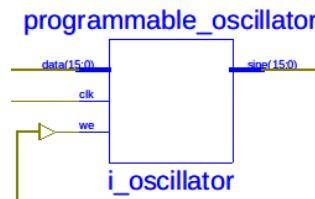


Figure 58: VHDL programmable oscillator module schematic.

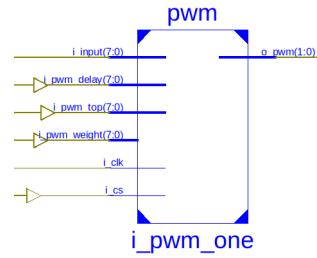


Figure 59: VHDL PWM modulator module schematic.

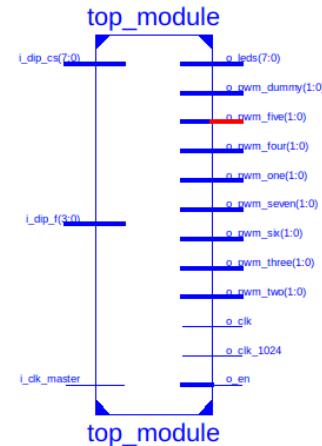


Figure 60: VHDL top module module schematic.

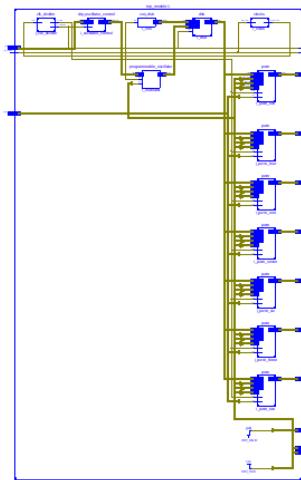


Figure 61: VHDL top module module schematic.

9.4 Project Planning

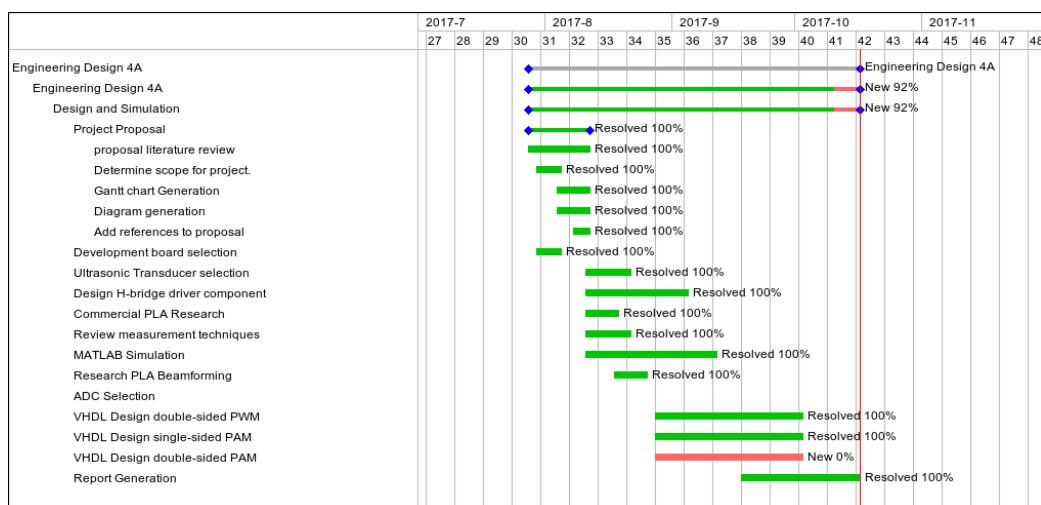


Figure 62: Engineering Design 4A Gantt Chart.

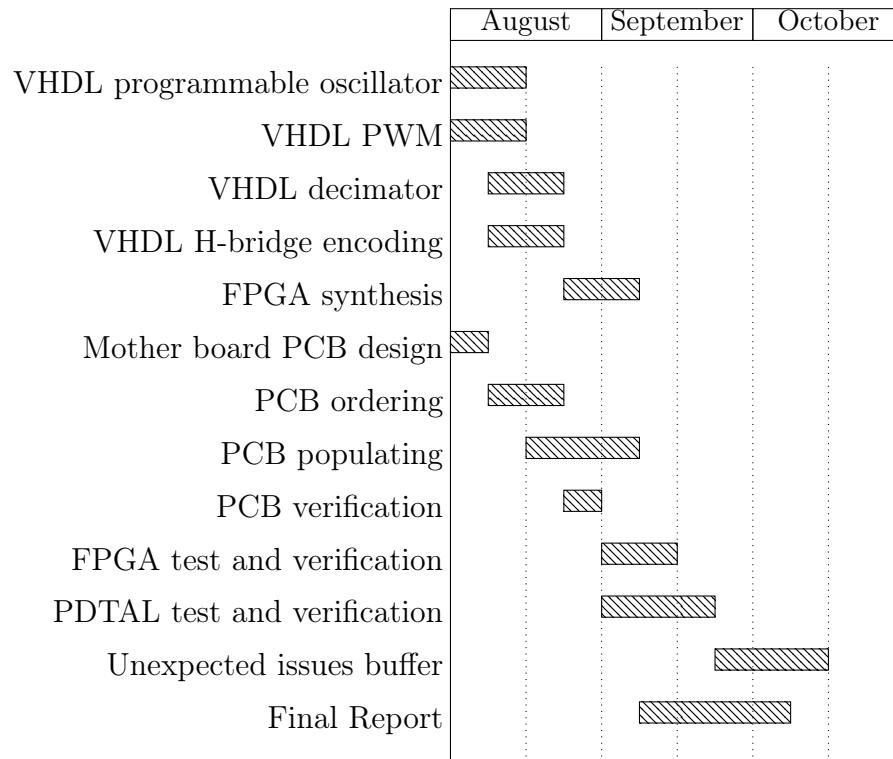


Figure 63: Capstone Project B Gantt Chart.

9.5 Prototype Part and Price List

Part Name	Source product n	Source	Price per part	Quantity
PINHD-2X8	S9171-ND	Digikey	\$0.57	2
MA40S4S	490-7707-ND	Digikey	\$5.81	28
100nF Cap	BC2665CT-ND	Digikey	\$0.18	10
1uF Cap	BC1168CT-ND	Digikey	\$0.45	4
220uF Cap	493-1082-ND	Digikey	\$0.45	2
27pF Cap	BC1035CT-ND	Digikey	\$0.28	1
13pF Cap	399-8912-ND	Digikey	\$0.92	1
10uF Cap	P5178-ND	Digikey	\$0.17	8
4.7uF Cap	P5177-ND	Digikey	\$0.24	4
	S9200-ND	Digikey	\$2.62	4
	S9175-ND	Digikey	\$0.99	4
10k Resistor	PPC10.0KYCT-ND	Digikey	\$0.18	1
100k Resistor	PPC100KYCT-ND	Digikey	\$0.18	2
LT1632	LT1632CN8#PBF-	Digikey	\$9.18	1
MAX152	MAX152CPP+-ND	Digikey	\$20.77	1
LTC1046	LTC1046CN8#PBF	Digikey	\$5.96	1
LT1086-3.3	LT1086CT-3.3#PBF	Digikey	\$5.54	1
LT1086-5	LT1086CT-5#PBF	Digikey	\$5.54	1
LT1086-12	LT1086CT-12#PBF	Digikey	\$5.54	1
L293NE	296-9519-5-ND	Digikey	\$4.98	4
Right Angle BNC AMP_	A32260-ND	Digikey	\$4.06	1
DC Power Jack	CP-102A-ND	Digikey	\$0.87	1

Figure 64: Part and price list for prototype.

9.6 Prototype PCB Design

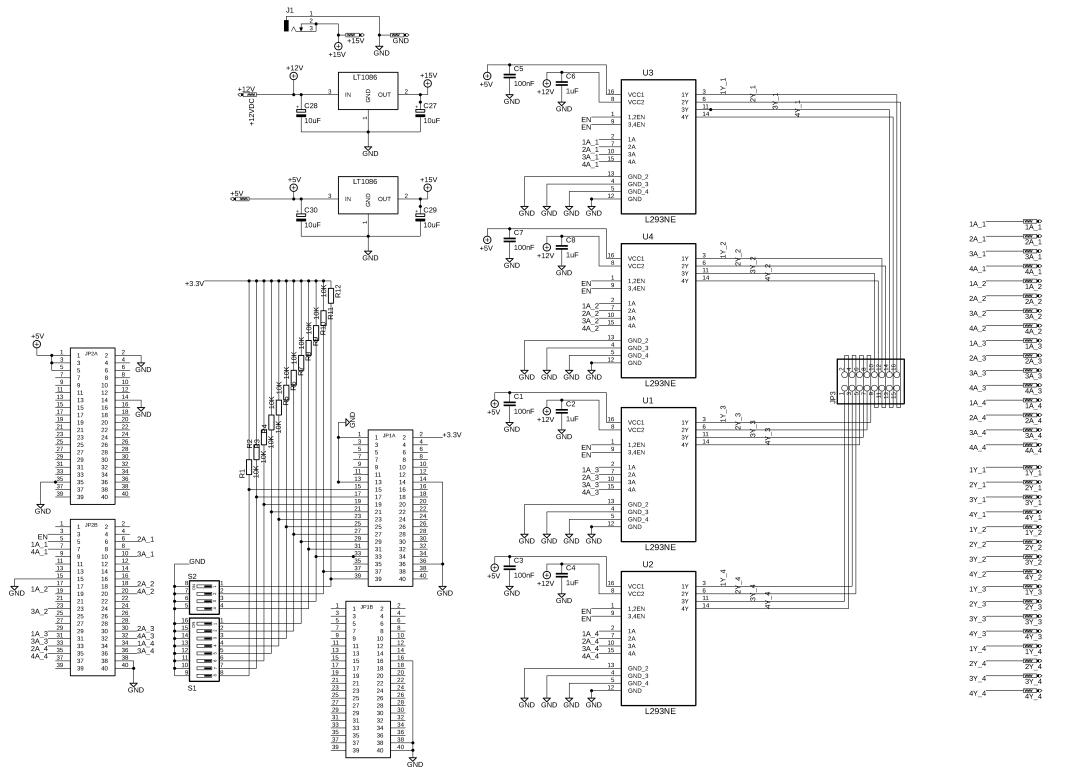


Figure 65: Schematic of the mother board circuit used in the prototype.

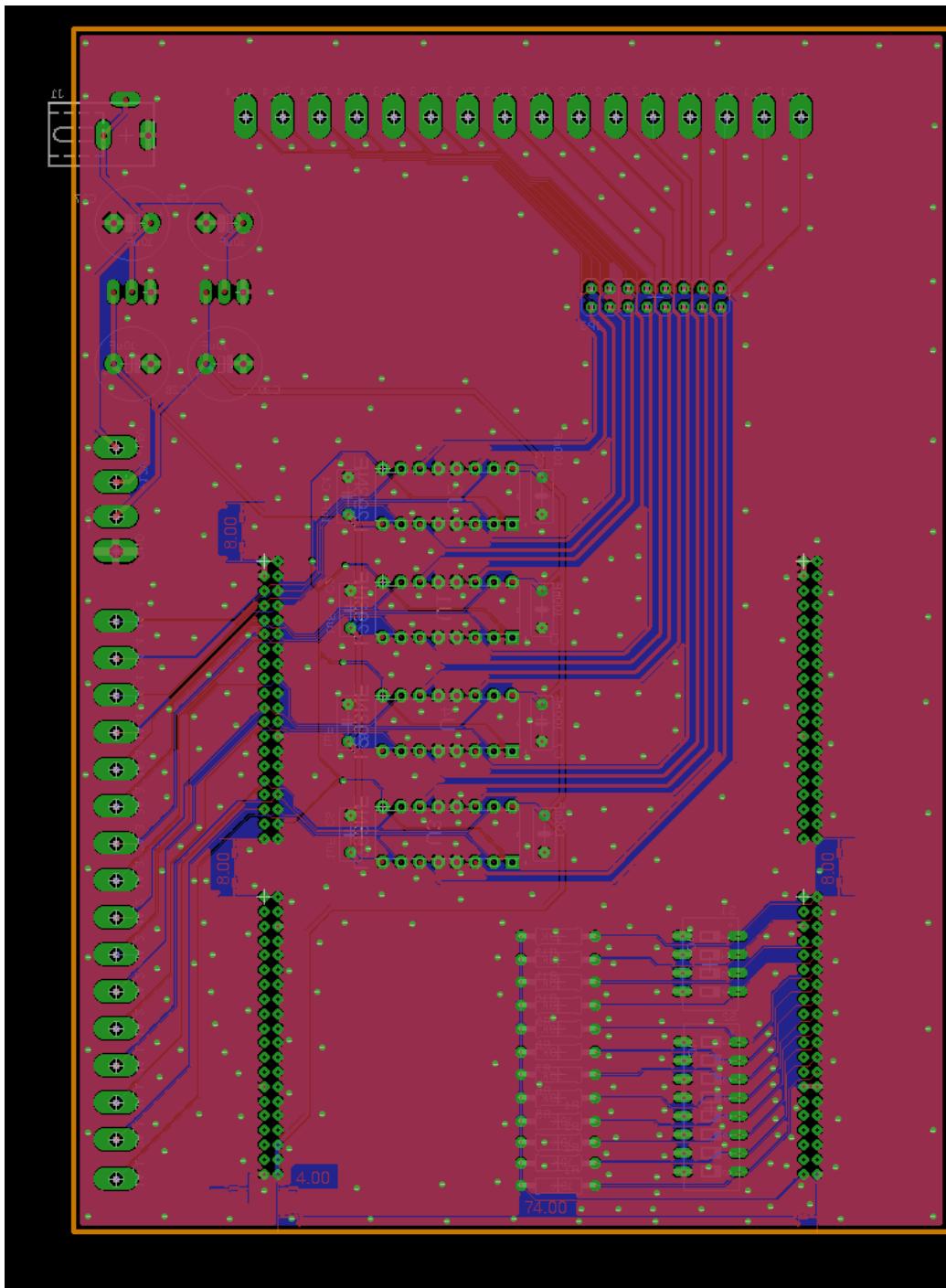


Figure 66: PCB layout of the mother board used in the prototype.

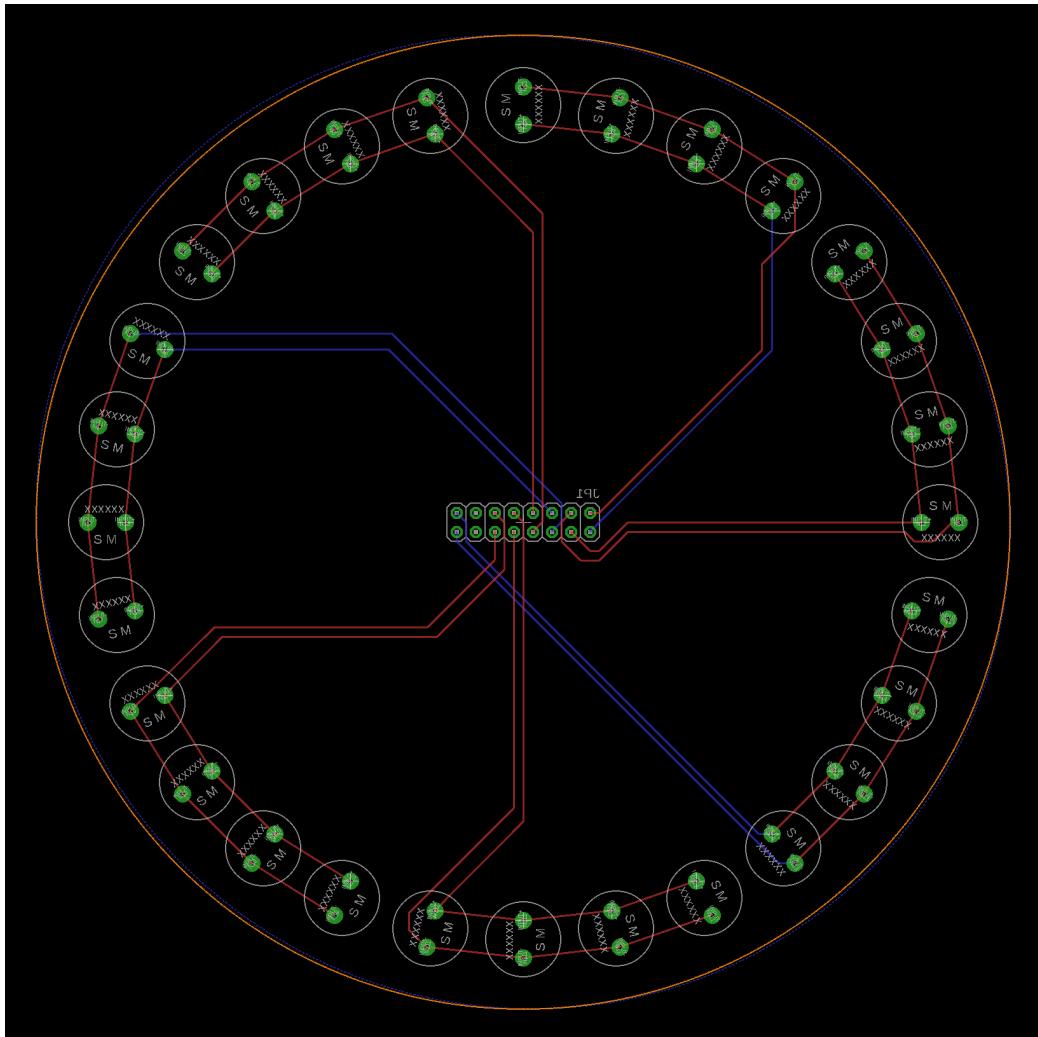


Figure 67: PCB layout of the piezo transducer array used in the prototype.

9.7 Turnitin

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