RMIT UNIVERSITY

SCHOOL OF ENGINEERING

EEET2162/2035 – ADVANCED DIGITAL DESIGN 1 / DESIGN WITH HARDWARE DESCRIPTION LANGUAGES

LABORATORY 1

INTRODUCTION TO QUARTUS PRIME

1 AIMS

(i) To design, simulate, implement and test a digital combinatorial circuit using the Quartus Prime toolchain.

(ii) To revise basic Boolean algebra and the associated techniques to convert a truth-table into a usable circuit.

(iii) To demonstrate the workflow when using schematic capture to construct a design for a physical Field Programmable Gate Array (FPGA) target.

(iv) To utilise modern electronic test equipment to confirm the final circuit implementation.

2 INTRODUCTION

Students are expected to work in individually and submit a report which will be assessed by the laboratory demonstrator. This particular laboratory session will run for one week (weeks 2), however the submission will occur at the end of week 4 (soft copy to the subject Canvas website – due to the Labour Day public holiday).

In this laboratory you will be required to design, simulate, implement and test a basic combinational circuit derived from a truth-table. The Quartus Prime toolchain will be used for this laboratory and the output verified via simulation and on physical hardware.

This laboratory serves as revision in fundamental digital system design. Students are expected to understand how to minimise a truth-table via standard processes such as Karnaugh maps and convert these to equivalent Sum-of-Products (SOP) forms. Full working should be shown for the minimisation process and only minimal forms will be accepted as a correct answer.

Table 1 depicts the truth-table that is to be implemented in Quartus. Note that you will develop a solution via schematic capture and verify the design via the waveform editor.

As part of the Quartus project development you will need to specify a set of physical inputs and outputs that can be used to exercise the entire table. The simplest method to achieve this is to use the slide switches and LEDs already available on the DE-10 Nano Development board. The mapping for the various interfaces appears in Table 2.

INPUTS				*OUTPUTS*		
D	**C**	**B**	**A**	**OUT_1**	**OUT_2**	**OUT_3**
0	0	0	0	1	1	0
0	0	0	1	1	0	0
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	0
0	1	0	1	0	0	0
0	1	1	0	1	1	1
0	1	1	1	1	0	1
1	0	0	0	0	1	1
1	0	0	1	0	0	0
1	0	1	0	1	1	1
1	0	1	1	0	0	1
1	1	0	0	0	1	1
1	1	0	1	0	0	0
1	1	1	0	0	0	0
1	1	1	1	0	0	1

Table 1 - Truth Table - Adapted from [1]

Function	Mapping	Physical I/O	I/O Standard
SW0	A	Y24	3.3-V LVTTL
SW1	B	W24	3.3-V LVTTL
SW2	C	W21	3.3-V LVTTL
SW3	D	W20	3.3-V LVTTL
LED0	OUT_1	W15	3.3-V LVTTL
LED1	OUT_2	AA24	3.3-V LVTTL
LED2	OUT_3	V16	3.3-V LVTTL

Table 2 - DE10 Nano Pin Mapping

When configuring a project in Quartus it is important to select the correct target FPGA (even if the target is purely simulation). For the DE10-Nano Development board, they target device is a 5CSEBA6U23I7DK. If an incorrect device is selected, then the configuration for the Logic Elements (LEs) will be incorrect and hence the system will not function.

3 DESIGN AND SIMULATION

The first part of the laboratory involves creating the SOP form for the truth-table in Table 1. Assume that the LEDs will be turned on with a logic 1 at the output. The required tasks are as follows (show all working):

a) Create a Karnaugh map for each output (OUT_1, OUT_2 and OUT_3) from Table 1. For simplicity, use inputs ‘DC’ as the rows and ‘BA’ for the column values. Remember to order the rows and columns correctly.

b) From the Karnaugh map create the SOP expression for each of the outputs. Ensure that you minimise the logic correctly.

c) Once the minimised SOP expressions have been created, the design can be entered into Quartus via the schematic capture tool. Launch Quartus, and create a new project via the 'File -> New Project Wizard' option. Ensure that the 'Working Directory' is set to a drive where you have write permissions. The name of the project and top-level entity should be set to a useful descriptor. The remaining project entries, with the exception of the device selection ('Family, Device & Board Settings' can be left at their default values. Ensure that you set the actual device to 5CSEBA6U23I7DK by entering the value in the 'Name Filter'. Step through the dialogs and press 'Finish' when complete to build the project.

d) To invoke the schematic entry tool, select 'File-> New' and then a 'Block Diagram / Schematic File'. A toolbar will be created when the block diagram editor opens and individual components can be place by using the 'Symbol Tool' button. For this particular laboratory you will need to use primitives such as 'and3, or3 and not'. Note that your particular SOP minimisation may require additional types of gates. The inputs and outputs also need to be implemented using the 'Pin Tool'. Ensure that the correct names for the I/O are utilised. The wiring between the various primitives can be completed using the 'Orthogonal Node Tool'. Once the schematic entry is complete, save the block diagram and close the schematic entry tool.

e) Before a simulation of the design can commence the pins need to be mapped to the physical FPGA. From the Quartus main toolbar, select 'Start Analysis and Synthesis'. This process will evaluate the schematic that has been created and determine the required external I/Os. Errors in this process need to be addressed before proceeding. If the synthesis is successful, then the 'Pin Planner' can be launched by the 'Assignments Menu'. As its name suggests the 'Pin Planner' displays an overview of the FPGA pins that can be connected to the Schematic / HDL models created. Assign the pins as demonstrated in Figure 1. Once completed, close the 'Pin Planner'.

Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved	Current Strength	Slew Rate
A	Input	PIN_Y24	5B	B5B_N0	3.3-V LVTTL		16mA (default)	
B	Input	PIN_W24	5B	B5B_N0	3.3-V LVTTL		16mA (default)	
C	Input	PIN_W21	5B	B5B_N0	3.3-V LVTTL		16mA (default)	
D	Input	PIN_W20	5B	B5B_N0	3.3-V LVTTL		16mA (default)	
OUT_1	Output	PIN_W15	5A	B5A_N0	3.3-V LVTTL		16mA (default)	1 (default)
OUT_2	Output	PIN_AA24	5A	B5A_N0	3.3-V LVTTL		16mA (default)	1 (default)
OUT_3	Output	PIN_V16	5A	B5A_N0	3.3-V LVTTL		16mA (default)	1 (default)
<<new node>>								

Figure 1 - Laboratory 1 Pin Mapping

f) The next step in the process is to perform a simulation of the logic developed. Within Quartus there are two different options for simulation: ModelSim and the Simluation Wave Editor. As this is a relatively simple design, the Wave Editor will be used. To create the waveforms to verify the design, from the Quartus menu select 'New->University Program VWF'. The individual nodes (I/Os) need to be added into the simulation. From the menu select 'Edit -> Insert Node or Bus' and then click on 'Node Finder'. Click the 'List' button, select all of the nodes and press the '>>' symbol to add all nodes into the simulation. Close all dialogs by selecting 'OK'.

g) Once the process is successful all inputs and outputs will be displayed as waveforms (by default inputs will be '0' and outputs 'X' (undefined). To exercise all of the input combinations (16 in total) the waveform needs to be manually created. At time increments of 100ns, the input states should change. By selecting the individual ranges (per input) the logic level can be

changed. Note that only the 'Forcing low' and 'Forcing high' buttons should be used to set the logic levels. Furthermore, to assist with entering of waveforms the grid should be changed to 100ns. One the input waveform is complete it will resemble Figure 2. To perform the actual simulation select 'Simulation->Run Functional Simulation' from the waveform editor window. Confirm that you actual solution matches the truth table in Table 1.

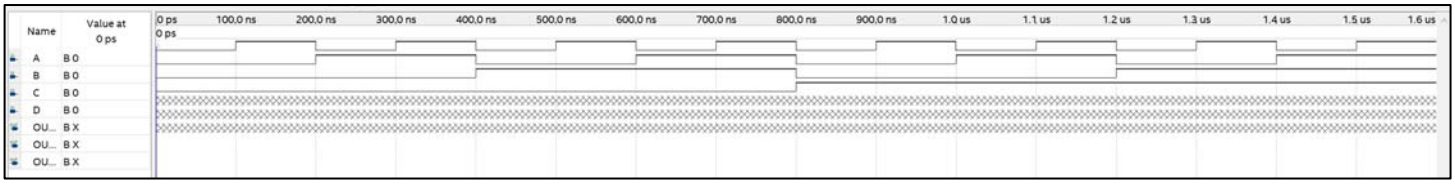

Figure 2 – Simulation Waveform

4 IMPLEMENTATION

The final section of this laboratory is to implement the actual design on the DE10-Nano Hardware Development platform. If the simulation is successful then it is relatively simple process. To begin the compilation process only the main Quartus Window should be open.

a) Although the simulation has been developed and verified, it is necessary to create the configuration that will be downloaded to the FPGA. This is achieved by selecting the 'Process ->Start Compilation' option from the Quartus main window. Note that depending on the complexity the compilation can take between 5 – 10 minutes. Once complete, a binary configuration file is ready to be uploaded to the development hardware.

b) Connect the DE10-Nano to the PC using the USB-Blaster port (located near the DC power port). From the 'Tools' menu select 'Programmer'. The development hardware will be detected automatically. As discussed in the lectures the platform that we are using is a System-on-Chip (SoC) and hence both the FPGA and Hard Processor System (HPS) will appear in the JTAG programming chain. To ensure successful deployment both the FPGA and HPS need to be entered into the device programming tool. This can be active by selecting the 'Autodetect' button. The additional device to add is a 5CSEBA6.

c) Once the new device has been added the programming file will need to be updated. Select the 5CSEBA6 device in the upper window and then press the 'Change File' button. Navigate to the 'output_files' directory and select the *project_name.sof* file. Select the device again in the upper window and press the 'Program / Configure' checkbox. The 'Start' button should now become active which you can press to send the configuration to the development board.

d) Now that the device has been programmed, exercise the truth table in Table 1 and confirm that is operates as expected.

5 REPORT

a) Record all results and observations. All calculations, schematics, waveforms and the corresponding discussions should be present in the report.

6 SUGGESTED REFERENCES

[1] Daniels, Jerry D, "*Digital Design from Zero to One*", First Edition, Wiley, 1996.