DALHOUSIE SPACE SYSTEMS Lab (DSS)

LORIS PROJECT

Power Subsystem Document

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1. Introduction

1.1 Executive Summary

This document provides an overview of the Electrical Power Subsystem for the LORIS CubeSat project. Its purpose is to help explain the design decisions, design processes, simulation results, prototypes and test plans.

1.2 Team Information

Table 1. Team Information

Full Name	Position/Responsibility	Email Address	Discipline
Brandon Allen	Lead	ballen@dal.ca	Electrical
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1.3 Definitions, Acronyms and Abbreviations

Table 2. List of Abbreviations

PDU	Power Distribution Unit
EPS	Electrical Power System
OBC	On board computer
ADC	Analog to Digital Converter
CCCV	Constant Current-Constant Voltage
LEO	Low Earth Orbit
PCB	Printed Circuit Board
MPB	Main Power Bus
MPPT	Maximum Power Point Tracking
SoC	State of Charge
EGSE	Electrical Ground Support Equipment

2. System Overview

The EPS is divided into three interrelated systems: the battery pack, the power Distribution Unit (PDU), and the solar panels. These three systems are largely independent from one another, will be housed on three different PCBs, and result in three different prototypes. The objectives of each system are listed below.

2.1 Battery pack objectives

- Protect battery pack against over-charge, over-discharge, and external short-circuit
- Relay State-of-Charge estimation to OBC
- Equip battery pack with heater for under-temperature protection
- Test battery cells to specification provided by Nanoracks
- Interface with external 5V source that exclusively powers the battery charger circuit
- Stake and harness battery cells to endure launch to LEO
- Employ only low-outgassing epoxies

2.2 PDU objectives

- Condition bus voltages to 5V and 3.3V
- Provide load-switching capability to the OBC
- Measure critical voltages and currents to be relayed to the OBC
- Protect bus lines against load short-circuit
- Interface with 30-minute timer circuit and system switch that activates in response to deployment switch configuration
- Restart 30-minute timer circuit upon toggling of any deployment switch
- Interface with RBF pin that prevents loads from receiving power when inserted
- Interface with external 5V source that bypasses 30-minute timer circuit
- Drive burn-wire circuit to deploy solar panels
- Stake and harness components to endure launch to LEO
- Employ only low-outgassing conformal coatings

2.3 Solar panel objectives

- Harvest enough power to fully-charge battery pack when LORIS is in standby mode
- Interface solar cells with MPPT
- Interface solar cells with the Main Power Bus
- Employ only low-outgassing epoxies and conformal coatings
- Fasten solar cells to endure launch to LEO

2.4 High Level Diagrams

Nanoracks, the launch provider for the LORIS mission requires that the electrical system design incorporates:

- A minimum of three independent inhibits switches that are actuated by physical deployment switches.
- A timer that keeps the satellite turned off for 30 minutes after being deployed.
- A remove before flight pin (RBF) that keeps the satellite in an unpowered state throughout the ground handling and integration into their deployer.

With this, the following system requirements were derived:

[SYS-POW-180] The power subsystem shall include a minimum of three inhibit switches that keep the satellite in a powered-down state.

[SYS-POW-181] The PDU shall provide power to the loads at least 30 minutes after all three inhibit switches are closed.

[SYS-POW-182] If any of the three inhibit switches are toggled during the 30-minute period, the timer must reset.

[SYS-POW-190] The power subsystem shall be in a power off state while integrated in the CubeSat deployer from the time of delivery to the Launch Vehicle (LV) through on-orbit deployment.

[SYS-POW-200] LORIS shall have a remove before flight (RBF) feature or an apply before flight (ABF) feature that keeps the satellite in an unpowered state throughout the ground handling and integration process into the deployer.

[SYS-POW-201] The RBF pin shall cut all power to the satellite once it is inserted into the CubeSat Deployer.

[SYS-POW-202] The RBF pin shall be removed after integration into the CubeSat Deployer.

[SYS-POW-210] The RBF pin shall protrude no more than 6.5 mm (TBC) from the rails when it is fully inserted into the satellite.

The block diagrams in Figure 1 and Figure 2 show the high-level architecture of the EPS system.

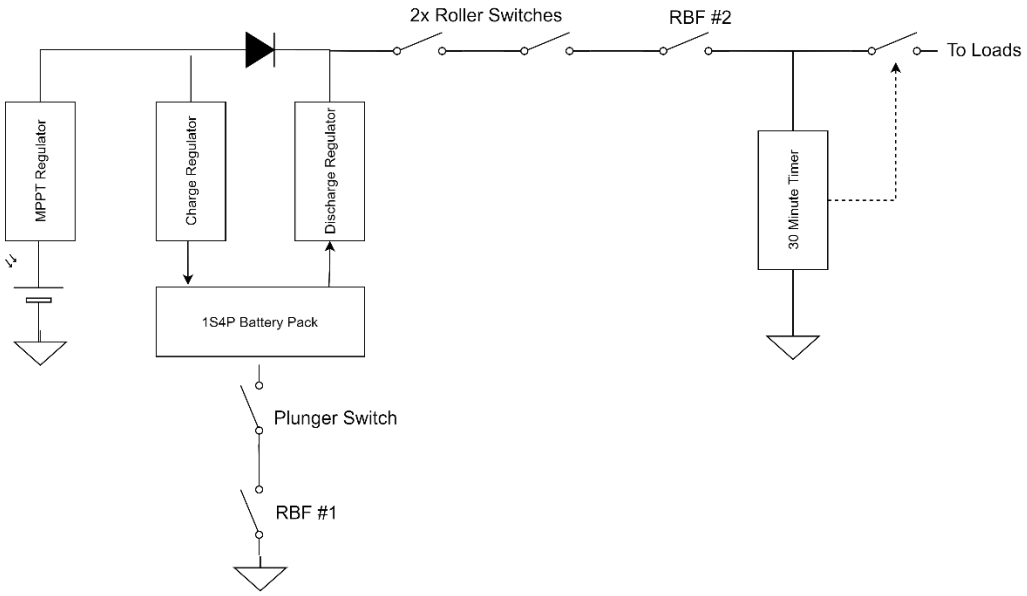


Figure 1. High Level Architecture of EPS.

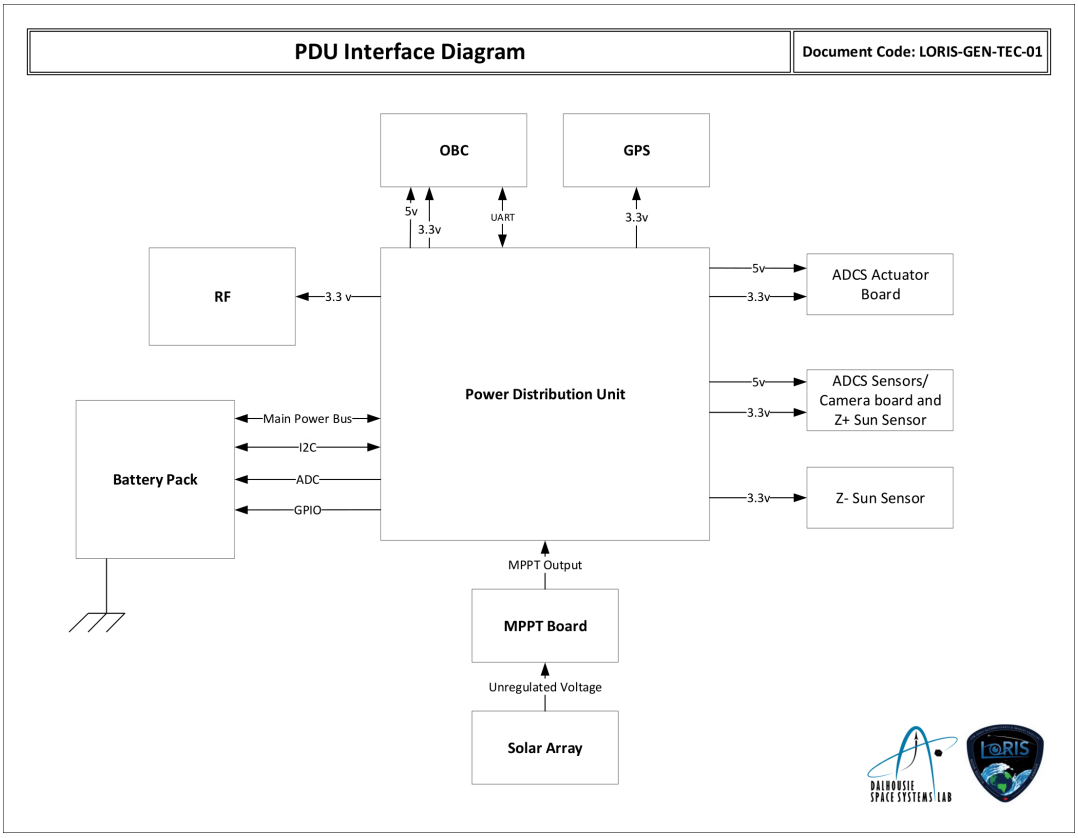


Figure 2. PDU Interface Diagram.

3. System Design

The system design will be broken into the Battery Pack board, the solar array wings/panels and the PDU board.

3.1 Battery Pack

The battery packs EAGLE project and its full schematics can be found in the folder this document is in.

3.1.1 Battery Chemistry Considerations

It is conventional for rechargeable CubeSat battery packs to employ either lithium ion or lithium polymer chemistries due to their high ratio of storage capacity to weight, known as specific energy. These two chemistries differ in their packaging style: lithium ion cells are cylindrical while lithium polymer cells are pouch cells. While more expensive, lithium polymer cells have higher specific energy than lithium ion cells. However, pouch cells must be restrained at all times with pressure restraints to prevent swelling in low-pressure environments. Opting for pouch cells would require special coordination with Nanoracks to ensure compliance with safety regulations. As a result, lithium polymer cells were ruled out.

This left us with the choice between different lithium ion chemistries. Factors considered were specific energy, cycle life, and flight heritage. Due to the lack of heavy-load transient events where high-current output would be required, specific power was not considered an important factor in the decision. Table 3 summarizes the battery chemistries considered.

Table 3. Battery Chemistry Considerations.

Battery Chemistry	**Voltage (V)**	**Specific Energy (Whr/kg)**	**Cycle Life**
Lithium Cobalt Oxide	3.0 - 4.2 3.6 nominal	150 - 200	500 - 1000
Lithium Manganese Oxide	3.0 - 4.2 3.8 nominal	100 - 150	300 – 700
Lithium Manganese Cobalt Oxide	3.0 - 4.2 3.7 nominal	150 - 220	1000 – 2000
Lithium Iron Phosphate	2.5 - 3.65 3.3 nominal	90 - 120	1000 – 2000
Lithium Nickel Cobalt Aluminum Oxide	3.0 - 4.2 3.6 nominal	200 - 260	500
Lithium Titanate	1.8 - 2.85 2.4 nominal	50 - 80	3000 - 7000

Lithium Nickel Cobalt Aluminum Oxide (NCA) batteries have the superior specific energy, making the NCA chemistry a top contender for the mission. However, lithium NCA batteries have one of the worst lifespans of the lithium-ion chemistries. It should be noted that a charge cycle refers to a complete charge and discharge of the battery. If the battery pack is sized to have a minimal depth of discharge, it would take

several orbital cycles before the battery completes a full charge cycle. Therefore, a lifespan of 500 charge cycles is more than sufficient for a mission length of 1 year, and the limited lifespan of lithium NCA batteries does not detract from their eligibility. Lithium NCA batteries also have considerable flight heritage. For instance, they are used in many COTS CubeSat battery packs. As a result, this chemistry was selected.

Twelve Panasonic 18650b Lithium Ion Battery (3400 mAh) were purchased from onlybatteries.com. The battery pack will be composed of four 18650b cells to meet the following system requirements.

[SYS-POW-030] The spacecraft battery shall store a minimum 40 Whr of electrical power to operate the payload and subsystems when solar power is not available.

[SYS-POW-032] Total chemical energy stored shall not exceed 80 Whr as specified by Nanoracks in [AD4].

3.1.2 Battery Pack over-charge, over-discharge, and external short protection

The battery pack will use the BQ29709 to protect the cells against over-charge, over-discharge, external short-circuit, charge over-current, and discharge over-current. The BQ29709 controls the gates of two external MOSFETS, which are chosen such that the on-resistance of each MOSFET determines the over-current threshold. The IC turns off the charging or discharging MOSFET when a fault is detected. It should be noted that each cell has its own BQ29709 circuit.

[SYS-POW-040] The battery pack must contain integrated protection against over-charge, over-discharge, short-circuit, charge over-current, and discharge over-current events.

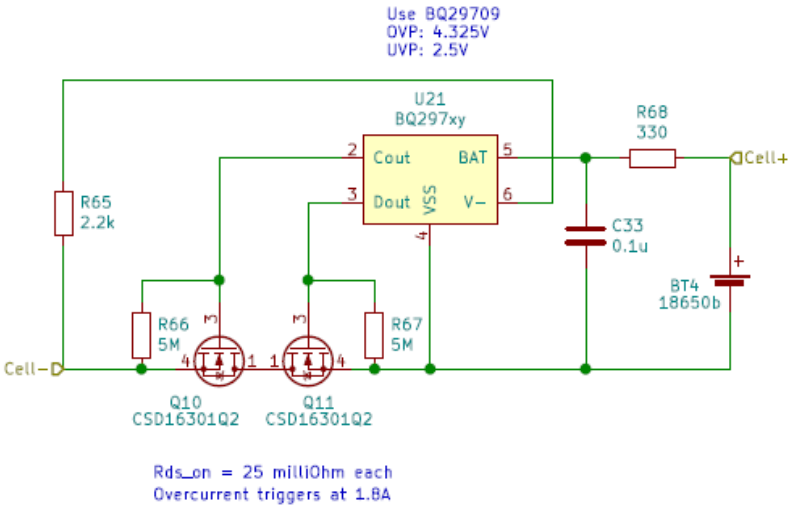


Figure 3. Cell level protection.

3.1.3 Battery Pack State-of-Charge estimation

The LTC2942 Coulomb Counter IC will be used to track the state of charge of the coulomb counter. The LTC2942 integrates the net current through a shunt over time to provide a more accurate SoC estimate. The LTC2942 will relay its SoC measured to the PDU via I2C.

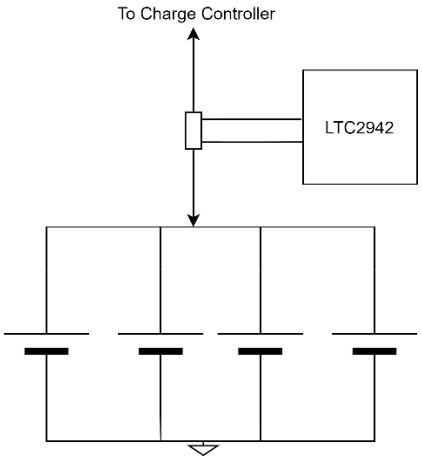


Figure 4. Coulomb counter block diagram.

Ideally, the coulomb counter shunt should be as small as possible to minimalize power loss.

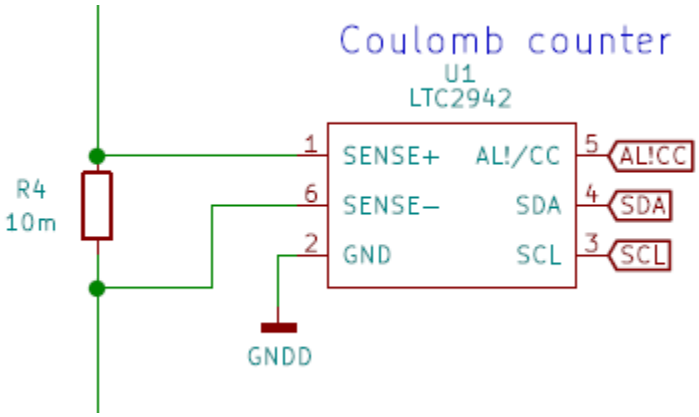


Figure 5. LTC2942 configuration.

3.1.4 Battery Ground Leg Inhibit Design

The inhibit located in the ground leg of the battery pack requires an electrical switch that is bidirectional. Using a single N-channel power MOSFET to achieve this is not possible due to the intrinsic body diode allowing current to pass from its anode to cathode while being off. Thus, when either the mechanical deployment switch or RBF switch is open, there is no path to ground for the battery pack.

The bidirectional switch was implemented by using two N-channel MOSFETS configured back-to-back with their sources and gates tied together, shown in Figure 6. The enable signal is referenced to the common

source node, rather than to common ground, to ensure that both MOSFETS turn on when required. Since the MOSFETS lie on the main power path, we selected MOSFETS with small on-resistance to minimize power losses.

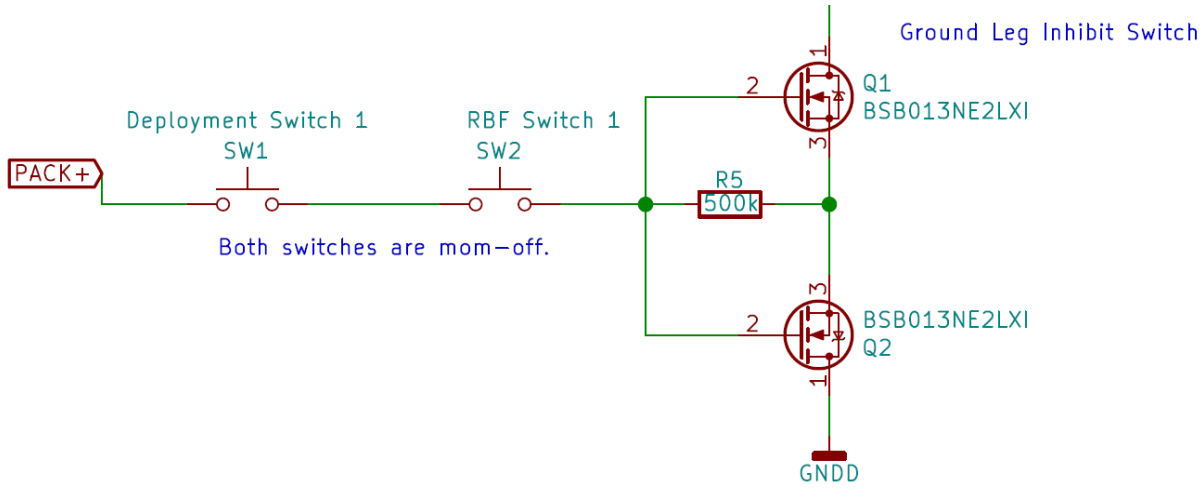


Figure 6. Ground Leg Inhibit located on battery pack board.

3.2 Solar Array Design

The solar array is composed of 28 XTJ Prime 26 cm^2 solar cells, these cells are triple junction GaInP/GaInAs/Ge chemistry. The cells are attached to the satellites side panels and deployable wings. The satellite has four side solar panels on the, X-, X+, Y- and Y+ faces; on each panel there are two XTJ Prime cells. The deployable solar wings have four solar cells each. Each solar cell is configured in parallel.

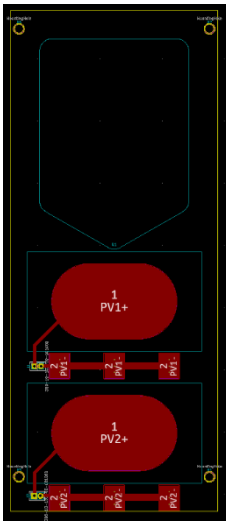


Figure 9. Solar side Panel.

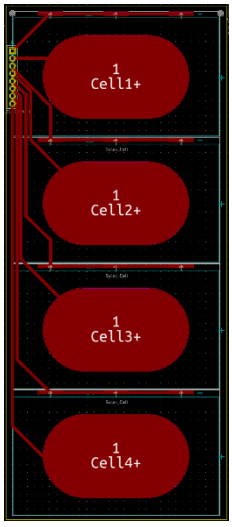


Figure 8. Solar wings.

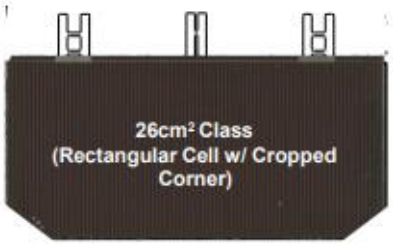


Figure 7. XTJ Prime Solar Cell.

Triple junction GaInP/GaInAs/Ge solar cells are ubiquitous among the CubeSat industry due to their high efficiency. Most COTS solar arrays source their solar cells from one of three companies: SpectroLab, AzurSpace, or SolAero. As a result, all three companies have impressive flight heritage. Each company was contacted for a quote of 32 cells and Table 4 summarizes each cost. The SpectroLab XTJ Prime cell was simultaneously the most efficient and the lowest price.

Table 4. Solar Cell Quote Summary

Manufacturer	Model No.	Efficiency	Unit Price (CAD)
AzureSpace	TJ 3G30A	30%	$372.67
SolAero	ZTJ	29.5%	$463.83
SpectroLab	XTJ Prime	30.7%	$364.43

3.2.1 Solar Array Topology and Simulation

The amount of power that must be generated by the chosen solar array topology is determined by the power budget of the satellite. When LORIS is in standby mode, with its radio transmitter and payload inactive, the solar array must generate excess power to charge the battery pack. These calculations use Orbit Average Power (OAP), where instantaneous power is averaged over one 90-minute orbit.

The power budget of the satellite requires the solar array to harvest at least 4.2 W OAP. At first glance, it is evident that no 2U CubeSat has published their power intake. This is most likely due to the fact that the 2U CubeSats are less common than 1U or 3U CubeSats. As a result, in-house simulations were done to determine precise numbers for OAP to determine a solar array topology.

MATLAB was used to simulate the OAP for various solar panel topologies. First, the simulation was validated by comparing the simulated OAP of 1U and 3U bodymounted topologies to the numbers given by ClydeSpace[1]. The resulting error was 2.4%, giving confidence in the simulation. We subsequently found that the power harvested with a 2U bodymounted topology, 3.34 W OAP, was not sufficient to meet the standby power consumption, presenting the necessity to use deployable panels. The optimal deployable panel configuration, keeping in mind the constraints of single-sided deployable panels and a nadir-pointing orbit, is a short-edge deployable topology deployed at 90°. This topology is predicted to harvest a worst case 4.38 W OAP, which exceeds the standby power consumption requirement. The results of the simulation for this topology are shown in Figure 10.

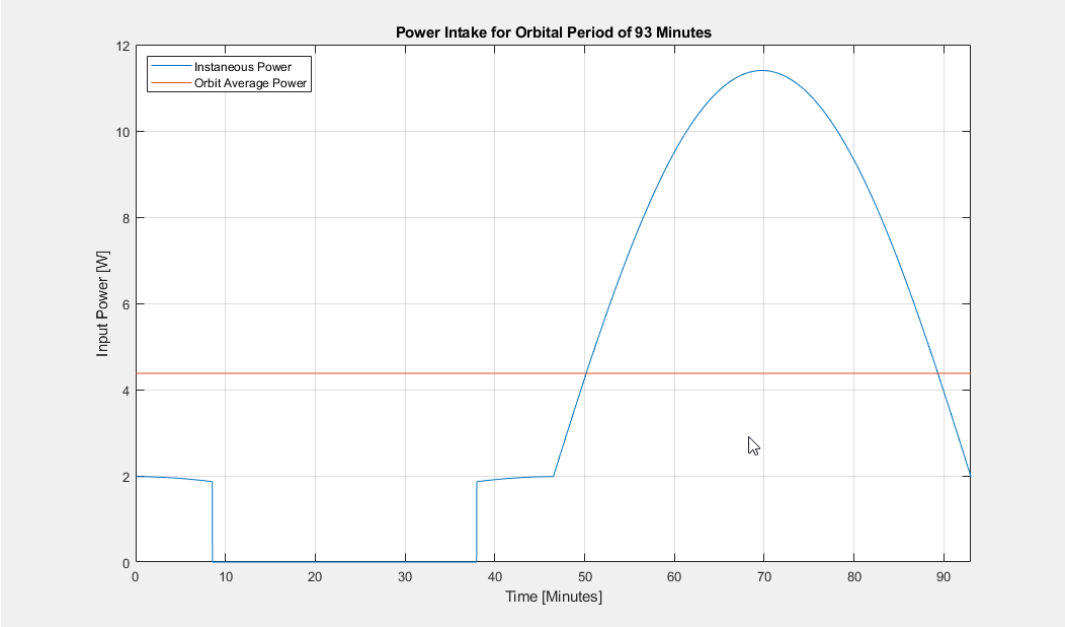


Figure 10. Solar array power intake for single orbit.

3.2.2 MPPT vs. DET

Another design choice related to the solar array configuration was the decision between Maximum Power Point Tracking (MPPT) and Direct Energy Transfer (DET). MPPT dynamically changes the operating point of the solar array to ensure it continually operates at its maximum power point, whereas the operating point of a DET architecture is statically fixed by the voltage of the battery pack.

The trade-off between these two architectures was summarized in a CSA technical webinar delivered to the students that is available upon request [2]. As described by the CSA, MPPT is superior to DET under varying environmental factors, such as when the solar array is cold post-eclipse. Furthermore, it decouples the solar array from the load, allowing for a simpler array design. The downside of MPPT is the additional electronics required for implementation, and the small power consumption of the MPPT circuitry (4-7% of total power) [12]. These downsides are partially mitigated by the availability of the SPV1040, a step-up converter that offers an embedded MPPT solution.

Both architectures have flight heritage. The ESTCube-1, a CubeSat that was operational for two years post-deployment, used the SPV1040 to implement MPPT [6]. The MinXSS-1 opted to use DET [10]. Based on our research, the split between these two architectures among CubeSats is around 50/50. MPPT is becoming more common among micro-satellites due to the availability of embedded solutions.

As MPPT enables a simpler architecture and allows the solar array to be maximally efficient post-eclipse when the battery pack will be at its lowest voltage, we chose to use MPPT over DET.

3.2.3 Interfacing the solar cells with the MPPT

The chosen MPPT implementation is the SPV1040 IC. The main functions of this IC are twofold: to regulate the solar cell voltage to 4.2V, and to keep the solar cell operating at its maximum power point. The SPV1040's target voltage is programmed by an external resistor network. The target voltage is set to 4.16V, rather than 4.2V, to reduce the potential for an overcharge fault in the battery pack. The SPV1040 circuit schematic is shown in Figure 11.

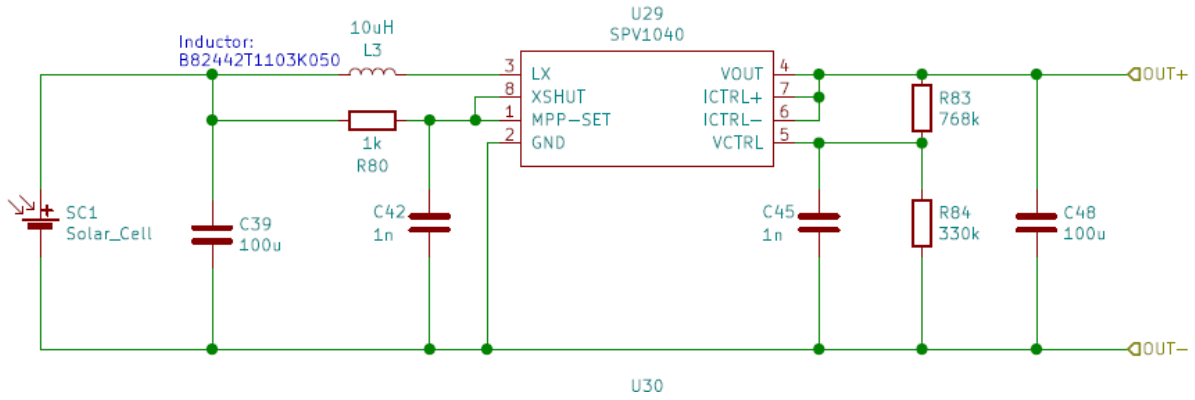


Figure 11. SPV1040 circuit.

The outputs of the MPPT regulators are tied together and connected to the MPB. Each solar cell on the solar wings will have its own dedicated SPV1040 solar regulator circuit. The solar cells on the side panels shall share its SPV1040 circuitry with its opposing face. Opposing solar cells (+-X, +-Y) can use the same SPV1040 circuitry since the geometry of the CubeSat ensures that opposing solar cells are not illuminated simultaneously.

While this design increases the footprint and weight of the final design, it has advantages. Firstly, it is maximally redundant, as the failure of a single solar cell has almost no impact on the solar array. Furthermore, it increases the efficiency of the power conversion by ensuring the maximum power point of each cell is independently tracked, and by allowing a smaller inductor to be chosen. Thus, 20 SPV1040 circuits will be on the reverse side of the PDU.

3.2.4 Attaching Solar Cells to Wings and Side Panels.

The positive terminal of the selected solar cell is its entire backside, where the cell requires a mechanical adhesive to attach to the PCB substrate. As a result, we will use an electrically conductive epoxy to fasten the solar cells to the solar panel PCB, where an exposed pad will be placed to form the positive connection.

CSA shared a in house experiment done in 2016 with the goal of figuring out a reasonable process to build a solar panel with an electrically conductive adhesive. They built up a small test panel consisting of only 2 solar cells. For one of these cells both the cell tabs and the back-side were attached to the PCB using the conductive epoxy EPO-TEK H20E, while for the other cell only the back-side was attached to the PCB with the conductive epoxy while its remaining tabs were soldered. The solar panel was subjected to some thermal cycling, adhesion and pull tests, and a final test which was a destructive pull test which revealed the breaking point of adhesion of each cell. The results of the test showed that after the thermal cycling a short circuit current reduction of 3 % was measured.

Along with the tests, they provided the exact assembly procedure they followed when assembling their panel. Thus, it was decided to use the EPO-TEK H20E as the electrically conduct epoxy.

3.2.5 Deployable Solar Wings

To fit the satellite inside of Nanoracks deployer, the solar wings must be held in a stowed position until it is launched into low earth orbit. Thus, a hold down and release mechanism (HDRM) is required. To keep the cost low, it was decided to come up with a in house HDRM using a Nichrome heating wire and a Vectron string.

The Vectron string is used to tie down the solar wings to the nichrome wire that is attached to the chassis. While the Vectron is attached, the hinges at the bottom of the panels push outwards causing tension. After deployment, ADCS subsystem will signal that the satellite has detumbled and the burn wire will release the stowed wings. Circuitry will be required to provide the Nichrome cutting wire enough current to successfully release each wing. This circuitry be located on the deployment board which is apart of the Chassis subsystem.

Figure 13. Stowed

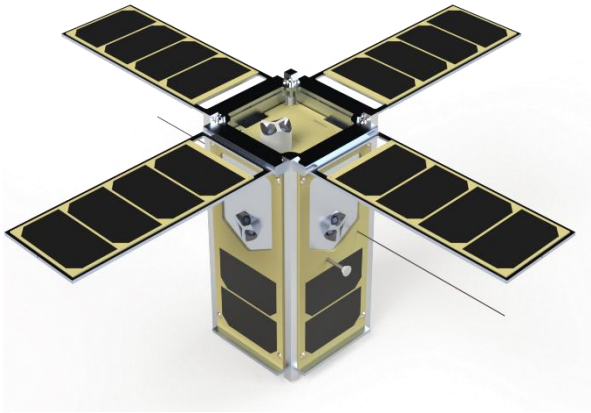


Figure 12. Deployed

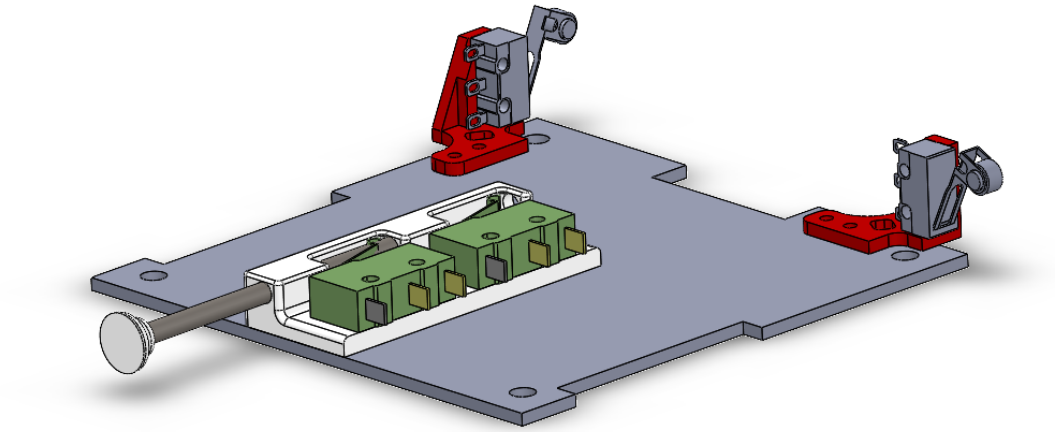


Figure 14. Deployment Board.

The location of the Vectron tie down and Nichrome wire within the satellite is still undetermined but will be finalized at a later stage in the build. The burn wire circuitry is also still in early stages of development.

3.3 Power Distribution Unit

The PDU EAGLE project and its full schematics can be found in the folder this document is in.

3.3.1 PDU Overview

CubeSat PDUs vary on whether they employ centralized or point-of-load power regulation. Centralized architectures supply all loads on a given voltage from one central location. In distributed architectures,

the EPS employs point-of-load regulation to ensure that each subsystem gets its own power converter. We reviewed two theses that highlighted the trade-off between these two architectures[3,4].

A centralized architecture is smaller in both size and weight, given that a single regulator can power multiple loads. The drawback of a centralized architecture is that the power converter must be sized for worst-case load conditions. When the load is less than worst-case, the converters suffer in efficiency. Distributed architectures are also more flexible than the alternative and can easily be modified or built upon for future missions.

However, we could not find any instances of CubeSats that employed a distributed architecture. Furthermore, since load conditions will not fluctuate drastically between different modes of operation, the reduced efficiency of the centralized architecture is mitigated. Due to the simplicity of the centralized architecture, we will employ a centralized architecture in the design of the PDU. The PDU was designed around the following requirements.

[SYS-POW-100] The PDU shall perform power conditioning, switching, internal monitoring and reporting of voltage and current.

[SYS-POW-110] The PDU shall include necessary over voltage, over current, and under voltage protection.

[SYS-POW-120] The PDU shall provide regulated 3.3±0.2V and 5±0.2V supply.

[SYS-POW-130] The PDU shall provide all necessary telemetry data to the OBC.

[SYS-POW-220] The power subsystem shall be designed to be free of any grounding issues that affect the performance of the components.

3.3.2 MSP430F5529 Microprocessor

The TI MSP430 family of ultra-low-power microcontrollers consists of several devices featuring peripheral sets targeted for a variety of applications. The architecture, combined with extensive low-power modes, is optimized to achieve extended battery life in portable measurement applications[11] . The specific MSP430 MCU chip being used is the MSP430F5529, which will be located on the PDU board.

The microcontroller will communicate with the OBC over a UART serial communication line. The microcontroller will receive two general types of commands from the EPS server running on the OBC: Power Commands and Data Request Commands.

The Power Commands are for either enabling and disabling a specific subsystem or switching to a specific power mode; specifically, three separate commands that have one parameter. If no parameter is sent with the command it is recognized as an invalid command. The Data Request Commands are for either reading the voltage level or current being drawn by a specific subsystem, the SOC of the battery array, or

the current temperature on the battery board; specifically, four separate commands. Voltage and current commands require a parameter for specifying the subsystem desired, the other two command types do not.

The General Purpose Input Output (GPIO), pins will be used to read the load switches fault status and used to enable or disable load switches either when requested by the OBC or after a fault condition has been cleared or set. The voltage and current of each subsystem will be recorded periodically by the microcontroller ADC pins. SoC will be measured by communicating to the LTC2942 over I2C. The following block diagram illustrates all the PDU peripherals that the MSP430 interacts with.

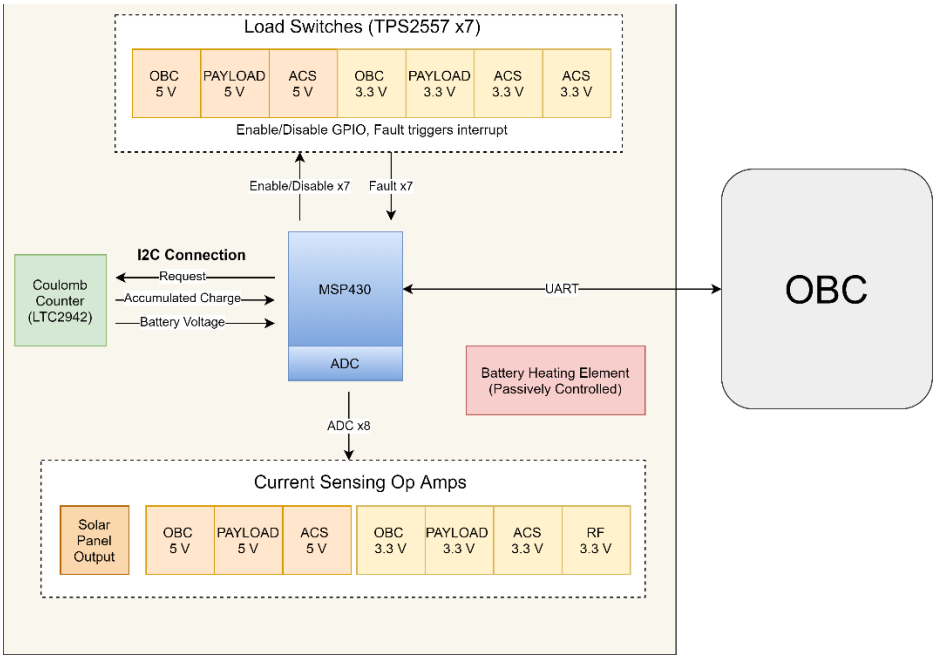
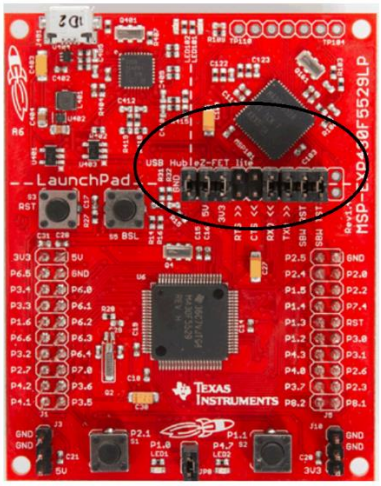


Figure 15. PDU peripherals.

3.3.3 Programming the MSP430F5529

As mentioned previously, the MSP430F5529 will be the MCU controlling the PDU. The MSP430F5529LP was used when modelling the PDU, but the chip is to be surface mounted on the PDU PCB. The schematics and information provided in the Launch Pad's user guide was used to design the circuitry needed to support the MCU on the PDU board. Only circuitry needed to support the operations of the PDU were replicated, saving space and power that would have been wasted if the entire Launch Pad were used. The MCU can be easily flashed and debugged while on the PDU PCB with eZ-FET lite emulator provided on the Launch Pad.



Four male headers will be placed on the PDU board for the code to be loaded on through the eZ-FET and have its processes monitored in real-time to ensure proper functionality. The MSP430F5529 LaunchPad User Guide should be referenced for further understanding.

3.3.4 Provide load-switching capability to the OBC.

Each subsystem connects to the power bus via the TPS2557 load switch. The load switch is current-limited, and the overcurrent threshold is set individually for each subsystem with an external resistor. Preliminary overcurrent thresholds have been established based on worst-case required power for each subsystem, but final values will be validated based on FlatSat testing. In the event that the overcurrent threshold is triggered, the TPS2557 will interrupt the MCU. Auto-relatching functionally can be configured with hardware. In total there are nine load switches supplying other systems with power each connection is noted in Table 5.

Table 5. PDU Power Connections.

Destination	Voltage Lines
OBC Board	3.3 V, 5 V
GPS Module (located on OBC board)	3.3 V
RF Board	3.3 V
ADCS Actuator Board	3.3 V, 5 V
ADCS Sensor/Camera Board	3.3 V, 5 V
ADCS Z- Sun Sensor Board	3.3 V

The configuration of the TPS2557 for supplying a load to another subsystem can be seen in Figure 14. The fault pin and enable pins are wired directly to the GPIO pins on the MSP430. The resistor attached to the

ILIM pin configures the point where the TPS2557 will limit the current; to determine this value, reference the TPS2557 datasheet.

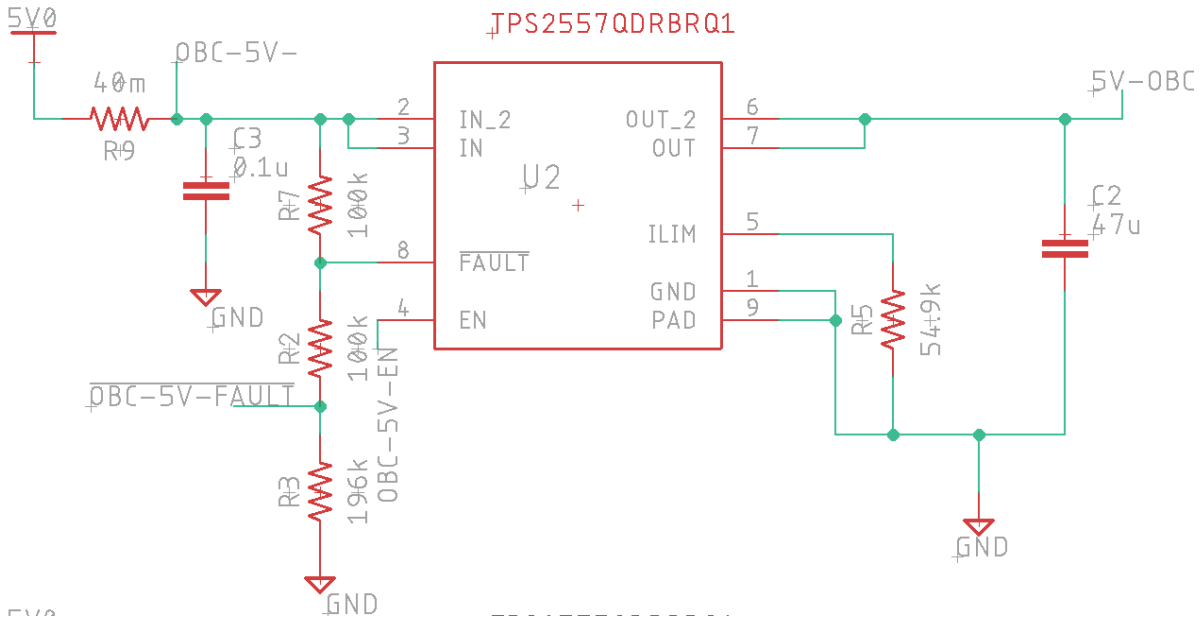


Figure 16. TPS2557 configuration for 5 V line to OBC.

3.3.5 Measuring Voltages and Currents for Telemetry

The MSP430 uses its ADC pins to read voltages and currents from the solar cells, battery pack, and each of the subsystem lines. Since the MCU operates off 3.3V, it cannot accurately read voltages above that level. Voltages above 3.3V, including the battery pack and the MPB, are read using a voltage divider. Currents are read using current sense resistors with resistances that fall in the range of milliOhms to reduce Ohmic losses. The small voltages produced by the current sense resistors are amplified using the INA181A2 current sense amplifier. The current sensor amplifiers purpose is to allow the MSP430 ADC to use its full range, therefore the following criteria was used to pick out the amplifier.

$$V_{max\_sunt} = 60 \text{ mV}$$

$$I_{max} = 1.5 \text{ A}$$

$$R_{shunt} = \frac{V_{max}}{I_{max}} = \frac{60 \times 10^{-3}\ V}{1.5\ A} = 0.04\ \Omega = 40\ \text{m}\Omega$$

The recommended max voltage drop across the shunt resistor for the INA181An series amplifiers is 60 mW, thus we used V_{max_sunt} and a worse-case current consumption I_{max} to determine the R_{shunt} value of 40 mΩ. With this the desired gain of the amplifier was found.

$$Gain = \frac{ADC\ Full\ Scale\ Voltage}{V_{max}} = \frac{3\ V}{60 \times 10^{-3}\ V} = 50$$

The output of the amplifier is fed to one of the ADC pins on the MSP430. The MSP430 pin ADC pin should be configured to enable its internal pull down resistor.

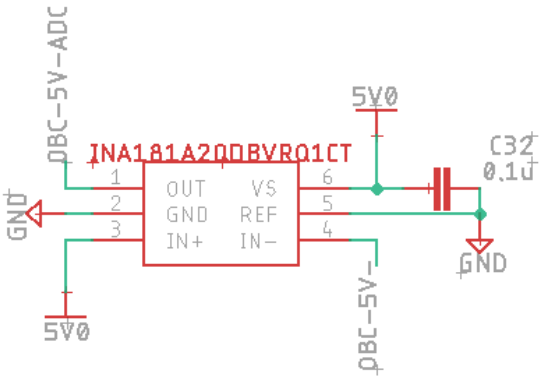


Figure 17. Current Sense Amplifier for OBC 5 V line.

The following table notes all the loads that have are being current sensed with an amplifier.

Table 6. Loads

Load Name	Voltage Lines
OBC Board	3.3 V, 5 V
GPS Module (located on OBC board)	3.3 V
RF Board	3.3 V
ADCS Actuator Board	3.3 V, 5 V
ADCS Sensor/Camera Board	3.3 V, 5 V
ADCS Z- Sun Sensor Board	3.3 V
*Solar Array Output	*4.2 V

The solar array output uses a different shunt value as the current varies due the solar array output current is larger than the 1.5 A value used for the subsystem amplifiers. Thus it requires a shunt resistor that is less than 40 mOhm.

3.3.6 Battery Charger Considerations

Lithium-ion battery chargers typically employ a method called Constant Current - Constant Voltage (CC-CV) . In the CC phase, the charging current is limited while the cell voltage linearly increases. In the CV phase, the cell voltage is held constant while the charging current drops off. CC-CV is employed to prolong the lifespan of the battery pack, ensuring that the capacity of the battery pack does not degrade significantly over multiple cycles.

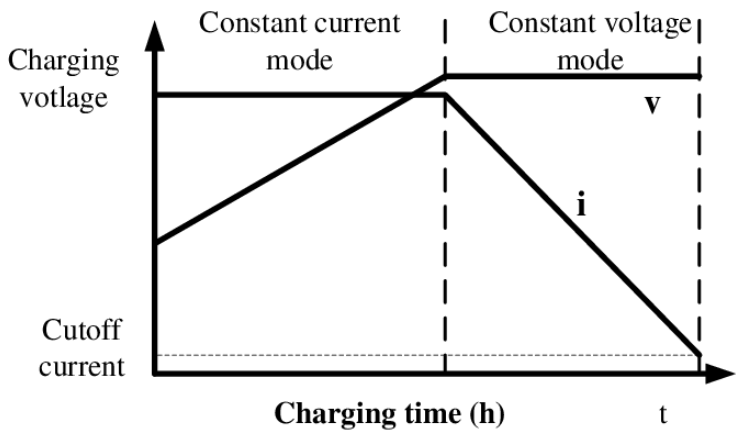


Figure 18. Constant Current - Constant Voltage graph.

We initially considered two different methods of implementing CC-CV. The first method would be to set the voltage of the main power bus (MPB) to the maximum voltage of the battery pack, which in our case is 4.2V. The charging controller simply consists of a current-limiting switch that keeps the charging current at a tolerable level while the battery voltage approaches 4.2V. No special hardware is required to implement the CV phase as the charging current will naturally decline as the battery voltage reaches 4.2V. Among the CubeSats that implement MPPT to regulate the MPB voltage, this architecture is the most common. For instance, the ESTCube-1, NUTS-1, and PW-Sat2 all employed or plan on employing this architecture[7,8,9].

The alternative method is to set the voltage of the MPB to 5V, and use a monolithic step-down converter that implements CC-CV to charge the battery pack. Using a dedicated charging IC would prolong the life of the battery pack with a superior charging curve and employ more sophisticated techniques such as trickle charging the battery when it is in a depleted state. To our knowledge, no CubeSat has implemented this architecture.

These two architectures present a trade-off. With the former, the MPB voltage is set to a voltage that is only used by the battery. The 4.2V MPB would need to pass through an additional step-up converter to condition the 5V line that will be used by most of the subsystems, making the power path between the solar cells and the loads less efficient. With the latter architecture, this power path is more efficient as there is only one regulator between the solar cells and the loads. However, the power path between the solar cells and the battery pack is made less efficient due to the addition of the step-down regulator.

The initial reasoning was to set the MPB voltage to 5V to optimize the power path from the solar cells to the load. The satellite will be sunlit for 2/3 of its orbit, during which time the loads will be drawing power from the solar cells. Using the second approach discussed, there is only a single regulator between the

solar cells and the load, minimizing losses along this power path. We planned to use a battery charger IC, such as the LTC4002, to implement CC-C charging between the 5V MPB and the battery pack, and even designed a first iteration of prototypes according to this philosophy. However, battery charger integrated circuits are not designed with a limited power supply in mind. Here, it is necessary to introduce the concept of voltage droop to further analyze the two designs.

If a load attempts to draw more current than what the power source can supply, the voltage of the power source will decline so that it can supply more current. Given that power is the product of voltage and current, voltage must decrease so that current can increase under aconstant-power constraint. This problem compounds due to the fact that loads may require more current when they are receiving less than the rated voltage, thus further reducing the voltage on the power bus. Simply put, voltage droop can lead to the failure of a power supply, and must be avoided at all costs.

The approach of using a CC-CV charger can be ruled out by analysis. CC-CV IC's require you to set the magnitude of the charging current that will be used in the CC phase with an external resistor network. The solar power available ranges between 4W and 11W over the course of the satellite's orbit. The constant current level of the charger would need to be sized to ensure that a 4W power supply does not lead to voltage droop. However, reducing the constant current level would mean there is wasted power when 11W is available. Thus, a CC phase is impractical in space applications. The charging current should be dynamically sized to ensure that all excess power available is shunted to the battery pack. For this reason, we opted to set the voltage of the MPB to 4.2V and use a current-limiting switch to avoid a charge over-current fault.

3.3.7 Battery Charger Design

The battery pack charge/discharge regulator is composed of two TPS2557 load switches that use analog comparators to determine if the battery packs voltage is in a safe range for it to either charge or discharge.

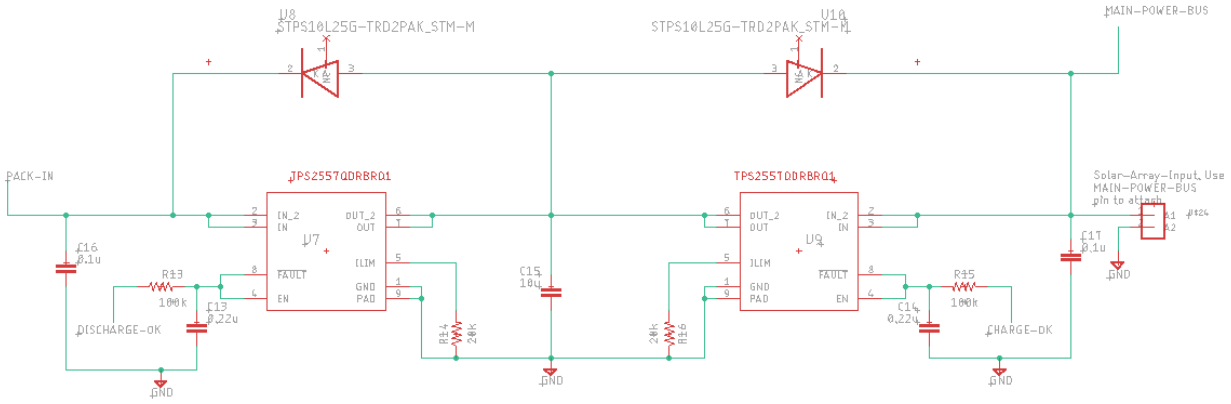


Figure 19. Charge/Discharge controller.

The TPS2557 load switches were selected as it had already been tested early on in one of the PDU prototypes. The load switches are enabled when the battery voltage acceptable range. The control circuitry is entirely passive to maintain functionality in the event of a software malfunction. The following table shows the logical operation of the switches,

Table 7. Charge/Discharge control logic.

Pack Voltage	Discharge Load Switch	Charge Load Switch
2.8 V < Pack Voltage < 4.2 V	Enabled	Enabled
Pack Voltage > 4.2 V	Enabled	Disabled
Pack Voltage < 2.8 V	Disabled	Enabled

The design uses the LM4120 precision 5V regulator, LM393 comparators and high precision resistors to monitor the voltage of the battery pack. Pull-up resistors attached to the comparator outputs were sized to reduce power loss while maintaining functionality over the range of possible leakage currents.

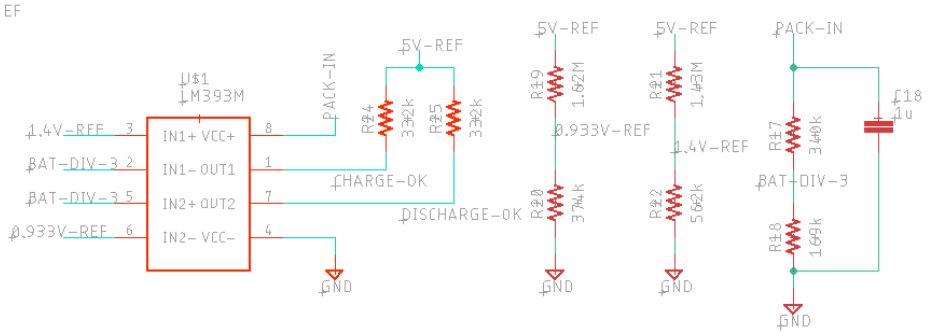


Figure 20. Charge/Discharge comparators.

3.3.8 Load Side Inhibits and 30-minute timer.

The two electrical inhibit switches on the PDU board are meant to disconnect the MPB path to the loads when the mechanical deployment or RBF switch is open. This was implemented with P-channel MOSFETs configured as high-side switches. The Si7137 P-channel power MOSFET was picked due to its low on resistance to minimize power loss.

The EPS timer circuit, shown in Figure 19, is composed of a single IC: the LTC6995. This component controls a high-side switch that is placed in series between the MPB and the loads. When all deployment switches are closed, the LTC6995 will receive power. On start-up, the IC turns on an internal oscillator that counts down to the time limit specified by an external resistor. After the timer expires, the LTC6995 will close the system switch that was preventing the other loads from receiving power. Toggling any of the deployment switches will interrupt the power supply of the LTC6995, restarting the timer. To implement this switch, another Si7137 P-channel power MOSFET was used.

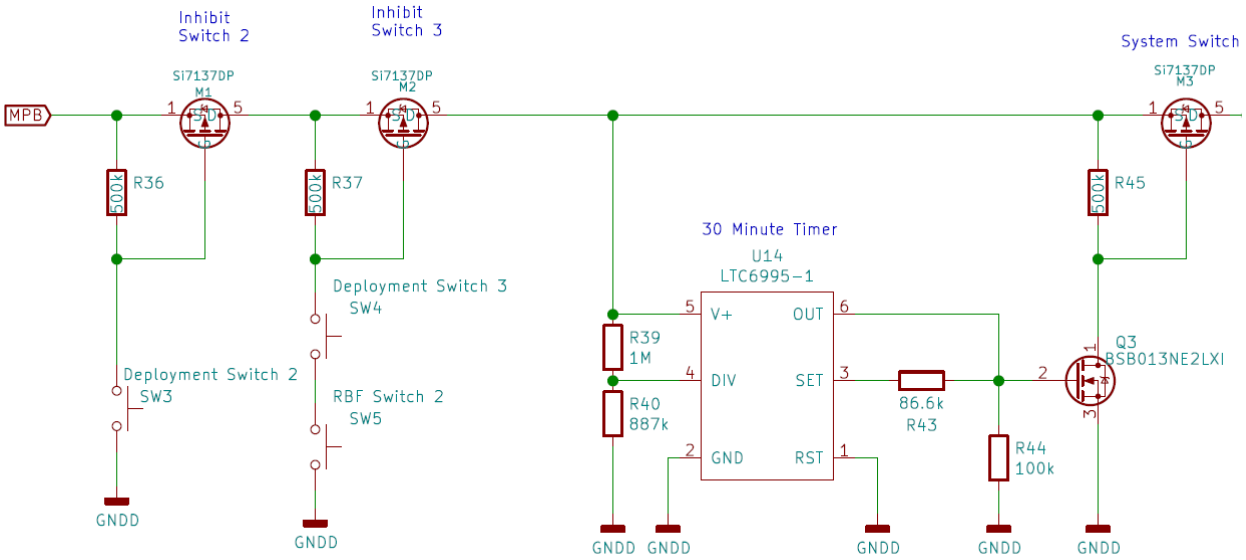


Figure 21. The load side inhibit switches located on the PDU board.

3.3.9 Condition bus voltages to 5 V and 3.3 V

Voltage regulators were selected to optimize efficiency given the constraints of expected input voltage range and maximum output current. The 5V regulator selected is the TPS61232. The TPS61232 is a DC-DC boost converter that is approximately 96% efficient up to 2 A of output current, which is much greater than the expected load on the 5 V bus.

A consideration in selecting the 3.3V regulator was whether to use a buck or buck-boost topology. Since the battery pack voltage will range between 2.8 V and 4.2 V, it makes sense to use a buck-boost topology that can provide 3.3 V over the full range of the battery. A buck converter, on the other hand, could only

provide 3.3V until the input voltage falls below 3.3 V. However, buck converters are more efficient than buck-boost converters. Since the more efficient converter would reduce current drawn from the battery, it's possible that a buck converter could be superior by increasing the time it takes the battery to reach the 3.3V cutoff. An engineer tested both topologies with a lithium ion battery and found, counter-intuitively, that buck converters could power a 3.3V load longer than buck-boost converters[5]. As a result, we selected the TPS62086, a buck converter that is over 95% efficient at the expected current range.

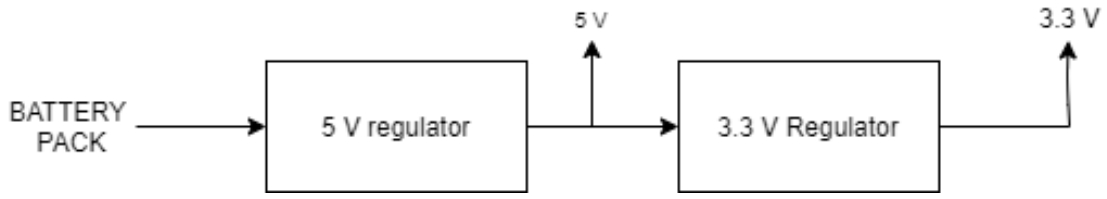


Figure 22. Cascaded regulators.

3.4 Grounding

The grounding configuration of the satellite is critical to ensure the absence of ground loops, where current can take multiple paths through the ground plane, creating a voltage gradient. While designing the grounding architecture of the EPS, we followed the guidelines described in the NASA Technical Handbook .[6] The EPS ground plane will be divided into a digital ground and analog ground that are bridged by the ADC. The digital ground will house high-frequency components such as switching regulators that can lead to a noisy ground plane. The analog ground will house the components that require a low-noise ground plane for sensitive ADC readings. The digital ground will be fed to each subsystem in a star configuration to avoid the daisy-chaining of grounds between subsystems. Lastly, the chassis is only bonded to the ground plane at a single location. All other PCBs will be electrically insulated from the chassis to avoid a ground loop.

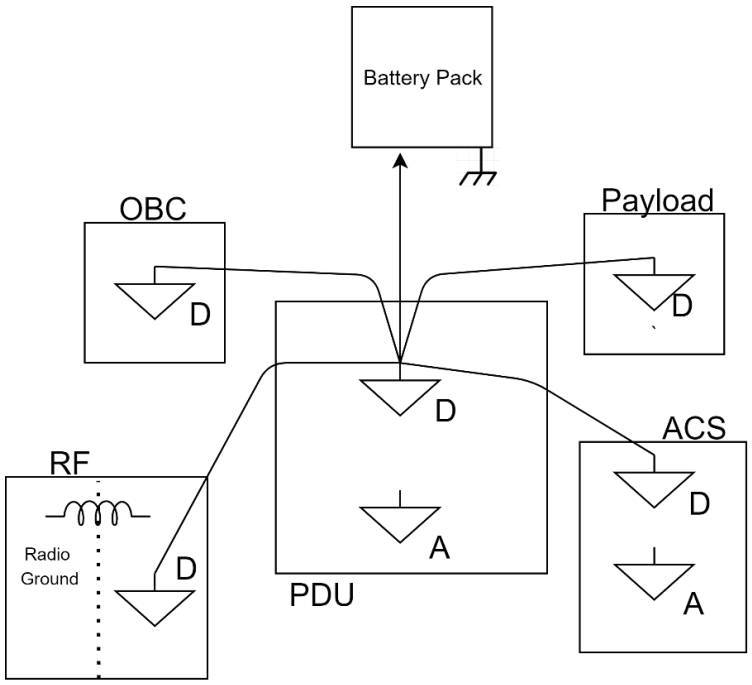


Figure 23. Star Point grounding topology

3.5 Conformal Coating

All of the EPS boards ICs will be covered with a layer of HumiSeal 1A33, a conformal coating that prevents outgassing. Due to its protective effect against outgassing, board components beneath a layer of it do not need to be listed on the Bill of Materials. This conformal coating also provides radiation and thermal stress resistance to the board[10] . Proper application of the coating can be verified with a UV indicator. The HumiSeal 1A33 was chosen due to it not requiring a mix tank or curing agent; it was also recommended by Nanoracks. A 11.5 Oz Aerosol spay can of it cost $31.94 USD.

Figure 24. HumiSeal 1A33 spray can.

3.6 Power Budget

The following power budget was made by each subsystem estimating their power consumption for each mode of operation. The power budget is constantly being updated as more test get completed.

System Breakdown													
		Mode 1: LEOP			Mode 2: FDIR			Mode 3: Safe Hold			Mode 4: Stand By		
Component		D.C %	Power (W)	Total	D.C%	Power (W)	Total	D.C %	Power (W)	Total	D.C %	Power (W)	Total
ADCS	Z+ Sun Sense Board	100%	0.0282	0.0282	100%	0.0282	0.0282	0%	0	0	100%	0.0282	0.0282
	Z- Sun Sense Board	100%	0.105	0.105	100%	0.105	0.105	0%	0	0	100%	0.105	0.105
	ADCS Motherboard	100%	0.16	0.16	100%	0.16	0.16	0%	0	0	100%	0.16	0.16
	Actuatuator Board	100%	0.26	0.26	100%	0.26	0.26	0%	0	0	100%	0.26	0.26
	Reaction Wheels	0%	0%	0	100%	0.00841	0.00841	0%	0	0	100%	0.00841	0.00841
	Magnetorquers	100%	0.0012	0.0012	100%	0.0012	0.0012	0%	0	0	100%	0.0012	0.0012
OBC	GPS	0%	1	0	10%	1	0.1	0%	1	0	10%	1	0.1
	OS	100%	1.24	1.24	100%	1.24	1.24	100%	1.24	1.24	100%	1.24	1.24
RF	nL400	0%	0	0	5.00%	0.0462	0.00231	5.00%	0.0462	0.0023	5.00%	0.0462	0.00231
Payload	Visible	0%	0	0	0.04%	0.85	0.00	0%	0	0	0.04%	0.85	0.00
	NIR	0%	0	0	0.04%	0.85	0.00	0%	0	0	0.04%	0.85	0.00
EPS	MCU	100%	0.1	0.1	100%	0.1	0.1	100%	0.1	0.1	100%	0.1	0.1
	Switches	100%	0.1	0.1	100%	0.1	0.1	100%	0.1	0.1	100%	0.1	0.1
	Regulators	100%	0.1	0.1	100%	0.1	0.1	100%	0.1	0.1	100%	0.1	0.1
Total OAP (W):				3.14			3.31			2.31			3.31
Net OAP with solar intake of 4.38 W				1.24			1.07			2.07			1.07

Figure 25. Power Budget.

4. Simulation

4.1 Battery Pack Charger

The battery pack charger analog comparators were simulated in LTSpice to ensure its configuration toggles the charge/discharge load switches at the correct voltage levels, as shown in Figure 24.

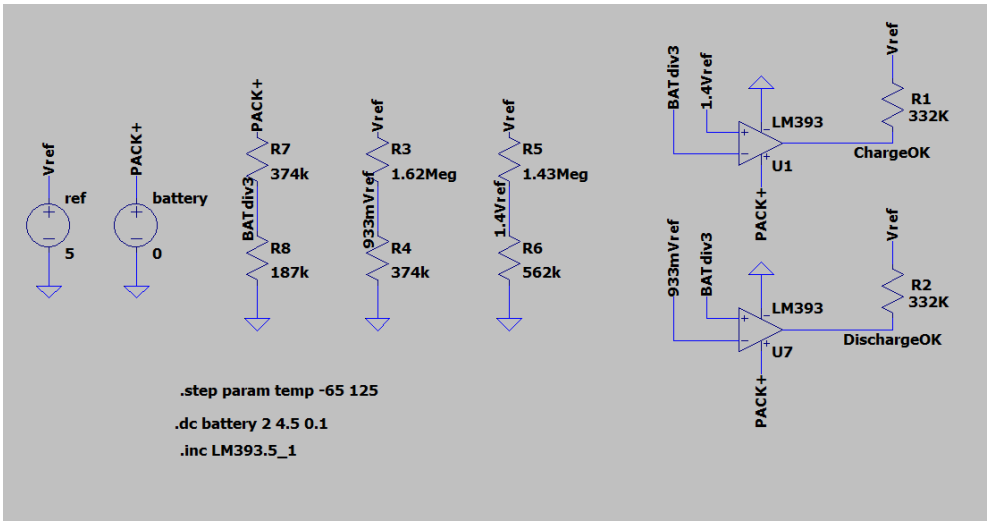


Figure 26. Battery Charger Schematic

The simulation steps the battery voltage from below 2 V to 4.5 V. Configuration of the comparators expect us to see the signals DischargeOK go high at 2.8 V and ChargeOK to go low at 4.2 V. The LTSpice results were positive, as the expected DischargeOK and ChargeOK signals were observed.

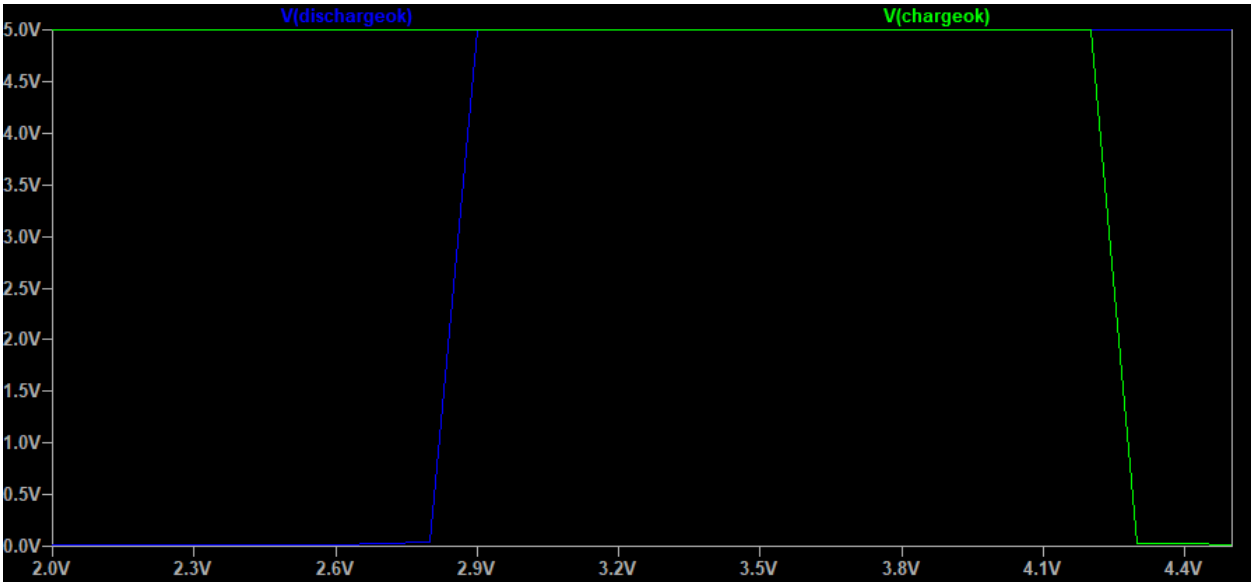


Figure 27. Battery Charging Logic sim.

4.2 Load Side Inhibits Power Loss

The purpose of these simulations were to observe the power loss due to the load side inhibits being in series with the MPB. The simulation was configured to step the MPB current from a light load to a heavy load. The simulation was configured as shown in Figure 26 below.

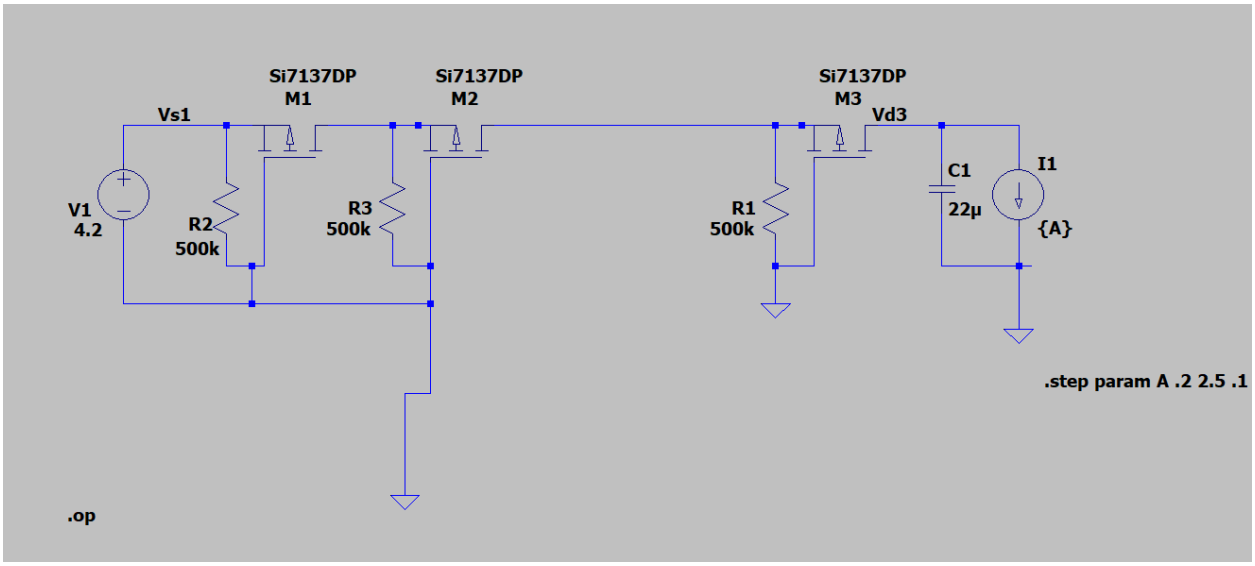


Figure 28. Load Side Inhibit LTSpice configuration.

It was found that while the MPB load is below 1 A the power loss over the MOSFETs is less than 8 mW. This is an acceptable power loss as the nominal current on the main power bus will typically be less than 1 A.

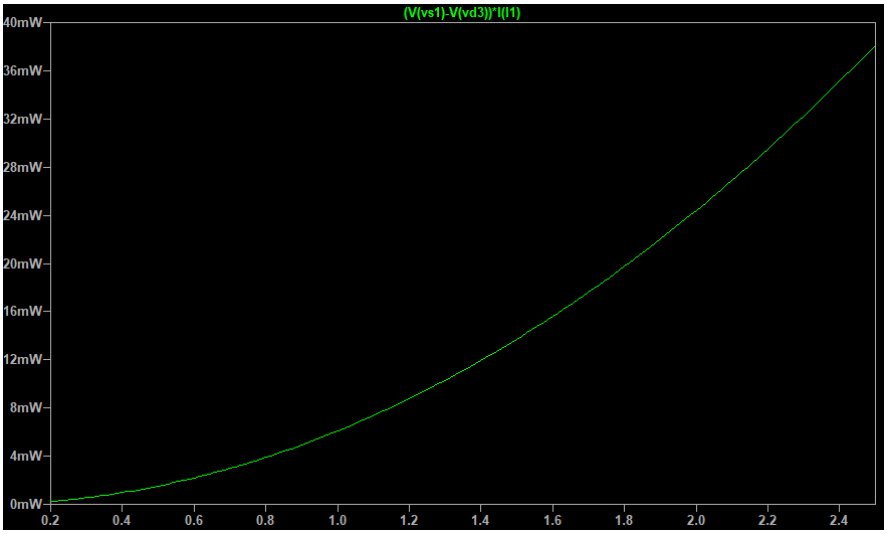


Figure 29. Load Side Inhibits power dissipation.

4.3 Ground Leg Inhibit Power Loss

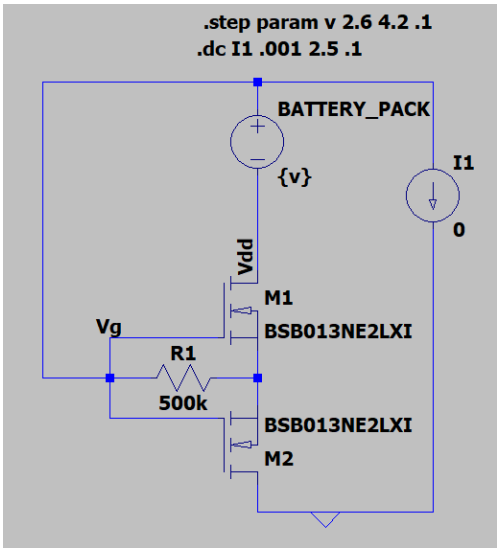


Figure 30. Ground Leg inhibit LTspice configuration.

The ground leg inhibit is two N-channel MOSFETS and its Rds_on will vary as the gate to drain voltage varies. Thus, in this simulation the battery pack voltage was stepped from 2.6 V to 4.2 V in 100 mV increments. For each step, the power loss was plotted for a load that varies from 0 A to 2.5 A.

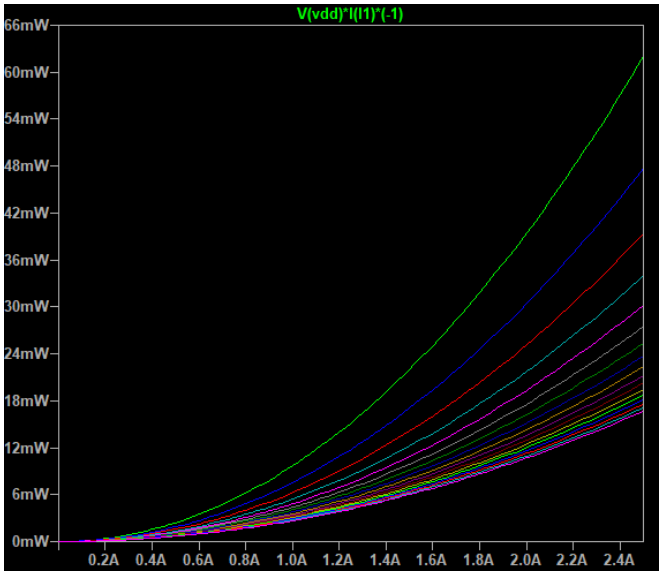


Figure 31. Ground Leg Inhibit Results.

The top green step is when the battery pack voltage is at its lowest value of 2.8 V which correlates to the highest on resistance of the two FETs, i.e. worst case power loss in the ground leg inhibit. It can be seen that it stays below 10 mW up to 1 A. This was deemed acceptable.

5. Prototypes

The source files for the prototype subsections can be found in the folder of this report.

5.1 EPS Prototype 1

The first EPS prototype is shown in Figure 30 and Figure 31, was designed to test several different parts of the EPS: the timer circuit, the battery protection circuitry, and the current-limiting load switch.

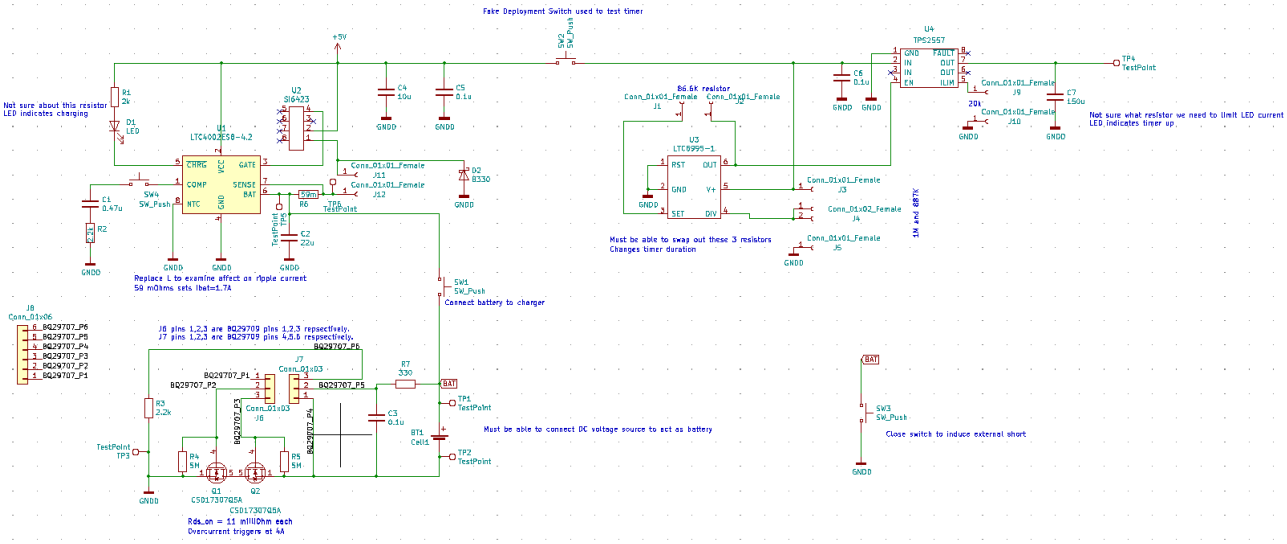


Figure 32. EPS Prototype 1.

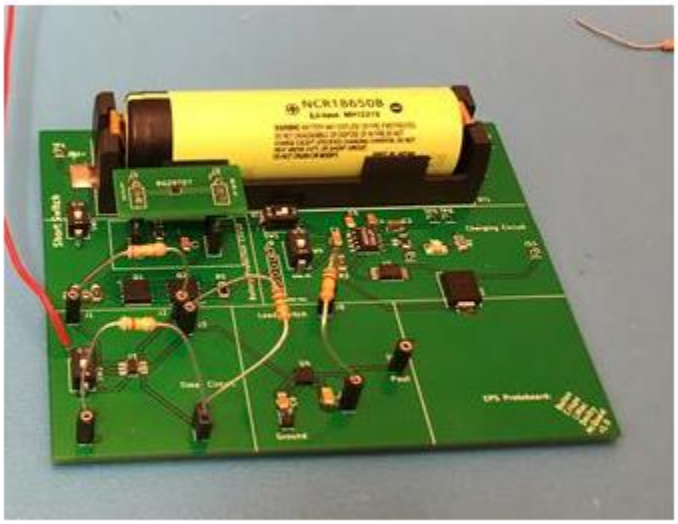


Figure 33. EPS Prototype 1

The first system tested was the LTC6995 timer circuit to determine if it properly inhibits power from the other subsystems for 30 minutes. The timer is configured using resistor enabled voltage dividers to provide specified voltage to the DIV port and placing a specified resistance between the OUT and SET ports. The external resistors that set the timer length used through-hole rather than surface mount form factors so various timer lengths could be tested. For our validation test, we used resistors to program the timer length to one minute. Then, we closed a switch that mimics the string of deployment switches separating the timer circuit from power. Exactly one minute after closing the switch, the timer circuit expired, allowing current to flow past. We considered this test to be a strong success.

The prototype also included the Texas Instruments BQ29709 IC that will provide battery protection against over-voltage, under-voltage and external short circuit conditions. Each condition will be simulated in the lab to ensure the IC functions reliably. These conditions are applied to the prototype through an external DC source, and the IC will be monitored using an oscilloscope attached to the designated test points. These tests have not yet been completed as we discovered an error where the pins of the BQ29707 were incorrectly soldered, causing the circuit to fail the external short-circuit test. We remedied this mistake on the next iteration of the PDU prototype.

The threshold of the TPS2557 current-limiting load switch is set by an external resistor. This component was made to be through-hole, rather than surface mount, to test various current limits. At the output of the load switch, we wired up an ammeter and potentiometer on a breadboard. We lowered the resistance of the potentiometer until it drew current that surpassed the threshold. When we lowered the resistance any further, the load switch reduced the voltage seen at the output while maintaining constant current. The test validated this component for protecting the PDU and other subsystems from short-circuit events, and additionally for providing a second layer of protection to the battery pack against charge over-current and discharge over-current faults.

5.2 MPPT Prototype

The first iteration of the solar cell voltage regulator, shown in Figure 32, was designed to test the SPV1040. The circuit was configurated to regulate the MPPT around 4.16V.

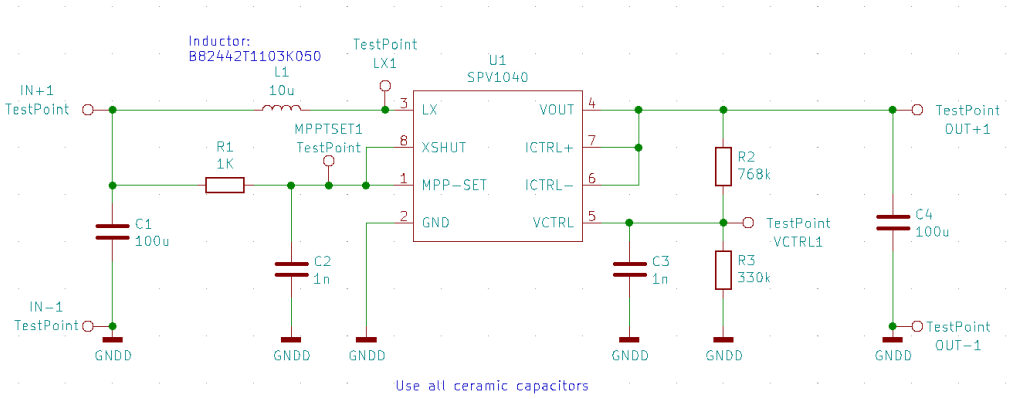


Figure 34. MPPT Prototype.

A solar cell holder breakout board was designed and manufactured to carry out the MPPT test. The solar cell was soldered directly to the breakout board.

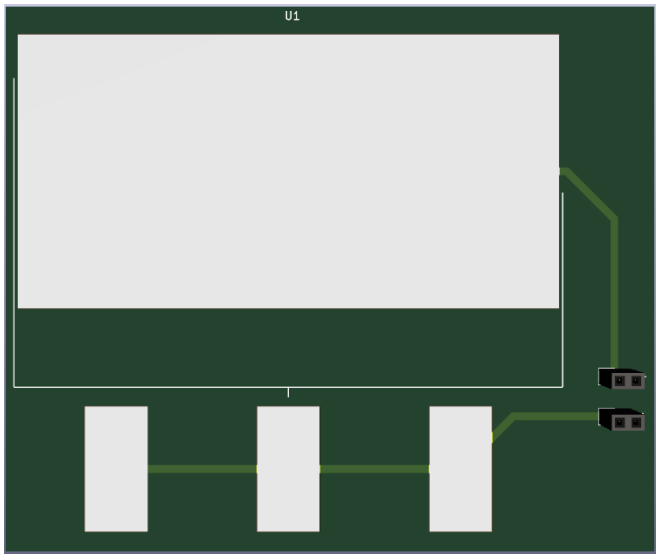


Figure 35. Solar Cell Holder.

A solar simulator was used to test the MPPT circuitry.

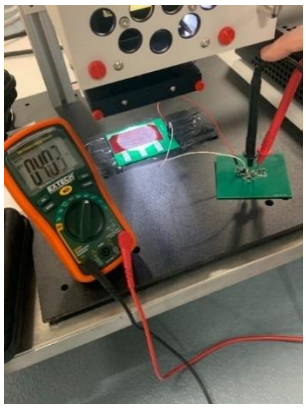


Figure 36. Testing the MPPT circuitry with the solar simulator.

We attribute the small error in output voltage to the fact that high tolerance resistors were used in the prototype and expect the discrepancy to be reduced when low tolerance resistors are employed on the flight model. Even if the output voltage does not increase past 4.03V, we consider this design to be validated due to the relatively flat nature of the lithium-ion battery discharge curve.

5.3 PDUv1 Prototype

The first version of the PDU was ordered. This version did not assemble the reverse side with the MPPT circuitry to reduce the cost of the prototype. The goal of this prototype was to flash the MSP430 with firmware and test the I2C, UART, toggling load switches and taking ADC readings.

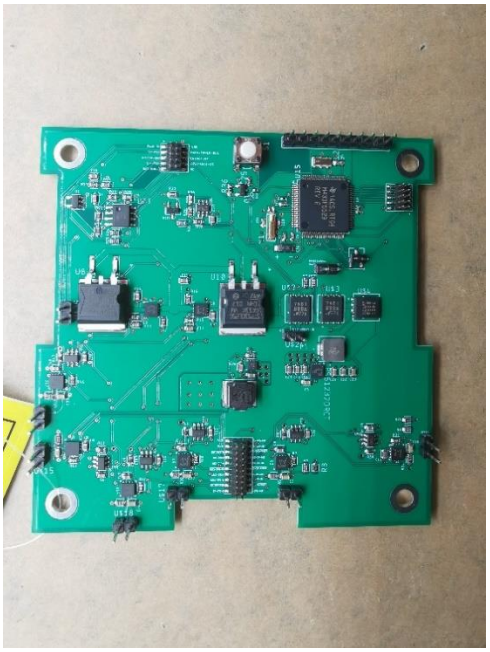


Figure 37. PDUv1 Prototype.

The PDU successfully flashed and was able to interact with PuTTY via its UART lines. No other test have been completed as of now.

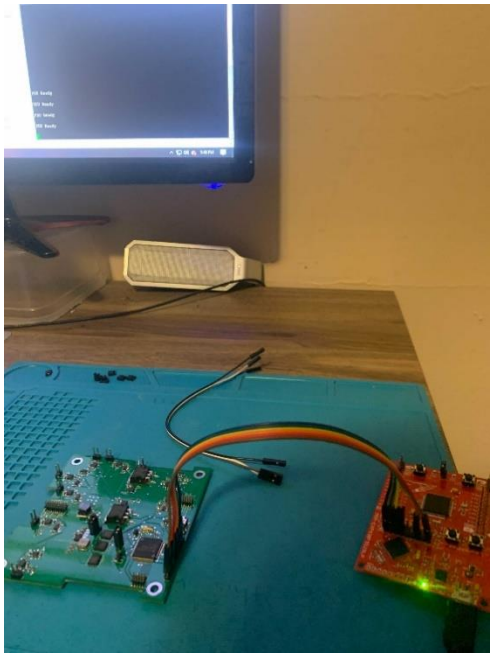


Figure 38. PDU flash.

5.4 Vendors/Procurement

Table 8. List of Vendors

Vendor	Vendor's POC	Vendor's Email	DSS POC	Title
Spectrolab	Alexander, Silvestra	silvestra.alexander@boeing.com	Brandon Allen	Solar Cells
Onlybatteries.com	N/A	N/A	N/A	18650b vendor
Paisley	Richard Beaulieu	richardb@paisley.ca	Brandon Allen	Conformal Coating vendor and EPO-TEK vendor

5.5 BOM

Table 9. Bill of Material

Material	Quantity	Unit Mass	Total Mass (g)	Usage
Panasonic NCR18650b	4	48.5	194	Lithium ion battery cell
FR4 PCB	3	28.3	84.9	Board PCB material
FR4 PCB	8	67	536	side / deployable panel PCB material

HumiSeal® 1A33 Clear Polyurethane Conformal Coating (Aeorosol Can)	-	-	-	Conformal coating
Solithane C113-300	-	-	-	Staking
Solar cell (GaInP2/GaAs/Ge)	28	2.25	63	Solar panel
Kapton Tape	-	-	-	Insulator
EPO-TEK- H20E	-	-	-	Solar panel conductive Adhesive
RTV CV-2943	-	-	-	Thermally conductive paste
Solder wire Sn63Pb37	-	-	-	Solder joints
Kester 186 flux type RMA	-	-	-	Flux
3M™ Scotch-Weld™ Epoxy Adhesive EC-2216 B/A Gray	-	-	-	Epoxy
TE M22759/33-22-# Crosslinked ETFE 22 AWG Wire	-	-	10	Wire used for power lines

5.6 Prototyping Schedule

Table 10. Prototyping Schedule

Milestone	Subtasks	Deadline	NOTE
PDU Prototype Testing		End of April 2021	
	Complete all PDU related test that are document in the EPS test plan doc.	End of March 2021	
	Revise changes and order next version of the PDU.	End of April 2021	
Battery Pack			
	Order full battery pack prototype	End of March 2021	
	Complete all battery pack test in the EPS test plan doc.	End of May 2021	
Assemble Flight Model Solar Arrays		End of July 2021	
	Test flight model Solar Arrays	End of July 2021	

6. Test Plan

6.1 Battery Test Plan

1. Required Test Procedures – Physical and Electrochemical Characteristics
    1. Serialize all cells
    2. Test Documentation

Record as much of the following data for each cell:

- Manufacturer
- Cell model number
- Date of manufacture
- Cell chemistry
- Electrolyte type
- Date of testing
- Temperature/humidity during testing

3. Visual Inspection

Inspect cells for any deformations including scrapes, bulges, and dents. Remove cell wrapping prior to inspection.

4. Measure Physical Properties
    A. Record the length, width, and height of the cell with 0.1mm precision.

B. Record the mass of the cell with 0.1g precision.

5. Measure Electrochemical Properties

A. Measure the Open Circuit Voltage of the fully charged cell with 0.1V precision.

B. Discharge the fully charged battery at C/2 and measure the Closed-Circuit Voltage after 30 seconds.

C. Discharge each cell at constant voltage to 2.5V and terminate the discharge when current tapers below C/100. Record OCV at discharge termination. Rest cell for 14 days while recording the OCV of the cell on days 1, 3, 7, 10, and 14. Cells with OCV declining >2.0mV shall be rejected.

2. Charge Cycling

Charge cycling procedures include the following cycle order:

- Charge
- Discharge
- Charge
- Discharge
- Charge

Monitor cell voltage, current and temperature during charging and discharging. Wait ten minutes between charge and discharge cycles. After the final charge cycle, record OCV and capacity.

A. A charge cycle consists of charging the cell to 4.2V using a current of C/2. Then hold the cell at 4.2V until the charge current drops to below 65mA.

B. A discharge cycle consists of discharging the cell at C/2 until the voltage drops to below 2.5V.

3. Vibration Test Procedure

Record OCV for each cell before vibration testing and between each axis of vibration. Vibration testing shall follow the spectrum outlined in Table 11 for one minute on each axis.

Table 11. Vibration Testing Spectrum

Frequency (Hz)	**ASD (G2/Hz)**	**dB/OCT**	**Grms**
20.00	0.028800	*	*
40.00	0.028800	0.00	0.76
70.00	0.072000	4.93	1.43
700.00	0.072000	0.00	6.89
2000.00	0.018720	-3.86	9.65

After vibration testing, perform the charge cycling procedure outlined in Section 2. Cells with more than 0.1% change in OCV and/or 5% change in capacity shall be rejected.

4. Vacuum Test Procedure

    A. Record length, width, and height of each cell to 0.1mm precision.

    B. Record the mass of each cell to 0.1g precision.

    C. Fully charge each cell and record the OCV.

    D. Place charged cells in vacuum chamber and pull vacuum at 8 psi/minute. Maintain vacuum (approximately 0.1 psia) for 6 hours. Re-pressurize chamber to ambient at 9 psi/minute.

    E. Visually inspect cells for leaks, deformations, or bulges. Record any findings.

    F. Record length, width, and height of each cell to 0.1mm precision post-vacuum testing.

    G. Record the mass of each cell to 0.1g precision post-vacuum testing. Cells with change of mass greater than 0.1% shall be rejected.

    H. Complete the charge cycling procedure outlined in Section 2. Cells with more than 0.1% change in OCV and/or 5% change in capacity shall be rejected.

5. Cell Matching and Battery Pack Assembly

Assemble 1S4P battery pack out of cells that passed acceptance screening. Cells that pass acceptance screening shall be matched based on capacity, impedance, and OCV. The remainder of the tests shall be completed at the pack-level with protection circuitry implemented.

6. Over-charge Procedure

    A. Over-charge the battery to 5.0V with current of 1C and record the voltage at which the battery protection activates to open the charging circuit.

    B. Discharge the battery at C/5 and record the voltage at which the protection circuitry resets.

7. Over-discharge Procedure

    A. Over-discharge battery at 1C and record the voltage at which the protection circuit opens.

    B. Charge the battery at C/5 and record the voltage at which the protection circuitry resets.

8. External Short Procedure

A. Apply an external short to the battery and demonstrate that the protection circuitry will open the circuit and remain open until the short is removed.

B. Record the time it takes for the protection circuitry to open the circuit after the external short is applied. Circuitry shall respond within 100ms or alternately function fast enough to prevent damaging the battery.

9. Circuit Schematic Analysis

Provide the protection circuitry schematic and a description of how it works including operating parameters and set points.

10. Reporting

Prepare a Battery Acceptance Test Report to document the acceptability of the cells/battery to be flown. Include all of the above data including test set-up and details and all results. Additionally, include photo documentation which accurately displays the test activity. The report shall be dated, signed, and approved by the appropriate program authority.

6.2 Test Plan Procedure

The full EPS test plan can be found in the folder of this document. Attaching it as a appendix is not feasible for viewing.

7. EGSE

Table 1. Electrical Ground Support Equipment.

Equipment Name	Part Number (if applicable)	Purpose
Oscilloscope		Testing and Troubleshooting
Adjustable DC power supply		
Umbilical Battery Connection		To be able to charge battery on ground.
Umbilical Serial Connection		Connecting the PDU to a computer terminal for bebugging.
Remove Before Flight Pin		To electrically inhibit the battery pack from the rest of the satelite.
1000 W LED light	B07RPVPN2H	For testing solar panels
Halogen Portable Work Lamp - 500 W	Model #XG-1009-Y Item #000379697 (Rona)	For testing solar panels

8. Power System Requirements

[SYS-POW-010] The spacecraft power generation system shall be made of solar arrays and batteries and shall cope with the power needs of the various spacecraft subsystems as required.

[SYS-POW-020] The Power subsystem shall generate, store, manage, and distribute power to support payload and housekeeping operations throughout all mission phases.

[SYS-POW-030] The spacecraft battery shall store a minimum 40 Whr of electrical power to operate the payload and subsystems when solar power is not available.

[SYS-POW-031] The spacecraft battery shall be sized for worst case eclipses.

[SYS-POW-032] Total chemical energy stored shall not exceed 80 Whr as specified by Nanoracks in [AD4].

[SYS-POW-040] The battery pack must contain integrated protection against over-charge, over-discharge, short-circuit, charge over-current, and discharge over-current events.

[SYS-POW-050] The battery pack must be integrated with an external charging port that can charge the battery pack after is integrated into the satellite.

[SYS-POW-051] The external charging port must not provide power to any of the loads.

[SYS-POW-060] Test batteries shall be used during ground test activities.

[SYS-POW-061] Flight batteries shall be included in final spacecraft level testing.

[SYS-POW-070] Removed

[SYS-POW-080] While in a cold launch configuration, the batteries shall be capable of holding a charge for 9 months with a resulting DoD of no more than 50%.

[SYS-POW-090] The PDU shall have centralized power distribution.

[SYS-POW-100] The PDU shall perform power conditioning, switching, internal monitoring and reporting of voltage and current.

[SYS-POW-110] The PDU shall include necessary over voltage, over current, and under voltage protection.

[SYS-POW-120] The PDU shall provide regulated 3.3±0.2V and 5±0.2V supply.

[SYS-POW-130] The PDU shall provide all necessary telemetry data to the OBC.

[SYS-POW-140] The PDU shall supply at least 10 W during transient power-intensive operations such as during downlink.

[SYS-POW-150] The PDU shall supply at least 4 W during nominal operations.

[SYS-POW-160] Each power line shall provide an appropriately sized resettable latching current limit equal to 150% of max expected load for each circuit.

[SYS-POW-170] Each power channel shall be capable of being turned on and off in response to commands from the OBC.

[SYS-POW-180] The power subsystem shall include a minimum of three inhibit switches that keep the satellite in a powered-down state.

[SYS-POW-181] The PDU shall provide power to the loads at least 30 minutes after all three inhibit switches are closed.

[SYS-POW-182] If any of the three inhibit switches are toggled during the 30-minute period, the timer must reset.

[SYS-POW-190] The power subsystem shall be in a power off state while integrated in the CubeSat deployer from the time of delivery to the Launch Vehicle (LV) through on-orbit deployment.

[SYS-POW-200] LORIS shall have a remove before flight (RBF) feature or an apply before flight (ABF) feature that keeps the satellite in an unpowered state throughout the ground handling and integration process into the deployer.

[SYS-POW-201] The RBF pin shall cut all power to the satellite once it is inserted into the CubeSat Deployer.

[SYS-POW-202] The RBF pin shall be removed after integration into the CubeSat Deployer.

[SYS-POW-210] The RBF pin shall protrude no more than 6.5 mm (TBC) from the rails when it is fully inserted into the satellite.

[SYS-POW-220] The power subsystem shall be designed to be free of any grounding issues that affect the performance of the components.

[SYS-POW-230] The solar panels shall have an operational lifetime of at least 1.5 years

[SYS-POW-231] The solar panels shall be at least 25% efficient at end of life.

[SYS-POW-232] The solar panels shall have an End Of Life (EOL) of 2 years.

[SYS-POW-240] The power subsystem shall provide the grounding and bonding interface between connected systems with no shorts between ground lines and power supply lines.

[SYS-POW-250] The power subsystem shall have a mass that does not exceed 500 g.

[SYS-POW-260] During the pre-launch phases, the satellite shall receive power from the EGSE via the spacecraft umbilical.

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