# **CSE 620:**

# **Project: HDL Test bench**

**ALU Test bench**

**Deliverables:**

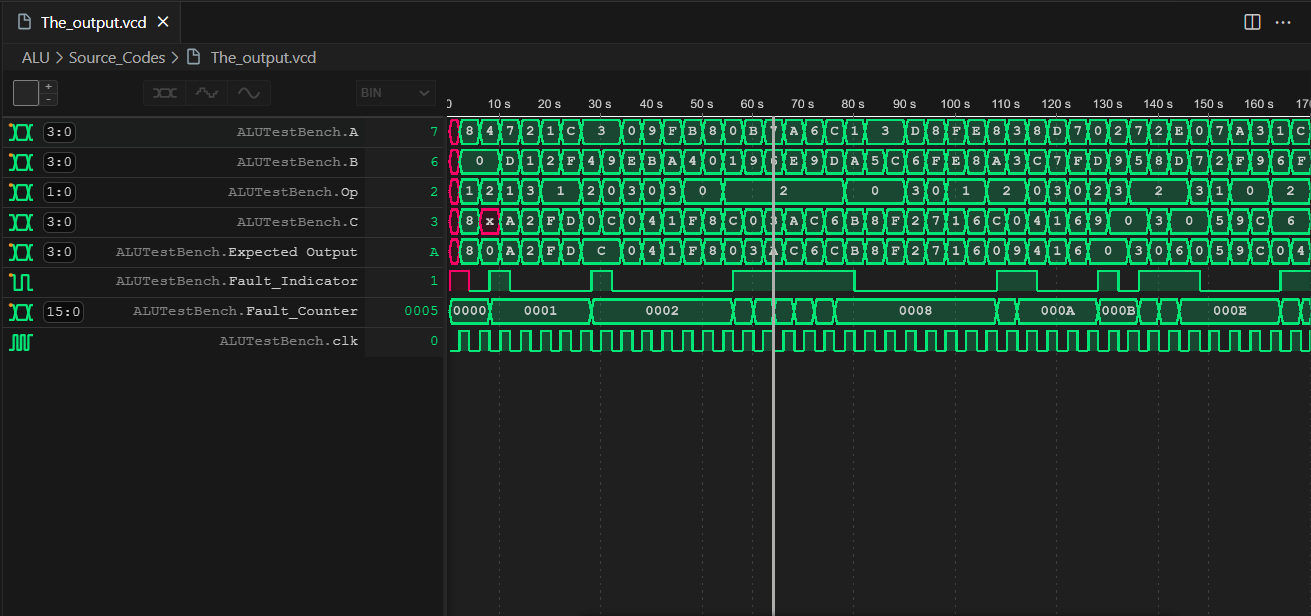
1. **Design example name and location in the slides**

Design Example name: ALU.

Location: Example 8, page 13-14, VHDL Combinational logic modeling slides.

The code is converted to Verilog and attached.

1. **Test strategy**
2. Creating a python scripts to create test vectors in text file, scan the file and insert the data into a 2D Array and testing the actual results vs the once in the test vectors, I set the two operands (A, B and the operation Op) and observe the result comparison.
3. Observing the output (C) which represents the operations done in an orderly fashion (add, subtract, multiply and division) and observing the signal “Fault\_Indicator”.
4. “Fault\_indicator” signal is 1 if there is a fault detected, and 0 otherwise.
5. Expected results: the output is correct for all operation
6. Actual results: the output is correct for addition and subtraction, but the output for multiplication is shifted by one and the division by zero is not handled.
7. **Simulation results**

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1. **Names of all used tools**

* I Verilog (Verilog open source Compiler)
* Vscode (Code Editor)
* Wave tracer extension for VSCode
* Python
* PowerShell

***End of Assignment***