# **CSE 620: Advanced Computer Architecture**

# **Project: HDL Test bench**

**Digital System Modeling using HDL**

**Counter Test bench**

**Deliverables:**

1. **Design example name and location in the slides**

Design Example name: Counter.

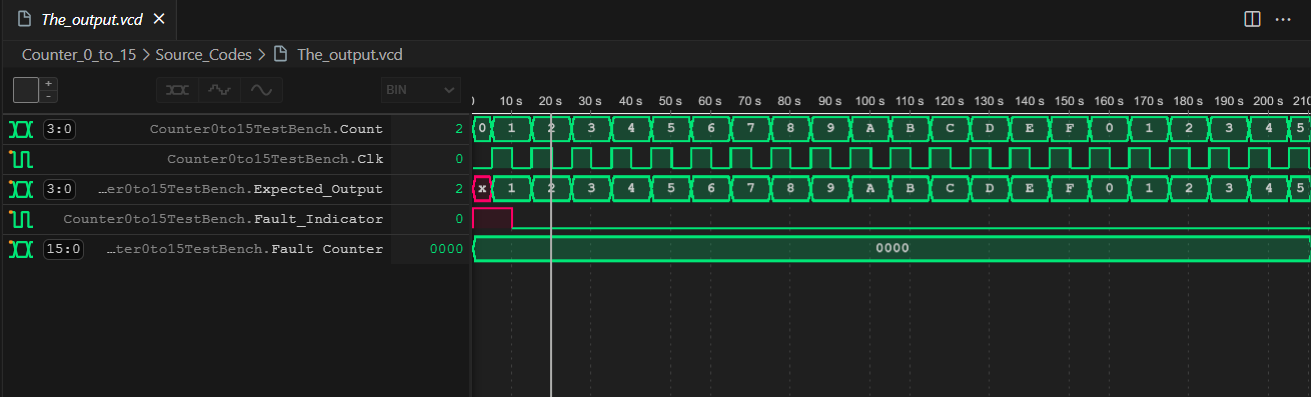
Location: Example 9, page 15 VHDL Combinational logic modeling slides.

The code is converted to Verilog and attached.

1. **Test strategy**
2. Generate a clock.
3. Generate a test vectors in a Text file in specific order.
4. Read that text file and push it to 2d Array.
5. Testing the result vs, the test vector.
6. Observe the output (count) for 2 behaviors, first one: the counter should start from 0 to 15 sequentially, second one: overflow should make the counter to start from 0 again.
7. Observing “Fault\_Indicator” signal if equals to 1 then fault detected.
8. Expected results: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, a, b, c, d, e, f and 0.

Actual results: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, a, b, c, d, e, f and 0.

1. The expected and actual are the same, thus verifies the functionality of the design.
2. **Simulation results**

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1. **Names of all used tools**

* I Verilog (Verilog open source Compiler)
* Vscode (Code Editor)
* Wave tracer extension for VSCode
* Python
* PowerShell

***End of Assignment***