# **CSE 620: Advanced Computer Architecture**

# **Project: HDL Test bench**

**Digital System Modeling using HDL**

**Counter Test bench**

**Deliverables:**

1. **Design example name and location in the slides**

Design Example name: Counter.

Location: Example 9, page 15 VHDL Combinational logic modeling slides.

The code is converted to Verilog and attached.

1. **Test strategy**
2. Manually start the clock (clk).
3. Observe the output (count) which represents the counter and it should increment at each rising edge of the clock then reset (the count is a register with 4 bits, at each clock cycle their values update).
4. Expected results: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, a, b, c, d, e, f and 0.

Actual results: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, a, b, c, d, e, f and 0.

1. The expected and actual are the same, thus verifies the functionality/behavior of the design.
2. **Simulation results**

Refer to the file name: “Counter0to15TestBench.bmp”

1. **Names of all used tools**

ModelSim PE student edition

***End of Assignment***