# **CSE 620: Advanced Computer Architecture**

# **Project: HDL Test bench**

**Digital System Modeling using HDL**

**Mux Test bench**

**Deliverables:**

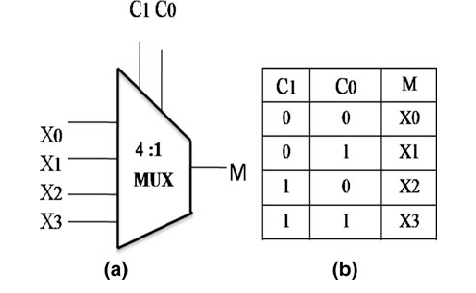
1. **Design example name and location in the slides**

Design Example name: Mux.

Location: Example 9, page 15 VHDL Combinational logic modeling slides.

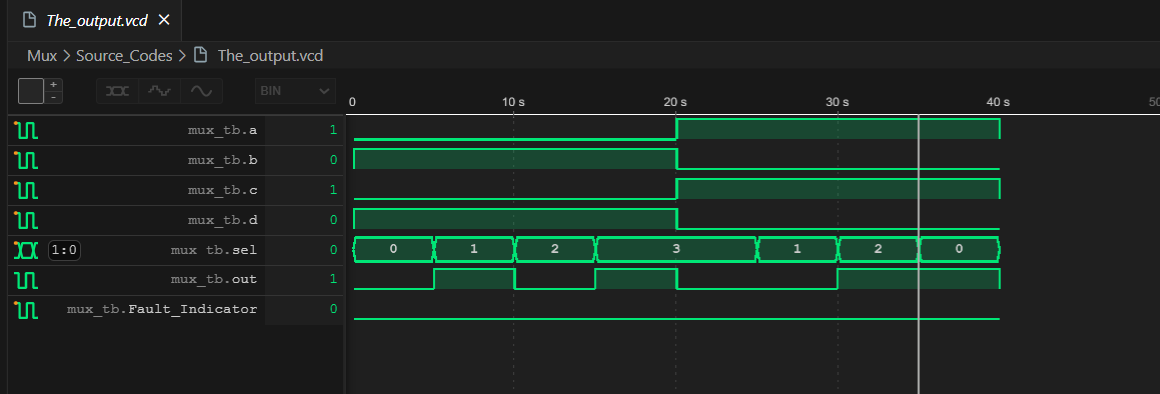
The code is converted to Verilog and attached.

1. **Test strategy**
2. Manually Generate a test vectors in the test bench to cover all possible cases for input sel.
3. Compare results in actual output signal “out” and expected output signal in the test cases and adjust a “Fault\_Indicator” signal to be used as flag.
4. Observing “Fault\_Indicator” signal if equals to 1 then fault detected.
5. Expected results: sel and out signals should follow this truth table of half adder



Actual results: the results match and no fault detected. Also the don’t care input is handled to by a default value (sel = 3).

1. The expected and actual are the same, thus verifies the functionality of the design.
2. **Simulation results**

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1. **Names of all used tools**

* I Verilog (Verilog open source Compiler)
* Vscode (Code Editor)
* Wave tracer extension for VSCode
* Python
* PowerShell

***End of Assignment***