# **CSE 620:**

# **Project: HDL Test bench**

**T Flip Flop Test bench**

**Deliverables:**

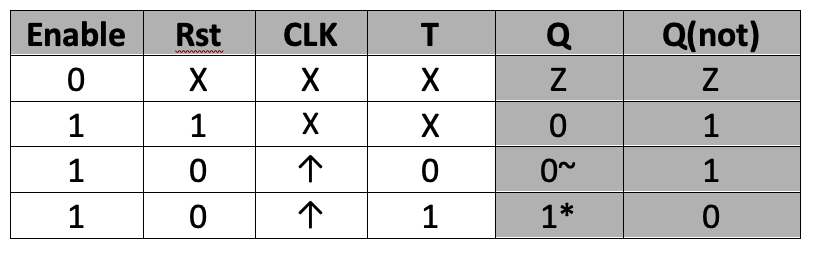
1. **Design example name and location in the slides**

Design Example name: T Flip Flop.

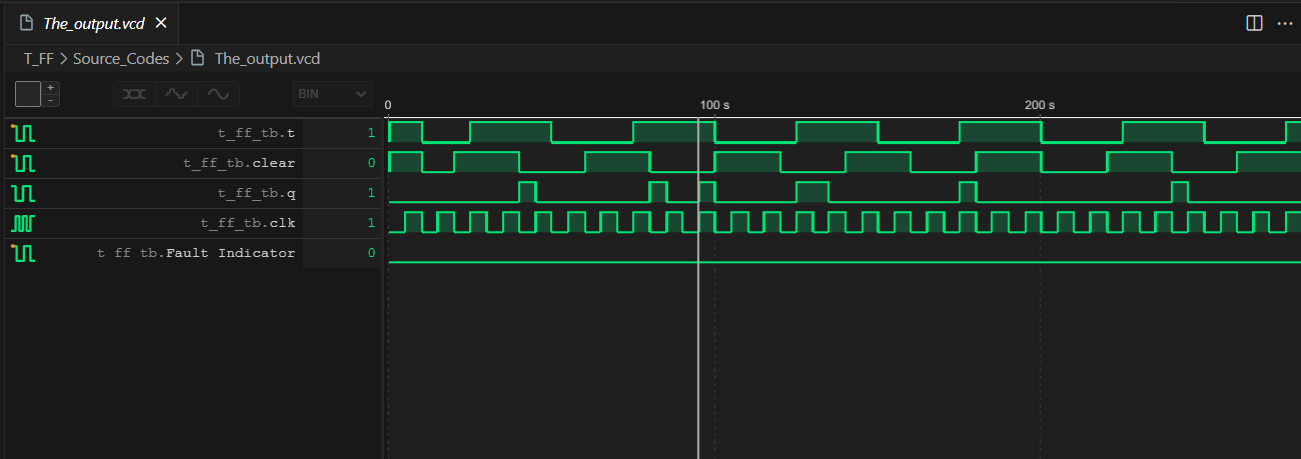
Location: Example 9, page 15 VHDL Combinational logic modeling slides.

The code is converted to Verilog and attached.

1. **Test strategy**
2. Generate an automatic and random input signals for (Clear, T) and generate uniform clock signal.
3. Generate a test vectors
4. Testing the Result VS, the test vector and verify that they are matched.
5. Observe the output (Q) Signal and generate “Fault\_Indicator” signal to detect any fault occur.
6. Observing “Fault\_Indicator” signal if equals to 1 then fault is detected.
7. Expected results: the results should follow this truth table of T FF



1. Actual results: the output signal Q follows it.
2. The expected and actual are the same, thus verifies the functionality of the design.
3. **Simulation results**

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1. **Names of all used tools**

* I Verilog (Verilog open source Compiler)
* Vscode (Code Editor)
* Wave tracer extension for VSCode
* Python
* PowerShell

***End of Assignment***