ECE437/CS481 COMPUTER OPERATING SYSTEMS

Final Exam

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I. Single Choice (2 points/question)

1 One solution to the problem of external fragmentation problem in memory management is to:

[✓ a) permit the logical address space of a process to be noncontiguous]

b) permit smaller processes to be allocated memory at first

c) permit larger processes to be allocated memory at last

d) all of the mentioned

2. When the memory allocated to a process is larger than the memory requirement of the process, then:

[✓ a) internal fragmentation occurs]

b) external fragmentation occurs

c) both internal and external fragmentation occurs

d) neither internal nor external fragmentation occurs

3. Physical memory is broken into fixed-sized blocks called__________:

[✓ a) frames]

b) pages

c) blocks

d) none of the mentioned

4. Logical memory is broken into blocks of the same size called _________?

a) frames

[✓ b) pages]

c) backing store

d) none of the mentioned

5. The __________ in a logical memory address is used as an index into the page table.

[✓ a) page number]

b) page offset

c) frame offset

d) none of the mentioned above

6. If the total size of logical address space is 2^m Bytes and a page size is 2^n Bytes, then the first _____ bits of a logical address designate the page number, and the next ____ bits of a logical address designate the page offset.

a) m, n

b) n, m

c) m – n, m

[✓ d) m – n, n]

7. When the valid-invalid bit in the page table is set to valid, it means that the associated page/frame:

[✓ a) is in the TLB]

b) has data in it

c) is located in the main memory

d) is located in the hard drive

8. If the logical address space of the system is 2^{64} Bytes, the size of a single-level page table for a process would be very large. Assume that the current physical memory size is 4 GB. Possible way(s) to reduce the size of page tables for the process is:

a) a multi-level paging memory management

b) an inverted page memory management

c) a hashed inverted page table memory management

[✓ d) all of the mentioned]

9. In the inverted page memory management, if the system applies 32-bit processors (i.e., 32 bits are used to address the logical memory space) and the total physical memory size is 8GB, then how many entries does the inverted page table have (Note that the frame/page size is 4KB)?

8GB ↓ 8,589,934,592B ↓ $2^{33}B$ ↓ $2^{33}B$

a) 2^{32}

[✓ b) 2^{21}]

c) 2^{33}

d) 2^{20}

4KB= 4096B ↓ $2^{12}B$

$$= \frac{2^{33}B}{2^{12}B}$$

$$\boxed{= 2^{21}B}$$

10. In segmentation, each logical address is specified by:

[✓ a) a segment number & offset]

b) an offset & value

c) a value & segment number

d) a key & value

11. Which of the following information must not be included in a single-level page table:

a) Frame number

b) Process ID

c) Valid/Invalid bit

[✓ d) None of the above]

12. A multilevel page table is preferred in comparison to a single level page table for translating virtual address to physical address because:

[✓ a) it reduces the memory access time to read or write a memory location]

b) it helps reduce the size of page table needed to implement the virtual address space of a process

c) it is required by the translation lookaside buffer

d) it helps reduce the number of page faults in page replacement algorithms

13. In order to enable the CPU to control I/O devices, each I/O device controller contains ______

a) control register

b) status register

c) data register

[✓ d) all of the mentioned]

14. In the I/O device addressing scheme, if we have to use two different types of instructions to access the main memory and I/O devices, respectively, then this kind of I/O device addressing scheme is called:

a) Memory-mapped I/O

[✓ b) Standard I/O]

c) Programmed I/O

d) Interrupt I/O

15 If the OS tries to swap a desired page (which is currently located in the hard drive) in the main memory and the main memory does not have any available frame, then the page replacement method is used to select a suitable page to be swapped out of the main memory such that the related frame can be used to store the desired page. Now, assume that the optimal page replacement is used. Initially, none of the pages are in the memory and there are totally 4 free frames in the memory. The reference string is 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5. Then, what is the page fault rate?

[✓ a) 1/3]

$\frac{4}{12} = 1/3$ ⇒ free
↓
Page fault rate

b) 1/2

c) 1/4

d) None of the mentioned

II. Right (√) or Wrong (×) (2 points/question)

1. Kernel memory allocation and user space memory allocation are very similar, i.e., the paging method can be applied to both. (X)

2. The AMD64 paging system only uses 48 bits to address virtual memory space. (✓)

3. Translation Lookaside Buffer (TLB) is considered as a fast-lookup cache to hold recent/popular page table entries. (✓)

4. In most of the paging systems, each process has its own page table. However, in the Inverted Page Table system, all the processes share the same inverted page table. (X)

5. There are different types of disk I/O scheduling algorithms that have been proposed, e.g., Shortest-service-time-first, Scan, circular SCAN, etc. The objective of these scheduling algorithms is to minimize the rotational latency of accessing contents in a hard disk. (X)

→ should be seek time

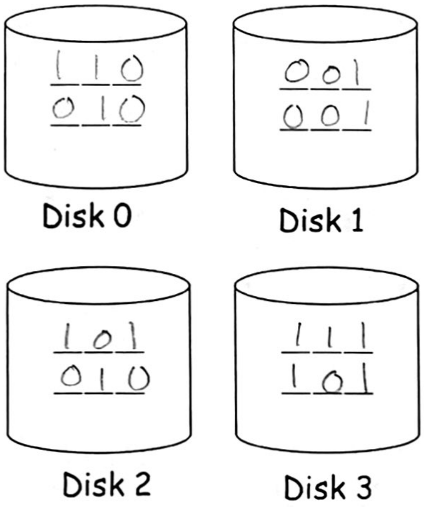
6. As the degree of multiprogramming increases (i.e., more processes will be brought into the main memory), the CPU utilization will monotonically increase. ( )

III. Fill in the blank (2 point/blank)

1. In RAID level-5 system (Block Interleaving with Distributed Parity), striping unit=3 bits. If we try to sequentially store 6 files into the RAID system, where

File-1: 110, File-2: 001, File-3: 101; File-4:001; File-5: 010, File-6: 101,

Then, how the contents of files will be distributed into the following 4 disks? (Note that the parity disk is picked based on a round-robin manner, starting at Disk 3, *i.e., Disk 3, Disk 0, Disk 1, Disk 2...*). ----4 blanks



2. Page tables are used to translate logical memory addresses into physical memory addresses. If the single-level page table scheme is applied, how many memory accesses are required for each load/store operation (if Translation Lookaside Buffer is not considered)? n - level requires n+1 memory accesses
in single level → 2 memory accesses

If the three-level page table scheme is applied, how many memory accesses are required for each load/store operation (if Translation Lookaside Buffer is not considered)? 3+1 => 4 memory accesses

If the hashed inverted page table scheme is applied, how many memory accesses are required for each load/store operation (if Translation Lookaside Buffer is not considered)? 2 memory accesses

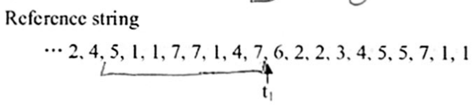
$m=3$
$n=?$
$m+n \leq 2^n$
$3+3 \leq 2^3$
$6 \leq 8$ ✓

3. In RAID level-2 system (Bit Interleaving of Data with HECC (Hamming Error Correcting Code)), if there are 3 data disks, how many check disks are needed? 3 check disks are needed

4. Consider the case that system has a 32-bit logical address space and the page size is 4 KB. If the single-level page table scheme is used for the paging, then there are 2^{20} entries in a page table. If the two-level page table scheme is used for the paging and the first 10 bits of the logical address are used to index the outer page table of a process, then there are 2^{10} entries in an inner page table of the process. Assume that each entry of the inner and outer page table needs 4 Bytes memory space. If a process needs 4MB memory space to store its data and instructions, then how many memory spaces are needed for storing the outer page table and inner page table(s) of the process? Outer page requires 4KB. Inner page requires 4MB.

5. Assume that there are totally 4 free frames in the main memory and the reference string is: 1, 2, 3, 4, 1, 2, 5. All the memory pages are initially stored in the hard drive. Which pages will finally be in the memory if the FIFO page replacement algorithm is used? 1, 2, 3, 5

6. The working set model is used to estimate which pages are needed for the running processes in the near future. If the working set window is 8 and the reference string is shown in the following figure, $\Delta = 8$



then what is the working set at time slot t_1? $WS(t_1) = \{1, 4, 5, 7\}$

single

$$\frac{2^{32}}{4kB} = \frac{2^{32}B}{2^{12}B} = 2^{20} \text{ entries}$$

two

4 bytes per table

$4 \cdot 2^{10} = 4kB \Leftarrow$ outer table

$4 \cdot 2^{10} \cdot 2^{10} = 4MB \Leftarrow$ inner table

2^{10} entrys $\Leftarrow$ outer page

2^{10} entrys $\Leftarrow$ inner page

IV. General Questions

1. In the paging system, assume that the logic address space is 2^{16} Bytes and the size of a page is 2 KB.

a) What is the format of the logical/virtual address? (2p) $m=16$, $n=2KB=2^{11}B$

$n=11$

p	d
5	11

$=m-n$
$=16-11$
$=5$
$n=11$

b) Given the following page table,

Page Number	Frame Number
1	6 (0110)
2	4 (0100)
3	8 (1000)
4	9 (1001)
5	1 (0001)
6	5 (0101)
7	2 (0010)
8	3 (0011)

Please convert the following logical address into physical address in the hexadecimal format (8p)

Logical Address	Physical Address (in hexadecimal)
0x1032	0x 7432
0x2164	0x D964
0x28AC	0x 68AC
0x397B	0x C17B

Logical

	Page #	Offset	Frame #
0x1032 =	0001 0	000 0011 0010	11101
0x2164 =	0010 0	001 0110 0100	11011
0x28AC =	0010 1	000 1010 1100	11010
0x397B =	0011 1	001 0111 1011	11000

Physical

1.) 1110 1000 0011 0010 → 0x7432

2) 1101 1001 0110 0100 → 0xD964

3) 1101 0000 1010 1100 → 0x68AC

4) 1100 0001 0111 1011 → 0x C17B

2. The buddy system is used for the kernel memory management. Assume that the total available kernel memory space is 2MB. There are three incoming memory requests, A, B, and C. The requested kernel memory size of the three requests are 100 KB, 390KB, and 450KB, respectively. The kernel will assign the memory space to the three requests sequentially.

a) Please fill out the following graph to show where are the three requests allocated by applying the buddy system. Note that the left-side buddy has the higher priority to be allocated to the request than the right-side buddy. (3p)

2 MB kernel memory space = 2048 KB

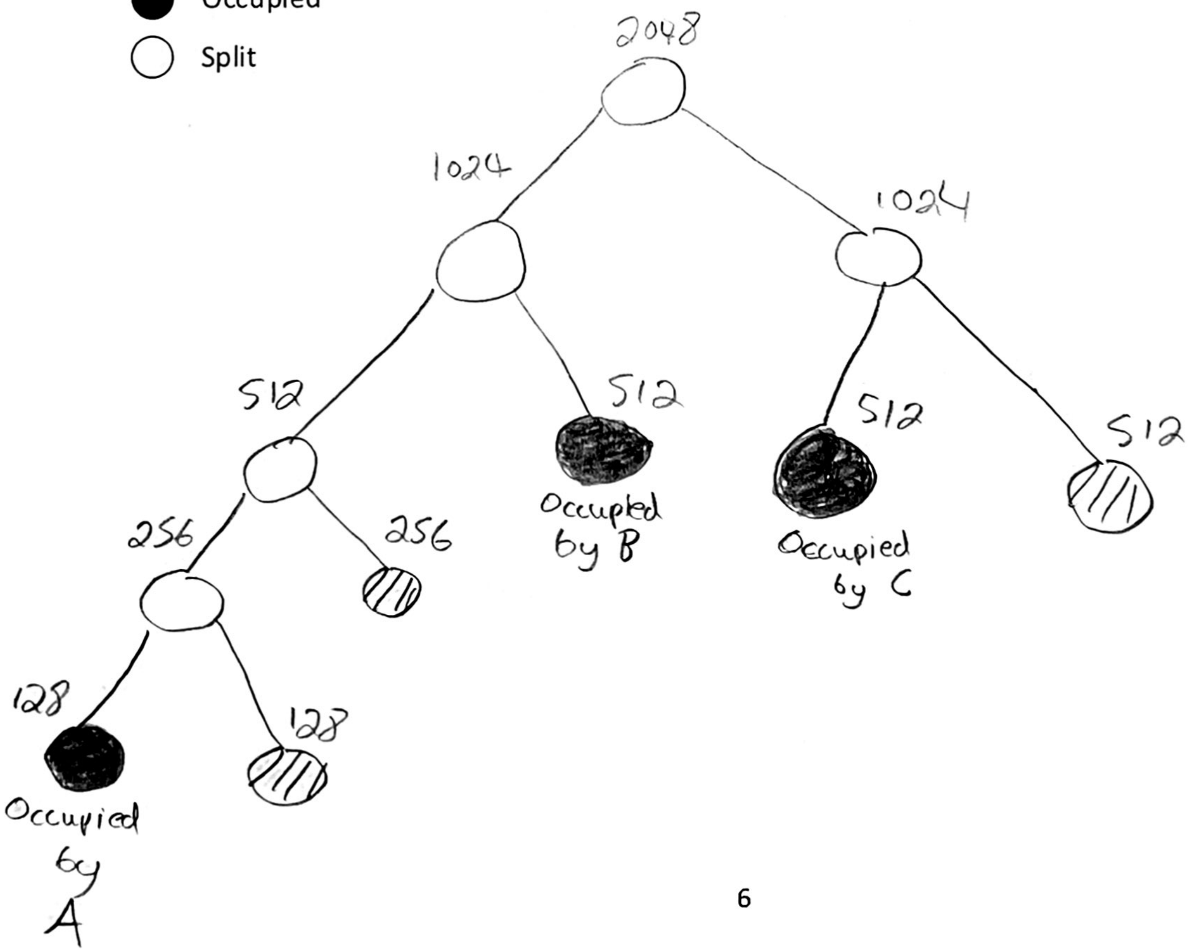
	2048 KB				
A=100KB	A	128	512	1024	
B=390KB	A	128	B	1024	
C=450KB	A	128	B	C	512

b) Please draw the related binary tree based on the kernel memory allocation graph derived from a) (3p)

▨ Free

● Occupied

○ Split



3. The Least recent used (LRU) page replacement algorithm is used to determine which page is swapped out of the main memory. Assume that the size of the memory is 3 frames and all the frames are initially unoccupied. Also, all the memory pages are initially in the hard disk. The referenced memory page sequence is: 2, 3, 5, 2, 1, 5, 3.

a) Please fill in the following blanks. (4p)

2	3	5	2	1	5	3
2	2	2	2	2	2	3
	3	3	3	3	3	3
		5	5	1	1	1

b) Please calculate the related page fault rate. (2p)

5/7 → Page fault

4. The delay of reading data from a hard disk is mainly determined by the internal response time, which is the sum of seek time, rotational delay, transfer time, and overhead. Assume a disk has the following specifications.

- An average seek time of 7ms
- A 7200 RPM rotational speed
- A 20MB/s average internal transfer rate
- 1 KB sector size $\rightarrow$ 1024 Bytes
- 2ms of overheads

What is the internal response time to read 35 continuous sectors? (4p)

Average rotational delay $= \dfrac{1/35}{7200\text{RPM}}$

$= 6.94 \times 10^{-5}$ min

$= 4.16$ ms

Transfer time $= \dfrac{(35 \times 1024 \text{ Bytes})}{20\text{MB/s}}$

$= 0.1$ms

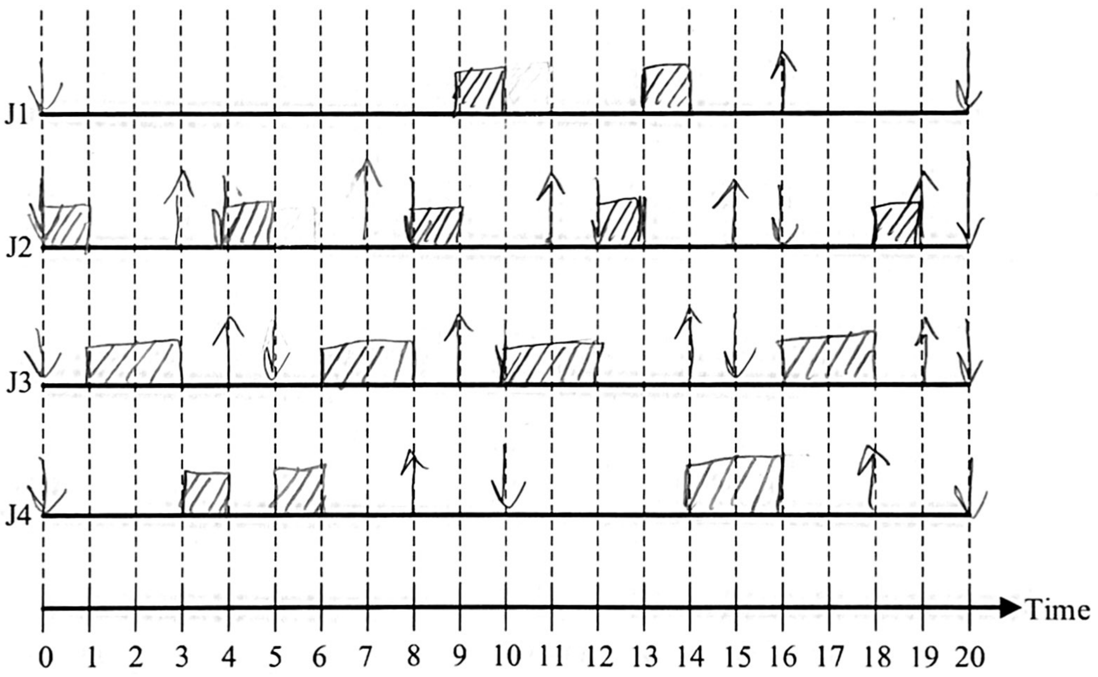
Internal response time $= 7$ms $+ 4.16$ms $+ 0.1$ms$+2$ms

$= 13.26$ ms

5. In the single-core real-time OS, ***Earliest Deadline First (EDF)*** is a very popular scheduling algorithm to schedule jobs in the job set. Assume that there are currently four jobs in the job set, and the information of these four jobs are as follows:

	Service time (C)	Relative deadline (D)	Period (T)
J1	2	16	20
J2	1	3	4
J3	2	4	5
J4	2	8	10

a) Please fill out the following job scheduling chart based on the above information (4p):



b) If the service time of J1 becomes 3, are there any jobs that miss their deadlines? If no, please calculate the overall CPU utilization; If yes, please specify which jobs and when their deadlines are missed. (2p)

Yes, there will be jobs that miss their deadlines.

J_2 and J_3 will miss its deadline.