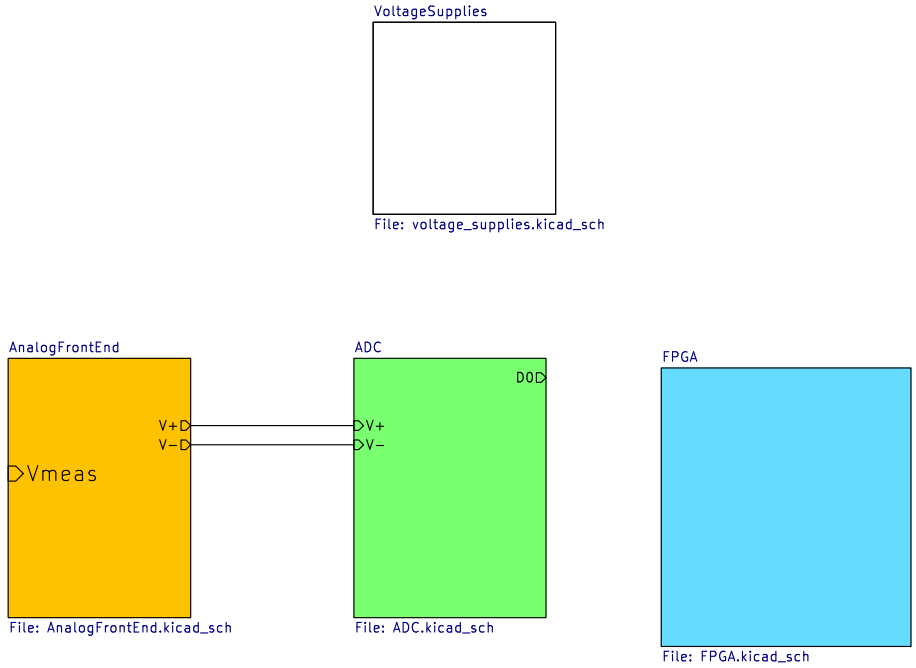

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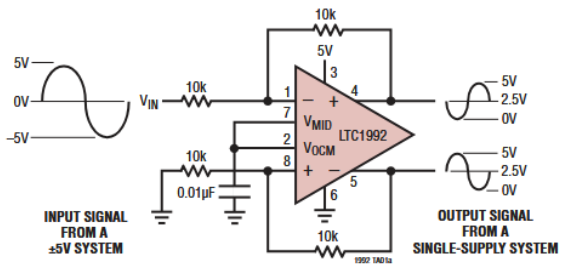
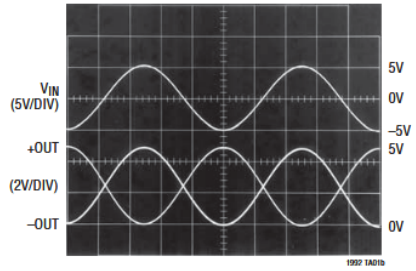
TYPICAL APPLICATION

Single-Supply, Single-Ended to Differential Conversion





Vmeas

DV+

DV–

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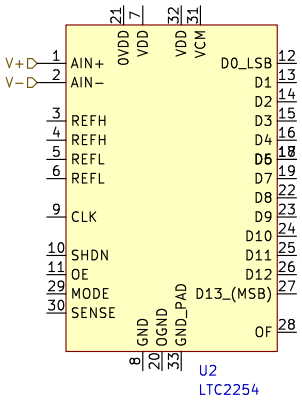


PIN FUNCTIONS

A_{IN+} (Pin 1): Positive Differential Analog Input.

A_{IN-} (Pin 2): Negative Differential Analog Input.

REFH (Pins 3, 4): ADC High Reference. Short together and bypass to pins 5, 6 with a 0.1µF ceramic chip capacitor as close to the pin as possible. Also bypass to pins 5, 6 with an additional 2.2µF ceramic chip capacitor and to ground with a 1µF ceramic chip capacitor.

REFL (Pins 5, 6): ADC Low Reference. Short together and bypass to pins 3, 4 with a 0.1µF ceramic chip capacitor as close to the pin as possible. Also bypass to pins 3, 4 with an additional 2.2µF ceramic chip capacitor and to ground with a 1µF ceramic chip capacitor.

V_{DD} (Pins 7, 32): 3V Supply. Bypass to GND with 0.1µF ceramic chip capacitors.

GND (Pin 8): ADC Power Ground.

CLK (Pin 9): Clock Input. The input sample starts on the positive edge.

SHDN (Pin 10): Shutdown Mode Selection Pin. Connecting SHDN to GND and OE to GND results in normal operation with the outputs enabled. Connecting SHDN to GND and OE to V_{DD} results in normal operation with the outputs at high impedance. Connecting SHDN to V_{DD} and OE to GND results in nap mode with the outputs at high impedance. Connecting SHDN to V_{DD} and OE to V_{DD} results in sleep mode with the outputs at high impedance.

OE (Pin 11): Output Enable Pin. Refer to SHDN pin function.

D0 – D13 (Pins 12, 13, 14, 15, 16, 17, 18, 19, 22, 23, 24, 25, 26, 27): Digital Outputs. D13 is the MSB.

OGND (Pin 28): Output Driver Ground.

OV_{DD} (Pin 21): Positive Supply for the Output Drivers. Bypass to ground with 0.1µF ceramic chip capacitor. OV_{DD} can be 0.5V to 3.6V.

OF (Pin 28): Over/Under Flow Output. High when an over or under flow has occurred.

MODE (Pin 29): Output Format and Clock Duty Cycle Stabilizer Selection Pin. Connecting MODE to GND selects offset binary output format and turns the clock duty cycle stabilizer off. 1/3 V_{DD} selects offset binary output format and turns the clock duty cycle stabilizer on. 2/3 V_{DD} selects 2's complement output format and turns the clock duty cycle stabilizer on. V_{DD} selects 2's complement output format and turns the clock duty cycle stabilizer off.

SENSE (Pin 30): Reference Programming Pin. Connecting SENSE to V_{CM} selects the internal reference and a ±0.5V input range. V_{DD} selects the internal reference and a ±1V input range. An external reference greater than 0.5V and less than 1V applied to SENSE selects an input range of $\pm V_{SENSE}$. ±1V is the largest valid input range.

V_{CM} (Pin 31): 1.5V Output and Input Common Mode Bias. Bypass to ground with 2.2µF ceramic chip capacitor.

GND (Exposed Pad) (Pin 33): ADC Power Ground. The exposed pad on the bottom of the package needs to be soldered to ground.

Clock Duty Cycle Stabilizer

An optional clock duty cycle stabilizer circuit ensures high performance even if the input clock has a non 50% duty cycle. Using the clock duty cycle stabilizer is recommended for most applications. To use the clock duty cycle stabilizer, the MODE pin should be connected to $1/3V_{DD}$ or $2/3V_{DD}$ using external resistors.

This circuit uses the rising edge of the CLK pin to sample the analog input. The falling edge of CLK is ignored and the internal falling edge is generated by a phase-locked loop. The input clock duty cycle can vary from 40% to 60% and the clock duty cycle stabilizer will maintain a constant 50% internal duty cycle. If the clock is turned off for a long period of time, the duty cycle stabilizer circuit will require a hundred clock cycles for the PLL to lock onto the input clock.

For applications where the sample rate needs to be changed quickly, the clock duty cycle stabilizer can be disabled. If the duty cycle stabilizer is disabled, care should be taken to make the sampling clock have a 50% (±5%) duty cycle.

Table 2. MODE Pin Function

MODE Pin	Output Format	Clock Duty Cycle Stablizer
0	Offset Binary	Off
$1/3V_{DD}$	Offset Binary	On
$2/3V_{DD}$	2's Complement	On
V_{DD}	2's Complement	Off

DIGITAL OUTPUTS

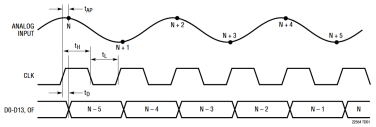
Table 1 shows the relationship between the analog input voltage, the digital data bits, and the overflow bit.

Table 1. Output Codes vs Input Voltage

$A_{IN}^+ - A_{IN}^-$ (2V Range)	OF	D13 – D0 (Offset Binary)	D13 – D0 (2's Complement)
>+1.000000V	1	11 1111 1111 1111	01 1111 1111 1111
+0.999878V	0	11 1111 1111 1111	01 1111 1111 1111
+0.999756V	0	11 1111 1111 1110	01 1111 1111 1110
+0.000122V	0	10 0000 0000 0001	00 0000 0000 0001
0.000000V	0	10 0000 0000 0000	00 0000 0000 0000
–0.000122V	0	01 1111 1111 1111	11 1111 1111 1111
–0.000244V	0	01 1111 1111 1110	11 1111 1111 1110
–0.999878V	0	00 0000 0000 0001	10 0000 0000 0001
–1.000000V	0	00 0000 0000 0000	10 0000 0000 0000
<–1.000000V	1	00 0000 0000 0000	10 0000 0000 0000

TIMING DIAGRAM

Timing Diagram



FUNCTIONAL BLOCK DIAGRAM

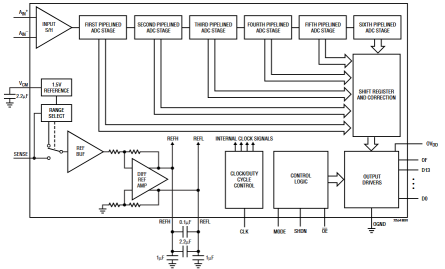


Figure 1. Functional Block Diagram

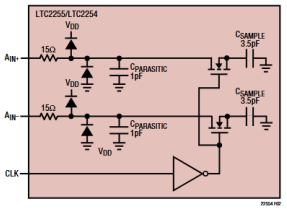


Figure 2. Equivalent Input Circuit

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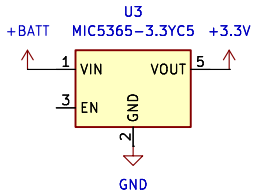

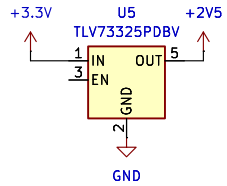

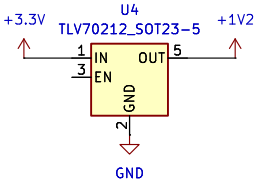

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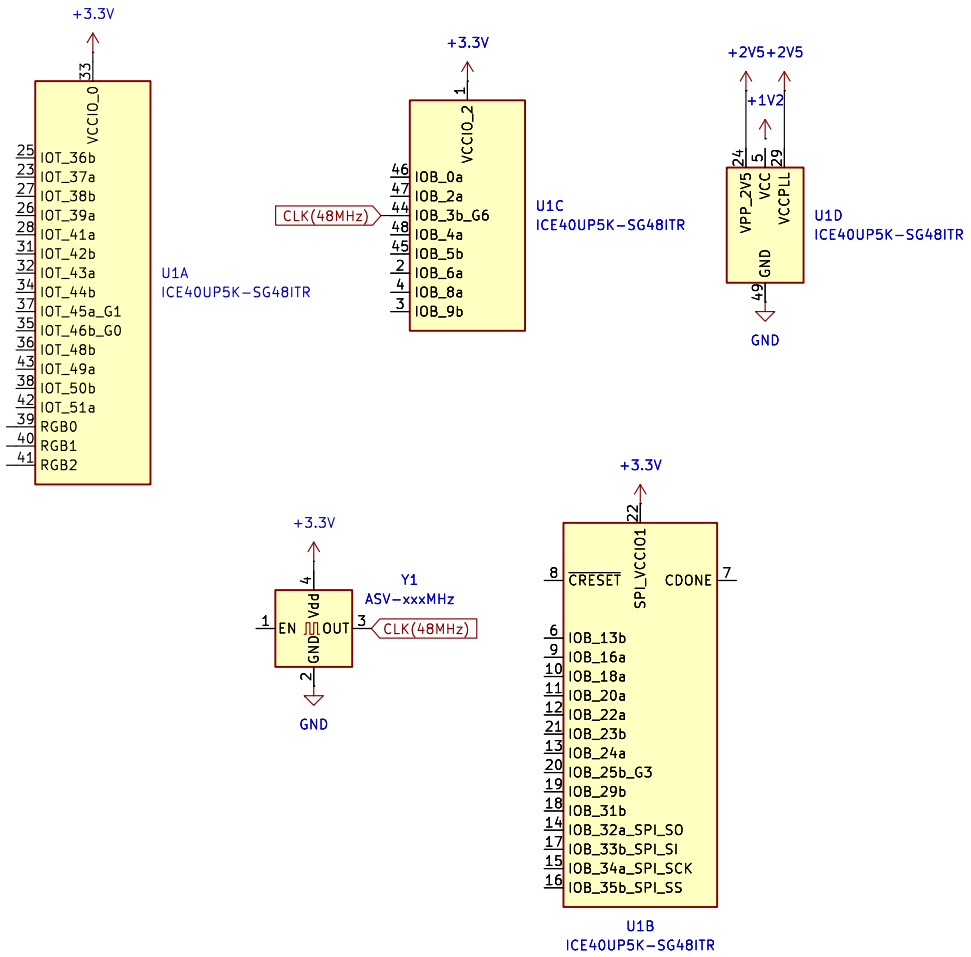

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