Lecture 13: CMOS Amplifiers: The Differential Pair - Third Part

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Reference: Razavi (Fundamentals) - Chapter 10

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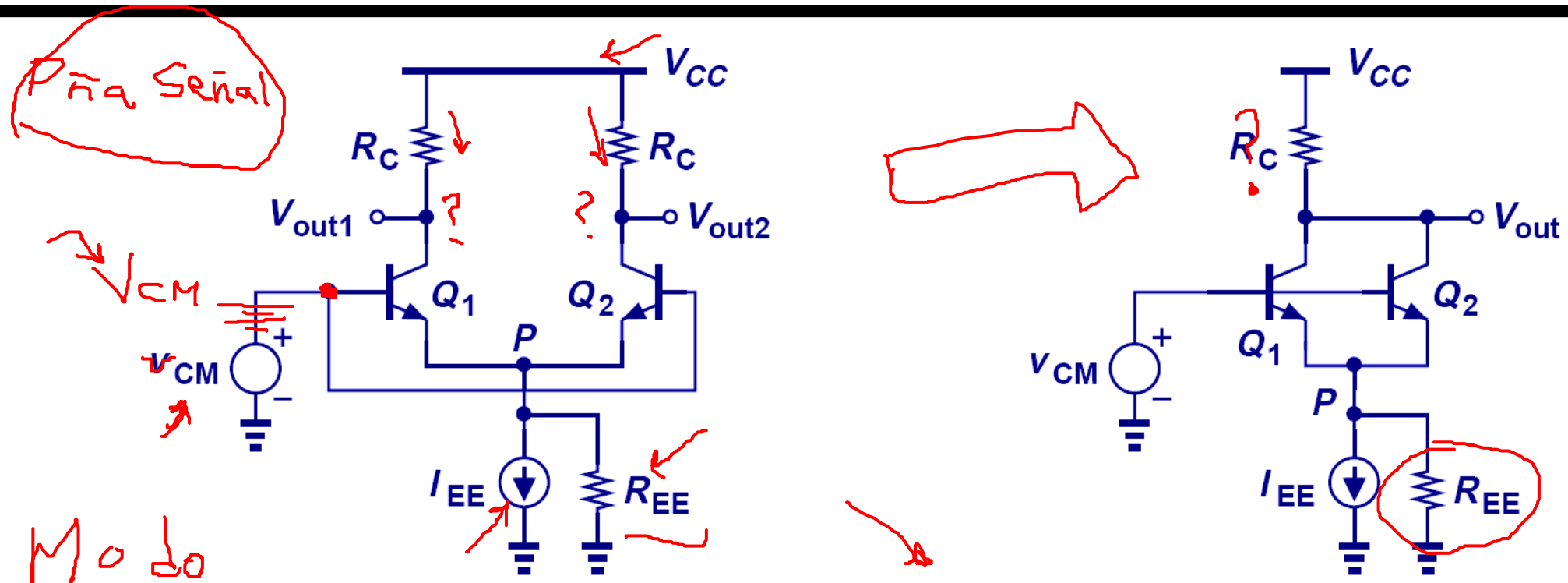
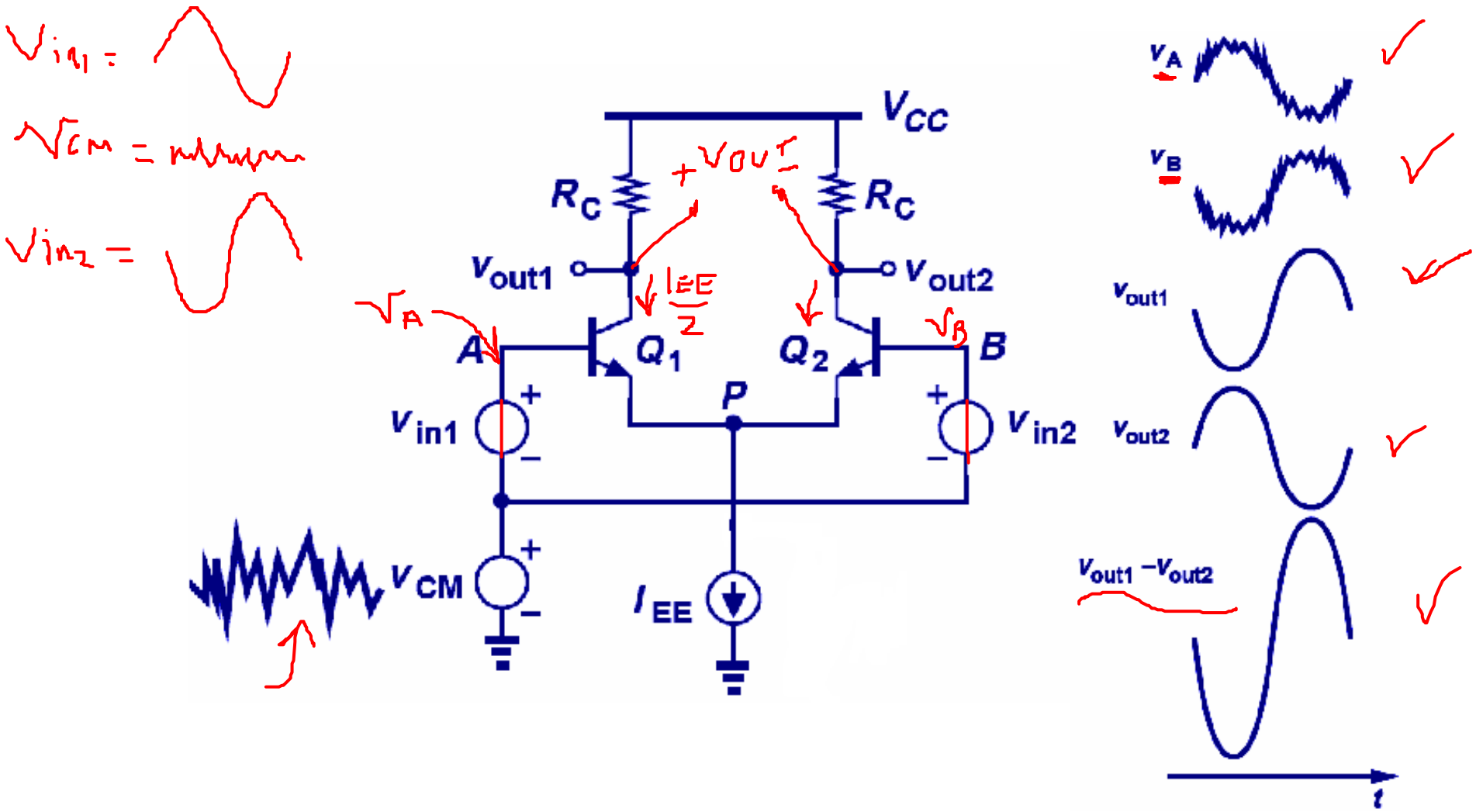
Effect of Finite Tail Impedance



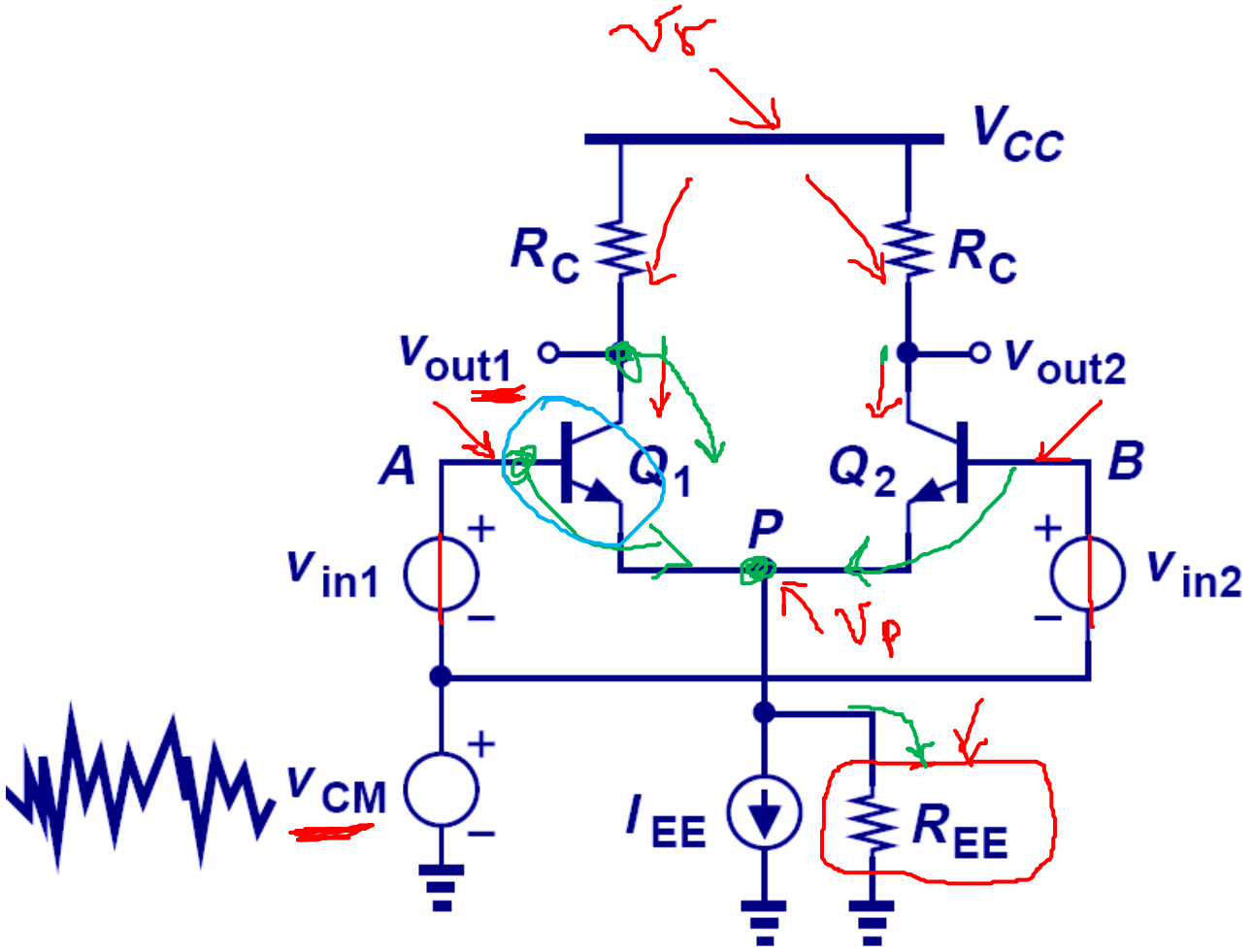
$$\frac{\Delta V_{out,CM}}{\Delta V_{in,CM}} = -\frac{R_C/2}{R_{EE}+1/2g_m}$$

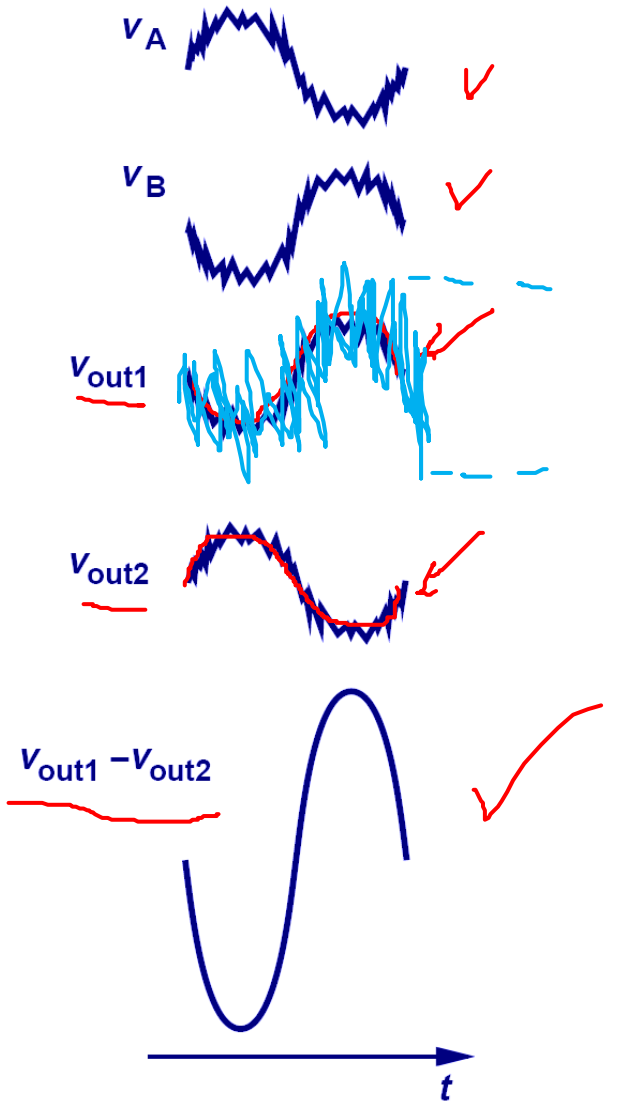
- If the tail current source is not ideal, then when an input CM voltage is applied, the currents in Q_1 and Q_2 and hence output CM voltage will change.

Input CM Noise with Ideal Tail Current

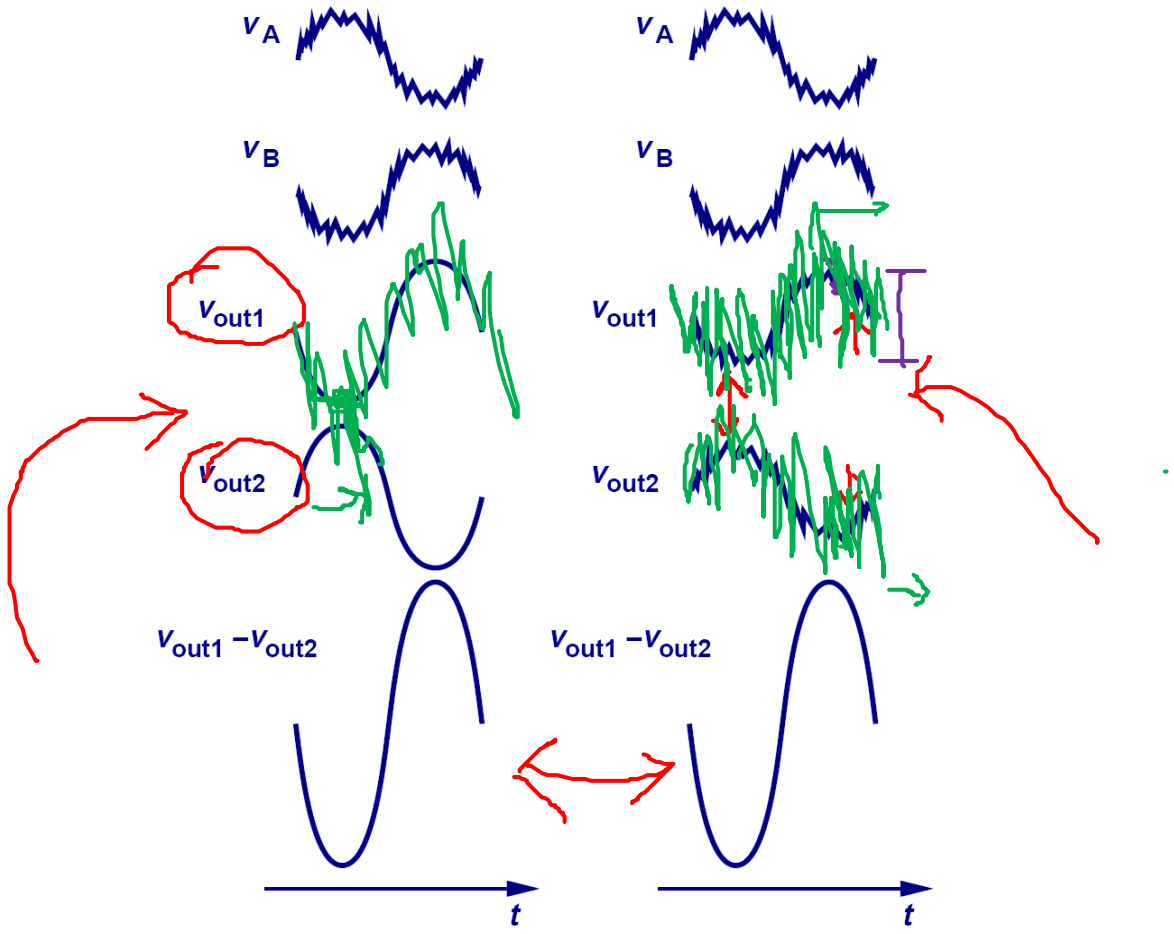


Input CM Noise with Non-ideal Tail Current





Comparison - Tail Current

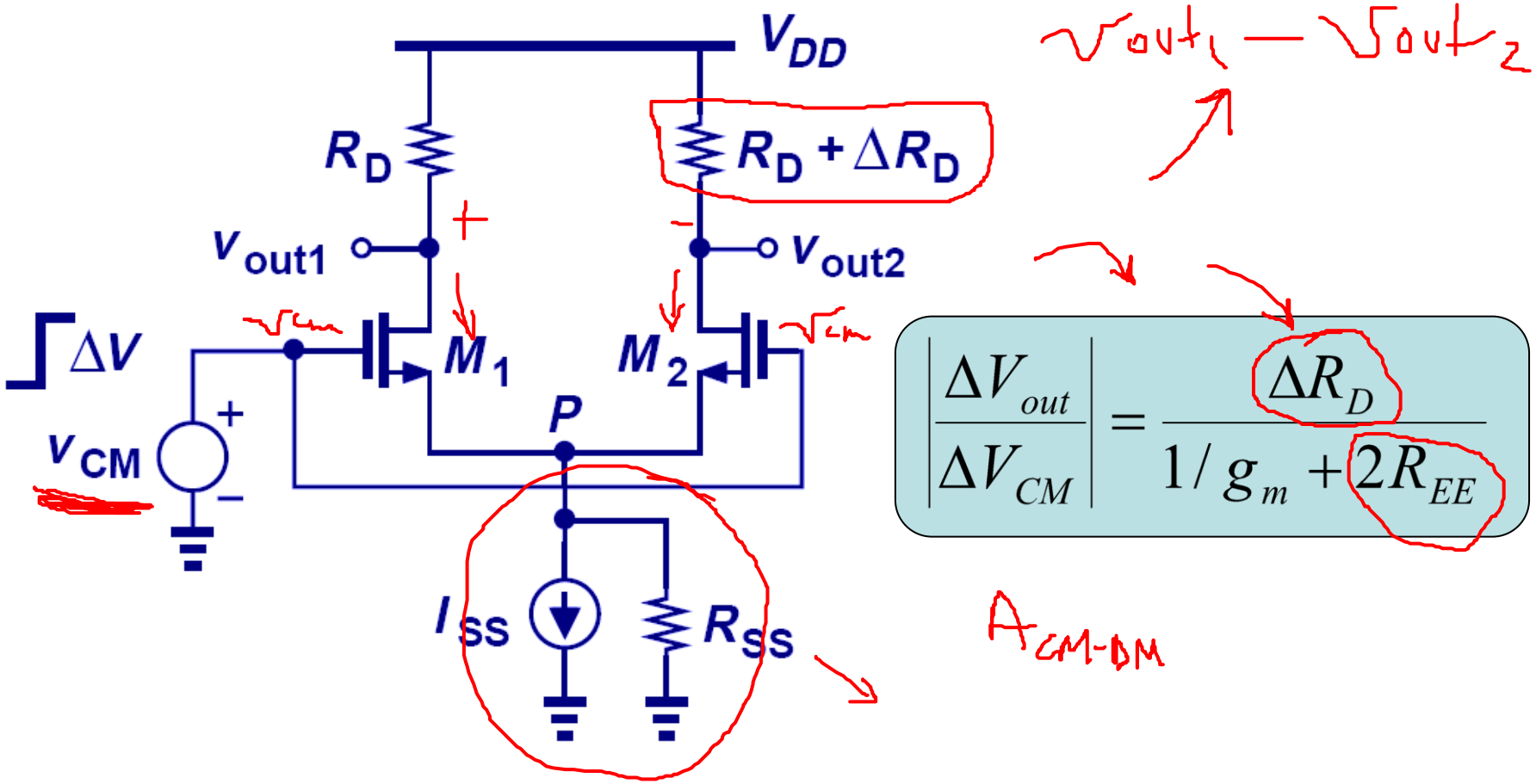


- **As it can be seen, the differential output voltages for both cases are the same. So for small input CM noise, the differential pair is not affected.**

Comparison - Tail Current

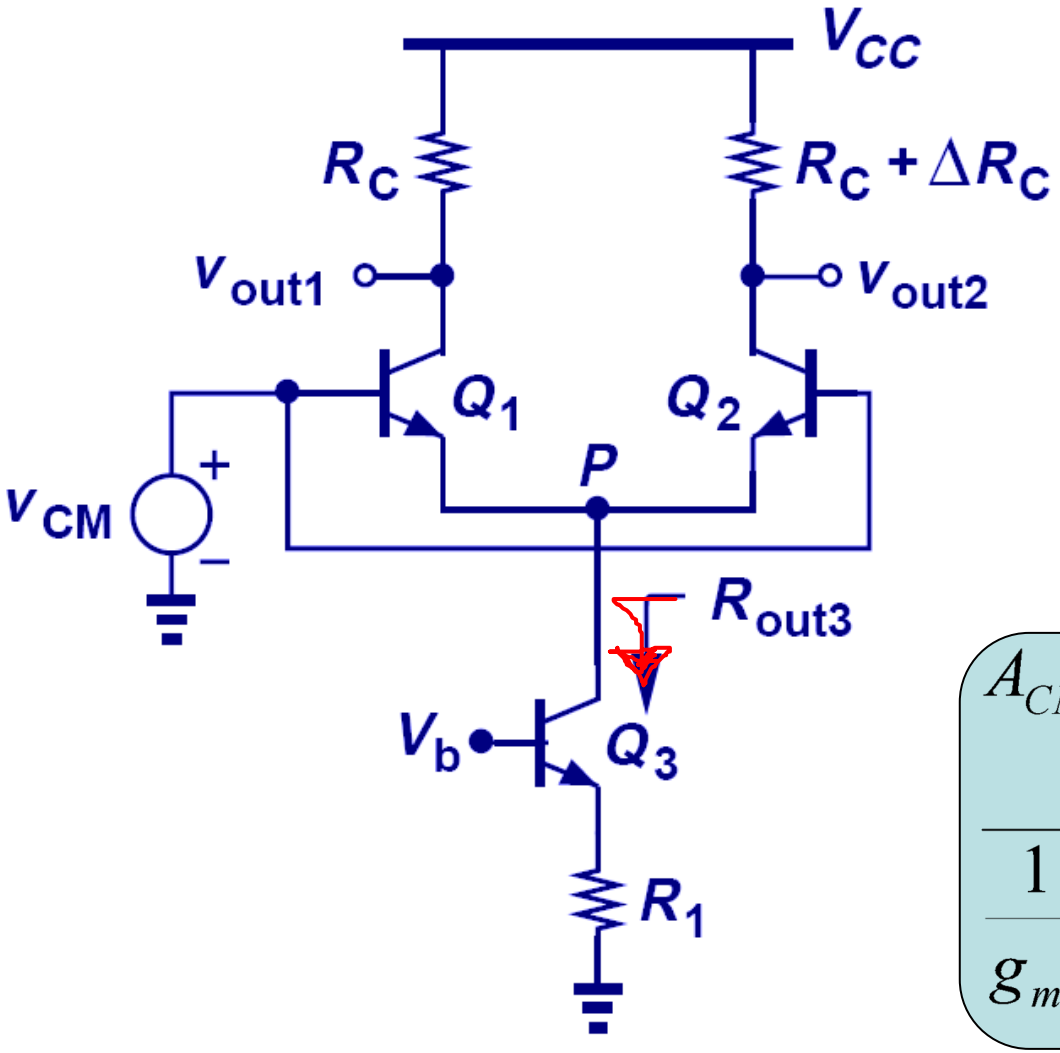
Common Mode Explanation

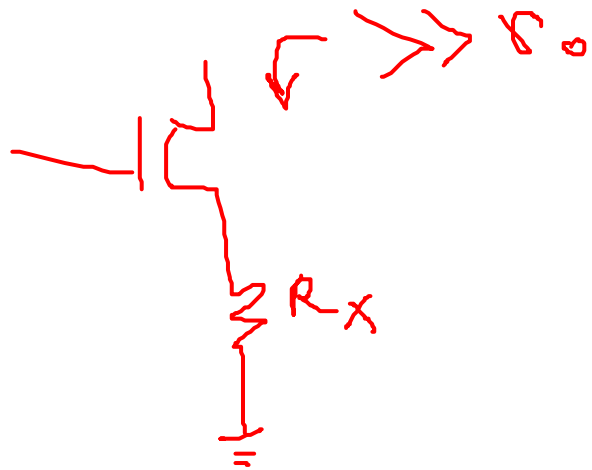
CM to DM Conversion, $A_{CM\text{-}DM}$



- **If finite tail impedance and asymmetry are both present, then the differential output signal will contain a portion of input common-mode signal.**

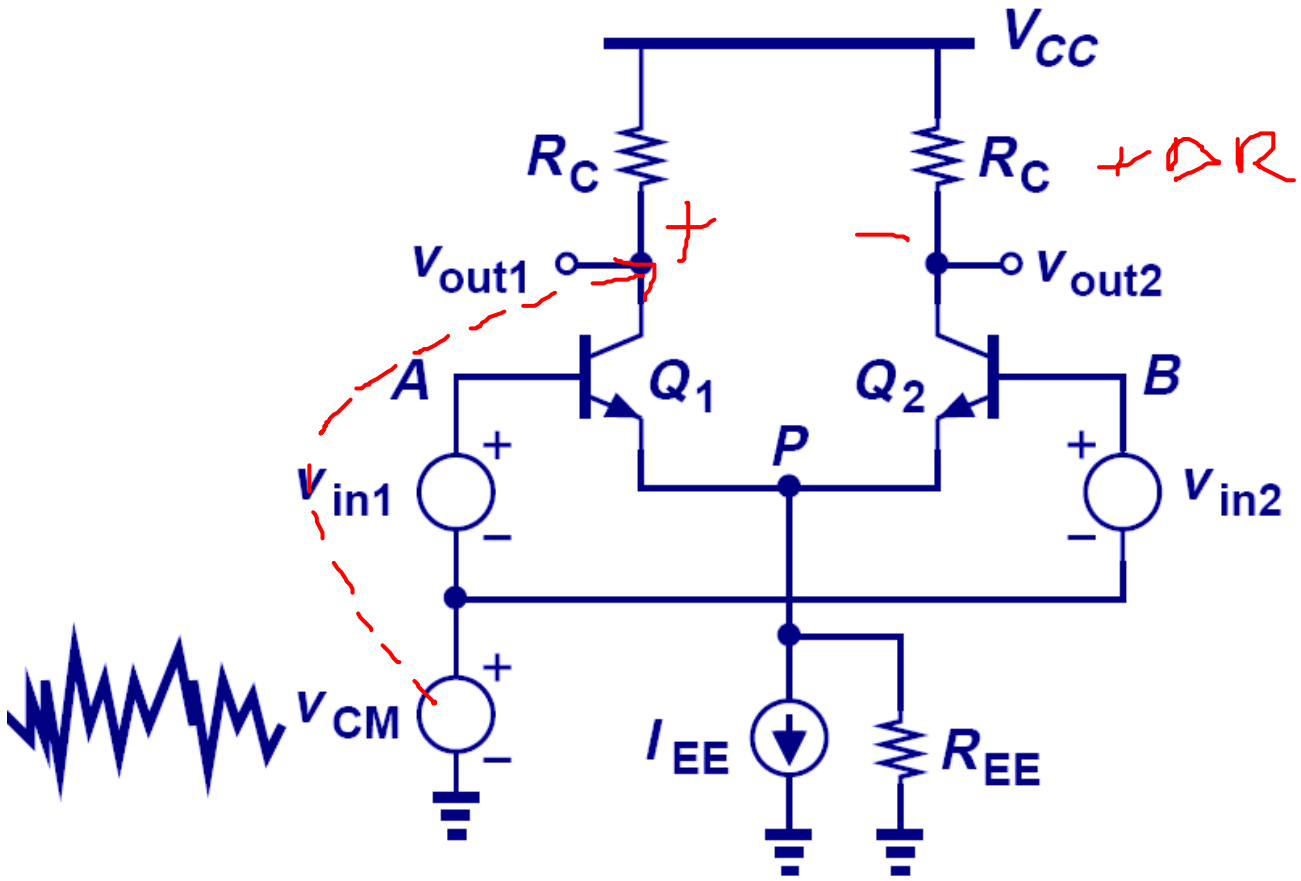
Example: A_{CM-DM}





$$A_{CM-DM} = \frac{\Delta R_C}{\frac{1}{g_{m1}} + 2\left[[1 + g_{m3}(R_1 \| r_{\pi 3})]r_{O3} + R_1 \| r_{\pi 3}\right]}$$

CMRR

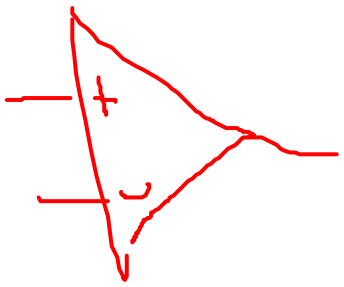


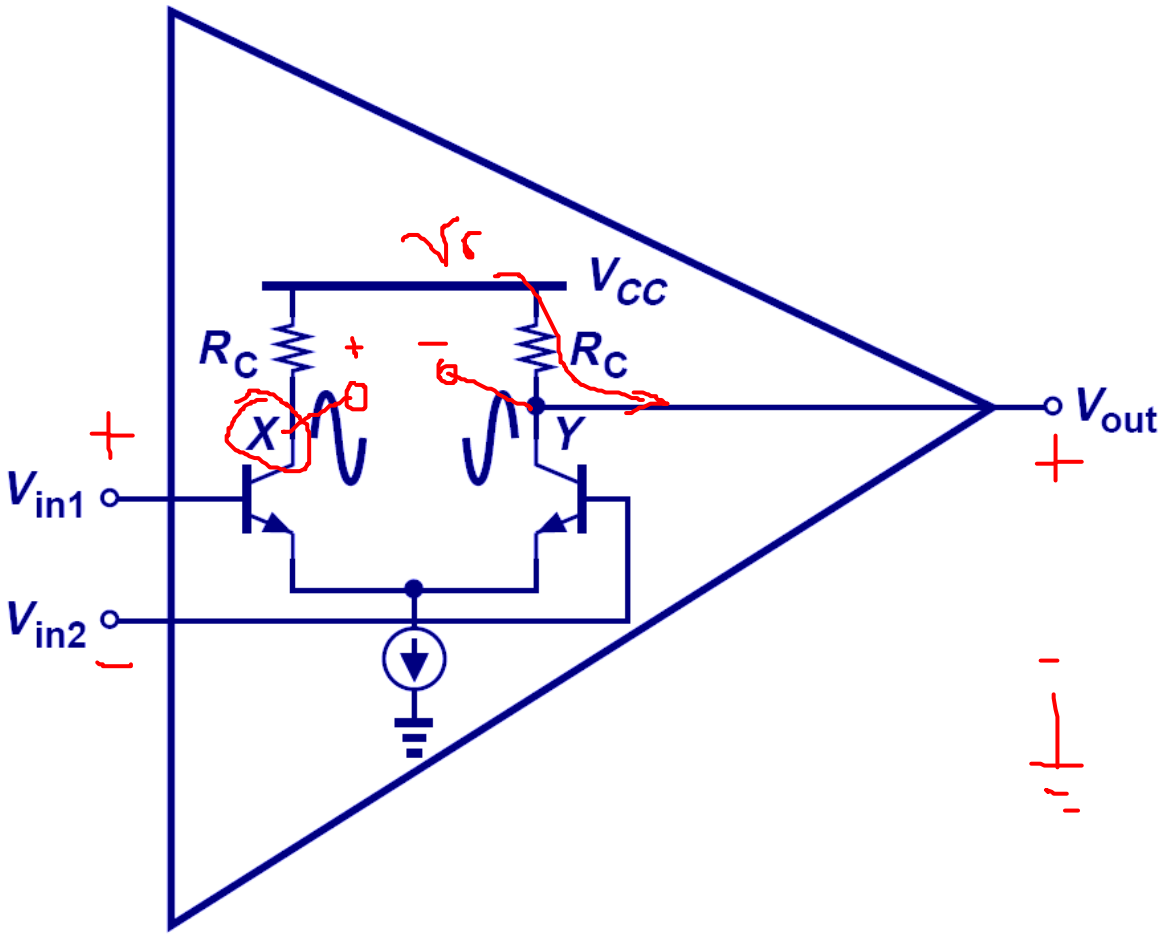
$$CMRR = \frac{A_{DM}}{A_{CM-DM}}$$

$$CMRR = \left| \frac{A_{DM}}{A_{CM}} \right|$$

- **CMRR defines the ratio of wanted amplified differential input signal to unwanted converted input common-mode noise that appears at the output.**

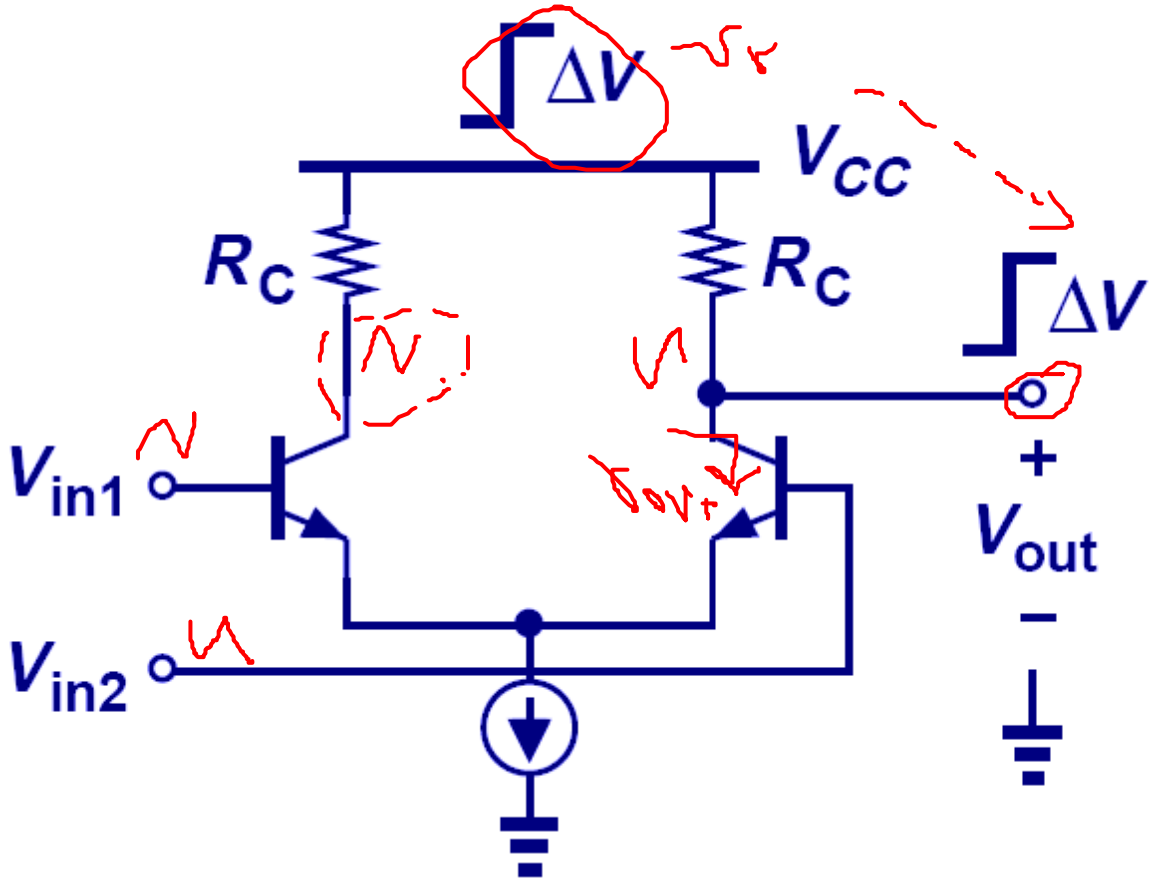
Differential to Single-Ended Conversion





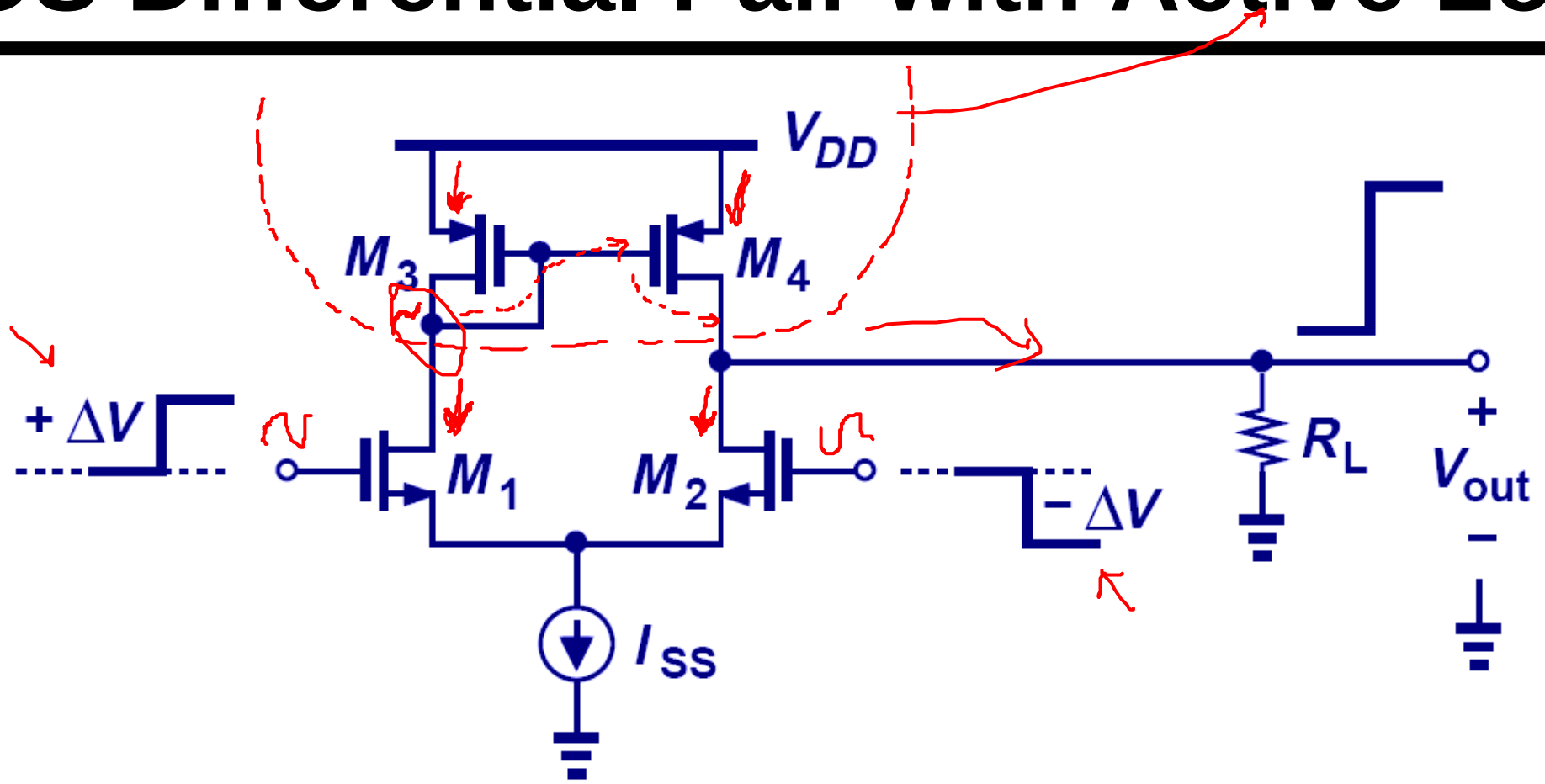
- **Many circuits require a differential to single-ended conversion, however, the above topology is not so good.**

Supply Noise Corruption



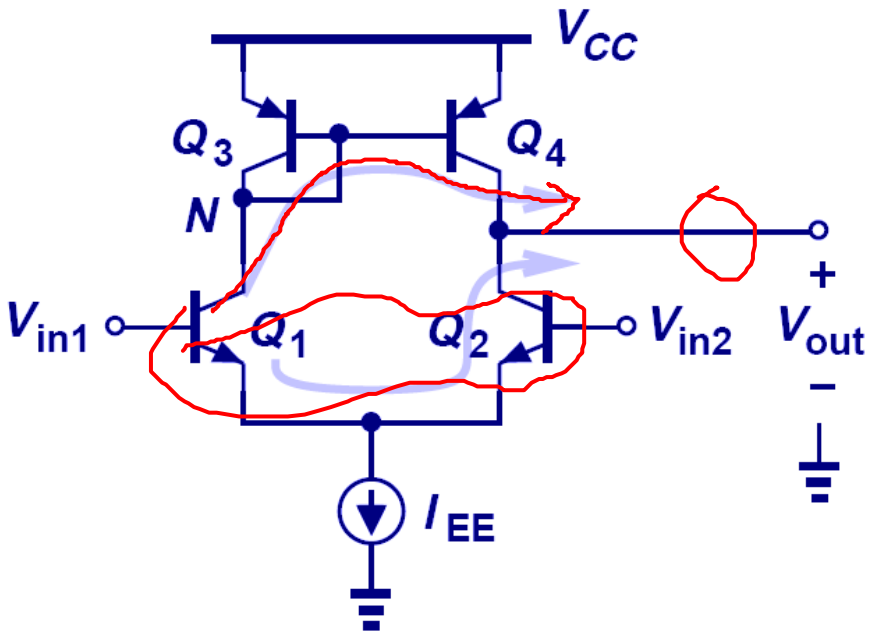
- **The most critical drawback of this topology is supply noise corruption, since no common-mode cancellation mechanism exists. Also, we lose half the signal.**

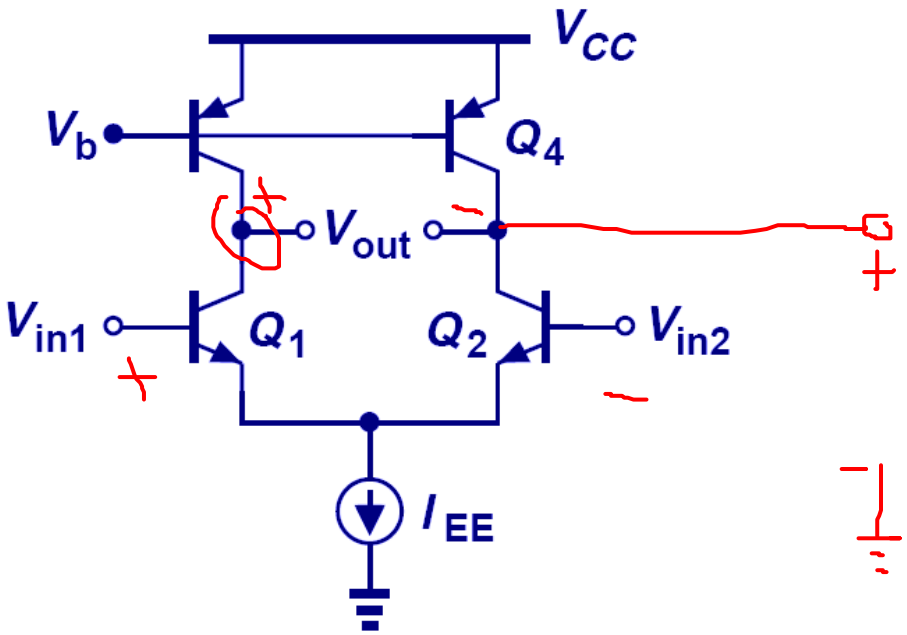
MOS Differential Pair with Active Load



- **Similar to its bipolar counterpart, MOS differential pair can also use active load to enhance its single-ended output.**

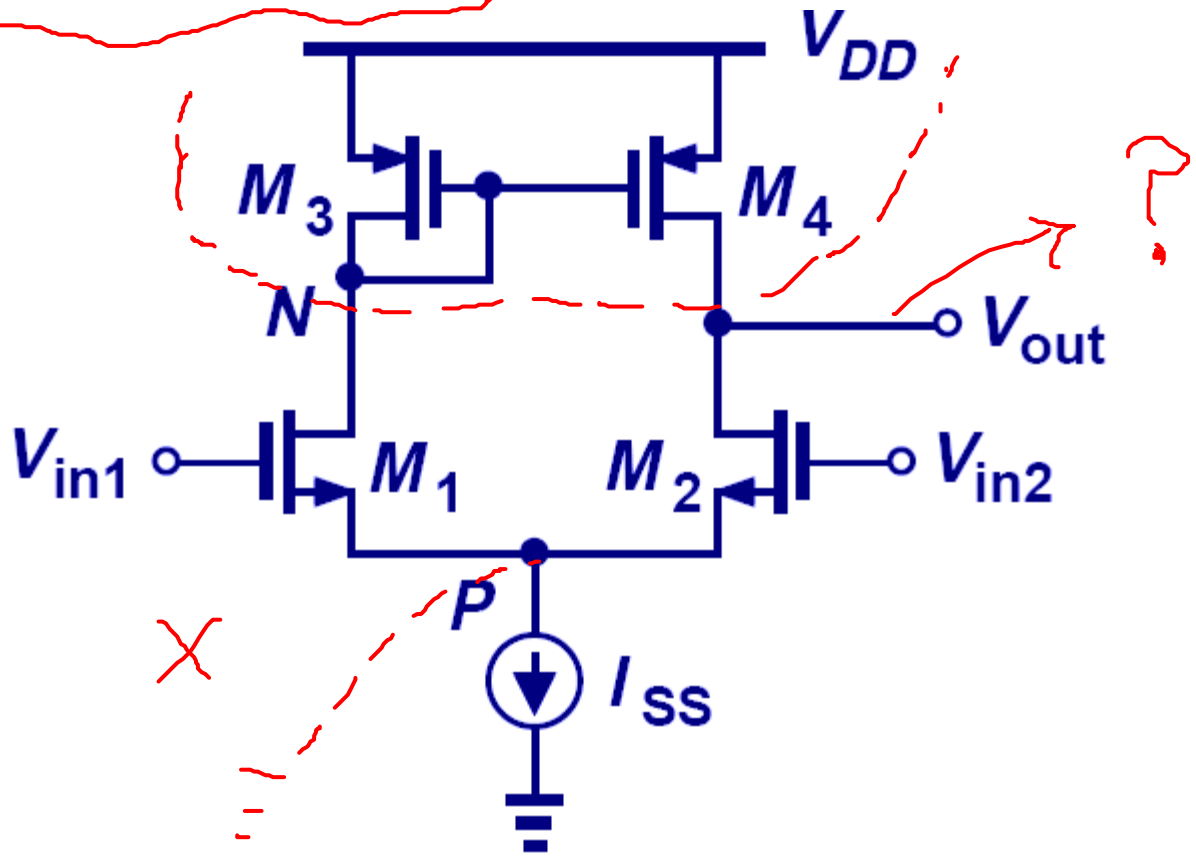
Active Load vs. Static Load



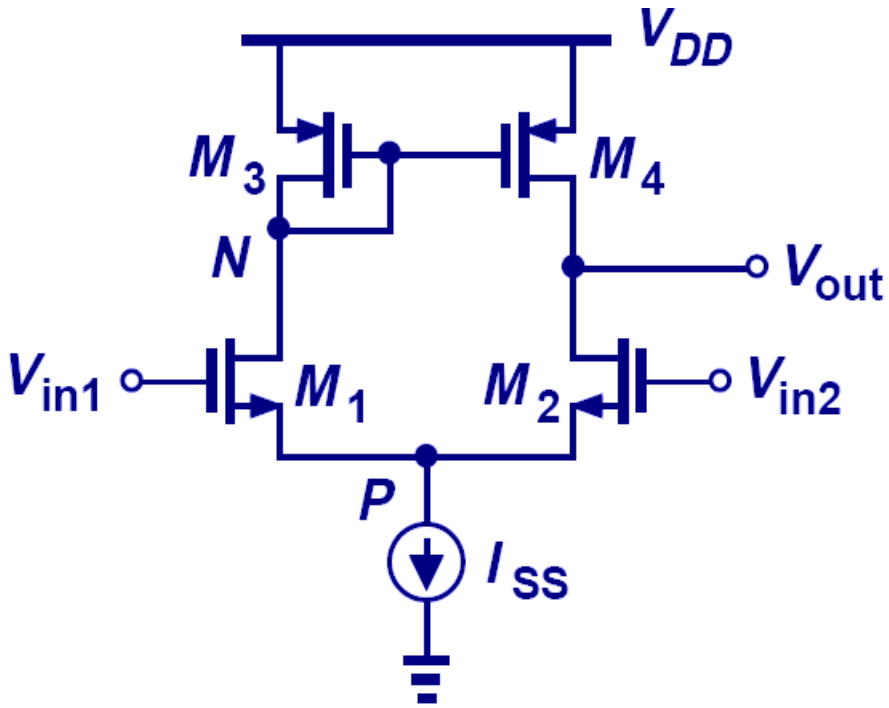


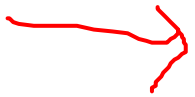
- **The load on the left responds to the input signal and enhances the single-ended output, whereas the load on the right does not.**

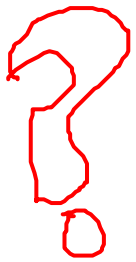
Asymmetric Differential Pair



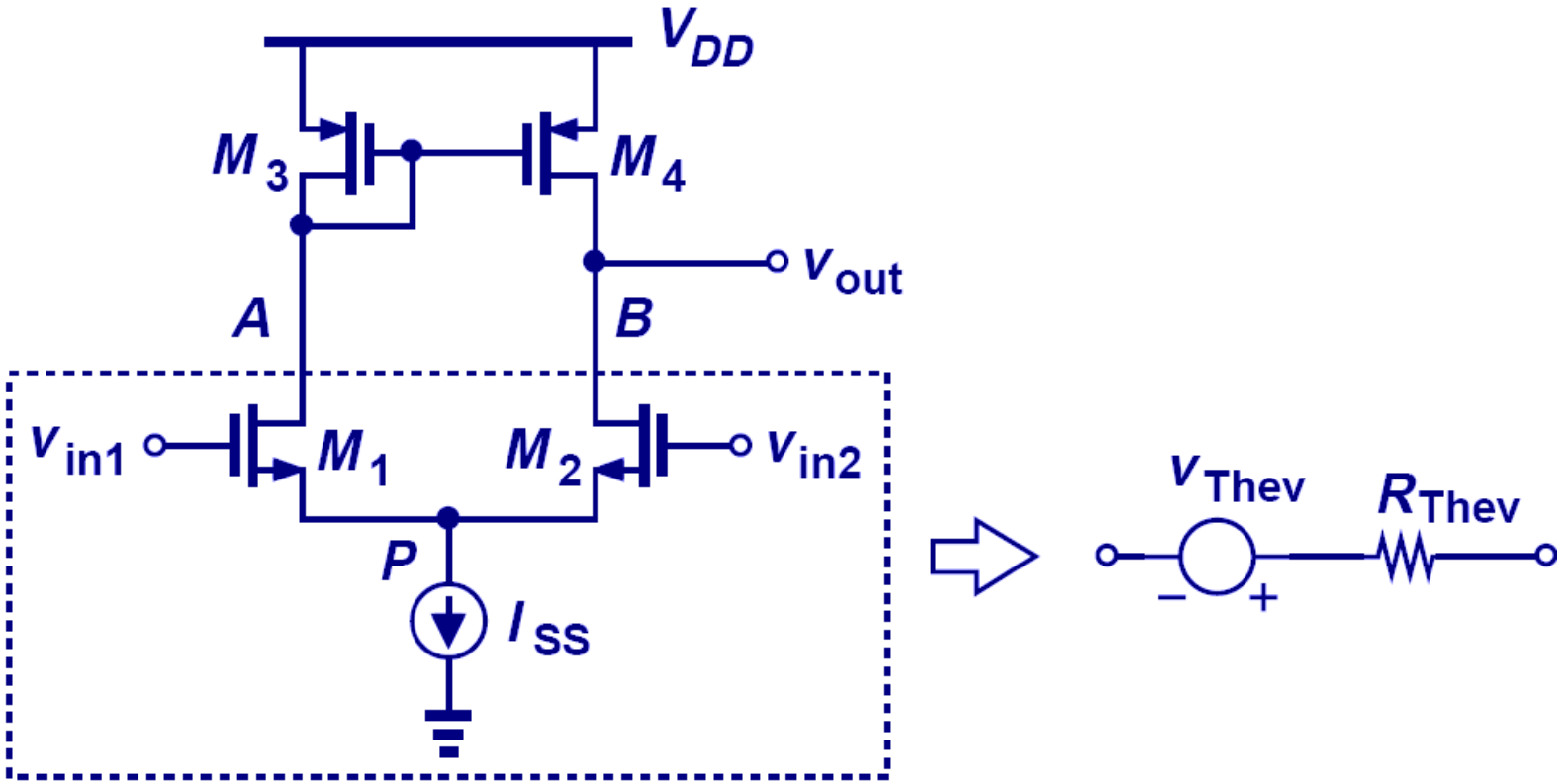
- **Because of the vastly different resistance magnitude at the drains of M_1 and M_2, the voltage swings at these two nodes are different and therefore node P cannot be viewed as a virtual ground.**


V_{DD}
M_3
M_4
N
V_{out}
V_{in1}
M_1
M_2
V_{in2}
P
I_{SS}





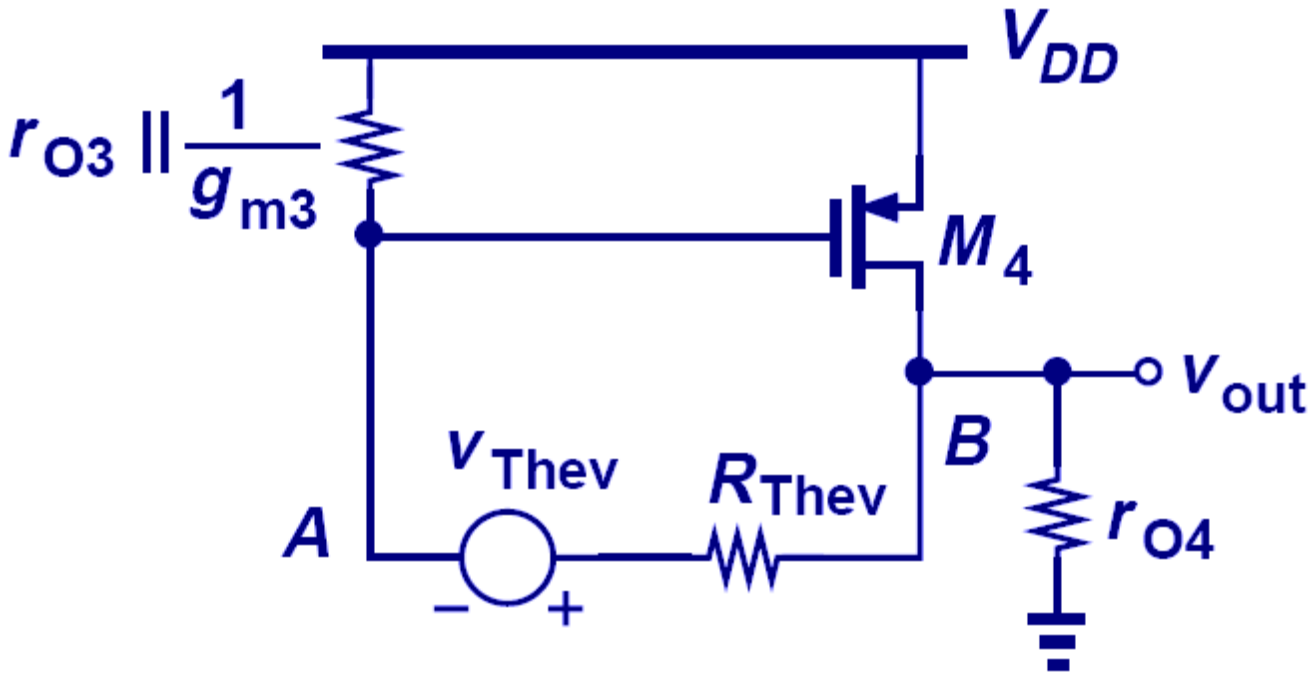
Thevenin Equivalent of the Input Pair



$$v_{Thev} = -g_{mN} r_{oN} (v_{in1} - v_{in2})$$

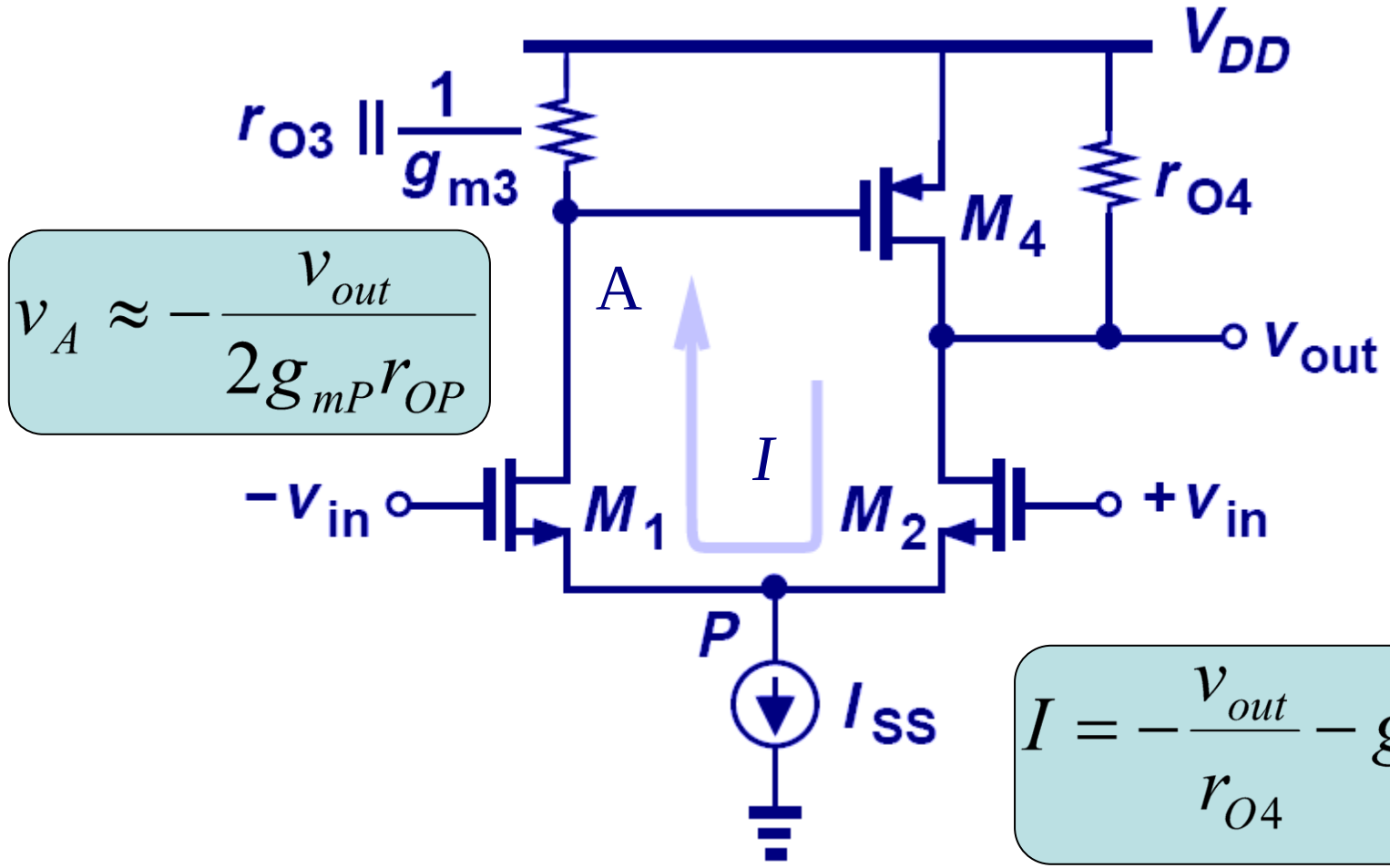
$$R_{Thev} = 2r_{oN}$$

Simplified Differential Pair with Active Load



$$\frac{v_{out}}{v_{in1} - v_{in2}} = g_{mN}(r_{ON} \| r_{OP})$$

Proof of V_A << V_{out}



$$v_A \approx -\frac{v_{out}}{2g_{mP}r_{OP}}$$

$$I = -\frac{v_{out}}{r_{O4}} - g_{m4}v_A$$

Thanks

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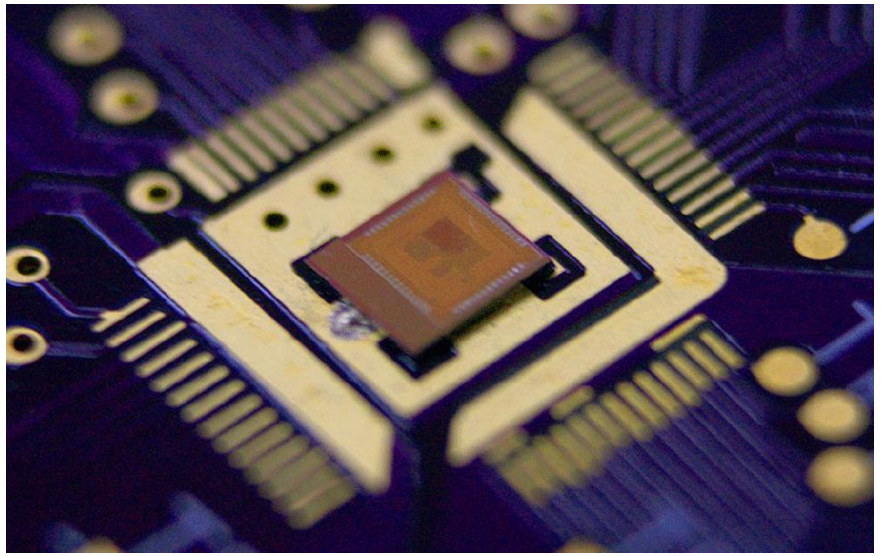

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