Foundations of Analog Circuits
Semester 2021-2
Problem Set – EXAM 1
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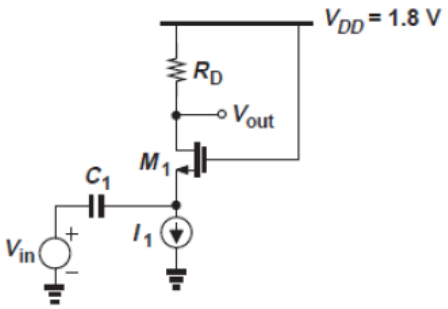
1. The CG amplifier shown below, is biased by means of I1 = 1mA. Assume λ=0 and C1 is very large. A) What value of RD places the transistor M1 100mV away from the triode region? B) What is the required W/L if the circuit must provide a voltage gain of 5 with the value of RD obtained in A)?



assume $\mu_n C_{ox} = 200\,\mu\text{A/V}^2$, $\mu_p C_{ox} = 100\,\mu\text{A/V}^2$, $\lambda = 0$, and $V_{TH} = 0.4$ V for NMOS devices and -0.4 V for PMOS devices.

Figure 1.

2. Consider the circuit shown in Figure 2. Find the expression for the small-signal voltage gain. What is the purpose of resistors R1 and R2?

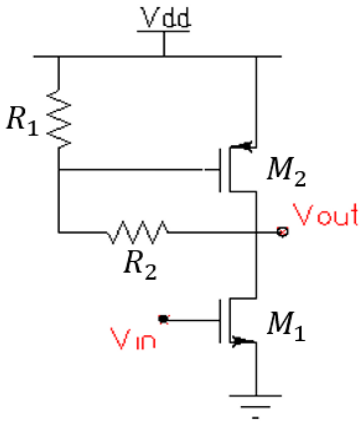


Figure 2.

3. Calculate the overall small-signal voltage gain for the configurations shown in Fig. 3. Take a look about How voltage gain changes according to different Mos configurations that look similar at first sight.

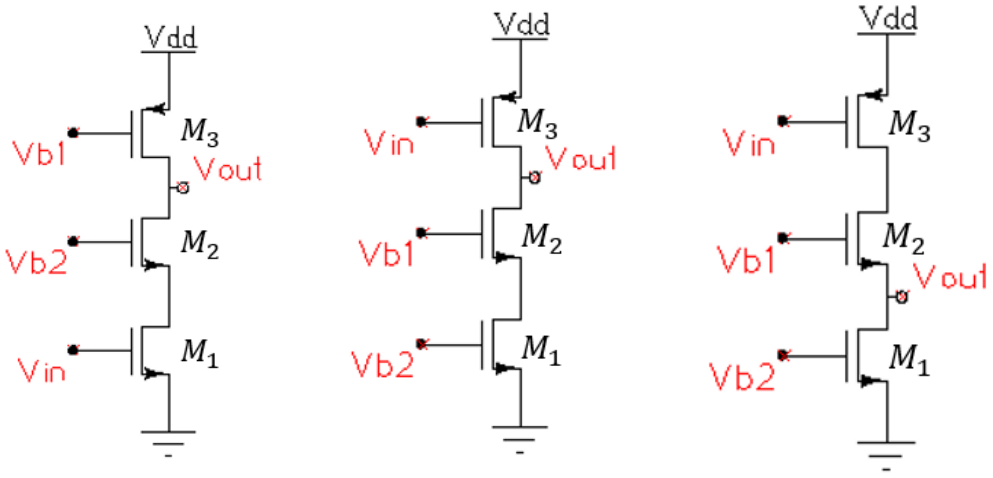


Figure 3.

4. Calculate the small-signal voltage gain of the circuit shown in Figure 4.

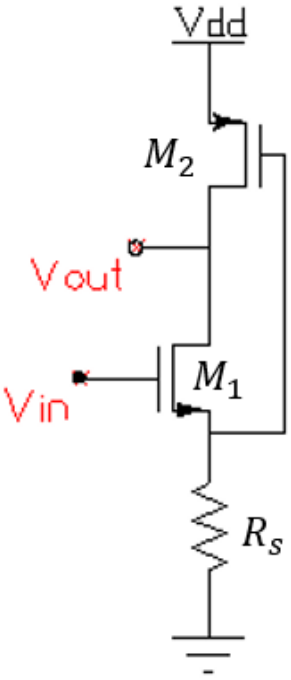


Figure 4.

5. Assuming all transistors are in saturation, calculate the small-signal voltage gain of the circuit shown in Figure 5.

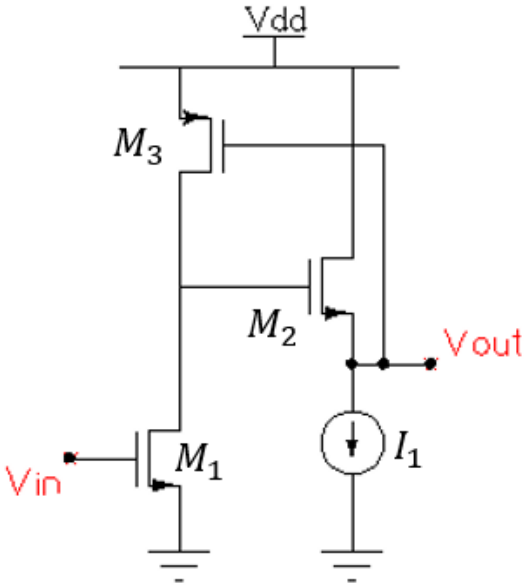


Figure 5.

6. Consider the circuit shown in Figure 6. The purpose is to establish a DC drain current $I_d = 0.5\,mA$. The manufacturer of the transistor specifies $V_t = 1\,V$ and $k_n'W/L = 1\,mA/V^2$. Calculate the value of the resistors that meet the requirement. Neglect channel-length modulation and $Vdd = 15\,V$.

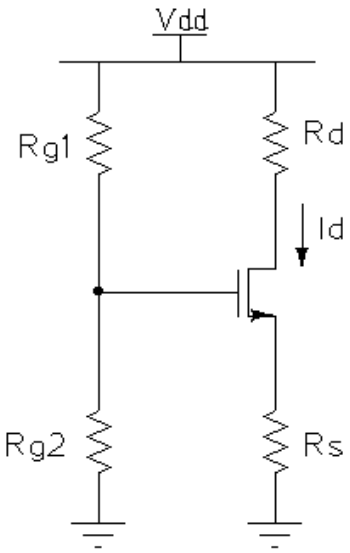


Figure 6.

7. En el circuito siguiente se tiene R1=45kΩ, R2=5kΩ y R3=45kΩ. Ignore el efecto cuerpo de los transistores que puedan presentarlo. Para cada transistor calcúlese: **a)** La corriente I_D, **b)** la transconductancia g_m y la resistencia r_o de pequeña señal, **c)** calcule la potencia que consume el circuito.

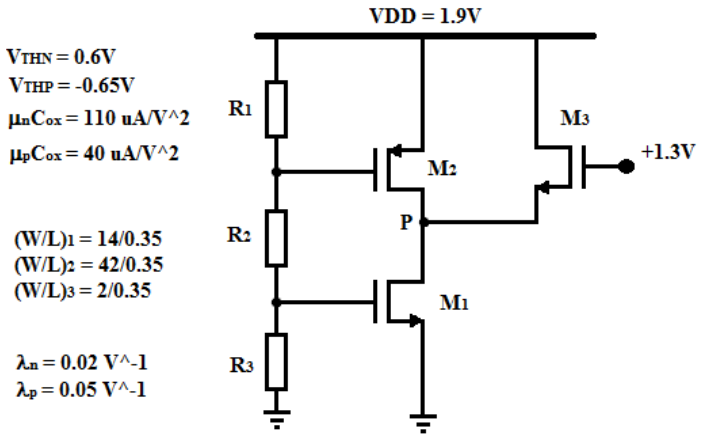


Figure 7.

8. The circuit shown in Figure 8 illustrates a discrete-circuit amplifier. The input signal is coupled to the gate through a very large capacitor as well as the transistor source. The output signal that develops at the drain is coupled to a load resistance via a very large capacitor. Capacitors behave as short circuits for signals and open circuits for DC. Find the voltage gain of the configuration.

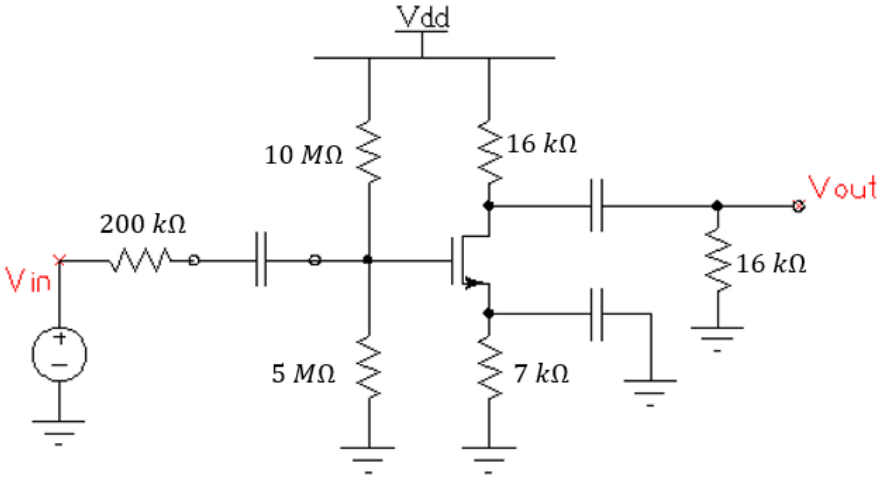


Figure 8.

9. The circuit shown in Figure 9 produces two outputs. Assume $\lambda = 0$. Calculate $Vout1/Vin$ and $Vout2/Vin$.

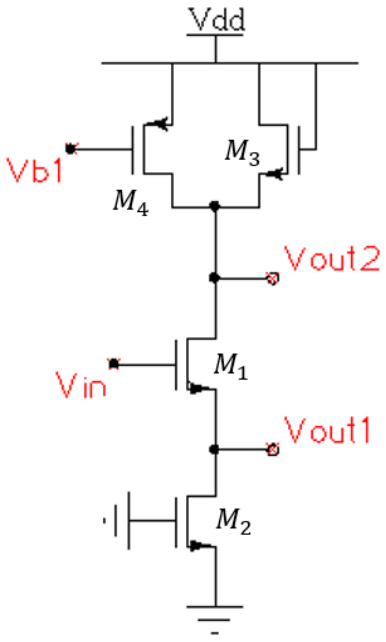


Figure 9.

10. Find the output impedance (Rout) of the configurations illustrated in Fig 10.

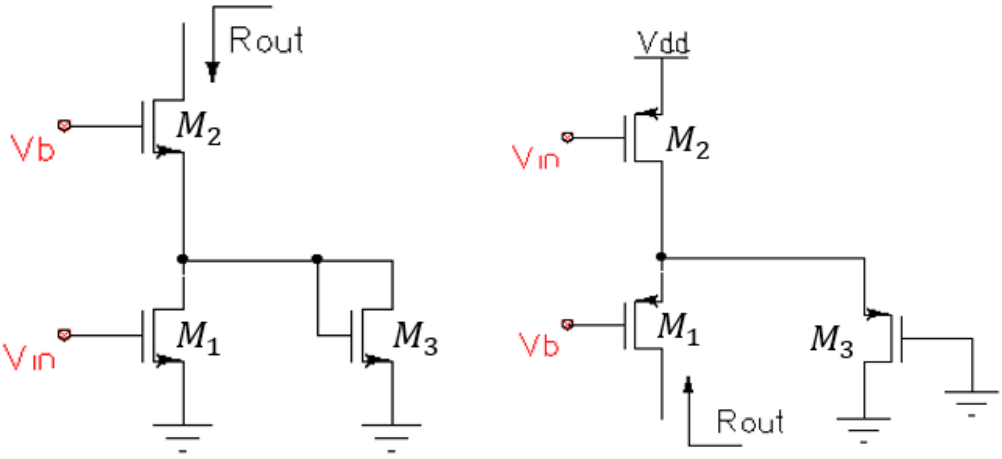


Figure 10.

11. Calculate the small-signal voltage gain of the configurations shown in Fig. 11.

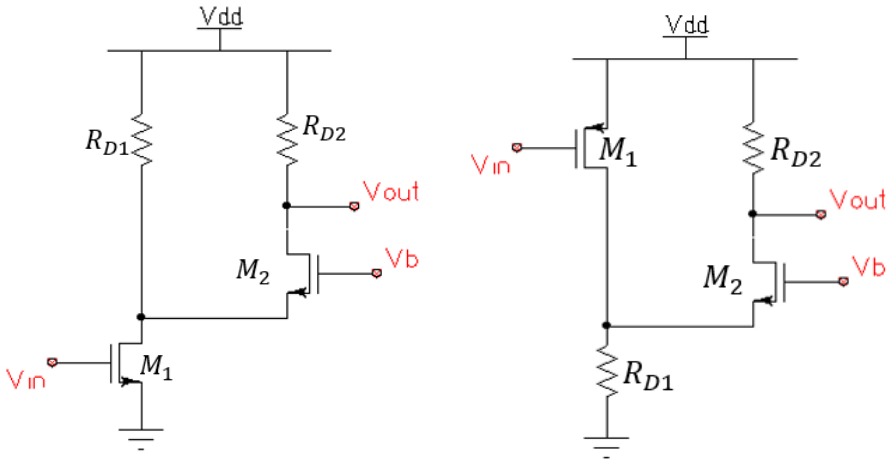


Figure 11.

12. Determine the region of operation (cut-off, triode, saturation) for each of the circuits shown in Figure 12.

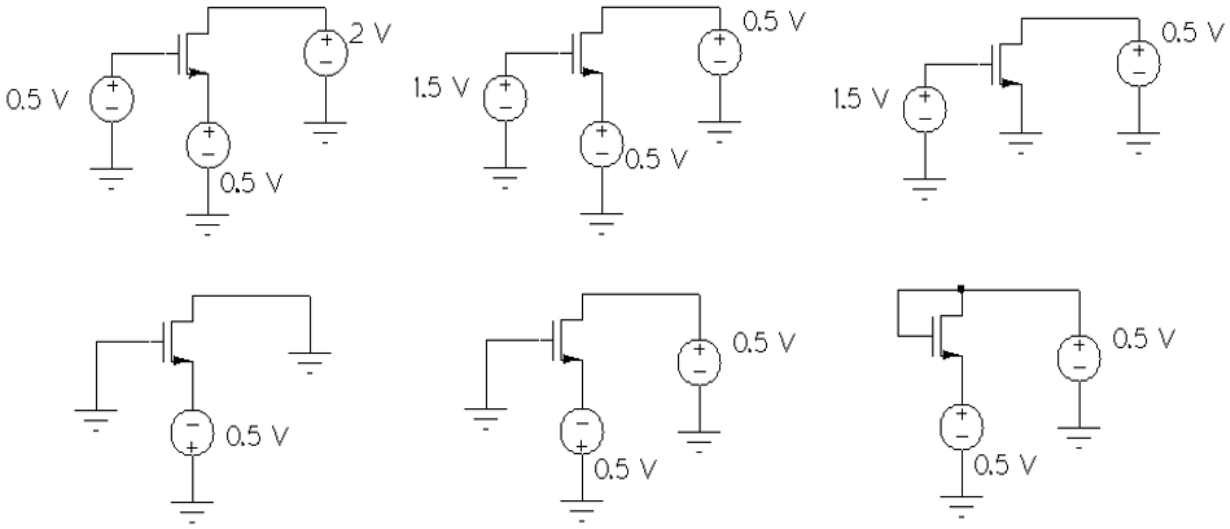


Figure 12.

13. For the circuit shown in Figure 13, plot and clearly label id vs vg, with Vg varying from 0 to 1.8V. The Nmos transistor has $V_t = 0.4\,V$ and $k_n'W/L = 1\,mA/V^2$. Give the equations used for each part of the final graph.

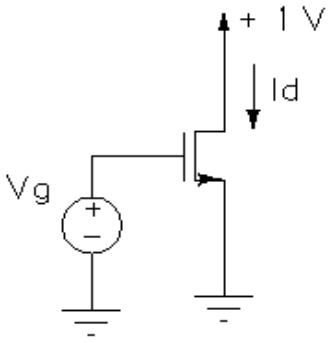


Figure 13.

14. Sketch Ix vs Vx for the circuit shown in Figure 14. Vx varies from 0 to 3V. The manufacturer specifies: PMOS Model: Level = 1, VTO = -0.8, GAMMA = 0.4, U0 = 100, LAMBDA = 0.2, TOX = 9e-9.

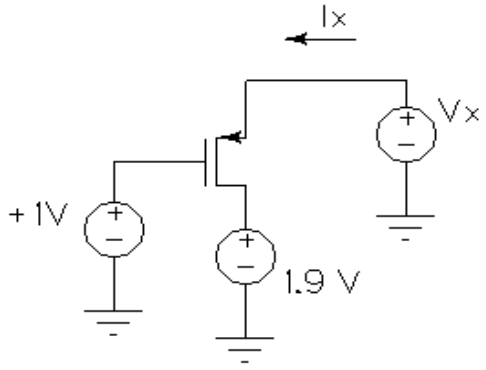


Figure 14.

15. Consider the circuit shown in Figure 15. Sketch Ix vs Vx. Vx varies from 0 to VDD. VDD = 3V. The manufacturer specifies: PMOS Model: Level = 1, VTO = -0.8, GAMMA = 0.4, U0 = 100, LAMBDA = 0.2, TOX = 9e-9.

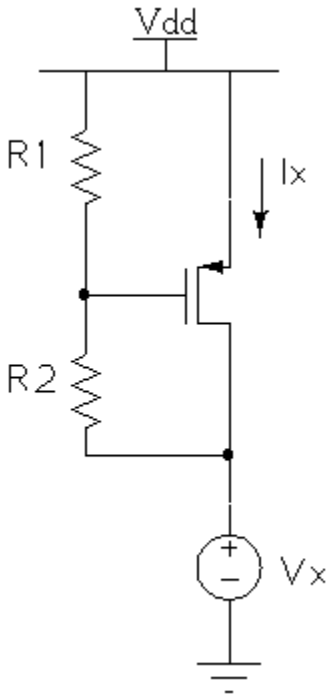


Figure 15.