

# Lecture 05: CMOS Amplifiers: Single-Ended First Part

**Javier Ardila**

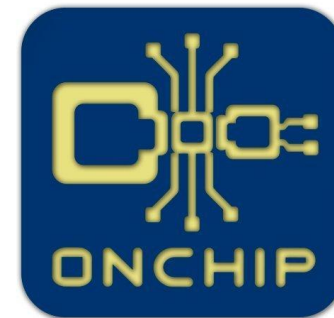
Reference: Razavi (Fundamentals) - Chapter 7

Slides by: Razavi & J. Ardila

Integrated Systems Research Group – OnChip

Universidad Industrial de Santander, Bucaramanga - Colombia

[javier.ardila@e3t.uis.edu.co](mailto:javier.ardila@e3t.uis.edu.co)



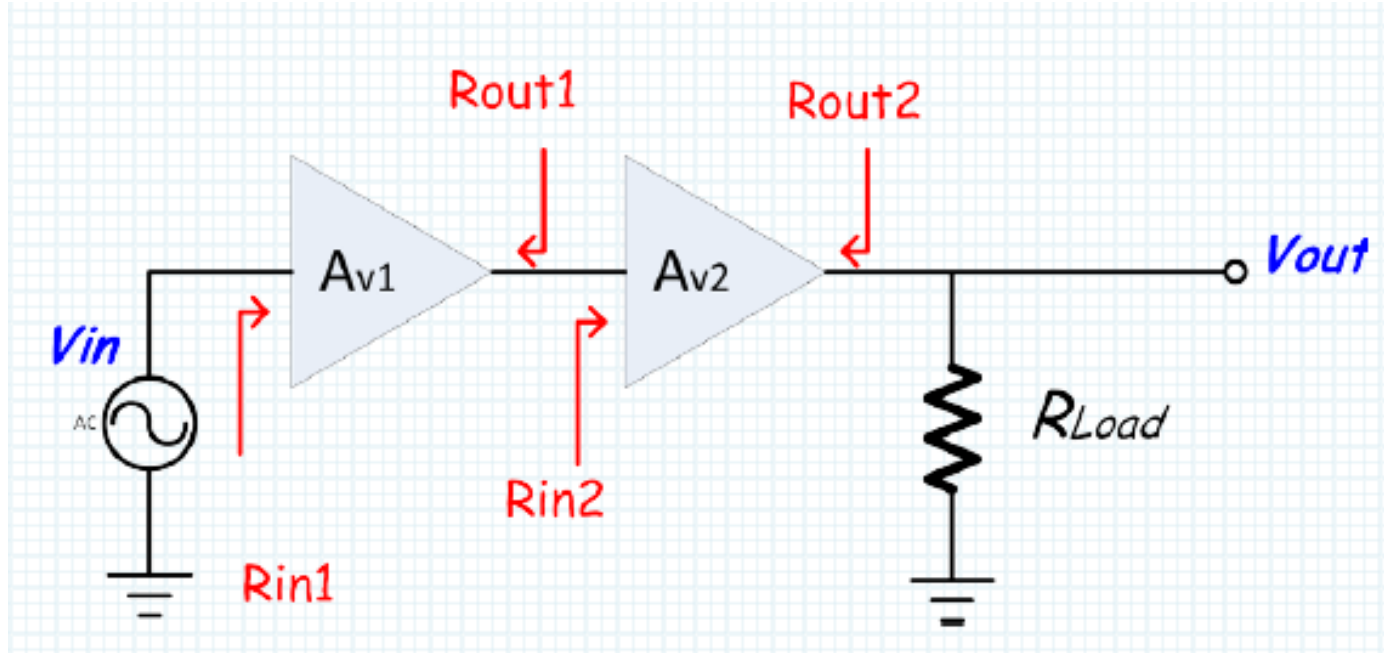
# Outline

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- ❑ General Considerations
- ❑ Common-Source Stage
- ❑ Common-Gate Stage
- ❑ Source-Follower Stage

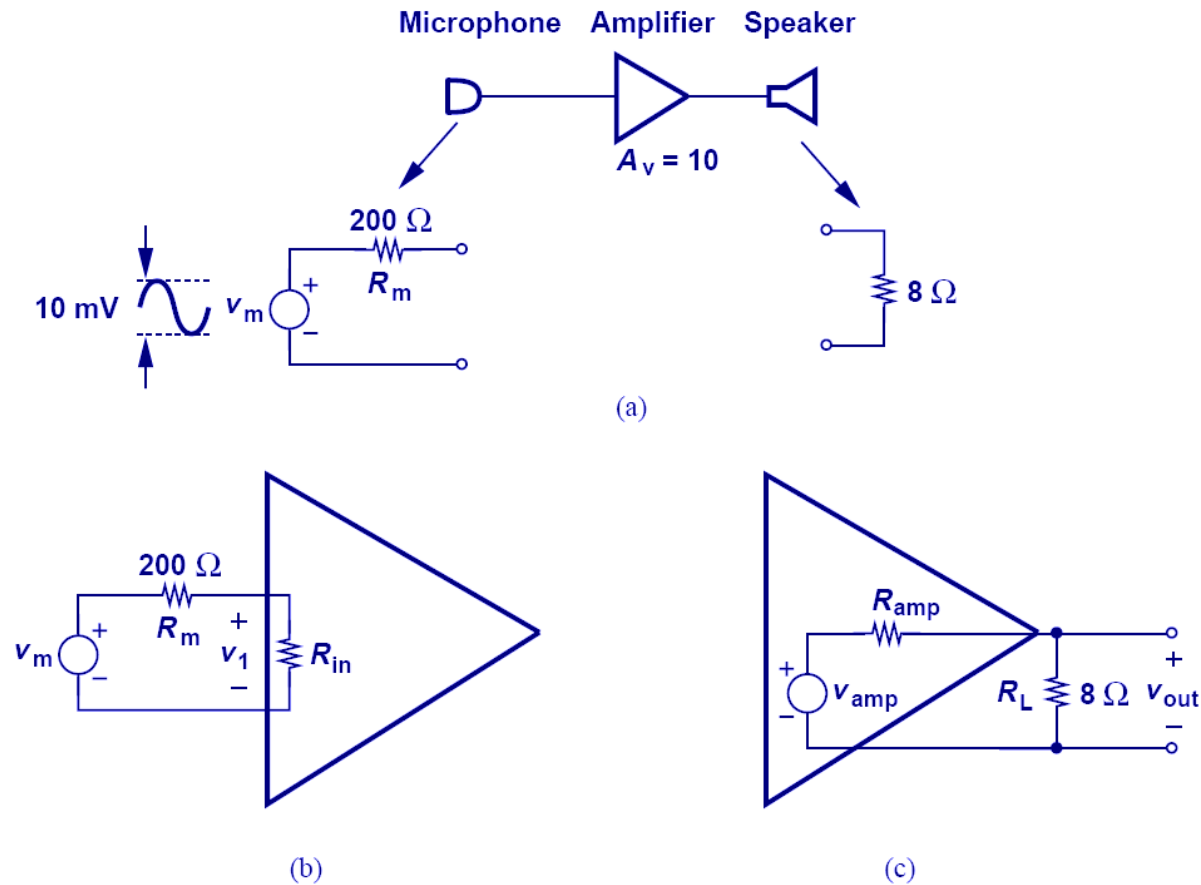
# Amplifier

- Amplification □ Why?



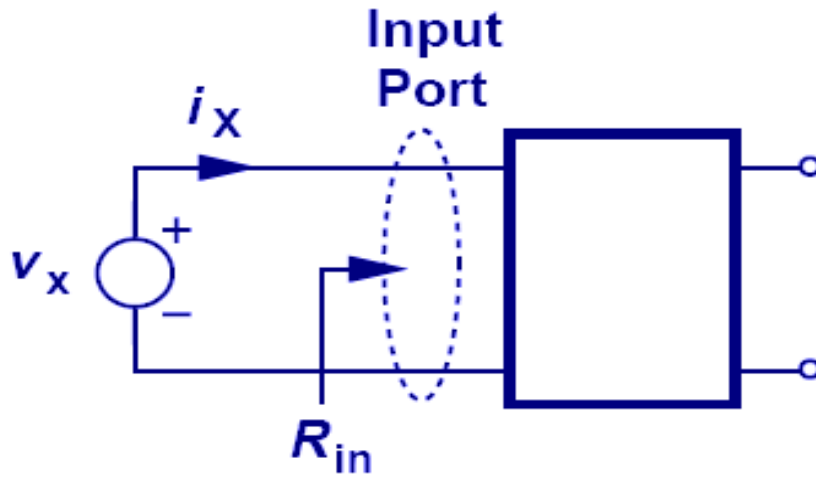
- Amplification is one of the most important concepts and function in electronics.
- We need and we want to amplify signals.

# Voltage Amplifier

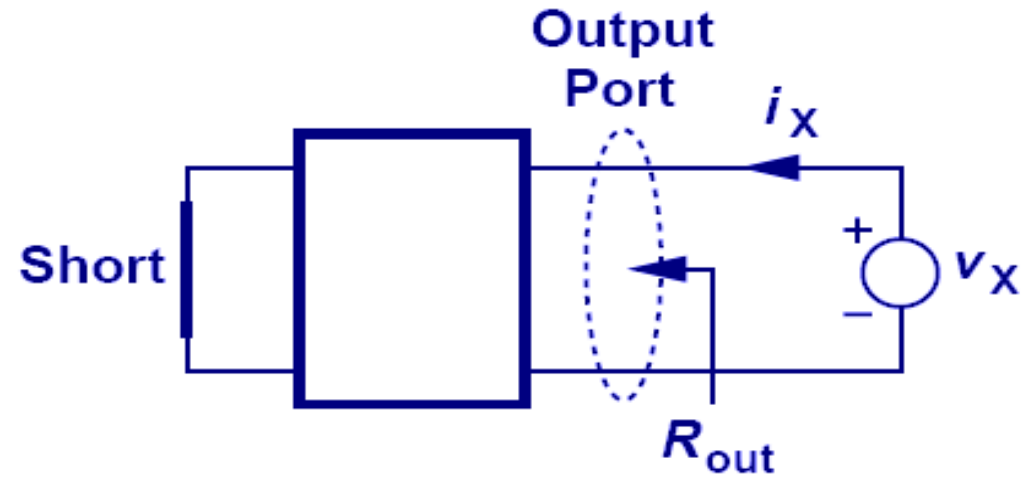


- ❑ In an ideal voltage amplifier, the input impedance is infinite and the output impedance zero.
- ❑ But in reality, input or output impedances depart from their ideal values.

# Input/Output Impedances



(a)

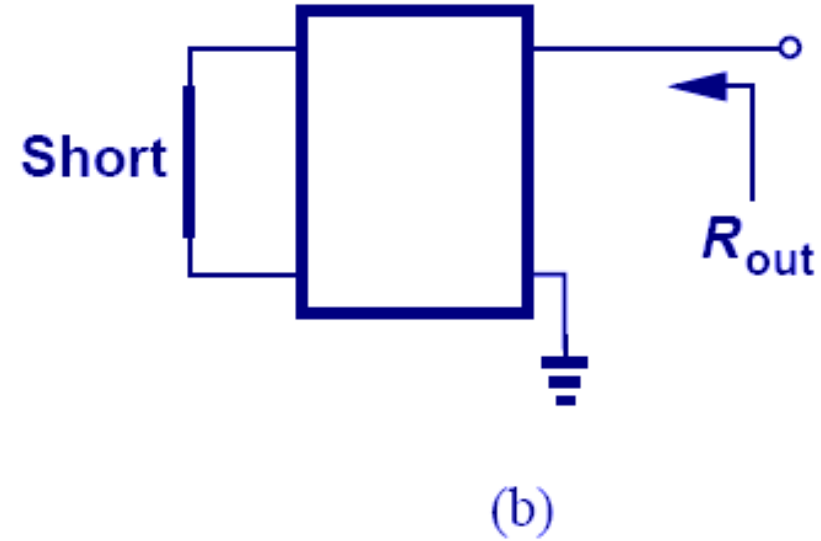
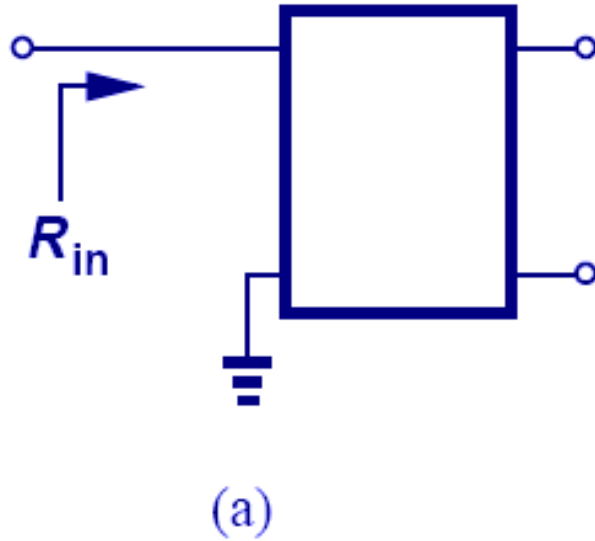


(b)

$$R_x = \frac{V_x}{i_x}$$

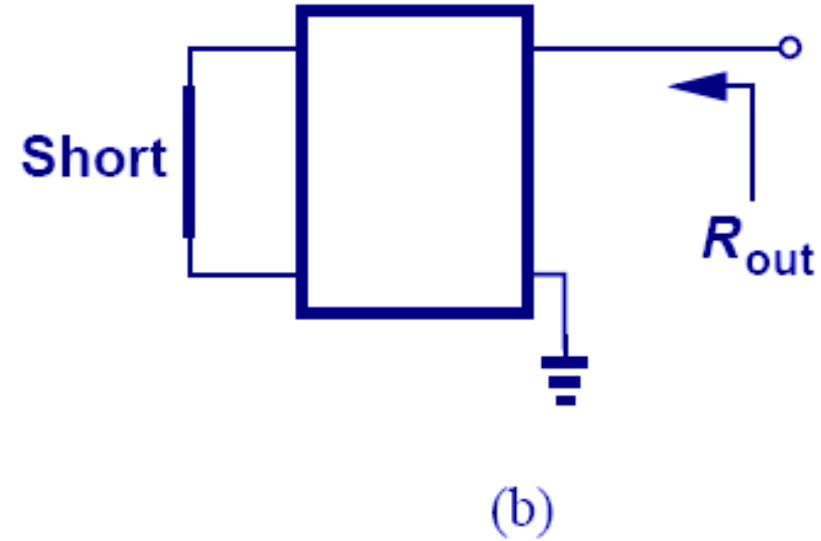
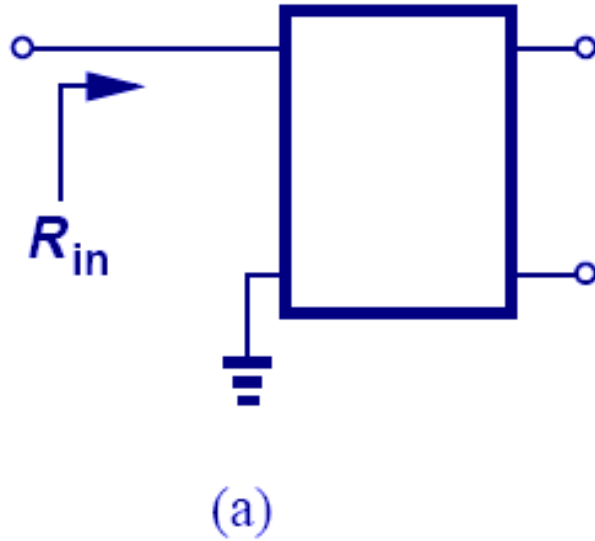
- The figure above shows the techniques for measuring input and output impedances.

# Impedance at a Node



- ❑ When calculating I/O impedances at a port, we usually ground one terminal while applying the test source to the other terminal of interest.
- ❑ Nodal impedance exercises

# Impedance at a Node

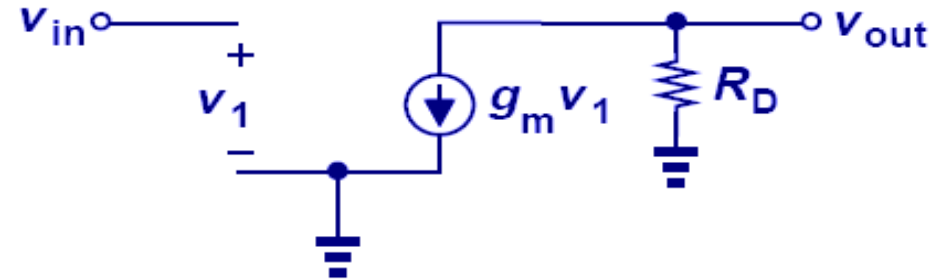
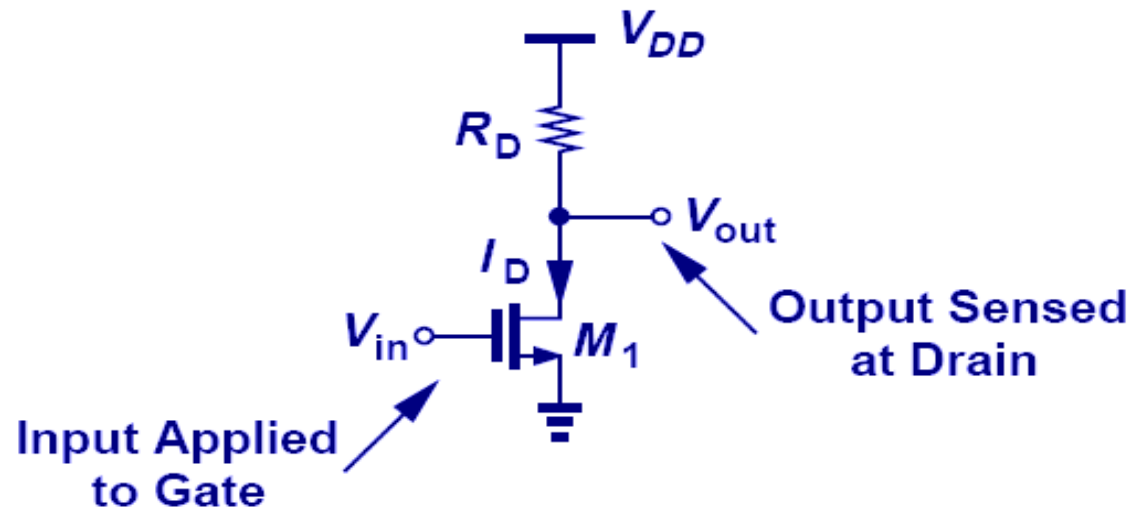


- ❑ When calculating I/O impedances at a port, we usually ground one terminal while applying the test source to the other terminal of interest.
- ❑ Nodal impedance exercises ❑ **TALLER!**



# Common-Source Stage

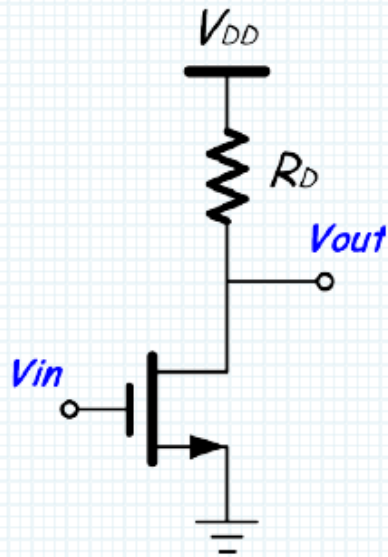
- ❑ How do you solve this?
- ❑ What is the meaning of “solving”?
- ❑ What are we doing?





# Common-Source Stage

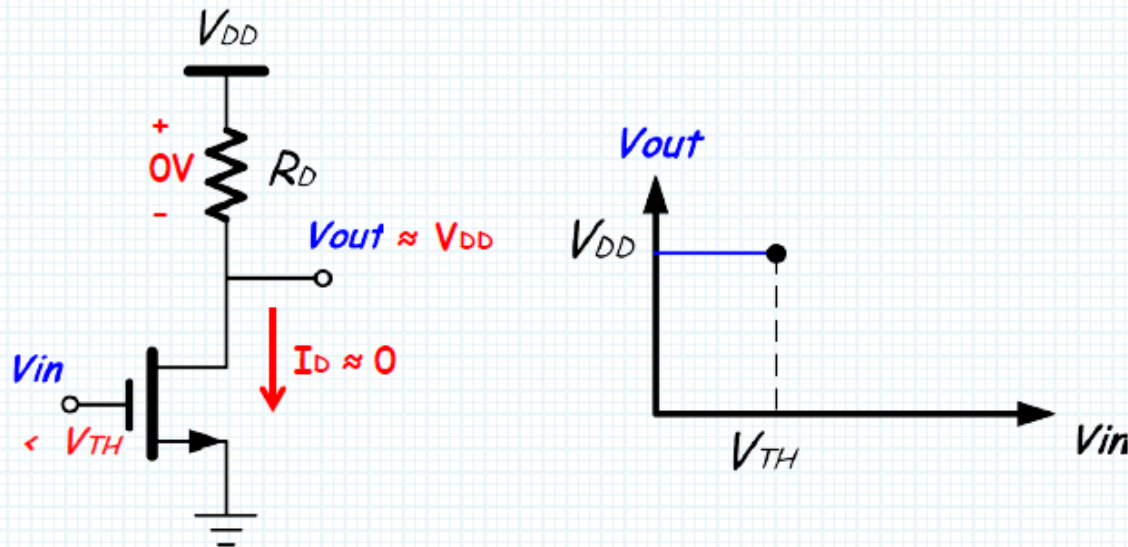
## *Fuente Común (Common Source CS)*



- Es la configuración más sencilla de amplificador de tensión.
- A través de ella se repasarán varios conceptos.

# Common-Source Stage

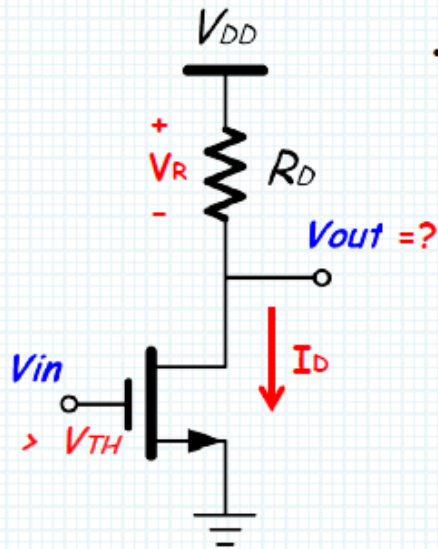
## *CS. Análisis a gran señal*



Mientras  $V_{in}$  no supere la tensión de umbral  $V_{TH}$  el transistor estará apagado y su corriente será aproximadamente igual a cero amperios. Esto se mantendrá así hasta que  $V_{in} = V_{TH}$

# Common-Source Stage

## CS Análisis gran señal



- $V_{out}$  comienza en un valor alto ( $\approx V_{DD}$ ) como se vio antes. Por tanto, se puede asumir que el transistor encenderá en saturación.

$$I_D = 0.5 \cdot \beta \cdot (V_{in} - V_{TH})^2$$

$$\text{siendo } \beta = \mu_n C_{ox} \cdot W/L$$

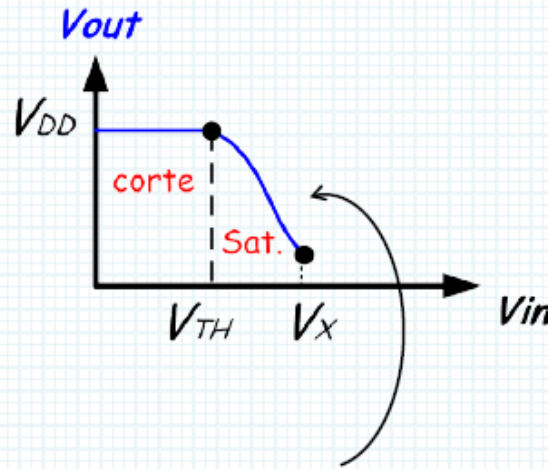
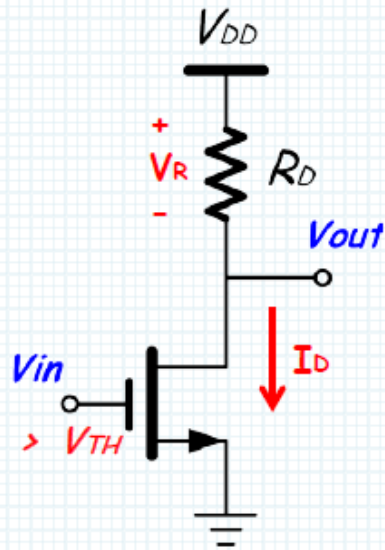
$$V_R = I_D \cdot R_D$$

$$\begin{aligned} V_{out} &= V_{DD} - V_R \\ &= V_{DD} - I_D \cdot R_D \end{aligned}$$

$$V_{out} = V_{DD} - 0.5 \cdot \beta \cdot R_D \cdot (V_{in} - V_{TH})^2$$

# Common-Source Stage

## CS Análisis gran señal

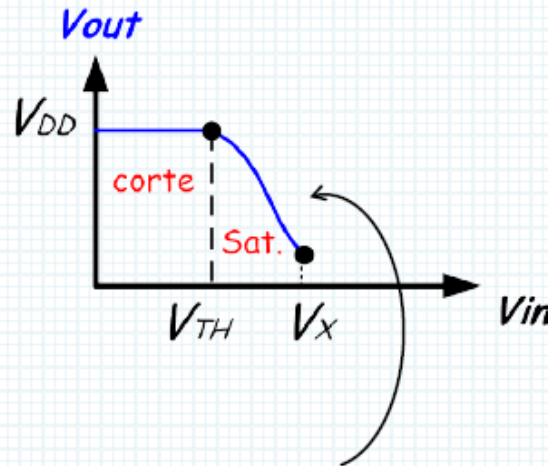
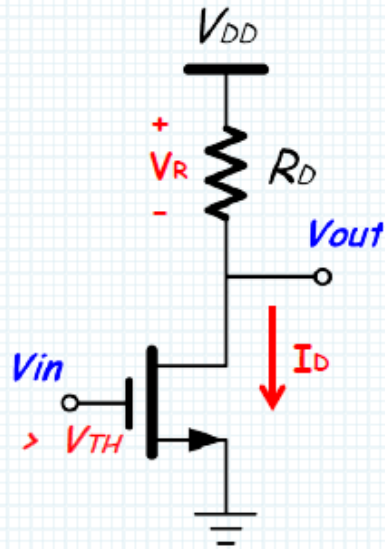


$$V_{out} = V_{DD} - 0.5 \cdot \beta \cdot R_D \cdot (V_{in} - V_{TH})^2$$

Esta ecuación corresponde a una parábola que abre hacia abajo. La condición se mantendrá hasta que el transistor entra en la región de triodo. **P:** ¿Por qué se sabe que entrará en triodo?

# Common-Source Stage

## CS Análisis gran señal



$$V_{out} = V_{DD} - 0.5 \cdot \beta \cdot R_D \cdot (V_{in} - V_{TH})^2$$

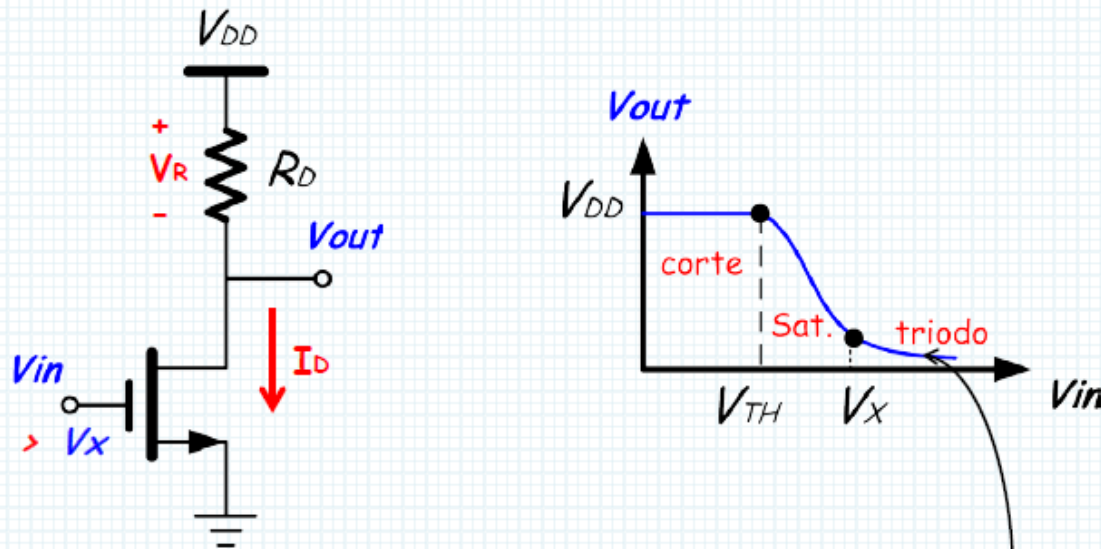
**R:** Observe que a medida que aumenta  $V_{in}$ , la tensión  $V_{out}$  está decreciendo. Esto favorece la operación en triodo ( $V_D < V_G - V_{TH}$ ). El transistor entrará en triodo cuando la tensión  $V_{in}$  alcance un valor  $V_x$  desconocido tal que:  $V_{out} = V_x - V_{TH}$

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# Common-Source Stage

## CS Análisis gran señal



A partir de esta región la ecuación que describe a la corriente se modifica:

$$I_D = \beta * [(V_{in} - V_{TH})V_{out} - 0.5 * V_{out}^2]$$

Y por tanto,

$$V_{out} = V_{DD} - \beta * [(V_{in} - V_{TH})V_{out} - 0.5 * V_{out}^2] * R_D$$

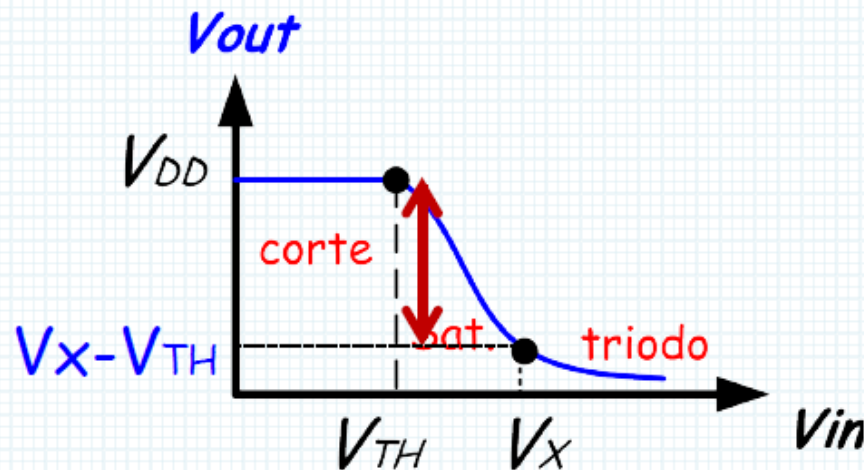
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# Common-Source Stage

## *Rangos de excursión*

- Máximo nivel de salida:  $V_{DD}$
- Mínimo nivel de salida:  $V_X - V_{TH}$
- Rango a la salida:  $V_{DD} - (V_X - V_{TH})$



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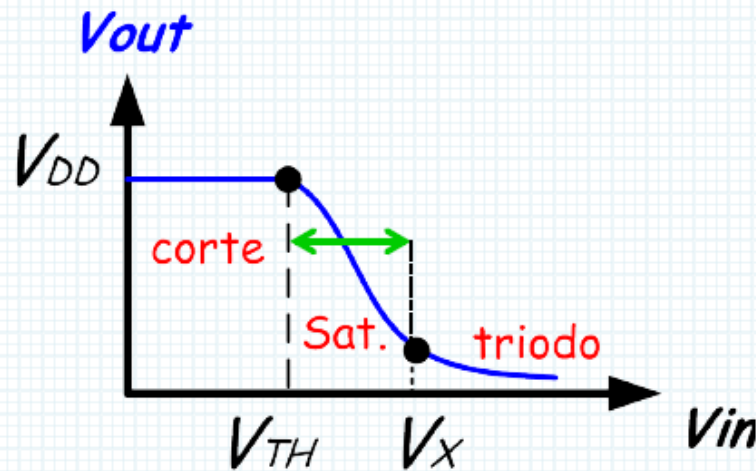
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# Common-Source Stage

## *Rangos de excursión*

- Máximo nivel de entrada:  $V_X$
- Mínimo nivel de entrada:  $V_{TH}$
- Rango de excursión a la entrada:  $V_X - V_{TH}$



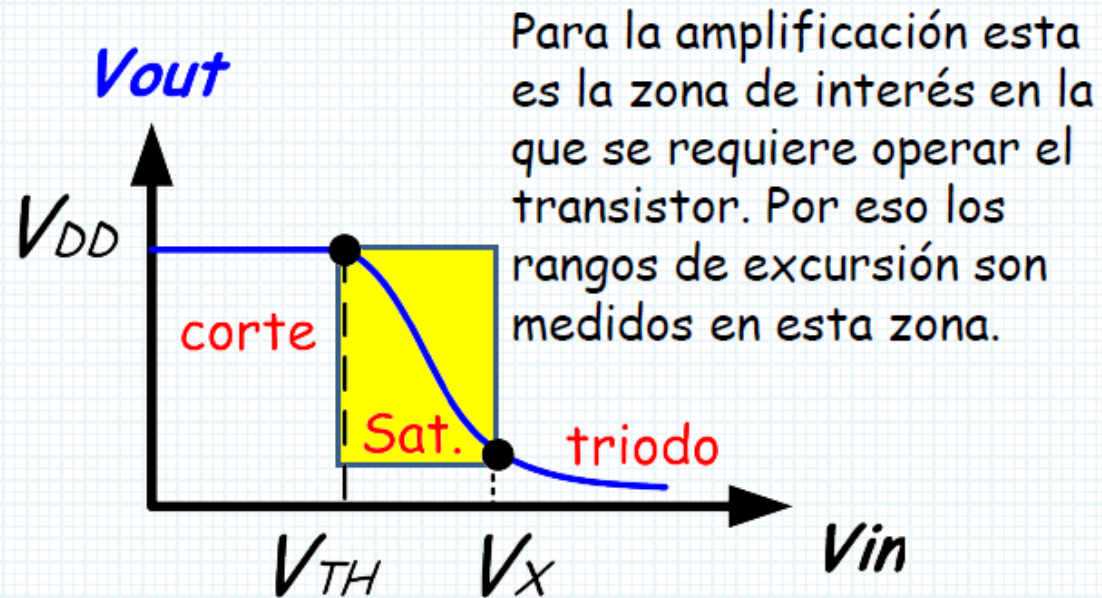
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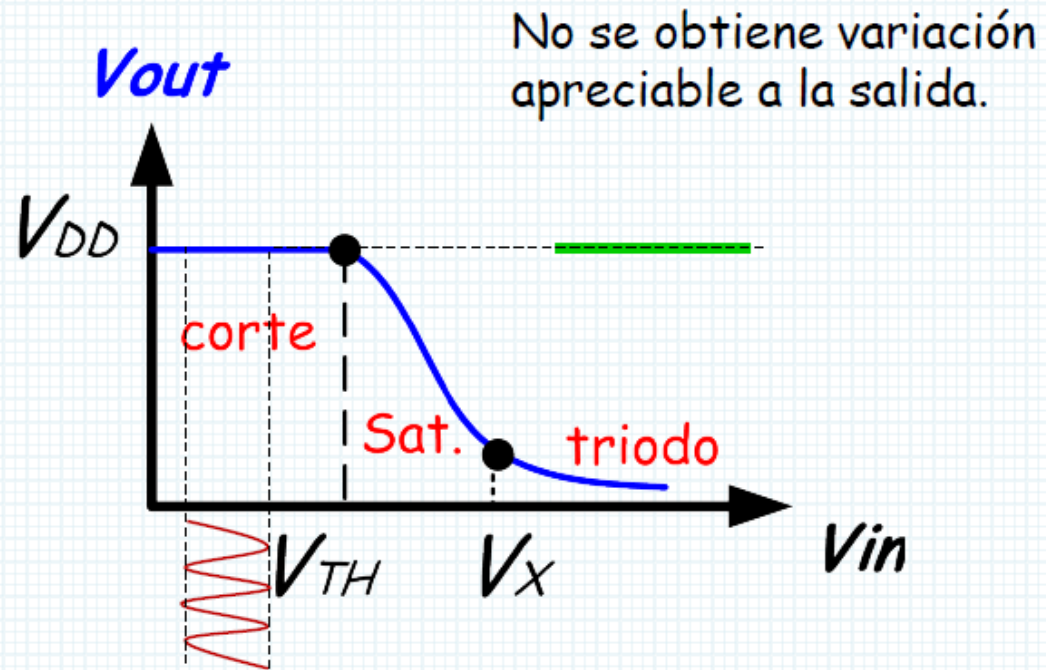
# Common-Source Stage

## *Zona de interés*



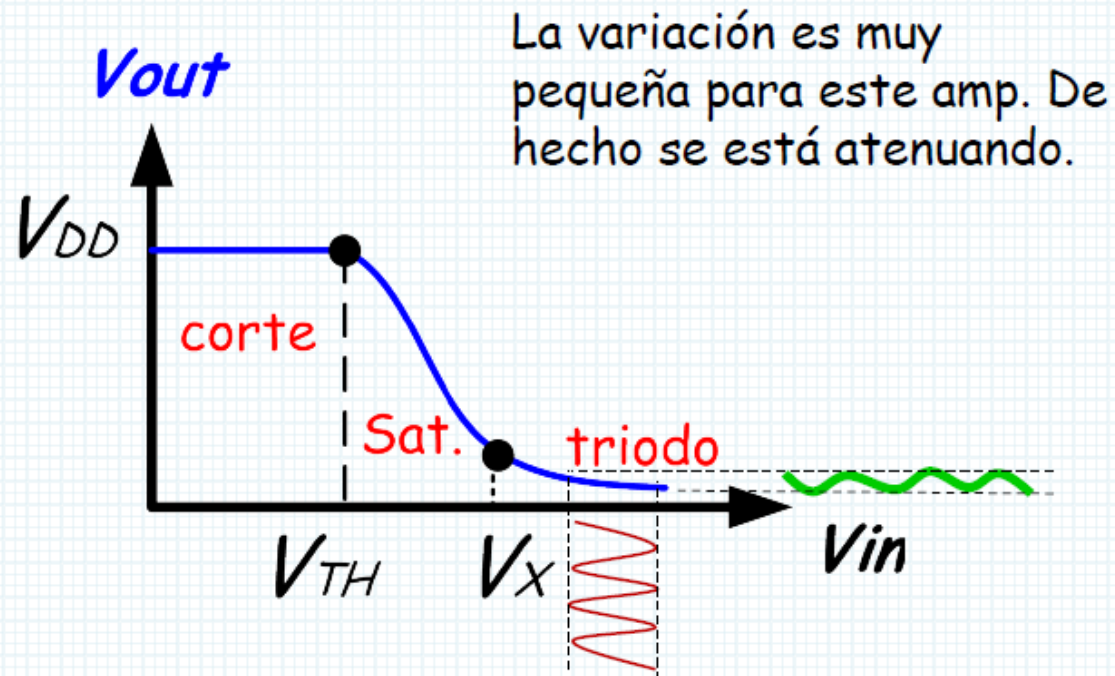
# Common-Source Stage

*En corte (?)*



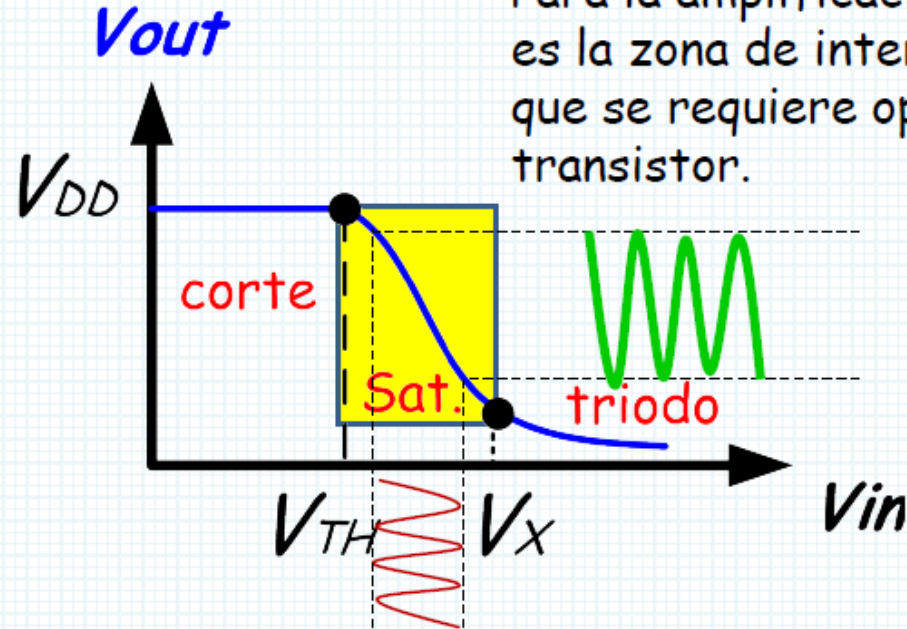
# Common-Source Stage

*En triodo (?)*



# Common-Source Stage

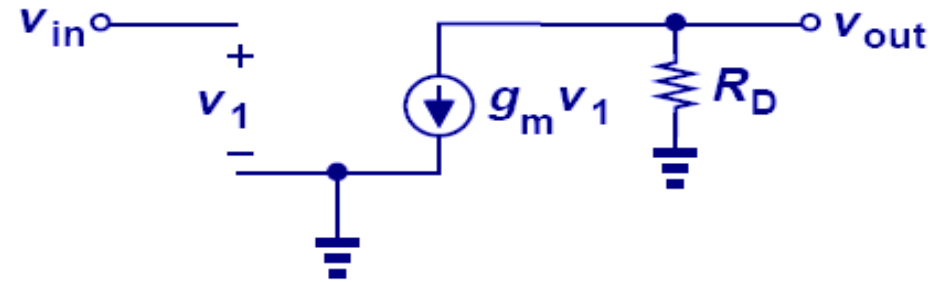
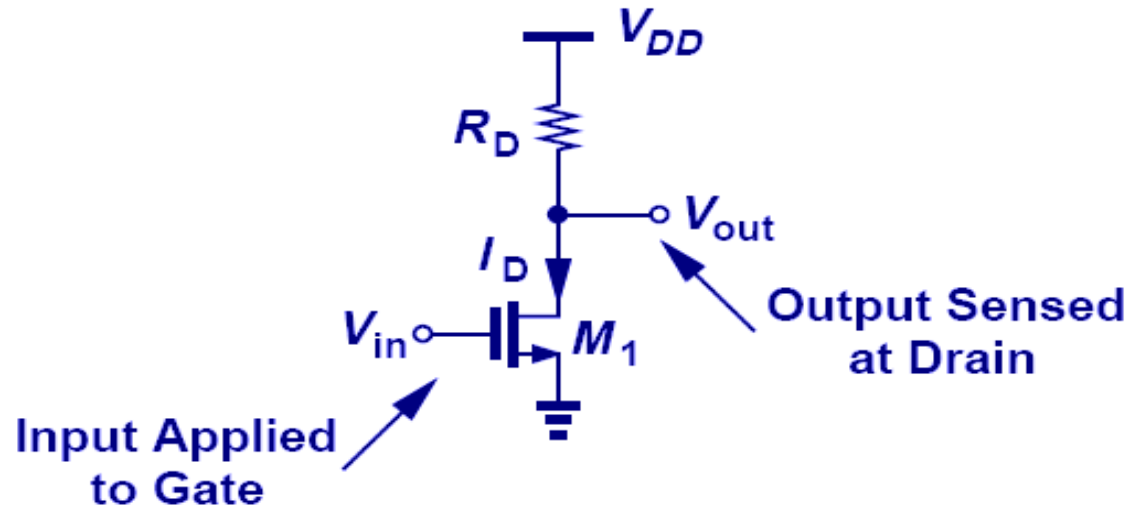
*Saturación*



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# Common-Source Stage with $\lambda=0$

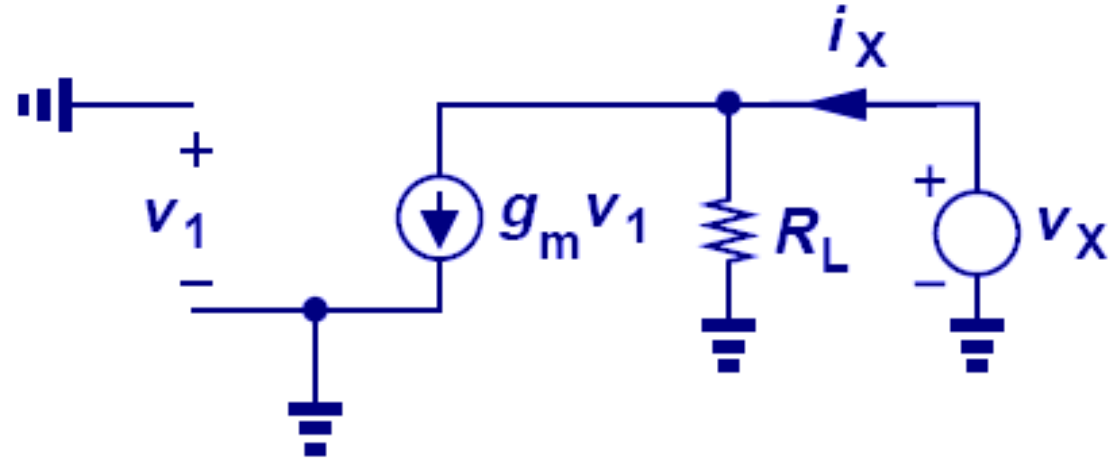


$$\lambda = 0$$

$$A_v = -g_m R_D$$

$$A_v = -\sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} R_D$$

# Common-Source Stage with $\lambda=0$

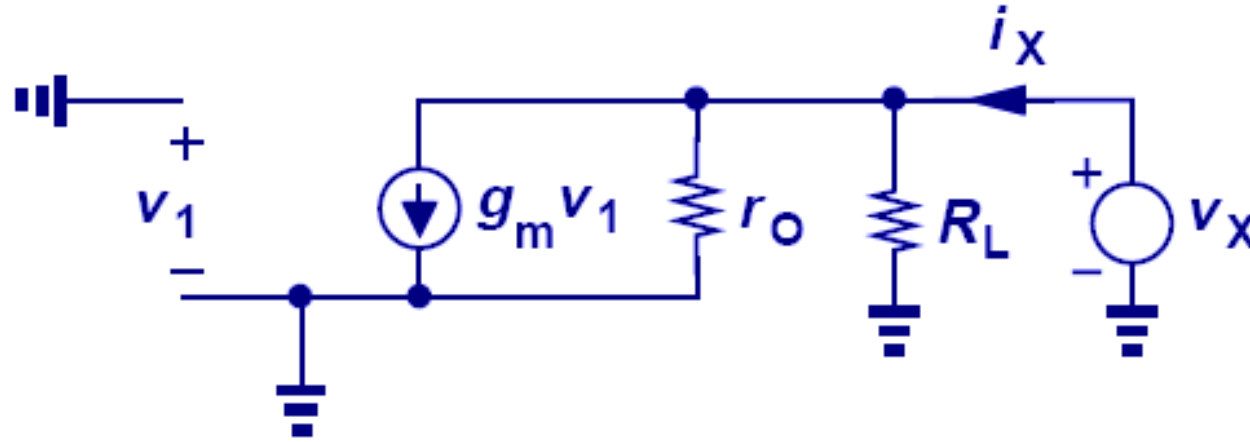


$$A_v = -g_m R_L$$

$$R_{in} = \infty$$

$$R_{out} = R_L$$

# Common-Source Stage with $\lambda \neq 0$



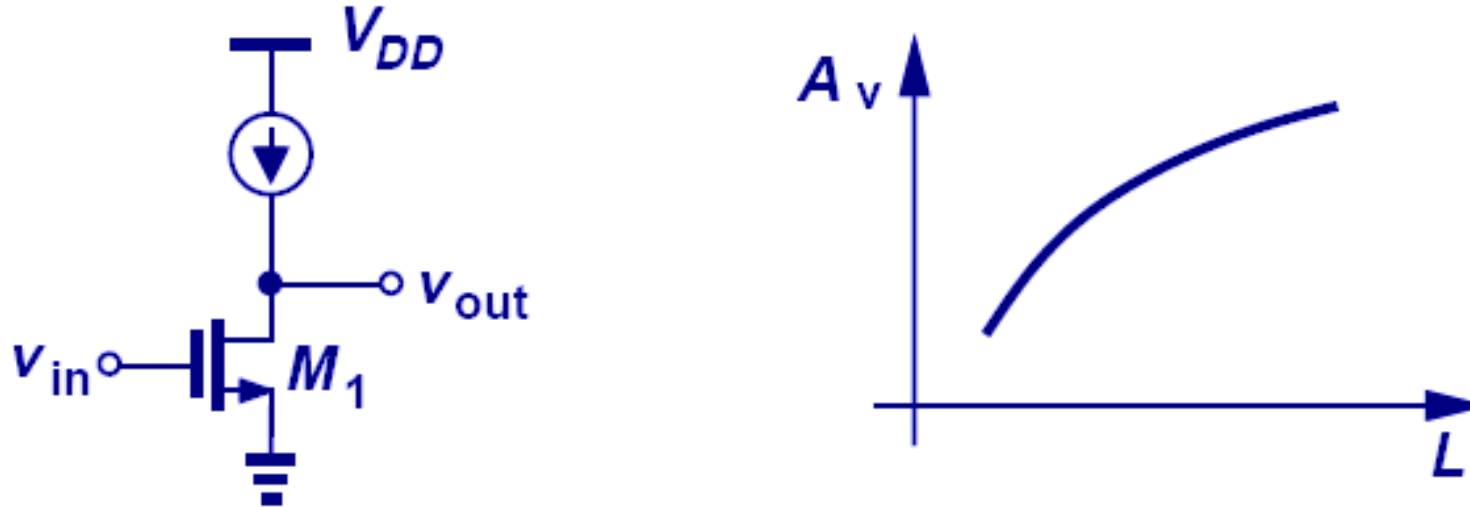
$$A_v = -g_m (R_L \parallel r_o)$$

$$R_{in} = \infty$$

$$R_{out} = R_L \parallel r_o$$

- However, Early effect and channel length modulation affect CE and CS stages in a similar manner.

# CS Gain Variation with Channel Length

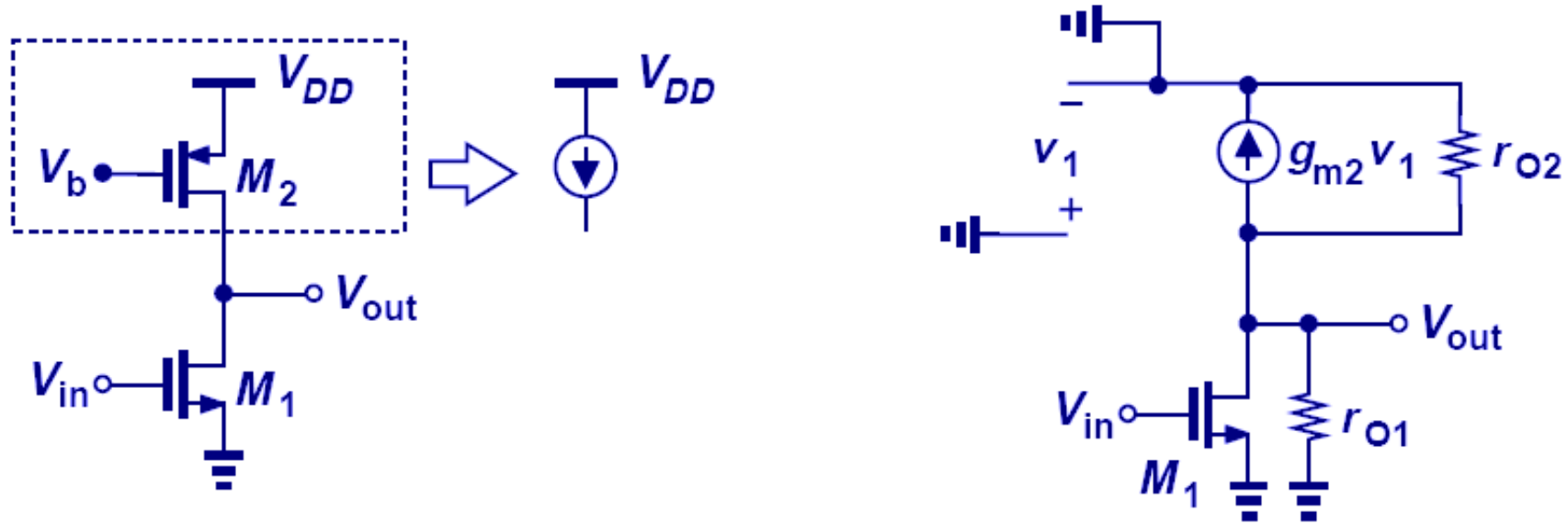


$$|A_v| = \frac{\sqrt{2\mu_n C_{ox} \frac{W}{L}}}{\lambda \sqrt{I_D}} \propto \sqrt{\frac{2\mu_n C_{ox} WL}{I_D}}$$

- Since  $\lambda$  is inversely proportional to  $L$ , the voltage gain actually becomes proportional to the square root of  $L$ .



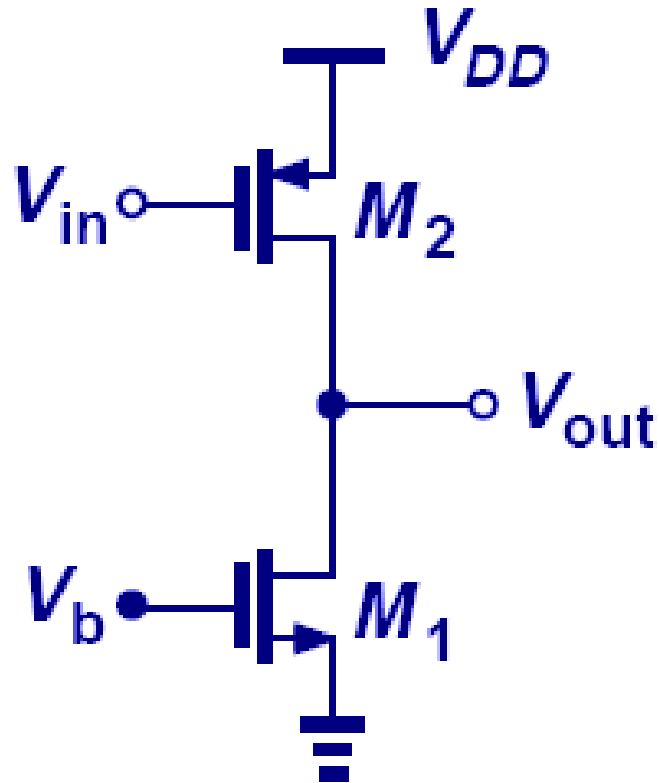
# CS Stage with Current-Source Load



$$A_v = -g_{m1} (r_{O1} \parallel r_{O2})$$
$$R_{out} = r_{O1} \parallel r_{O2}$$

- To alleviate the headroom problem, an active current-source load is used.
- This is advantageous because a current-source has a high output resistance and can tolerate a small voltage drop across it.

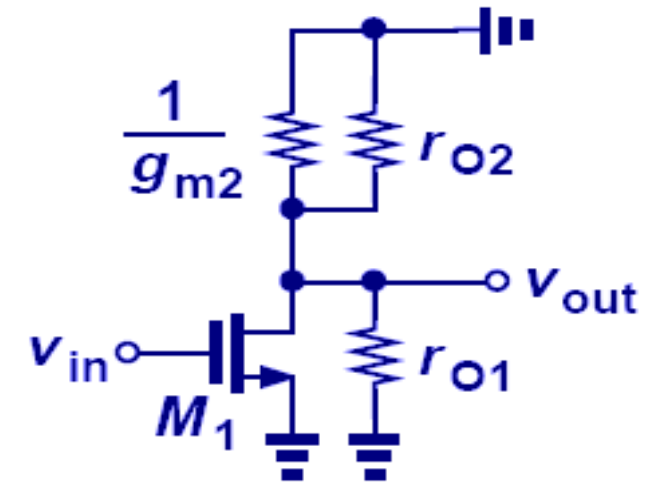
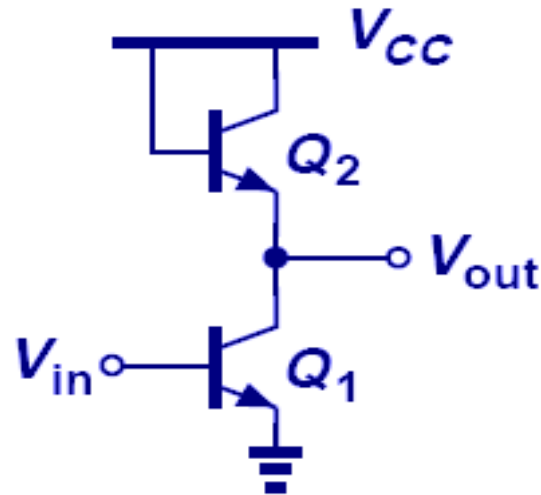
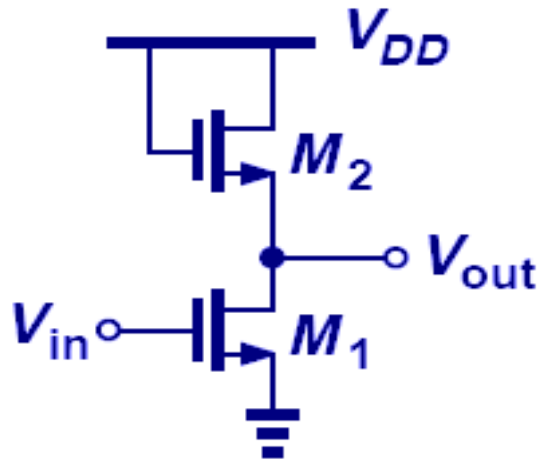
# PMOS CS Stage with NMOS as Load



$$A_v = -g_{m2}(r_{o1} \parallel r_{o2})$$

- Similarly, with PMOS as input stage and NMOS as the load, the voltage gain is the same as before.

# CS Stage with Diode-Connected Load

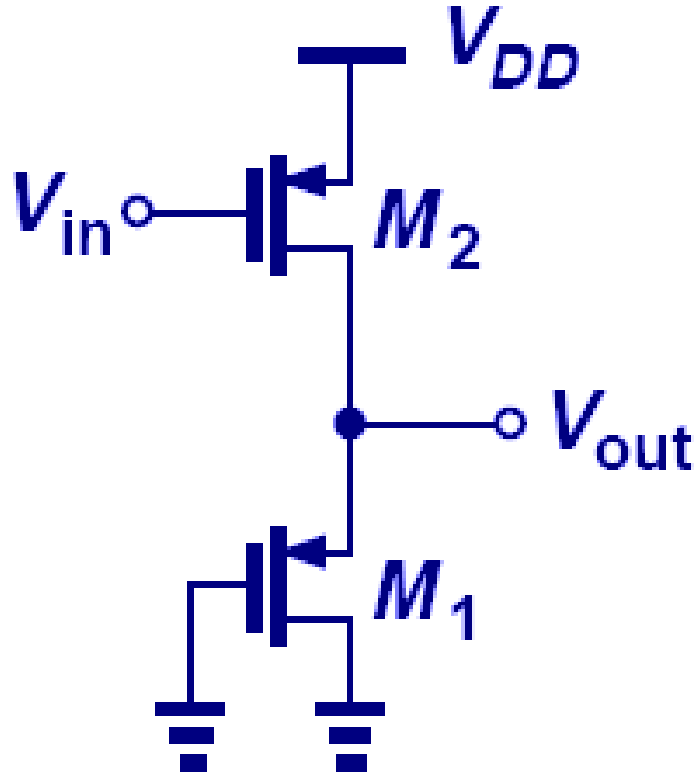


$$A_v = -g_{m1} \cdot \frac{1}{g_{m2}} = -\sqrt{\frac{(W/L)_1}{(W/L)_2}}$$

$$A_v = -g_{m1} \left( \frac{1}{g_{m2}} \parallel r_{o2} \parallel r_{o1} \right)$$

➤ Lower gain, but less dependent on process parameters.

# CS Stage - Diode-Connected PMOS Device



$$A_v = -g_{m2} \left( \frac{1}{g_{m1}} \parallel r_{o1} \parallel r_{o2} \right)$$

- Note that PMOS circuit symbol is usually drawn with the source on top of the drain.

# Something else about basic amp. stages

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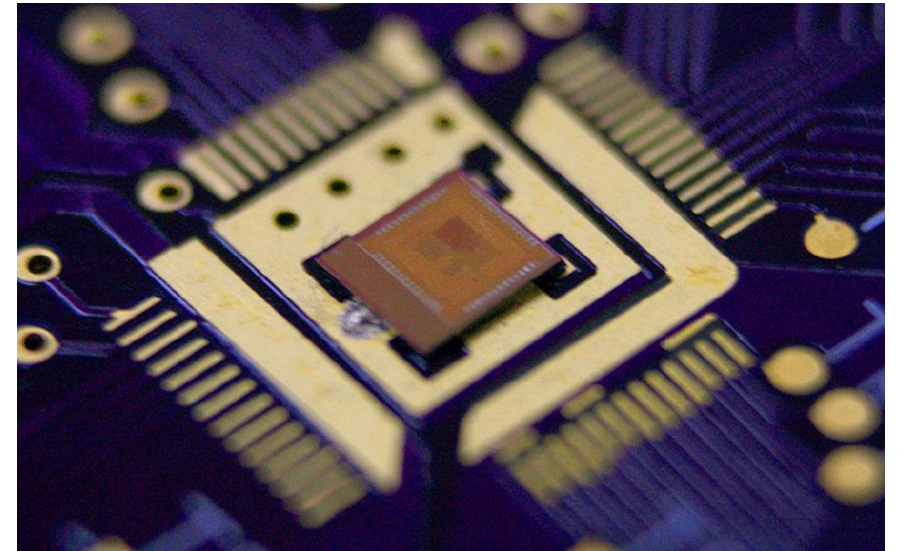
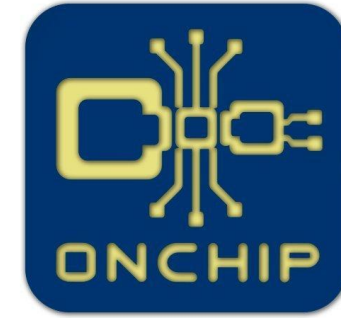
Common-Source Stage	Source Follower	Common-Gate Stage	Cascode
With Resistive Load	With Resistive Bias	With Resistive Load	Telescopic
With Diode-Connected Load	With Current-Source Bias	With Current-Source Load	Folded
With Current-Source Load			
With Active Load			
With Source Degeneration			

# Thanks

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*[javier.ardila@correo.uis.edu.co](mailto:javier.ardila@correo.uis.edu.co)*



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