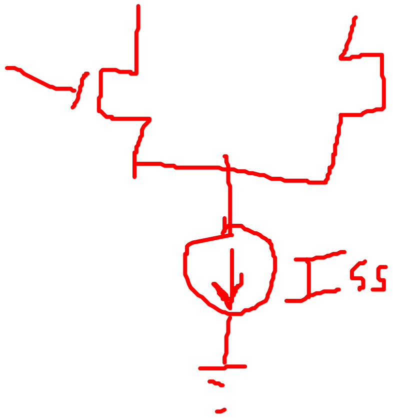
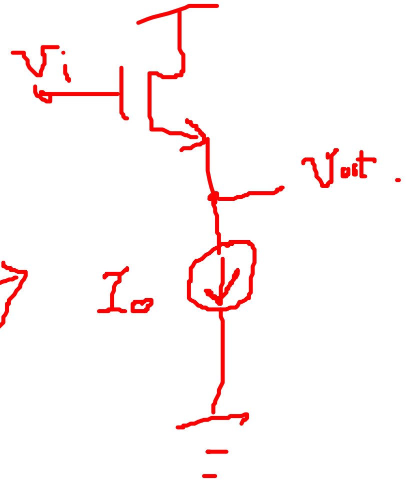


Current Mirrors



Javier Ardila

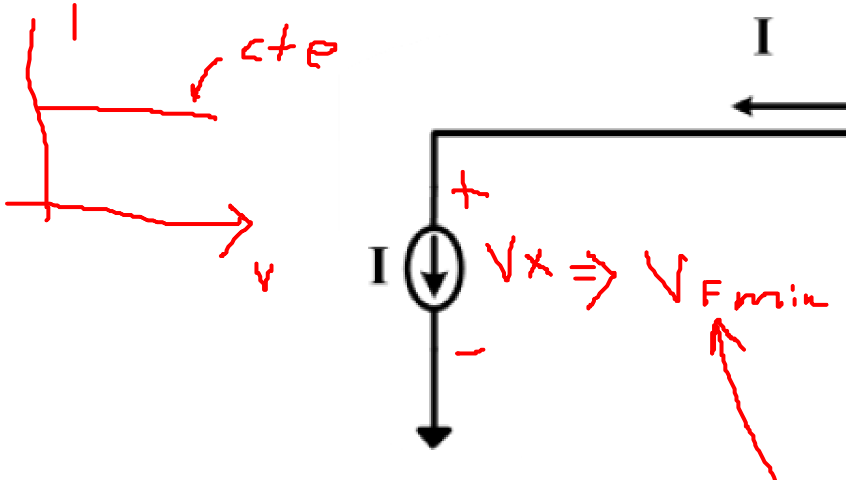
Integrated Systems Research Group – OnChip

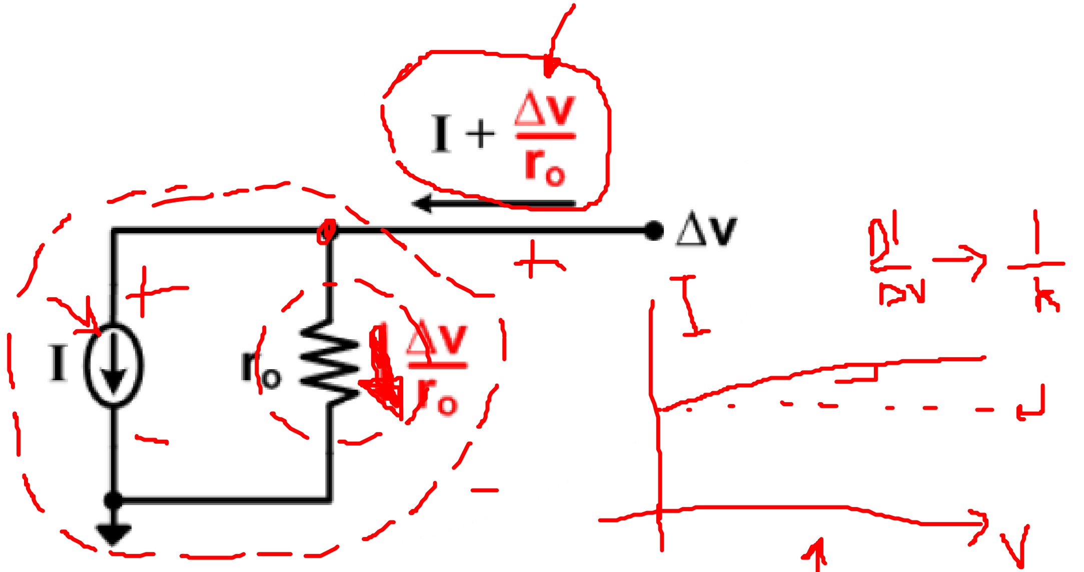
Universidad Industrial de Santander, Bucaramanga - Colombia

javier.ardila@e3t.uis.edu.co

Current Source Properties

➢ Output resistance:

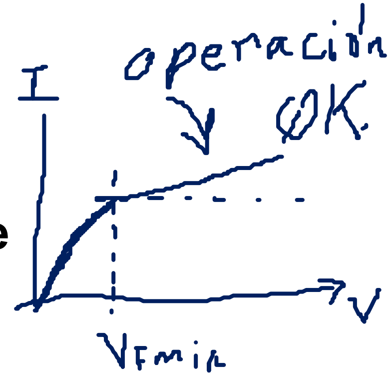




➢ Finite output resistance degrades current source accuracy and amplifier gain.

➢ Other important properties:

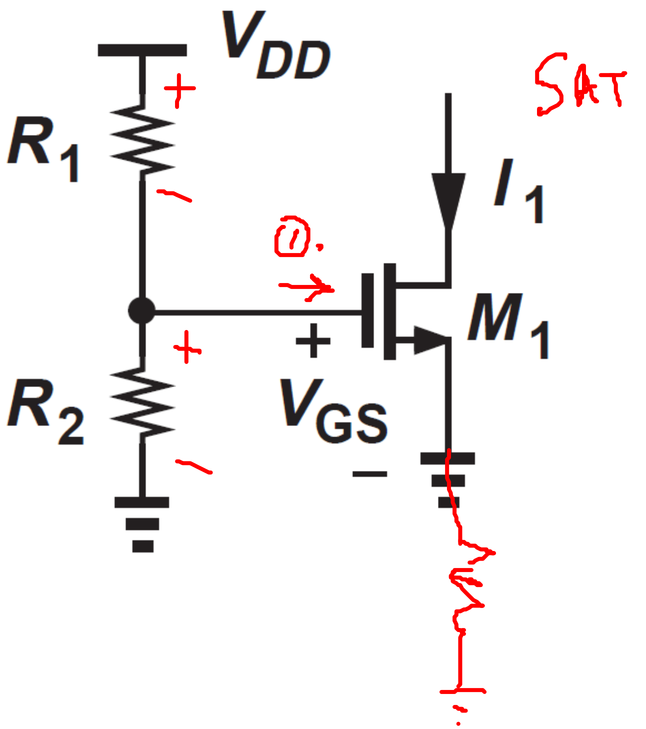
- Compliance voltage (headroom voltage in this case) → maximum voltage that the current source can supply to a load.



- Accuracy → Copias

- Noise

Circuits Biasing Issues

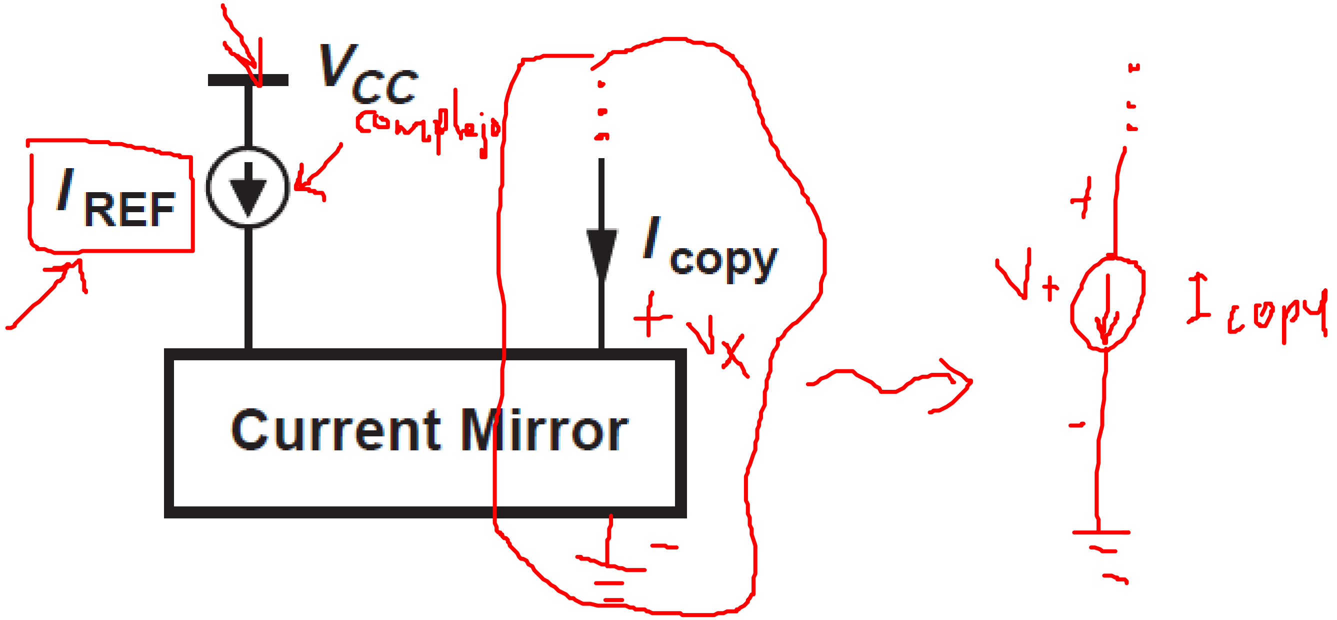


$$I_1 = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(\frac{R_2}{R_1 + R_2}V_{DD} - V_{TH}\right)^2$$

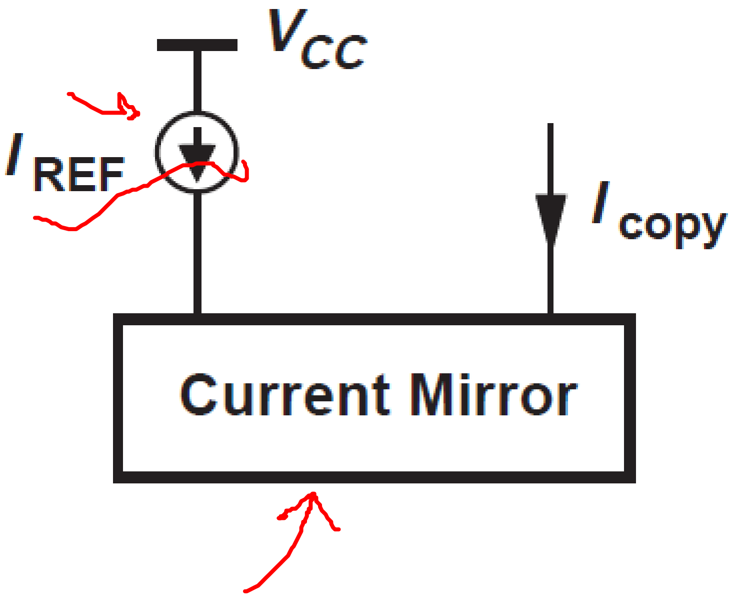
➢ **Assuming saturation, I_D is sensitive to: supply (V_{DD}), process (V_{TH} & $\mu_n C_{OX}$) and Temperature (V_{TH} & μ_n). So this is not a good biasing.**

High-Accuracy Current Sources



- Generating a high-accuracy current source (I_{REF}) is possible through a "bandgap reference" circuit, which employs several tens of devices to generate a supply-, process- and temperature-independent voltage.
- However, putting I_{REF} wherever it's needed implies a high cost in terms of area.

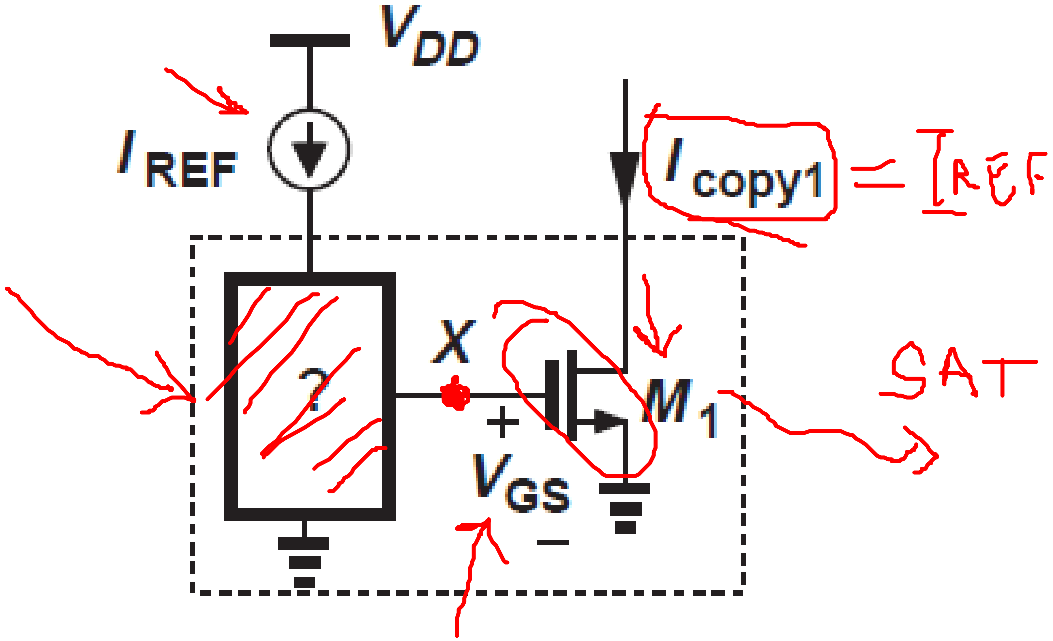
Current Mirror as a Solution



- Given the area problems, generating only one I_{REF} and copying its current value to wherever it's necessary rises as a possible solution.

How to copy current?

λ=0

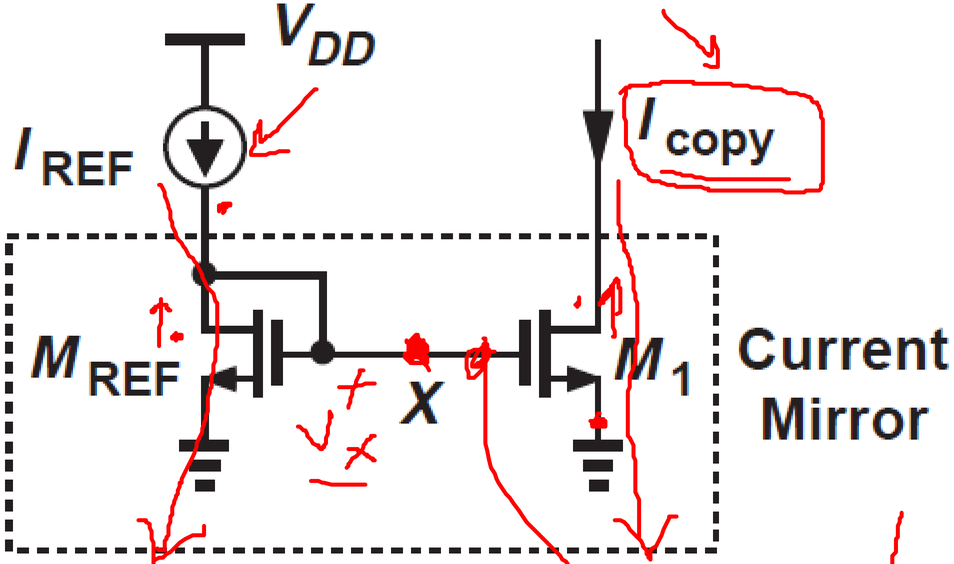


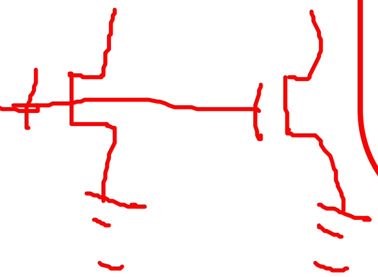
$$\boxed{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_X - V_{TH1})^2 = I_{REF}}$$

➢ **What should the black box be so that $I_{REF} \approx I_{copy1}$?**

Simple Current Mirror

$\boxed{\lambda=0}$





SAT

$$I_{D,REF} = \frac{1}{2}\cancel{\mu_n C_{ox}}\left(\frac{W}{L}\right)_{REF}(V_X - \cancel{V_{TH}})^2$$

$$I_{copy} = \frac{1}{2}\cancel{\mu_n C_{ox}}\left(\frac{W}{L}\right)_1(V_X - \cancel{V_{TH}})^2$$

$$I_{copy} = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_{REF}} I_{REF}$$

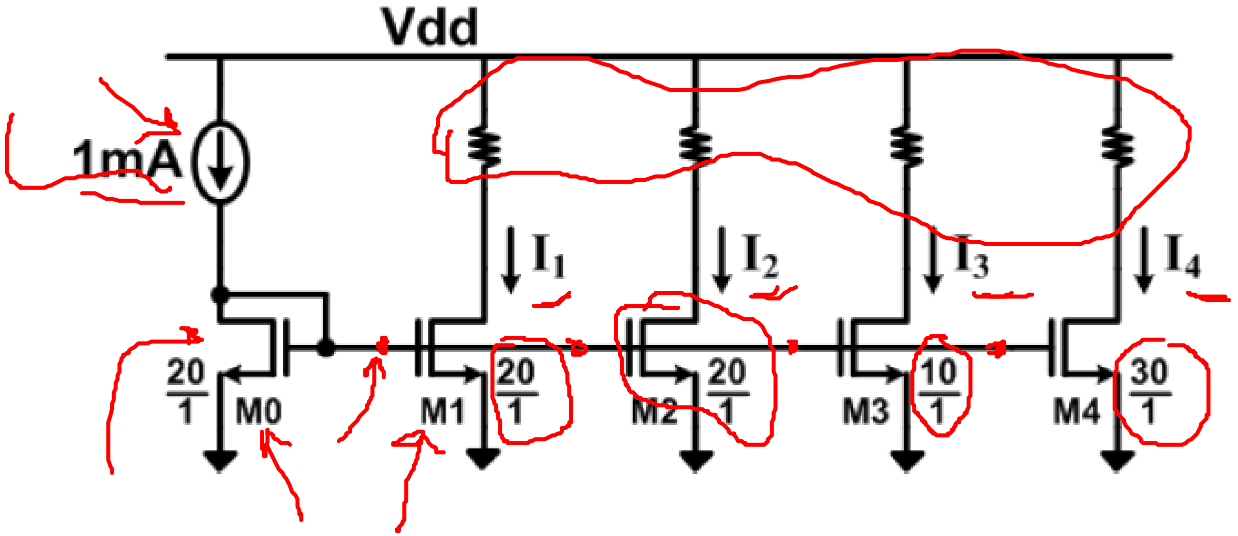
Si $M_1 = M_{REF}$

- $I_{D,REF} \approx I_{copy}$ if $(W/L)_{REF} = (W/L)_1$

Current Multiplication With CMs

$K' = \mu_n C_{ox} \frac{W}{L}$

λ=0



$I_1 = 1mA$

$I_2 = 1mA$

$I_3 = 0.5mA$

$I_4 = 1.5mA$

$$I_{copy} = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_{REF}} I_{REF}$$

$\frac{20}{1} = \frac{20\mu m}{1\mu m}$

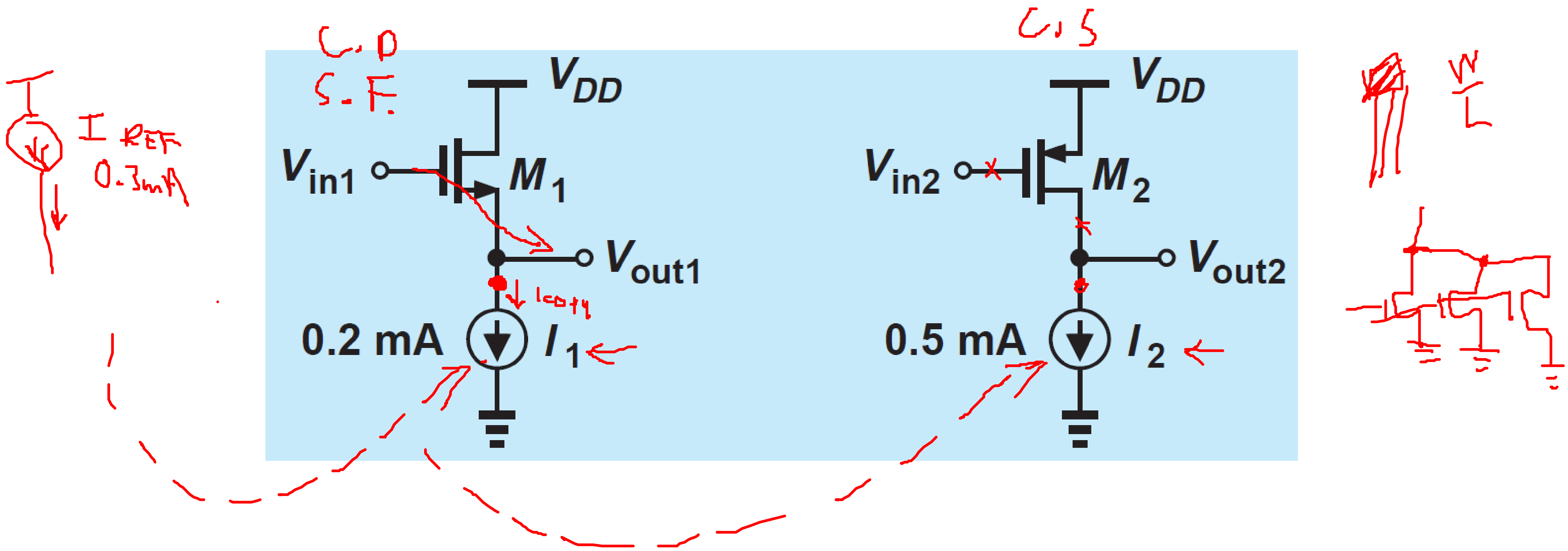
- **Next time: What happens if we consider λ=0?**

  Are there more current mirror configurations?

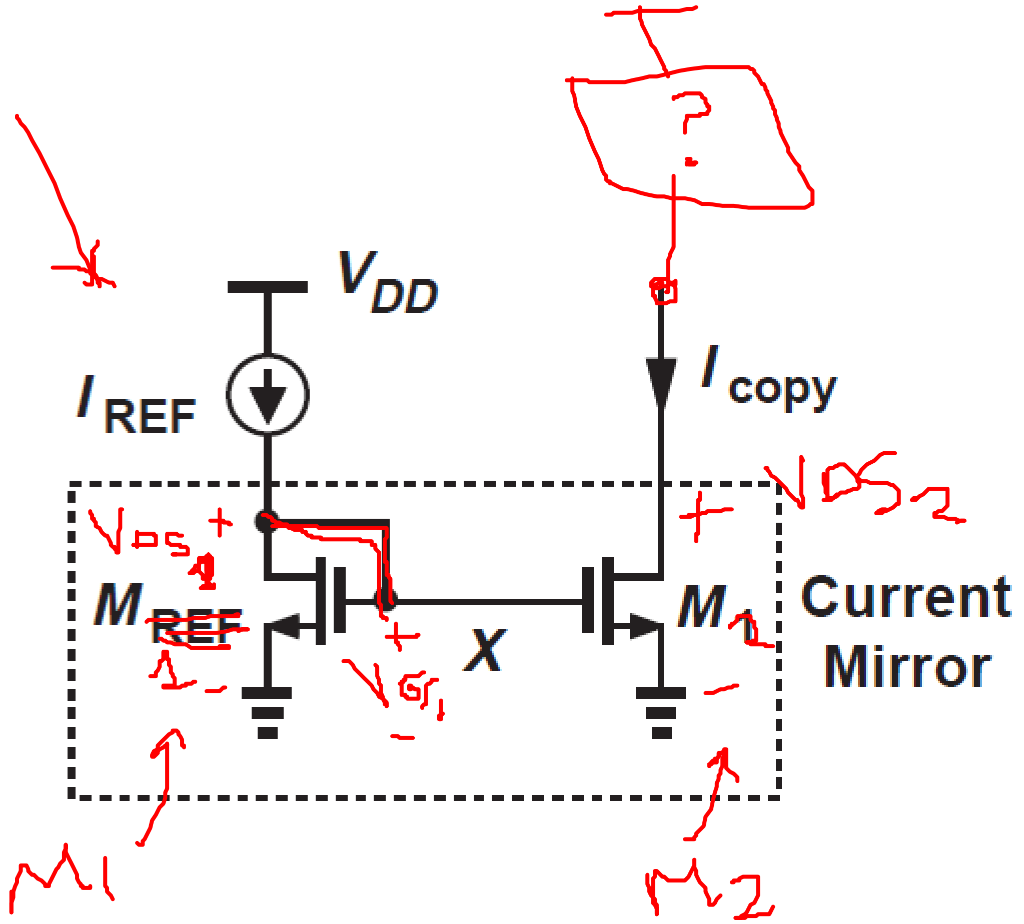
Additional points!!! - Design Exercise

- In 10min, design a current mirror that produces I_1 and I_2 from an I_{REF} of 0.3mA.

$\lambda=0$



Accuracy Limitations of Simple CMs



$$I_{D1} = \frac{1}{2}\cancel{\mu_n C_{ox}}\left(\frac{W}{L}\right)_1 \cancel{(V_{GS} - V_{TH})^2}(1 + \lambda V_{DS1})$$

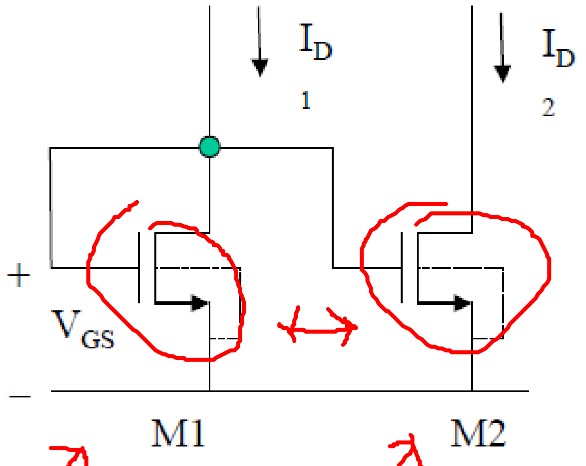
$$I_{D2} = \frac{1}{2}\cancel{\mu_n C_{ox}}\left(\frac{W}{L}\right)_2 \cancel{(V_{GS} - V_{TH})^2}(1 + \lambda V_{DS2})$$

$$\frac{I_{D2}}{I_{D1}} = \boxed{\frac{(W/L)_2}{(W/L)_1}} \cdot \boxed{\frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}}$$

V_{GS_1}

➢ **Channel-length modulation induces inaccuracy in simple current mirrors.**

Accuracy Limitations of Simple CMs



In general $(W/L)_2=N(W/L)_1$, most probably VT1≠VT2, then

$$I_{D2} = \frac{\mu_n C_{OX}}{2}\left(\frac{W}{L}\right)_2 (V_{GS}-V_T)^2(1+\lambda_2 V_{DS2})$$

$$I_{D2} = \frac{\frac{\mu_n C_{OX}}{2}\left(\frac{W}{L}\right)_2 (V_{GS}-V_{T2})^2(1+\lambda_2 V_{DS2})}{\frac{\mu_n C_{OX}}{2}\left(\frac{W}{L}\right)_1 (V_{GS}-V_{T1})^2(1+\lambda_1 V_{DS1})} I_{D1} = \frac{K_{P2}(V_{GS}-V_{T2})^2(1+\lambda_2 V_{DS2})}{K_{P1}(V_{GS}-V_{T1})^2(1+\lambda_1 V_{DS1})} N I_{D1}$$

$$\text{Error} \approx \lambda_2 V_{DS2} \neq \lambda_1 V_{DS1}$$

$$\text{Error} \approx K_{P2} \neq K_{P1}$$

$$\text{Error} \approx V_{T2} \neq V_{T1}$$

$$\lambda \propto \frac{1}{L}$$

Long devices reduce the error; make VDS1=VDS2

Errors can be reduced (but not eliminated) by using replicas of the main device and good layout!

Effective mobility and threshold voltages are sensitive to V_{DS}.and Vdsat

Good solution ==> use cascode structures

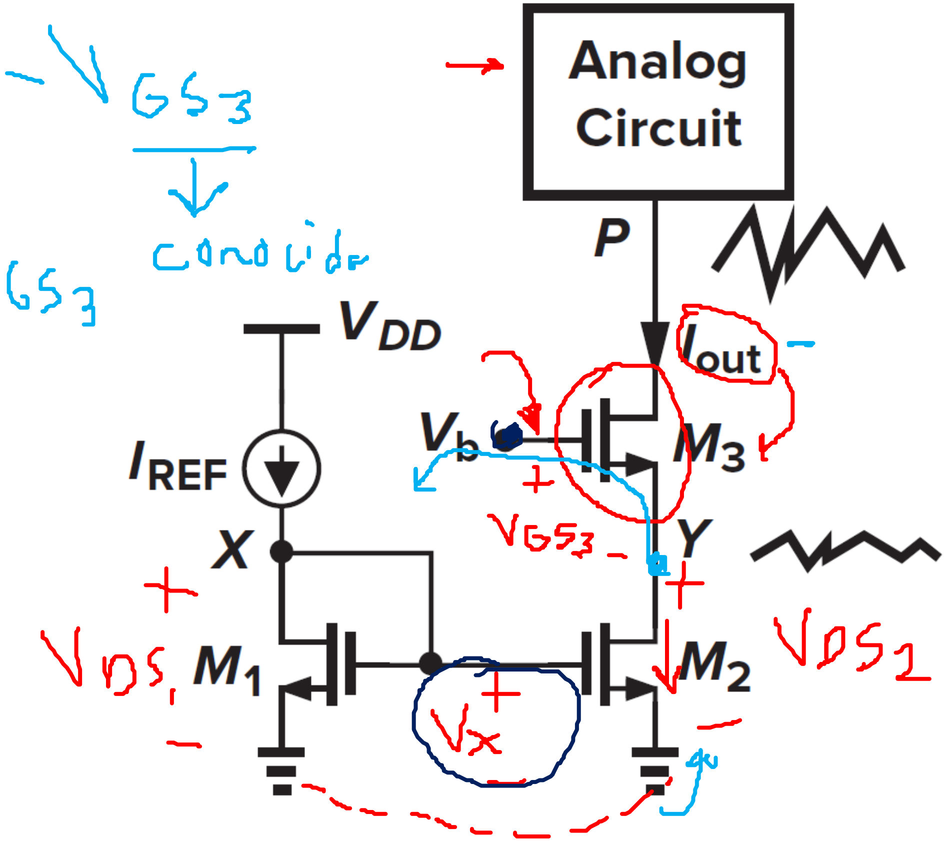
How to equal V_{DS1} and V_{DS2}?

$V_{DS_2} = V_b - V_{GS3}$

$V_{DS_1} = V_b - V_{GS3}$

consider

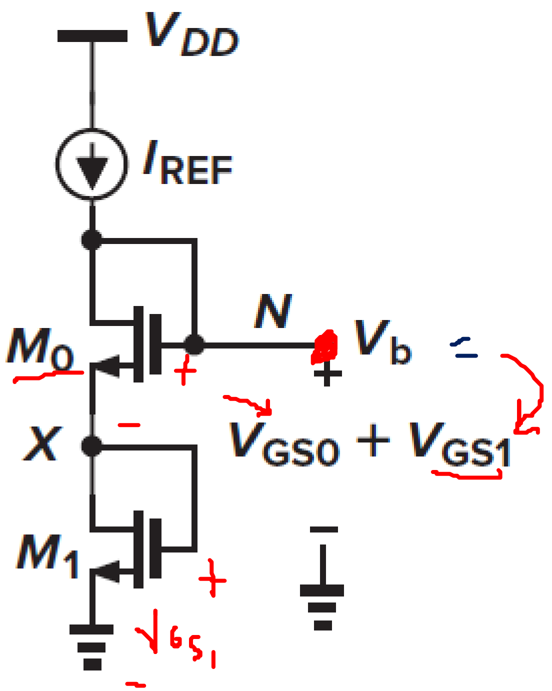
$V_b = V_{GS_1} + V_{GS_3}$



➢ M_3 shields node Y from variations in P, thus keeping node Y *relatively constant*.

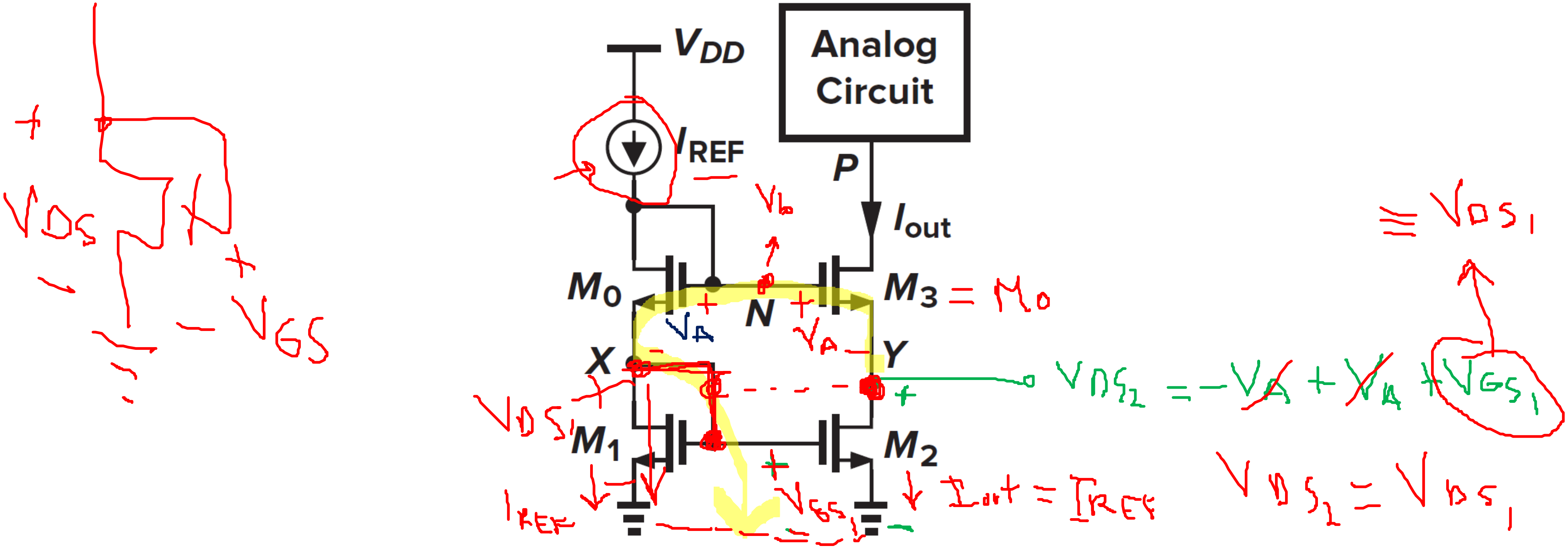
➢ Generate V_b such that $V_{S3}=V_b-V_{GS3}=V_{DS1}$, which means $V_b=V_{GS3}+V_{DS1}$.

How to generate V_b?



- $V_b = V_{GS3} + V_{DS1}$ means that V_b can be generated from two diode-connected transistors.
- In this case, $V_{GS0} = V_{GS3}$.

Cascode Current Mirror

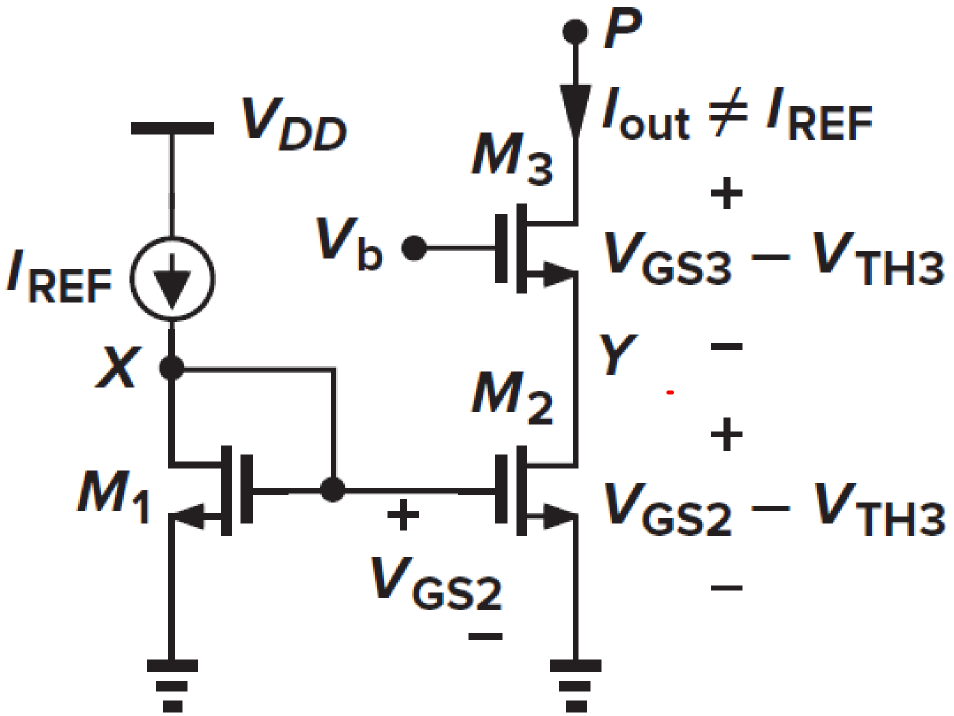


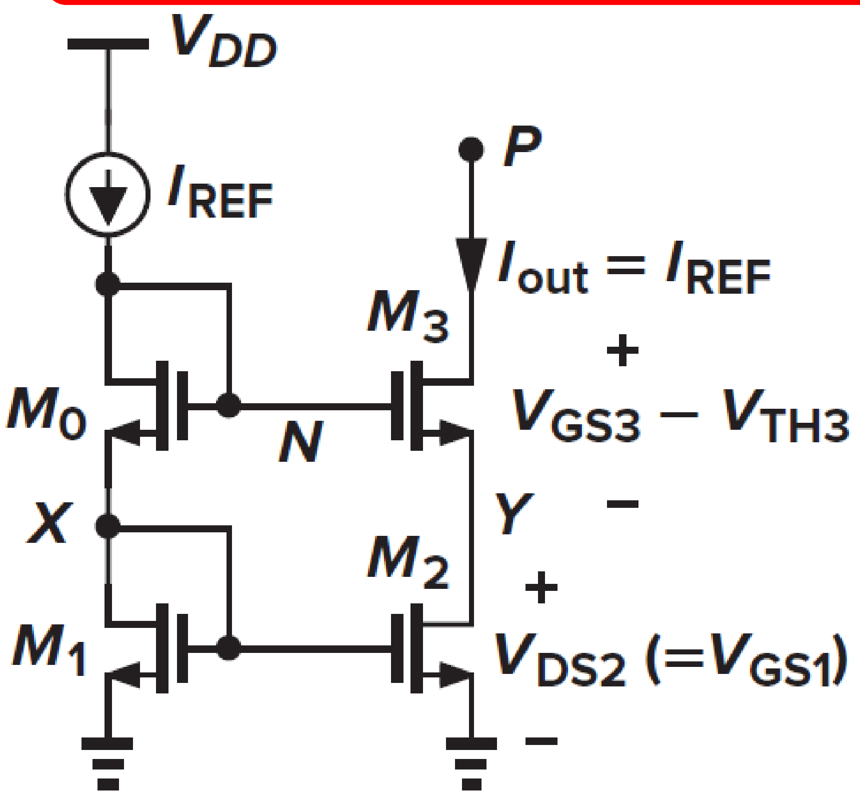
➢ **Therefore, a cascode current mirror allows generating an accurate current copy at I_{out}.**

Trouble in Paradise?

$V_P=(V_{GS3}-V_{TH})+(V_{GS2}-V_{TH})=2V_{OV}$

$V_P=(V_{GS3}-V_{TH})+(V_{GS1})=2V_{OV}+V_{TH}$





➢ **While operating with a high output impedance value and an accurate current, the cascode CM consumes significant voltage headroom.**

Comparing Simple and Cascode CMs

$V_P > V_{OV}$ ~ 100-400mV

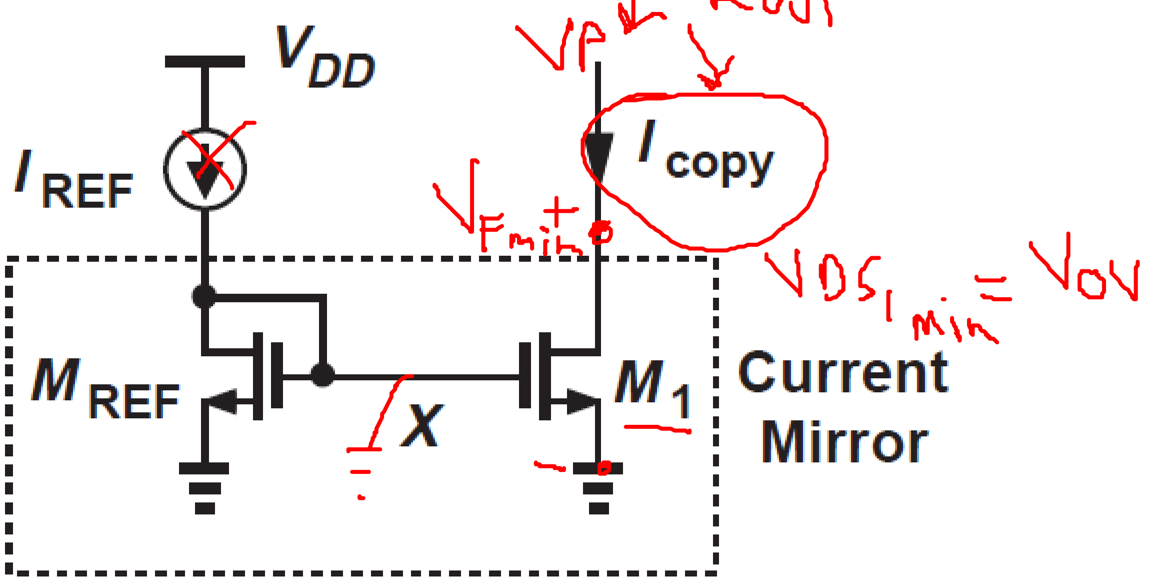
$R_{out}=r_{O1}$

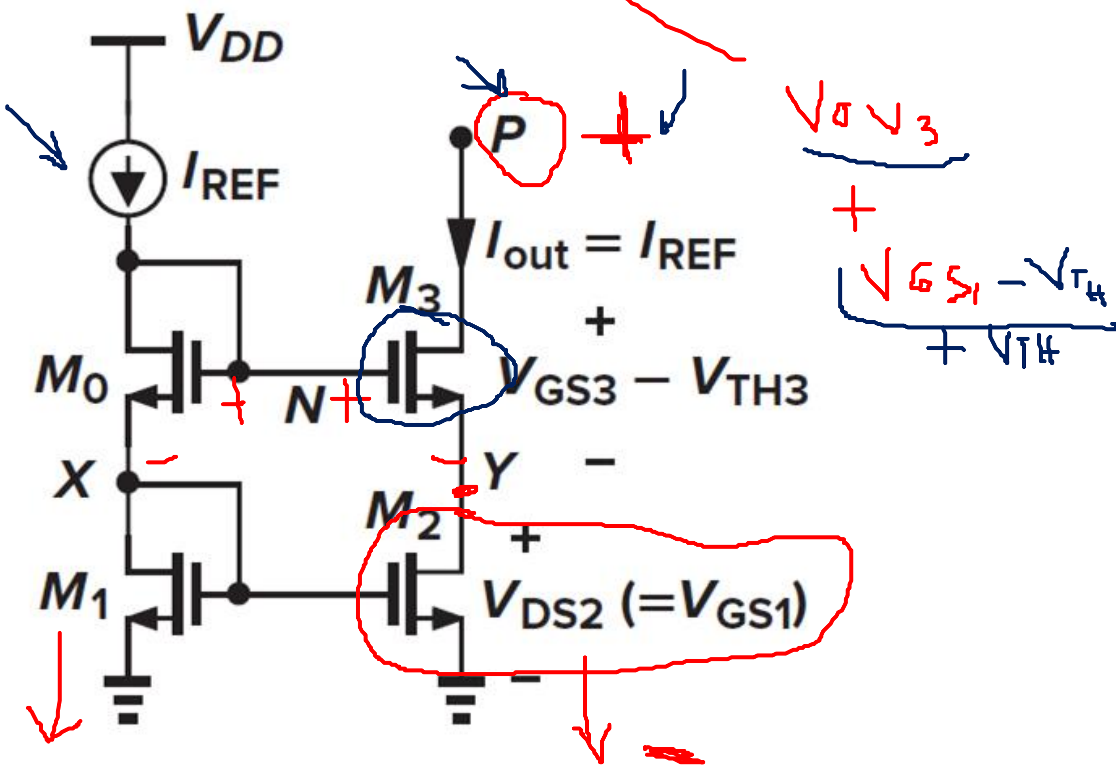
V_{ov}

$V_P > 2V_{OV}+V_{TH}$ ~ 0.9-1.5V!!!

$R_{out}=g_{m3}r_{O2}r_{O3}$

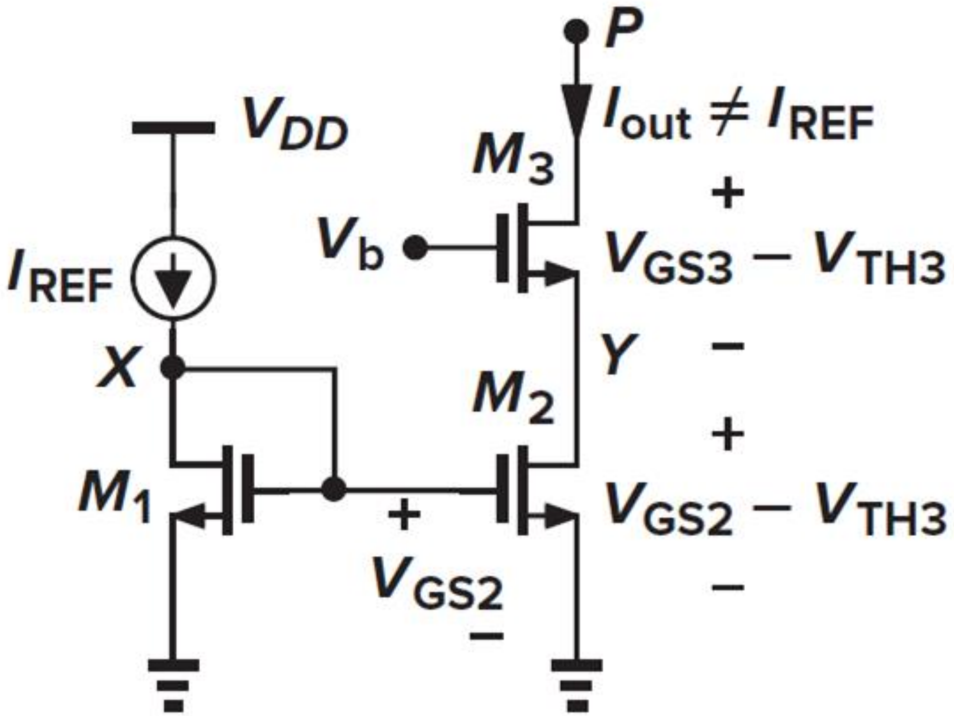
$2V_{ov} + V_{TH}$





➢ **While operating with a high output impedance value and an accurate current, the cascode CM consumes significant voltage headroom.**

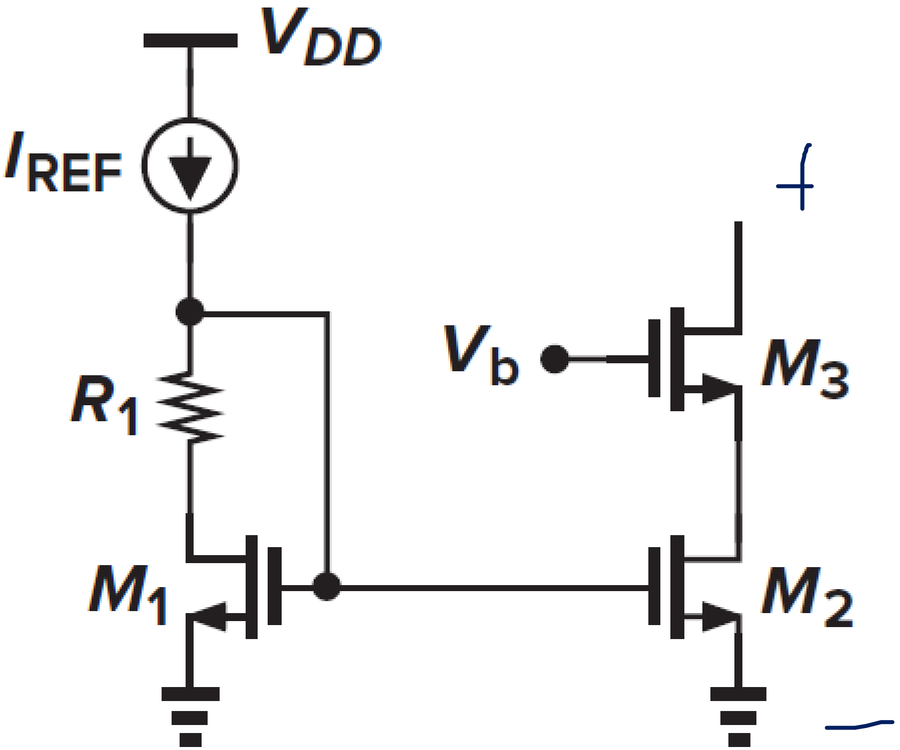
Solution?



The headroom issue would be mitigated if $V_b = V_{GS3} + (V_{GS2} - V_{TH})$, i.e., $V_{DS2} \sim V_{OV}$

➢ **Instead of forcing V_{DS2} equal to V_{GS1}, which causes problems, we can force V_{GS1} equal to V_{DS2}.**

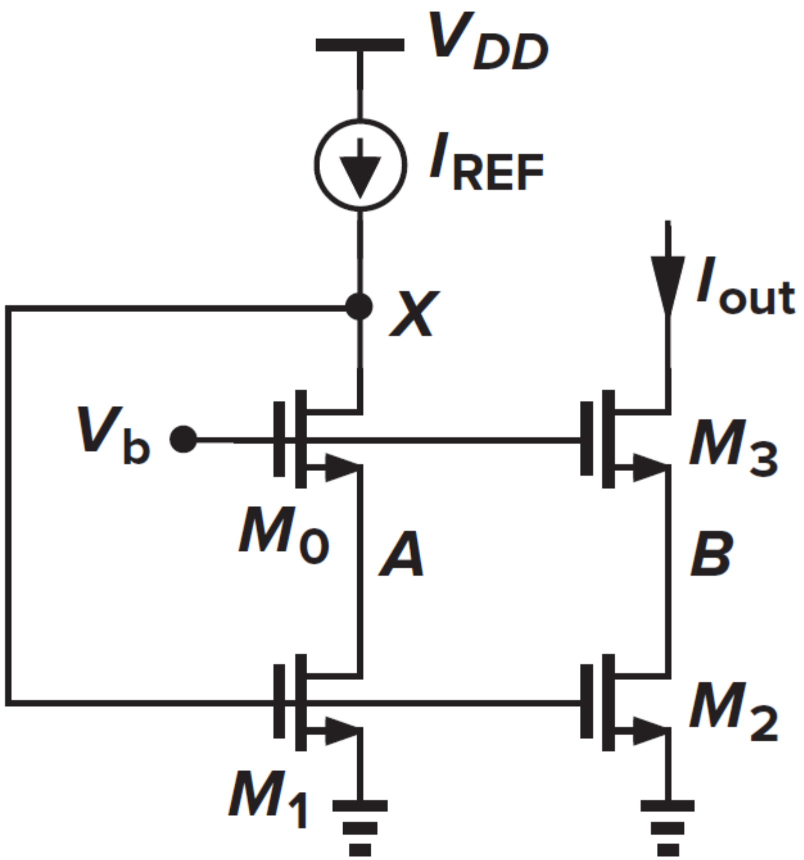
An Intuitive Modification



If $I_{REF}*R_1=V_{TH}$ and $V_b=V_{GS3}+(V_{GS1}-V_{TH})$, we can ensure $V_{DS1}=V_{DS2}=V_{OV}$

➢ Instead of forcing V_{DS2} equal to V_{GS1}, which causes problems, we can force V_{GS1} equal to V_{DS2}.

Avoiding PVT Variations on Resistor



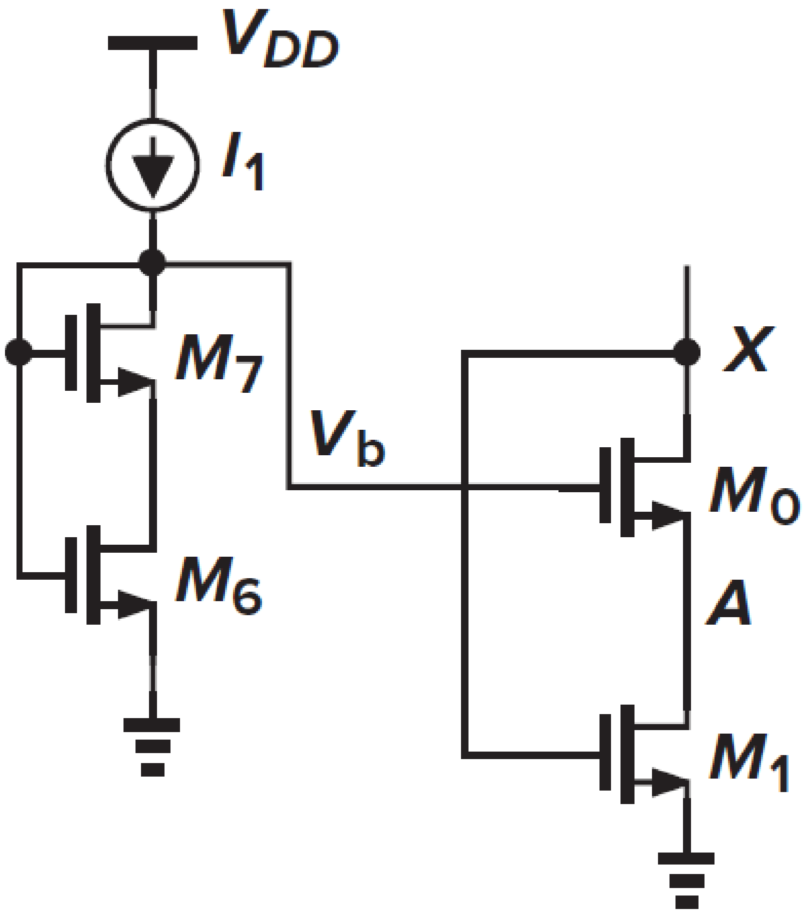
If $V_{GS0}=V_{GS3}$, we can ensure $V_{DS1}=V_{DS2}=V_b-V_{GS0,3}$

under some conditions:

1. $V_{GS0}-V_{TH} < V_{TH}$
2. $V_b=V_{GS0}+(V_{GS1}-V_{TH})$

➢ Instead of forcing V_{DS2} equal to V_{GS1}, which causes problems, we can force V_{GS1} equal to V_{DS2}.

Accomplishing Conditions



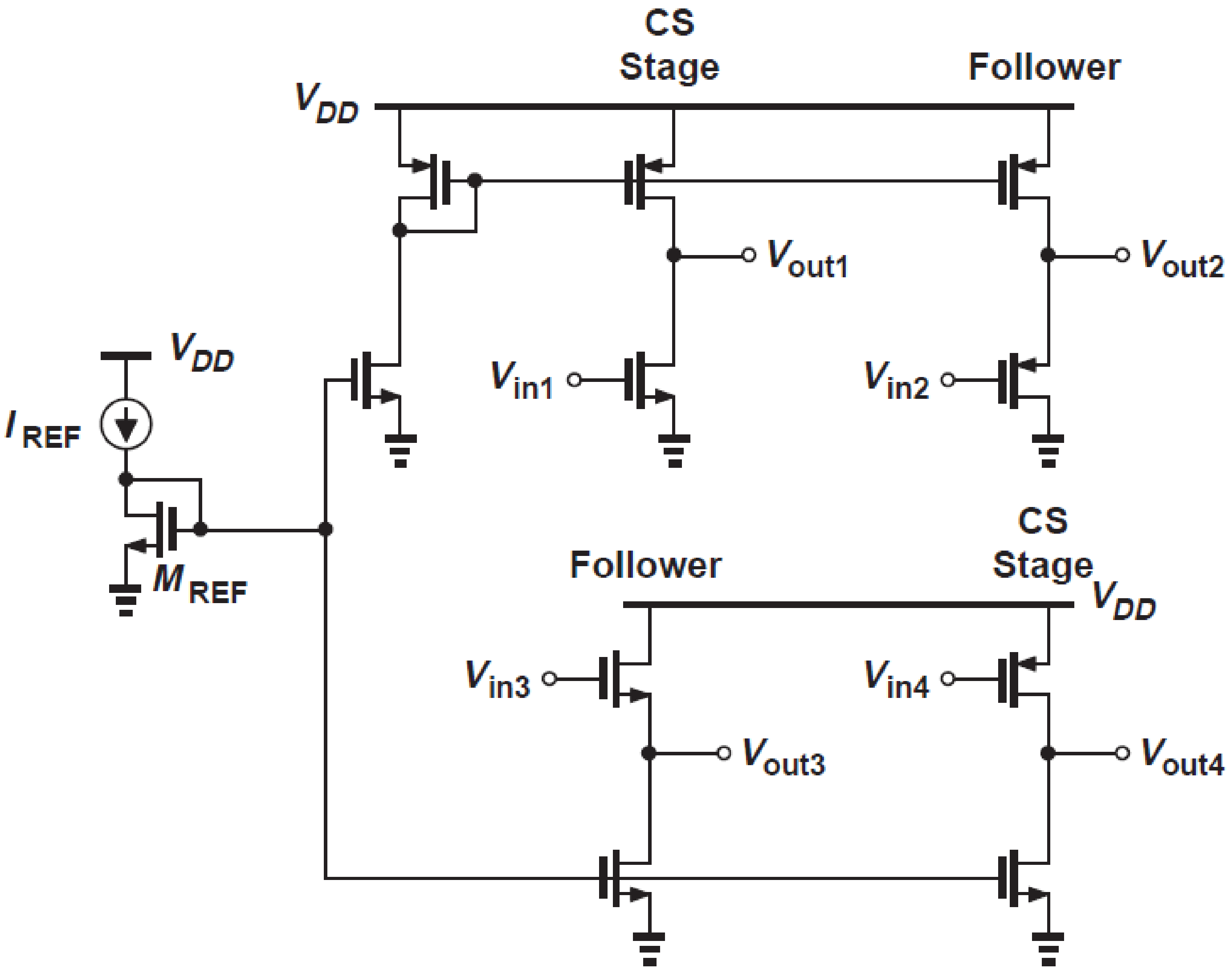
If $V_{GS0}=V_{GS3}$, we can ensure $V_{DS1}=V_{DS2}=V_b-V_{GS0,3}$

under some conditions:

1. $V_{GS0}-V_{TH} < V_{TH} \rightarrow M_0$ Sizing
2. $V_b=V_{GS0}+(V_{GS1}-V_{TH}) \rightarrow$ This topology

- $V_b=V_{GS7}+(V_{GS6}-V_{TH})$, $V_{GS7}=V_{GS0}$, $V_{GS6}=V_{GS1}$. This topology produces a headroom of $2V_{OV}$.

Exercise - CMs in Typical Circuits



PMOS CMs

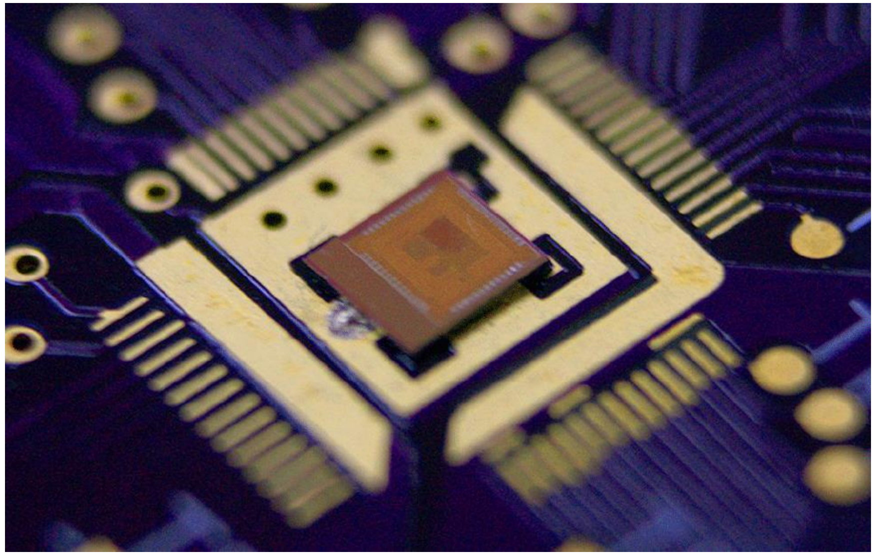
NMOS CMs

Thanks

Universidad Industrial de Santander

javier.ardila@correo.uis.edu.co

ONCHIP



@onchipUIS