CO224 Computer Architecture – 2020
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Lab 6 - Building a Memory Hierarchy

Comparison of the system performance of a system without cache and system with the cache

- Following are the observations of number of clock cycles spent in both systems for the Sample programs

Sample Program 1

	Instruction	No of clock cycles	
		Without the Cache	With the cache
1	loadi 0 0x02	1	1
2	loadi 1 0x05	1	1
3	swi 2 0x03	6	23
4	swd 1 0	6	1
5	lwi 3 0x 03	6	1
6	lwd 4 1	6	23
7	loadi 5 0x21	1	1
8	swi 5 0x20	6	44
9	swd 1 5	6	1

- In the cache-less implementation every memory access should spend6 clock cycles
- Since the 3rd instruction(1st memory access) is a cold miss & it should spend 23 clock cycles
- Then the 4th & 5th instructions are hits based on the locality. So it should only spend 1 clock cycle per each instruction.
- Then 8th instruction is a conflict miss & it spent 44 clock cycles.
- Then 9th instruction is a hit. So it should spend only 1 clock cycle.

Sample Program 2

	Instruction	No of clock cycles	
		Without the Cache	With the cache
1	loadi 0 0x00	1	1
2	loadi 1 0x01	1	1
3	swi 1 0x00	6	23
4	swi 1 0x01	6	1
5	swi 1 0x02	6	1
6	swi 1 0x03	6	1
7	lwi 2 0x00	6	1
8	lwi 3 0x01	6	1
9	lwi 4 0x02	6	1
10	lwi 5 0x03	6	1

- This sample test program shows the behavior of both systems when the program consecutively call the memory addresses in the same block of memory.
- In the cache less system it repeatedly spend 6 clock cycles for each memory access.
- But in the system with cache , after the data block loaded to the cache , it only spend one clock cycle for rest of the corresponding memory accesses.
- This kind of situations are occur when loops are executing.

Conclusion

- The purpose of using a cache based hierarchical memory is to reduce the clock cycles for accessing memory .
- Considering Principle of localities , it improve memory access performances.
- But the cold misses are unavoidable in the cache systems.
- The conflict misses can be minimized by using another method methods of designing caches such as set associative methods.
- By observing above results it can be determined that , the purpose of hierarchical memory system has achieved for a reasonable level.